1. In 32-bit addressing mode, address field is either 1 byte or?
o 4 bytes
2. If a block can be placed at every location in cache, this cache is said to be?
o Full associative
3. Information when is written in cache, both to block in cache and block present in lower-level memory, refers to?
o Write-through
4. Average access time of memory for having memory-hierarchy performance is given as?
Average memory access time = Hit time + Miss rate*Miss penalty
5. As segment or a page is normally used for block, page-fault and address-fault is used for
o Miss
6. Virtual memory producing virtual-addresses, are translated by
o Physical addresses
7. Per memory reference, miss-rate can be turned into per instruction misses rate by
o Miss rate= Memory accesses/ instructions
8. Cutting of physical-memory into form of blocks and allocating them to different processes, stated technique is known as
o Virtual memory
9. For reducing frequency on replacement of write-back blocks, commonly used feature, is known as
o Dirty bit
10. **If cache is not able for containing all blocks needed while execution, miss is then known as**
Cache miss

11. For completing programmer's desire for unlimited quick memory, suggested economical solution was
o Memory hierarchy

12. An instruction that does no operation for changing state is known as
o NOP
13. Set of instructions examined as candidates for potential execution is called the
o Window
14. Different types of parallelism in applications like:
o All above
15. Term 'computer architecture' is sometimes referred only to
o Instruction set design
16. General categories of instructions' operation are
4 All above
17. The effectiveness of the cache memory is based on the property of _____
o Locality of reference
18. The memory which is used to store the copy of data or instructions stored in larger memories, inside the CPU is called _____.
o Level 1 cache
19. The last on the hierarchy scale of memory devices is _____.
o Secondary memory
20. In the memory hierarchy, as the speed of operation increases the memory size also increases
o False
21. A common measure of performance is
Price/performance ratie
22. The number successful accesses to memory stated as a fraction is called as _____
Hit rate
23. With respect to changing among states of accomplishment and interruption, a measure of continuous service-accomplishment, is known as
Module availability

24. From a reference initial instant, a measure of service accomplishment. is known as

module reliability

25. To initialize any port as an output port what value is to be given to it?
d) A port is by default an output port

26. In AVR, which registers are there for the I/O programming of ports?
d) All of the mentioned

27. The data will not go from the port registers to the pin unless:
c) DDR register of that port is set to 1
28. What is the file extension that is loaded in a micro controller for executing any instruction?

- .hex

29. What type of coherence misses is - that arise from the communication of data through the cache coherence mechanism?
- True sharing misses

30. What type of coherence misses is - that arises from the use of an invalidation based coherence algorithm with a single valid bit per cache block?:
- False sharing

31. At Directory-Based Cache Coherence Protocols: The Basics, which state in the following called “Shared” in a simple protocol?
- One or more processors have the block cached, and the value in memory is up to date

32. At Directory-Based Cache Coherence Protocols: The Basics, which state in the following called “Modified” in a simple protocol?
- Exactly One processor has a copy of the cache block and it has written the block, so the memory copy is out of date.

33. In Non-Blocking Caches what does mean “Early restart”?

Fetch the words in normal order, but as soon as the requested word of the block arrives, send it to processor and let the processor continue execution

34. Far more sophisticated techniques are possible What is a Latency:
is time for a single access-Main memory latency is usually >>than processor cycle time

35. What occurs at Instruction fetches when we speak about Common And Predictable Memory Reference Patterns?
n loop iterations
36. What occurs at Stack access when we speak about Common And Predictable Memory Reference Patterns?
Subroutine call

37. What occurs at Data access when we speak about Common And Predictable Memory Reference Patterns?
vector access

38. What is kernel process?

Provide at least two modes, indicating whether the running process is a user process or an operating system process

39. Which one is NOT concerning to pitfall?

a. Predicting cache performance of one program from another

40. Which one is concerning to fallacy?

predicting cache performance of one program from another

41. At VLIW by “performance and loop iteration” which time is longer?

Loop Unrolled

42. At VLIW by “performance and loop iteration” which time is shorter?

Software Pipelined

43. At VLIW Speculative Execution, which of this solution is true about problem: Branches restrict compiler code motion?

Speculative operations that don’t cause exceptions

44. At VLIW Speculative Execution, which of this solution is true about problem: Possible memory hazards limit code scheduling:

Hardware to check pointer hazards

45. At VLIW Multi-Way Branches, which of this solution is true about problem: Long instructions provide few opportunities for branches:

a. Allow one instructions to branch multiple directions

46. In Multilevel Caches “Local miss rate” equals =

- misses in a cache/ accesses to cache

47. In Multilevel Caches “Global miss rate” equals =

- misses in a cache/ CPU memory accesses

48. In Multilevel Caches “Misses per instruction” equals =

- Misses in cache / number of instructions

49. Network performance depends of what?

a. Performance of switches and transmission system

50. The time between the start and the completion of an event ,such as milliseconds for a disk access is…

- Latency

51. Total amount of work done in a given time , such as megabytes per second for disk transfer…

- bandwidth

52. Products that are sold by multiple vendors in large volumes and are essentially identical

Commodities

53. Integrated circuit processes are characterized by the

- Feature size

54. Manufacturing costs that decrease over time are ____the learning curve

55. Volume is a _____ key factor in determining cost.

- second

56. The most companies spend only _____ of their income on R&D, which includes all engineering.
- 4% to 12%

57. Desktop benchmarks divide into __ broad classes:
- Two

58. A widely held rule of thumb is that a program spends __ of its execution time in only __ of the code.
- 90% 10 %

59. (Performance for entire task using the enhancement when possible) / (Performance for entire task without using the enhancement) is equals to:
- speedup

60. Which of the following descriptions corresponds to static power?

a. Grows proportionally to the transistor count (whether or not the transistors are switching)

61. If we want to sustain four instructions per clock
- We must fetch more, issue more, and inishiate execution on more than four instractions

62. What is a hash table?

Popular data structure for organizing a large collection of data items so that one can quickly answer questions

63. How this process called: “Operations execute as soon as their operands are available”
- a. Data flow execution

64. For what the used :
- To pass result among instructions that may be speculated.

65. Which one is not the major flavor of Multiple-issue processors:
- statistically superscalar processors

66. Examples of superscalar(static):
MIPS and ARM

67. Examples of superscalar(dynamic) :
None at the present

68. Examples of VLIW processor:
TI C6x

69. Which is not the function of integrated instruction fetch unit:
Instruction memory commit

70. What is a topology in interconnection networks?
in indicates how the nodes a notebook are organised

71. What is a Network Diameter?
a. It is the minimum distance between the farthest nodes in a network

72. What is a Node degree?
Number of edges connected with a node is called node degree.

73. What is a Bisection Bandwidth?

Number of edges required to be cut to divide a network into two halves is called bisection bandwidth.

74. What is Latency?

It is the delay in transferring the message between two nodes.

75. What is a Hardware Cost?

It refers to the cost involved in the implementation of an interconnection network.

76. What is a Blocking and Non-Blocking network?

Network In non-blocking networks the route from any free input node to any free output node can always be provided.

77. Design issue of interconnection network

Symmetry of the network

78. Design issue of interconnection network

Dimension and size of network

79. What is a Data transfer time?

How long does it take for a message to reach to another processor.

80. Select two-dimensional interconnection network

o Mesh

81. Select multi-dimensional interconnection network

o cube, hyper cube,

82. Select multi-dimensional interconnection network

o cube

83. Select non-blocking interconnection network

o Cross bar

84. A modified version of the tree interconnection network

o fat tree

85. A interconnection network is a type of pipelined array architecture and it is designed for multidimensional flow of data

o Systolic array

86. A _____ interconnection network is an extension of cube network

o Hyper cube

87. In computer architecture, _____ is the ability of a central processing unit (CPU) or a single core in a multi-core processor to execute multiple processes or threads concurrently, appropriately supported by the operating system.

o multithreading

88. Select non-blocking interconnection network

CrossBar

88. Select two-dimensional interconnection network

• Mesh

89. Single Instruction, Single Data (SISD)

o Only one instruction stream is being acted on by the CPU during any one clock cycle

90. In Parallel Computing

o A problem is broken into discrete parts that can be solved concurrently

91. Pipelining …
- Breaking a task into steps performed by different processor units, with inputs streaming through, much like an assembly line

92. Shared Memory…
- From a strictly hardware point of view, describes a computer architecture where all processors have direct(usually base based) access to common physical memory

93. What is a RISC computers?
- RISC (reduced instruction set computer)

94. When single-processor performance improvement has dropped?
- 2003

95. How much in percentage single-processor performance improvement has dropped to less than?
- 22%

96. How many classes of computers classified?
- 5

97. What is the PMD in computer classes?

Personal mobile device

98. What is the Thread Level Parallelism -
- exploits either data-level parallelism or task-level parallelism in a tightly coupled hardware model that allows for interaction among parallel threads.

99. What is the Request Level Parallelism:
- exploits parallelism among largely decoupled tasks specified by the programmer or the operating system

100. What is the Instruction Level Parallelism:

exploits data-level parallelism at modest levels with compiler help using ideas like pipelining and at medium levels using ideas like speculative execution.

101. What is the MISD one of the categories of computers?:

multiple instruction, single data

102. How many elements in Trends of Technology?

5

103. How many elements of the Instruction Set Architecture (ISA):

7

104. How many types of dependencies do you know?
- 3

105. How many possible Elements of Data Hazards?
- 3

106. What is the “ISSUE” in Pipelining Basics?
- Decode instruction, check for structural hazard

107. What is the “Read Operands” in Pipelining Basics?
- Wait until no data hazards, then read operands.

108. How many Optimizations’ in Cache memory Performance?
- 10

109. What is the Compulsory in main categories in Cache Memory?
- First Reference to a block, occur even with infinite cache.

110. What is the Capacity in main categories in Cache Memory?

o Cache is too small to hold all data needed by program, occur even under perfect replacement policy(loop over 5 cache lines)

111. What is the Conflict in main categories in Cache Memory?

o Misses that occur because of collisions due to less than full associativity(loop over 3 cache lines)

112. What is the Temporal Locality?

o Exploit by remembering the contents of recently accessed locations.

113. What is the Spatial Locality?

o Exploit by fetching blocks of data around recently accessed locations.

114. What is the Reducing the Hit time?

o Small and simple first-level caches and way-prediction.

115. What is the Increasing cache bandwidth?

o Pipeland caches, multibanked caches, nonoblocked caches.

116. What is the Reducing the Miss Penalty?

o Critical word first and merging write buffer.

117. What is the Reducing the Miss Rate?

o Compiler Optimization

118. Main term of dependability is SLAs?

o Service Level Agreements

119. Main term of dependability is SLOs?

o Service Level objectives

120. The second type of dependence is?

o name dependence

121. RAW (read after write)?

a. This hazard is the most common type and corresponds to a true data dependence.

122. WAW (write after write)?

This hazard corresponds to an output dependence

123. WAR (write after read)?

This hazard arises from an anti-dependence (or name dependence)

124. What is the element “Read Operands” in simple five-stage pipeline?

125. What is the ROB?

o ReOrder Buffer

126. How many steps in instruction execution?

4

127. How many restrictions RAW hazards through memory are maintained?

2

128. How many major flavors in Multiple-issue processors?

3

129. How many functions at Integrated Instruction Fetch Units

3

130. Speculation and the Challenge of Energy Efficiency consume excess energy in how many ways?

2 ways

131. The hardware model represents the assumptions made for an ideal or perfect processor is as how many follow elements?

5

132. Infinite register renaming at The Hardware Model?

There are an infinite number of virtual registers available

133. Perfect caches at The Hardware Model?

o All memory accesses take one clock cycle

134. Perfect memory address alias analysis at The Hardware Model?

All memory addresses are known exactly

135. Perfect jump prediction at The Hardware Model?

All jumps are perfectly predicted.

136. What is Personal mobile device (PMD)?

Personal mobile device (PMD)

137. Where the embedded microprocessors are used?

In microwaves, washing machines

138. What functions has Instruction Set Architecture (ISA)?

a. Serves as the boundary between the software and hardware?

139. What is the TLP?

Task level parallelism

140. By Moore's law, growth rate in transistor count on a chip is doubling?

every 18 to 24 months

141. How should a system architect or a user think about performance, power, and energy? From the viewpoint of a system designer, how many concerns are there?:

3

142. What is the “Module reliability” in Dependability?

measure of the continuous service accomplishment from a reference initial instant

143. What is response time?

the time between the start and the completion of an event

144. The guiding principle of reporting performance measurements should be?

a. reproducibility

145. What is Temporal Locality?

o Exploit by remembering the contents of recently acessed locations

146. What is Spatial Locality?

items whose addresses are near one another tend to be refrenced close together in time

147. What is Amdahl's law?

a. Defines the speedup that can be gained by using a particular feature

148. The most popular scheme is set associative, where a set is?

o A groups of blocks

o

149. The three Cs model sorts all misses into three simple categories: Compulsory, Capacity, Conflict. What is Compulsory?

o The very first access to a block cannot be in the cache, so the block must be brought into the cache.

150. The three Cs model sorts all misses into three simple categories: Compulsory, Capacity, Conflict. What is Capacity?

o If the cache cannot contain all the blocks needed during execution of a program

151. The three Cs model sorts all misses into three simple categories: Compulsory, Capacity, Conflict. What is Conflict?

o If the block placement strategy is not fully associative

152. The “natural” unit of organization of memory

o Word

153. Main element of cache memory is …

o b . Tag

154. Typical levels of Cache memories …

o 1, 2, 3 levels

155. Select internal memory …

o Processor register

156. Select internal memory

o Cache

157. Select internal memory

o Main memory

158. Select external memory?

b. Magnetic tape;

159. Select external memory

hard disk

160. Select external memory

c. Optical Disk

162. Physical types of memories:

Magneto-optical

162. Physical types of memories:

Semiconductor. Magnetic

163. Physical types of memories:

Semiconductor, optical

164. Select correct memory hierarchy:

o cache-main memory-secondary storage

165. Select correct memory hierarchy:

Processor registers-Cache memory-main memory

166. External, nonvolatile memory is also referred to as …

o auxillary memory

167. Types of cache addresses

o logical and physical

168. A logical cache stores data using …

o Virtual addresses

169. The two basic forms of semiconductor random access memory are

o dynamic RAM(DRAM) and static RAM(SRAM)

170. Main element of cache memory

a. Line;

171. A number of chips can be grouped together to form …

o Memory bank

172. Data are recorded on and later retrieved from the disk via a conducting coil named

o The head

173. The information can then be scanned at the same rate by rotating the disk at a fixed speed, known as …

the constant angular velocity

174. To increase density, modern hard disk systems use a technique known as

o multiple zone recording

175. … can be removed and replaced with another disk.

removable disk

176. For most disks, the magnetizable coating is applied to both sides of the platter, which is then referred to as …

double sided

177. The set of all the tracks in the same relative position on the platter is referred to as …

cylinder

178. On a movable head system, the time it takes to position the head at the track is known as …

seek time

179. The operating system …

is the software that controls the execution of
programs on a processor and that manages the processor's resources.

180. The most important functions of the Operating System are

The scheduling of processes or tasks

181. The important function of the Operating System is

a. Memory management

182. How is the following service called? The Operating System provides a variety of facilities and services, such as editors and debuggers, to assist the programmer in creating programs…

Program creation:

183. How is the following service called? A number of tasks need to be performed to execute a program. Instructions and data must be loaded into main memory, I/O devices and files must be initialized, and other resources must be prepared. The Operating System handles all of this for the user.

o Program execution

184. How is the following service called? Each I/O device requires its own specific set of instructions or control signals for operation. The Operating System takes care of the details so that the programmer can think in terms of simple reads and writes.

o Access to I/O devices

185. How is the following service called? In the case of a shared or public system, the Operating System controls access to the system as a whole and to specific system resources.

System access.

186. How is the following service called? These are internal and external hardware errors, such as a memory error, or a device failure or malfunction; and various software errors, such as arithmetic overflow, attempt to access forbidden memory location, and inability of the OS to grant the request of an application. In each case, the Operating System must make the response that clears the error condition with the least impact on running applications.

o Error detection and response

187. How is the following service called? A good Operating System collects usage statistics for various resources and monitor performance parameters such as response time. On any system, this information is useful in anticipating the need for future enhancements and in tuning the system to improve performance.

o Accounting

188. Select two independent dimensions of the Operating System

a. Batch and Interactive

189. Select the ARM Memory-Management Parameter according to this description. These bits control access to the corresponding memory region. If an access is made to an area of memory without the required permissions, a Permission Fault is raised.
o Access Permission (AP), Access Permission Extension (APX)

190. Select ARM Memory-Management Parameter according to this description. Determines, with the TEX bits, how the write buffer is used for cacheable memory.
o Bufferable (B) bit

191. Select the ARM Memory-Management Parameter according to this description. These bits, together with the B and C bits, control accesses to the caches, how the write buffer is used, and if the memory region is shareable and therefore must be kept coherent.
o Type Extension (TEX)

192. Select the Pentium Memory Management Parameter according to this description: Specifies the privilege level of the segment referred to by this segment descriptor.
o Descriptor Privilege Level (DPL)

193. Select the Pentium Memory Management Parameter according to this description. Used for nonpaged systems. It indicates whether the segment is present in main memory. For paged systems, this bit is always set to 1.
o Segment Present bit (P)

194. Select the Pentium Memory Management Parameter according to this description. This bit is set to 1 by the processor in both levels of page tables when a read or write operation to the corresponding page occurs.
o Accessed bit (A)

195. Select the Pentium Memory Management Parameter according to this description. Provides the physical address of the page in memory if the present bit is set. Since page frames are aligned on 4K boundaries, the bottom 12 bits are 0, and only the top 20 bits are included in the entry. In a page directory, the address is that of a page table.
o Page Frame Address

196. Select the Pentium Memory Management Parameter according to this description. Indicates whether the page is available only to the operating system (supervisor level) or is available to both operating system and applications (user level).
o User/Supervisor bit (US)

197. Select the Pentium Memory Management Parameter according to this description. Indicates whether write-through or write-back caching policy will be used for data in the corresponding page.
o Page Write Through bit (PWT)

198. Convert given number from decimal to binary number system. Decimal number: -13.3125

-1101 0101

199. Convert given number using sign-magnitude representation from decimal to binary number system. Decimal number (use 8 bit): -18

1001 0010

200. Convert given number using sign-magnitude representation from decimal to binary number system. Decimal number (use 16 bit): -150

1000 0000 1001 0110

201. Convert given number using sign-magnitude representation from decimal to binary number system. Decimal number (use 16 bit): 150

0000 0000 1001 0110

202. Convert given number using twos complement representation from decimal to binary number system. Decimal number (use 16 bit): - 150

1111111101101010

203. Convert given number using complement representation from decimal to binary number system. Decimal number: - 8

1000

204. Convert given number using twos complement representation from decimal to binary number system. Decimal number: - 7

0111

205. Convert given number using sign-magnitude representation from decimal to binary number system. Decimal number: - 5

1101

206. Subtract one number from another and show the result of the subtraction in binary. Task: 2 – 7

1011

207. Subtract one number from another and show the result of the subtraction in binary. Task: 165 – 200

a. 1111 1111 1101 1101

208. Subtract one number from another and show the result of the subtraction in binary. Task: 950 - 1100 1111 1111 0110 1010