1. In 32-bit addressing mode, address field is either 1 byte or? #

* 4 bytes

1. If a block can be placed at every location in cache, this cache is said to be? #

* **Fully associative**

1. Information when is written in cache, both to block in cache and block present in lower-level memory, refers to?

* **Write through**

1. Average access time of memory for having memory-hierarchy performance is given as? #

* **Average memory access time = Hit time + Miss rate × Miss penalty**

1. As segment or a page is normally used for block, page-fault and address-fault is used for #

* **Miss**

1. Virtual memory producing virtual-addresses, are translated by #

* **Physical addresses**

1. Per memory reference, miss-rate can be turned into per instruction misses rate by

* **Miss rate= Memory accesses/ instructions**

1. Cutting of physical-memory into form of blocks and allocating them to different processes, stated technique is known as #

* **Virtual memory**

1. For reducing frequency on replacement of write-back blocks, commonly used feature, is known as #

* **Dirty bit**

1. If cache is not able for containing all blocks needed while execution, miss is then known as

* **capacity**

1. For completing programmer's desire for unlimited quick memory, suggested economical solution was

* **Memory hierarchy**

1. An instruction that does no operation for changing state is known as

* **NOP**

1. Set of instructions examined as candidates for potential execution is called the

* **Window**

1. Different types of parallelism in applications like:

* **All above**

1. Term 'computer architecture' is sometimes referred only to#

* **Instruction set design**

1. General categories of instructions' operation are

1 Data transfer

2 Arithmetic logical

3 floating point

4 All above

1. The effectiveness of the cache memory is based on the property of \_\_\_\_\_\_\_\_ #

* **Locality of reference**

1. The memory which is used to store the copy of data or instructions stored in larger memories, inside the CPU is called \_\_\_\_\_\_\_. #

* **Level 1 cache**

1. The last on the hierarchy scale of memory devices is \_\_\_\_\_\_.

* **Secondary memory**

1. In the memory hierarchy, as the speed of operation increases the memory size also increases

* **False :As the speed of operation increases the cost increases and the size decreases.**

1. A common measure of performance is

* **MIPS rate = f \* IPC the rate at which instructions are executed**

1. The number successful accesses to memory stated as a fraction is called as \_\_\_\_\_

* **Hit ratе**

1. With respect to changing among states of accomplishment and interruption, a measure of continuous service-accomplishment, is known as

* **Module availability**

1. From a reference initial instant, a measure of service accomplishment. is known as

* **Module reliability**

1. To initialize any port as an output port what value is to be given to it?

0xFF

0x00

0x01

* **A port is by default an output port**

1. In AVR, which registers are there for the I/O programming of ports?

PORT

PIN

DDR

* **All of the mentioned**

1. The data will not go from the port registers to the pin unless:

* **DDR register of that port is set to 1**

1. What is the file extension that is loaded in a micro controller for executing any instruction?

* .doc
* .c
* .txt
* **.hex**

1. What type of coherence misses is - that arise from the communication of data through the cache coherence mechanism?

* **True sharing misses**

1. What type of coherence misses is - that arises from the use of an invalidation based coherence algorithm with a single valid bit per cache block?:

* **False sharing**

1. At Directory-Based Cache Coherence Protocols: The Basics, which state in the following called “Shared” in a simple protocol?

* **One or more processors have the block cached, and the value in memory is up to date**

1. At Directory-Based Cache Coherence Protocols: The Basics, which state in the following called “Modified” in a simple protocol?

* **One processor has a copy of the cache block and it has written the block, so the memory copy is out of date. The processor is called the owner of the block.**

1. In Non-Blocking Caches what does mean “Early restart”?

* **Fetch the words in normal order, but as soon as the requested word of the block arrives, send it to processor and let the processor continue execution**

1. Far more sophisticated techniques are possible    What is a Latency:

* **Is time between the start and completion of the event, such as milliseconds for a disk access**
* **Memory latency: Memory speeds lag processor speeds, as previously discussed.**

1. What occurs at Instruction fetches when we speak about Common And Predictable Memory Reference Patterns?
2. What occurs at Stack access when we speak about Common And Predictable Memory Reference Patterns?
3. What occurs at Data access when we speak about Common And Predictable Memory Reference Patterns?
4. What is kernel process?

* **Execution in OS that is neither idle not in synchronization access**
* **The kernel is a computer program that is the core of a computer's operating system, with complete control over everything in the system.**

1. Which one is NOT concerning to pitfall?

* **Pitfall: Moving functions from the CPU to the I/O processor, expecting to improve performance without analysis.**

1. Which one is concerning to fallacy?

* Здесь я написала какие бывает, ответ будет тот, которого здесь нет
* **Fallacy: the rated mean time to failure of disks is 1,200,000 hours, so disks practically never fail.**
* **Fallacy: magnetic disk storage is on its last legs, will be replaced.**
* **Fallacy: A 100 MB/sec bus can transfer 100 MB/sec.**
* the 8 fallacies of distributed computing are being rendered obsolete:

8 ошибок распределенных вычислений становятся устаревшими

* **The network is reliable**
* **Latency is zero**
* **Bandwidth is infinite**
* **The network is secure**
* **Topology doesn’t change**
* **There is one administrator**
* **Transport cost is zero**
* **The network is homogenous**

1. At VLIW by “performance and loop iteration” which time is longer?

* **Loop Unrolled**
* **Software Pipelined**

1. At VLIW Speculative Execution, which of this solution is true about problem: Branches restrict compiler code motion?

* **Speculative operations that don't cause exceptions**

1. At VLIW Speculative Execution, which of this solution is true about problem: Possible memory hazards limit code scheduling:

* **Hardware to check pointer hazards**

1. At VLIW Multi-Way Branches, which of this solution is true about problem: Long instructions provide few opportunities for branches:
2. In Multilevel Caches “Local miss rate” equals =

* **Number of misses in a  cache/ Memory accesses to this cache**

1. In Multilevel Caches “Global miss rate” equals =

* **Number of misses in a  cache/ Memory accesses generated be CPU**

1. In Multilevel Caches “Misses per instruction” equals =

* **Misses per instruction = Memory accesses per instruction x Miss rate**

1. Network performance depends of what?

* **mode of replication**
* **Network bandwidth or capacity - Available data transfer**
* **Network throughput - Amount of data successfully transferred over the network in a given time**
* **Network delay, latency and jittering - Any network issue causing packet transfer to be slower than usual**
* **Data loss and network errors - Packets dropped or lost in transmission and delivery**

1. The time between the start and the completion of an event ,such as milliseconds for a disk access is…

* **Latency or response time**

1. Total amount of work done in a given time , such as megabytes per second for disk transfer…

* **bandwidth or throughput**

1. Products that are sold by multiple vendors in large volumes and are essentially identical

* **Commodities**

1. Integrated circuit processes are characterized by the

* **presence of logic gates, process information discretely**

1. Manufacturing costs that decrease over time are \_\_

* **even without major improvements in the basic implementation technology. The underlying principle that drives costs down is the learning curve—manufacturing costs decrease over time.\_\_**

1. Volume is a \_\_\_\_\_\_\_\_ key factor in determining cost.

* **integrated circuits**
* **second**

1. The most companies spend only \_\_\_\_\_\_\_\_\_\_\_\_ of their income on R&D, which

includes all engineering.

* **4% to 12%**

1. Desktop benchmarks divide into \_\_ broad classes:

* **Two broad classes: processor-intensive benchmark and graphics-intensive benchmark**

1. A widely held rule of thumb is that a program spends \_\_ of its execution time in only \_\_ of the code.

* **Spends 90%  in only 10 % of the code**

1. (Performance for entire task using the enhancement when possible) / (Performance for entire task without using the enhancement) is equals to:

* **speedup**

1. Which of the following descriptions corresponds to static power?
2. If we want to sustain four instructions per clock

* **two processor cores each capable of sustaining four instructions per clock, including two FP and two load-store instructions.**

1. What is a hash table?

* **A hash table is a popular data structure for organization a large collection of data items**.

1. How this process called: “Operations execute as soon as their operands are available”

* **Data flow**

1. For what the reorder buffer is used :

* **To pass result among instructions that may be speculated.**
* **Is the explicit use of a larger physical set of registers combined with register renaming;**

1. Which one is not the major flavor of Multiple-issue processors:

* **Осылардын биреуи болмаса сол ответ**
* **1 statically schedule superscalar processor**
* **2 VLIW very long instruction word**
* **3 dynamically schedule superscalar  processors**

67. Examples of superscalar(static):

68. Examples  of superscalar(dynamic) :

69. Examples  of  VLIW processor:

* **Itanium (3 operations)**
* **Transmeta Crusoe**
* **(4 operations) embedded processors**

70. Which is not the function of  integrated instruction fetch unit:

71. What is a topology in interconnection networks?

72. What is a Network Diameter?

* **closes distance between two nods**

73. What is a Node degree?

* **Number of edges connected with a node is called node degree.**

74. What is a Bisection Bandwidth?

* **Number of edges required to be cut to divide a network into two halves is called bisection bandwidth.**

75. What is Latency?

* **It is the delay in transferring the message between two nodes.**

76. What is a Hardware Cost?

* **It refers to the cost involved in the implementation of an interconnection network. It includes the cost of switches, arbiter unit, connectors, arbitration unit, and interface logic.**

77. What is a Blocking and Non-Blocking network?

* **In non-blocking networks the route from any free input node to any free output node can always be provided. Crossbar is an example of non-blocking network. In a blocking network simultaneous route establishment between a pair of nodes may not be possible. There may be situations where blocking can occur. Blocking refers to the situation where one switch is required to establish more than one connection simultaneously and end-to-end path cannot be established even if the input nodes and output nodes are free. The example of this is a blocking multistage network.**

78. Design issue of interconnection network

79. What is a Data transfer time?

* **time which spend to message transfer between two nods**

80. Select two-dimensional interconnection network

* **Mesh cross bar**

81. Select multi-dimensional interconnection  network

* **Systolic array, cube, hyper cube,**

82. Select multi-dimensional interconnection  network

* **cube**

83. Select non-blocking interconnection  network

* **Cross bar**

84. A modified version of the tree interconnection  network

* **fat tree**

85. A interconnection network is a type of pipelined array architecture and it is designed for multidimensional flow of data

* **Systolic array**

86. A \_\_\_\_\_\_\_\_\_\_\_\_\_ interconnection network is an extension of cube network

* **Hyper cube**

87. In computer architecture, \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ is the ability of a central processing unit (CPU) or a single core in a multi-core processor to execute multiple processes or threads concurrently, appropriately supported by the operating system.

* **multithreading**

88. Select two-dimensional interconnection network

* Mesh
* Linear Array
* Cross Bar

1. Single Instruction, Single Data (SISD)

* Single Instruction, Single Data (SISD) computers have one processor that handles one algorithm using one source of data at a time. The computer tackles and processes each task in order, and so sometimes people use the word "sequential" to describe SISD computers. They aren't capable of performing parallel processing on their own

1. In Parallel Computing

* **parallel computing is the simultaneous use of multiple compute resources to solve a computational problem**
* **A problem is broken into discrete parts that can be solved concurrently**
* **Each part is further broken down to a series of instructions**
* **Instructions from each part execute simultaneously on different processors**
* **An overall control/coordination mechanism is employed**

1. Pipelining …

* **Pipelining is an implementation technique where multiple instructions are overlapped in execution**.

1. Shared Memory…

* **is an extra piece of memory that is attached to some address spaces for their owners to use.**

1. What is a RISC computers?

* **RISC (reduced instruction set computer) is a microprocessor that is designed to perform a smaller number of types of computer instructions so that it can operate at a higher speed**

1. When single-processor performance improvement has dropped?

* **Since 2003**

1. How much in percentage single-processor performance improvement has dropped to less than?

* **22%**

1. What is the PMD in computer classes?

* Personal Mobile Device

1. What is the Thread Level Parallelism -

* **Exploits either data-level parallelism or task level parallelism in a tightly coupled hardware model that allows for interaction among parallel threads.**

1. What is the Request Level Parallelism(RLP)

* **exploits parallelism among largely decoupled tasks specified by the programmer or the operating system**

1. What is the Instruction Level Parallelism:

* **Exploits data-level parallelism at modest levels with compiler help using ideas like pipelinig and at medium levels using like speculative execution.**

1. What is the MISD one of the categories of computers?:

* **Multiple Instruction Streams , Multiple data Streams.**

1. How many elements in Trends of Technology? 5

* **Integrated circuit logic technology**
* **Semiconductor DRAM**
* **Semiconductor Flash**
* **Magnetic disk technology**
* **Network Technology**

1. How many elements of the Instruction Set Architecture (ISA):

* **8**

1. How many types of dependencies do you know? 3

**1) Structural Dependency  
2) Control Dependency  
3) Data Dependency**

1. How many possible Elements of Data Hazards? 3

**Structural Hazard**

**Data Hazard**

**Control Hazard**

1. What is the “ISSUE” in Pipelining Basics?

* **Decode instruction, check for structural hazard**

1. What is the “Read Operands” in Pipelining Basics?

* **Wait until no data hazards, then read operands.**

1. How many Optimizations’ in Cache memory Performance?

6

**Reducing the Miss Rate:**

* Larger Block size (Compulsory misses)
* Larger Cache size (Capacity misses)
* Higher Associativity Conflict misses)

**Reducing the Miss Penalty:**

* Multilevel Caches
* Giving Reads Priority over Writes

**Reducing the time to hit in the cache:**

* Avoiding Address Translation during Cache Indexing.

1. What is the Compulsory in main categories in Cache Memory?

* **First Reference to a block, occur even with infinite cache.**

1. What is the Capacity in main categories in Cache Memory?

* **Cache is too small to hold all data needed by program, occur even under perfect replacement policy(loop over 5 cache lines)**

1. What is the Conflict in main categories in Cache Memory?

* **Misses that occur because of collisions due to less than full associativity(loop over 3 cache lines)**

1. What is the Temporal Locality?

* **Exploit by remembering the contents of recently accessed locations.**

1. What is the Spatial Locality?

* **Exploit by fetching blocks of data around recently accessed locations.**

1. What is the Reducing the Hit time?

* **Small and simple first-level caches and way-prediction.**

1. What is the Increasing cache bandwidth?

* **Pipeland caches, multibanked caches, nonoblocked caches.**

1. What is the Reducing the Miss Penalty?

* **Critical word first and merging write buffer.**

1. What is the Reducing the Miss Rate?

* **Compiler Optimization**

1. Main term of dependability is SLAs?

* **Service Level Agreements**

1. Main term of dependability is SLOs?

* **Smith–Lemli–Opitz**

1. The second type of dependence is?

* **name dependence**

1. RAW (read after write)?

* j tries to read a source before i writes it, so j incorrectly gets the old value.

1. WAW (write after write)?

* ***j* tries to write an operand before it is written by *i*.**

1. WAR (write after read)?

* ***j* tries to write a destination before it is read by *i,* so *i* incorrectly gets the *new* value**

1. What is the element “Read Operands” in simple five-stage pipeline?
2. What is the ROB?

* **ReOrder Buffer**

1. How many steps in instruction execution? 4

* ISSUE
* **EXECUTE**
* **WRITE RESULT**
* **COMMIT**

1. How many restrictions RAW hazards through memory are maintained?

* **2**

1. How many major flavors in Multiple-issue processors? 3

* **statically scheduled superscalar processors,**
* **VLIW (very long instruction word) processors, and**
* **dynamically scheduled superscalar processors**

1. How many functions at Integrated Instruction Fetch Units 3

* **Integrated branch prediction**
* **Instruction prefetch**
* **Instruction memory access and buffering**

1. Speculation and the Challenge of Energy Efficiency consume excess energy in how many ways?

* **2 ways**

1. The hardware model represents the assumptions made for an ideal or perfect processor is as how many follow elements? 5

**The assumptions made for an ideal or perfect processor are as follows:**

**1.**

***Register renaming***

**—There are an infinite number of virtual registers available,**

**and hence all WAW and WAR hazards are avoided and an unbounded**

**number of instructions can begin execution simultaneously.**

**2.**

***Branch prediction***

**—Branch prediction is perfect. All conditional branches**

**are predicted exactly.**

**3.**

***Jump prediction***

**—All jumps (including jump register used for return and**

**computed jumps) are perfectly predicted. When combined with perfect**

**branch prediction, this is equivalent to having a processor with perfect speculation**

**and an unbounded buffer of instructions available for execution.**

**4.**

***Memory address alias analysis***

**—All memory addresses are known exactly,**

**and a load can be moved before a store provided that the addresses are not**

**identical. Note that this implements perfect address alias analysis.**

**5.**

***Perfect caches***

**—All memory accesses take 1 clock cycle. In practice, superscalar**

**processors will typically consume large amounts of ILP hiding cache**

**misses, making these results highly optimistic**

1. Infinite register renaming at The Hardware Model?

* **There are an infinite number of virtual registers available, and hence all WAW and WAR hazards are avoided and an unbounded number of instructions can begin execution simultaneously**

1. Perfect caches at The Hardware Model?

* **All memory accesses take 1 clock cycle. In practice, superscalar**

1. Perfect memory address alias analysis at The Hardware Model?

* **All memory addresses are known exactly, and a load can be moved before a store provided that the addresses are not identical All memory addresses are known exactly, and a load can be moved before a store provided that the addresses are not identical**

1. Perfect jump prediction at The Hardware Model?

* **All jumps (including jump register used for return and computed jumps) are perfectly predicted.**

1. What is Personal mobile device (PMD)?

* **Personal mobile device (PMD) is the term we apply to a collection of wireless devices with multimedia user interfaces such as cell phones, tablet computers, and so on.**

1. Where the embedded microprocessors are used?

* **These devices range from everyday machines—most microwaves, most washing machines, most printers, most networking switches, and all cars contain simple embedded microprocessors—to handheld digital devices, such as cell phones and smart cards, to video games and digital set-top boxes.**

1. What functions has Instruction Set Architecture (ISA)?
2. What is the TLP?

* **Task Level Parallesism arises because tasks of work are created that can operate independently and largely in parallel**

1. By Moore's law, growth rate in transistor count on a chip is doubling?

* **of about 40% to 55% per year.**

1. How should a system architect or a user think about performance, power, and energy? From the viewpoint of a system designer, how many concerns are there

* **First, what is the maximum power a processor ever requires**
* **Second, what is the sustained power consumption?**
* **The third factor that designers and users need to consider is energy and energy efficiency**

1. What is the “Module reliability” in Dependability?

* **is a measure of the continuous service accomplishment (or, equivalently, of the time to failure) from a reference initial instant**

1. What is response time?

* **the time between the start and the completion of an event—also referred to as *execution time*.**

1. The guiding principle of reporting performance measurements should be?

* **Reproducibility - List everything another experimenter would need to duplicate the results**

1. What is Temporal Locality?

* **Recently accessed items are likely to be accessed in the near future.**

1. What is Spatial Locality?

* **Items whose addresses are near one another, tend to be referenced close together in time.**

1. What is Amdahl's law?

* **Defines the speed up that can be gained by using a particular feature.**

1. The most popular scheme is set associative, where a set is?

* **A groups of blocks in the cache**

1. The three Cs model sorts all misses into three simple categories: Compulsory, Capacity, Conflict. What is Compulsory?

* **The very first access to a block cannot be in the cache, so the block must be brought into the cache.**

1. The three Cs model sorts all misses into three simple categories: Compulsory, Capacity, Conflict. What is Capacity?

* **If the cache cannot contain all the blocks needed during execution of a program**

1. The three Cs model sorts all misses into three simple categories: Compulsory, Capacity, Conflict. What is Conflict?

* **If the block placement strategy is not fully associative.**

1. The “natural” unit of organization of memory

**Word sizee**

1. Main element of cache memory is …

* Addresses (size)
* Tag

1. Typical levels of Cache memories …

* L1, L2,L3

1. Select internal memory …

* **register**

1. Select internal memory

* **cache**

1. Select internal memory

* **Main memory**

1. Select external memory?

* Disk magnetic tape storage devise, cards ,tape, flash cards

1. Physical types of memories:

* **Semiconductor(ram)**
* **Magnetic  surface memory(disk and tape)**
* **Optical (cd dvd)**
* **Hologram buble**

1. Select correct memory hierarchy:

* Registeer- cache-main memory-magnetic disk cd dvd- magnetic tape- worm external memory

1. External, nonvolatile memory is also referred to as …

* secondary memory or auxiliary memory

1. Types of cache addresses

* **2 logical and physical**
* 1. Fully Associative 2. Direct Mapped 3. Set Associative

1. A logical cache stores data using …

* **Virtual addresses**

1. The two basic forms of semiconductor random access memory are

* **Read and write**

1. Main element of cache memory

* **Address size function I DUNNO**

1. A number of chips can be grouped together to form …

* **Memory bank or SIIMS or DIIMS or memory moduels**

1. Data are recorded on and later retrieved from the disk via a conducting coil named

* **The head**

1. The information can then be scanned at the same rate by rotating the disk at a fixed speed, known as …

* **constant angular velocity**

1. To increase density, modern hard disk systems use a technique known as

* **Multiple zone recording**

1. … can be removed and replaced with another disk.

* **removable disk**

1. For most disks, the magnetizable coating is applied to both sides of the platter, which is then referred to as ...

* **double sided**

1. The set of all the tracks in the same relative position on the platter is referred to as …

* cylinder

1. On a movable head system, the time it takes to position the head at the track is known as …

* **seek time**

1. The operating system …

* **An os is a program that controls the execution of application programs and acts an interface between the user of a computer and computer hardware.**

1. The most important functions of the Operating System are

* **scheduling of processes or tasks**

1. The important function of the Operating System is

* **scheduling of processes or tasks**

1. How is the following service called? The Operating System provides a variety of facilities and services, such as editors and debuggers, to assist the programmer in creating programs…

* **Program creation**

1. How is the following service called? A number of tasks need to be performed to execute a program. Instructions and data must be loaded into main memory, I/O devices and files must be initialized, and other resources must be prepared. The Operating System handles all of this for the user.

* **Program execution**

1. How is the following service called? Each I/O device requires its own specific set of instructions or control signals for operation. The Operating System takes care of the details so that the programmer can think in terms of simple reads and writes.

* **Access to I/O devices**

1. How is the following service called? In the case of a shared or public system, the Operating System controls access to the system as a whole and to specific system resources.  
    System access.
2. How is the following service called? These are internal and external hardware errors, such as a memory error, or a device failure or malfunction; and various software errors, such as arithmetic overflow, attempt to access forbidden memory location, and inability of the OS to grant the request of an application. In each case, the Operating System must make the response that clears the error condition with the least impact on running applications.

* **Error detection and response**

1. How is the following service called? A good Operating System collects usage statistics for various resources and monitor performance parameters such as response time. On any system, this information is useful in anticipating the need for future enhancements and in tuning the system to improve performance.

* **Accounting**

1. Select two independent dimensions of the Operating System

* **Variation and Composition**

1. Select the ARM Memory-Management Parameter according to this description. These bits control access to the corresponding memory region. If an access is made to an area of memory without the required permissions, a Permission Fault is raised.

* **Access Permission (AP), Access Permission Extension (APX)**

1. Select ARM Memory-Management Parameter according to this description. Determines, with the TEX bits, how the write buffer is used for cacheable memory.

* **Bufferable (B) bit**

1. Select the ARM Memory-Management Parameter according to this description. These bits, together with the B and C bits, control accesses to the caches, how the write buffer is used, and if the memory region is shareable and therefore must be kept coherent.

* **Type Extension (TEX)**

1. Select the Pentium Memory Management Parameter according to this description: Specifies the privilege level of the segment referred to by this segment descriptor.

* **Descriptor Privilege Level (DPL)**

1. Select the Pentium Memory Management Parameter according to this description. Used for nonpaged systems. It indicates whether the segment is present in main memory. For paged systems, this bit is always set to 1.

* **Segment Present bit (P)**

1. Select the Pentium Memory Management Parameter according to this description. This bit is set to 1 by the processor in both levels of page tables when a read or write operation to the corresponding page occurs.

* **Accessed bit (A)**

1. Select the Pentium Memory Management Parameter according to this description. Provides the physical address of the page in memory if the present bit is set. Since page frames are aligned on 4K boundaries, the bottom 12 bits are 0, and only the top 20 bits are included in the entry. In a page directory, the address is that of a page table.

* **Page Frame Address**

1. Select the Pentium Memory Management Parameter according to this description. Indicates whether the page is available only to the operating system (supervisor level) or is available to both operating system and applications (user level).

* **User/Supervisor bit (US)**

1. Select the Pentium Memory Management Parameter according to this description. Indicates whether write-through or write-back caching policy will be used for data in the corresponding page.

* **Page Write Through bit (PWT)**

1. Convert given number from decimal to binary number system. Decimal number: -13.3125

* **-1101.0101**

1. Convert given number using sign-magnitude representation from decimal to binary number system. Decimal number (use 8 bit): -18

* **1111 1000**

1. Convert given number using sign-magnitude representation from decimal to binary number system. Decimal number (use 16 bit): -150

* **1000000010010110**

1. Convert given number using sign-magnitude representation from decimal to binary number system. Decimal number (use 16 bit): 150

* **0000000010010110**

1. Convert given number using twos complement representation from decimal to binary number system. Decimal number (use 16 bit): - 150

* **1111111101101010**

1. Convert given number using twos complement representation from decimal to binary number system. Decimal number: - 8

* **1111 1000**

1. Convert given number using twos complement representation from decimal to binary number system. Decimal number: - 7

* **1111 1001**

1. Convert given number using sign-magnitude representation from decimal to binary number system. Decimal number: - 5

* **1111 1011**

1. Subtract one number from another and show the result of the subtraction in binary. Task: 2 – 7
2. Subtract one number from another and show the result of the subtraction in binary. Task: 165 – 200
3. Subtract one number from another and show the result of the subtraction in binary. Task: 950 -1100