United International University
Department of CSE
CSE 313: Computer Architecture
Final Examination
Fall 2021

Time: 2 Hours **Full Marks: 40**

[Any examinee found adopting unfair means will be expelled from the trimester / program as per UIU disciplinary rules.]

[N.B.: Answer all the questions. Assume any data if it is not mentioned explicitly.]

<table>
<tr><td>1.</td><td>a) Modify the block diagram for single-cycle datapath so that it can execute the following instruction “sa”. Note that, this instruction saves the address(2000) onto the PC register if the source register($s1) is greater than the source register($s2).
sa $s1,$s2, 2000

Also write down the control unit values for this instruction.</td><td>[5]</td></tr>
<tr><td></td><td>b) Modify the block diagram for a single-cycle data path and write down the control unit values for the following instruction “str”. The job of the given instruction is to store to the destination register($t0). It compares the two source registers ($s0 &$s1) and if they are equal it stores ‘0’ otherwise it stores ‘1’.
str $t0, $s0, $s1</td><td>[5]</td></tr>
<tr><td>2.</td><td>a) Consider a processor that goes through the following six stages to implement the “lw” instruction that you have studied in class. The time for each stage (in ps) is also shown in the table.
<table>
<tr><th>IF (Instruction Fetch)</th><th>ID (Instruction Decode)</th><th>RR(Register Read)</th><th>EXE (ALU Execution)</th><th>MEM (Memory Access)</th><th>WB (Register Write Back)</th></tr>
<tr><td>200</td><td>50</td><td>75</td><td>175</td><td>200</td><td>100</td></tr>
</table>
a) State the clock cycle time (T_c) for the single cycle implementation of such a processor. Using the value of T_c, calculate the total time taken for the following instructions to execute (Given that, initially, the register $s0 contains 50, and the register $s1 contains 0).

loop:
beq $s0, $0, exit
add $s1, $s1, $so
addi $s0, $s0, -10
j loop
exit:</td><td>[5]</td></tr>
</table>

	b) Suppose you have now implemented **basic pipelining** in this processor. Consider the following piece of code. *add $s0, $s0, $t1* *sub $s0, $s0, $t2* *lw $s1, 20($t3)* *add $s2, $s1, $s0* A friend of yours explains the following about the execution time of this code: *"The clock cycle time of the pipelined processor will be 50 ps, since this is the minimum time taken by any individual stage. The first instruction will require six clock cycles, and every following instruction will require one additional cycle. The total number of clock cycles will therefore be 6 + 1 + 1 + 1 = 9. The execution time of this code will therefore be 9 * 50 = 450 ps."* You are worried your friend may not pass their final examination. Explain why your friend is wrong. In your answer, clearly mention the **reasons** that your friend is wrong, along with the correct values of **the clock cycle time of the processor**, **the number of clock cycles required for the given code to execute, and the total time taken for this code**. **Include a timing diagram/s** as well.	[5]
	c) Suppose you have now implemented **bypassing** in your pipelined processor. State and explain the modified time required for the code in part (b) to execute. You should include a timing diagram in your answer.	[3]
	d) Explain how the execution time of the code in (b) can be improved **further** after bypassing has been implemented.	[2]
3.	a) Consider a cache memory of size **4KB** and block size having **4 words** (1 word = 4 bytes). Determine the miss rate if the following bytes are addressed sequentially. **1, 2, 10, 4097, 4098, 15**	[5]
	b) If we **change the block size** in Q3(a) to **8 words**, find out the miss rate for similar memory address access. Find out the miss rate.	[5]
	c) Compare the miss rate in Q3(a) & Q3(b) and explain the **principle of locality**.	[3]
	d) If the block size in **16 words** then find the actual size of the cache in unit of bit.	[2]