

Figure 01: Output Voltage versus Output Current Graph for Resistive, Inductive and Capacitive Load (D-Connection)

VR vs (I_2) Graph for Resistive, Inductive and Capacitive Load

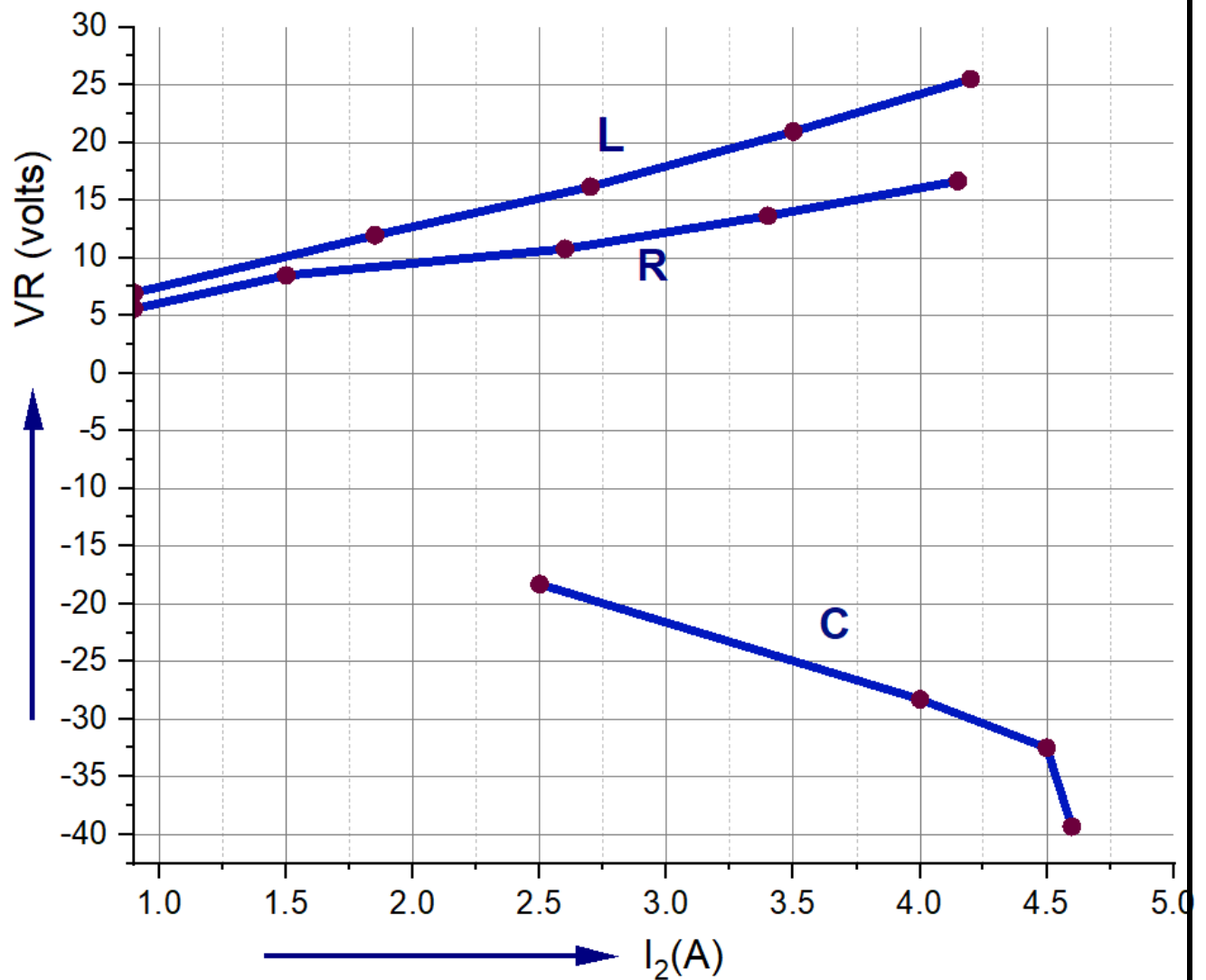


Figure 2: Voltage Regulation (VR) vs Currents (I_2) Graph for Resistive, Inductive and Capacitive Load (D-Connection)