

****Quick Start****

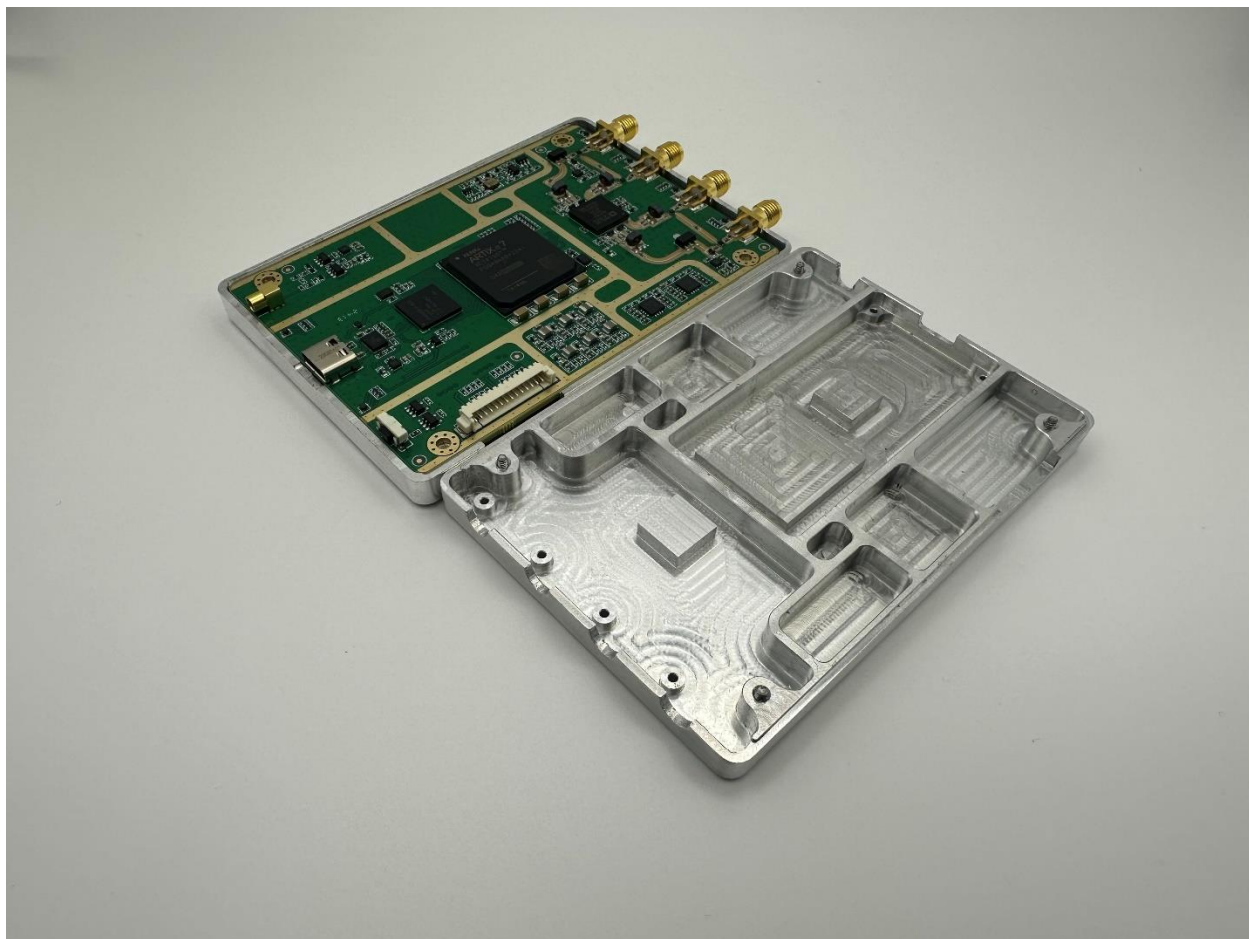
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****Overview****

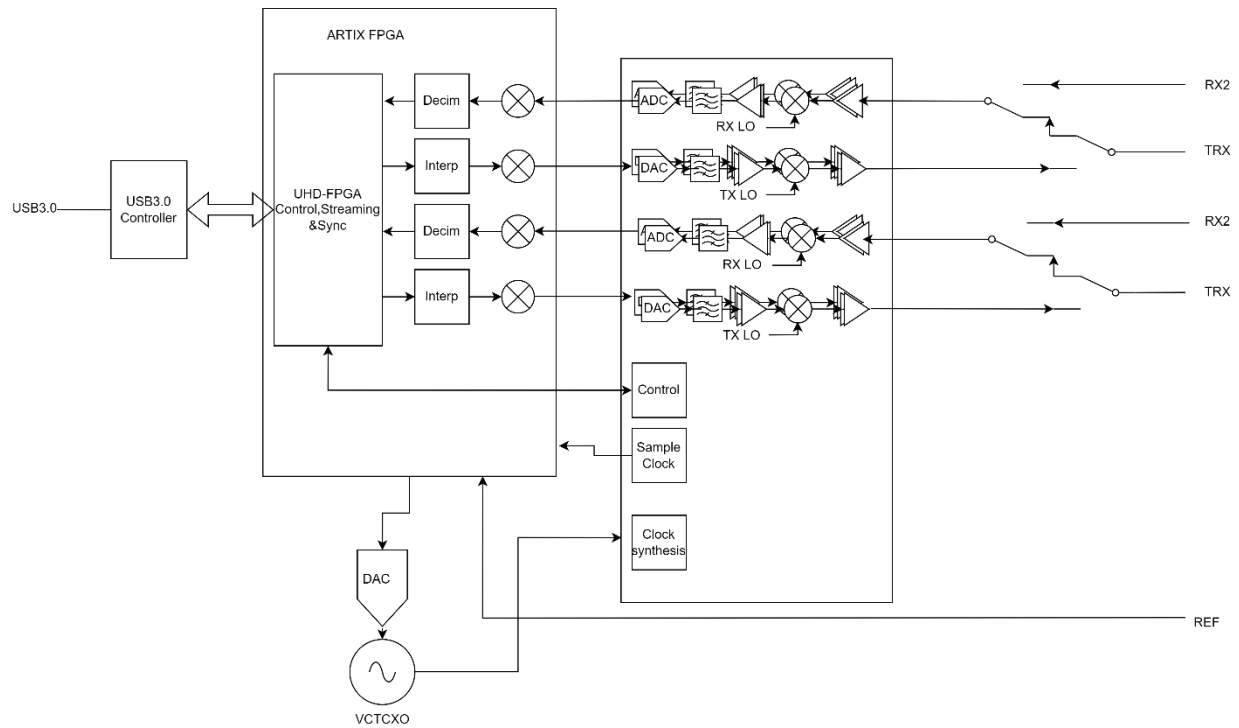
The B210/B220mini primarily utilizes the A7 series FPGA to replace the S6 series, enhancing performance and reducing power consumption while optimizing the PCB design to reduce volume. It combines the advantages of B210 and B205mini, with a software interface fully compatible with UHD¹.

- Maximum bandwidth of 56MHz, with a sampling rate of 61.44MHz
- USB3.0 interface, backward compatible with USB2.0 interface
- Adopts XC7A200T/XC7A100T for more advanced chip technology and resources
- Features a Type-C interface
- Supports PPS/10MHz synchronization
- Fully compatible with UHD interface
- Tested and fully supports UHD, Matlab/Simulink, Labview, SDRangel, Gnuradio, OAI, DroneSecurity





*****Figure 1 B210min PCBA and Housing Display*****

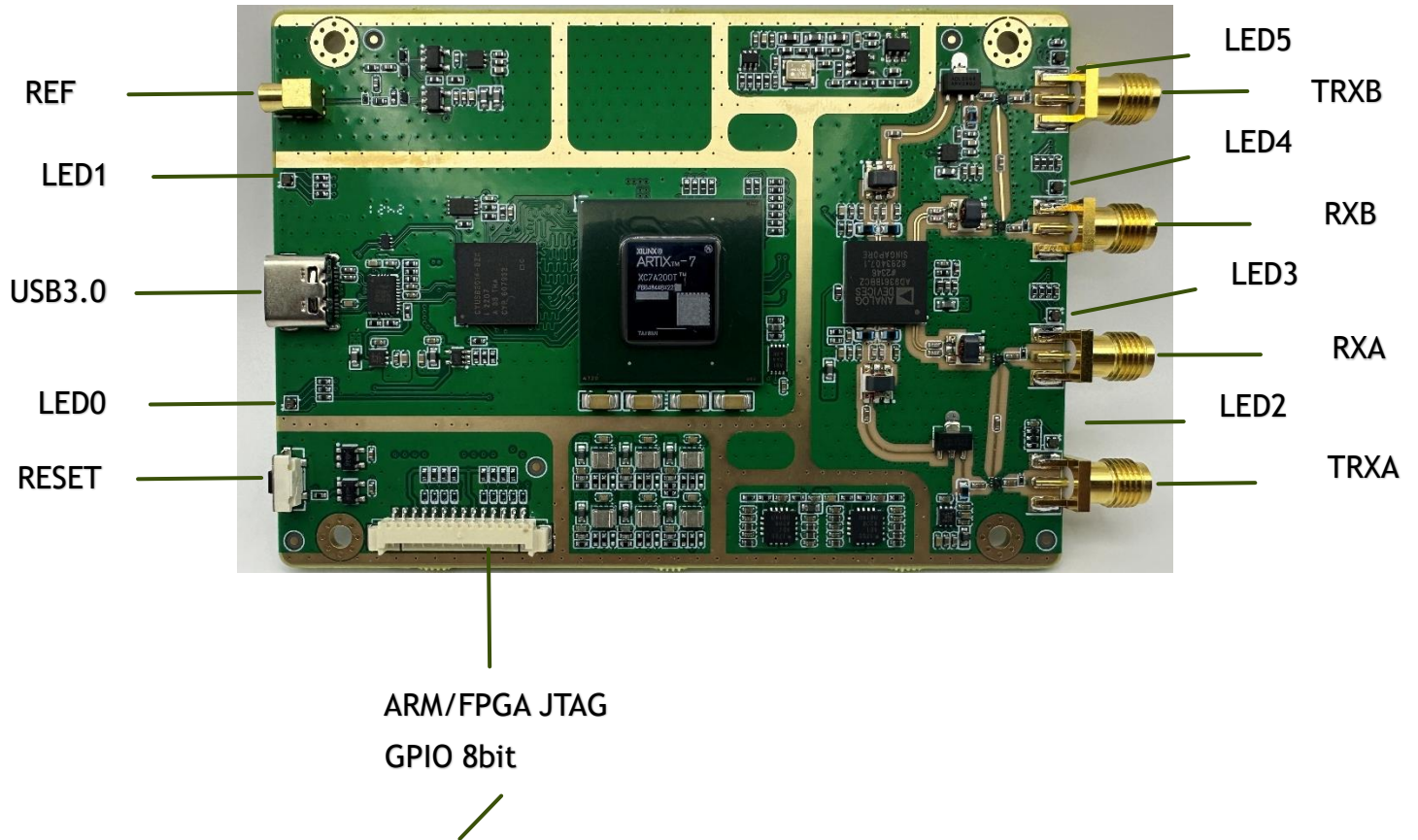


****Figure 2 Block Diagram****

1. You will need to replace the FPGA configuration bin file.

(The FPGAs for B210mini and B220mini are not compatible; please replace them with different FPGA files for each.)

port



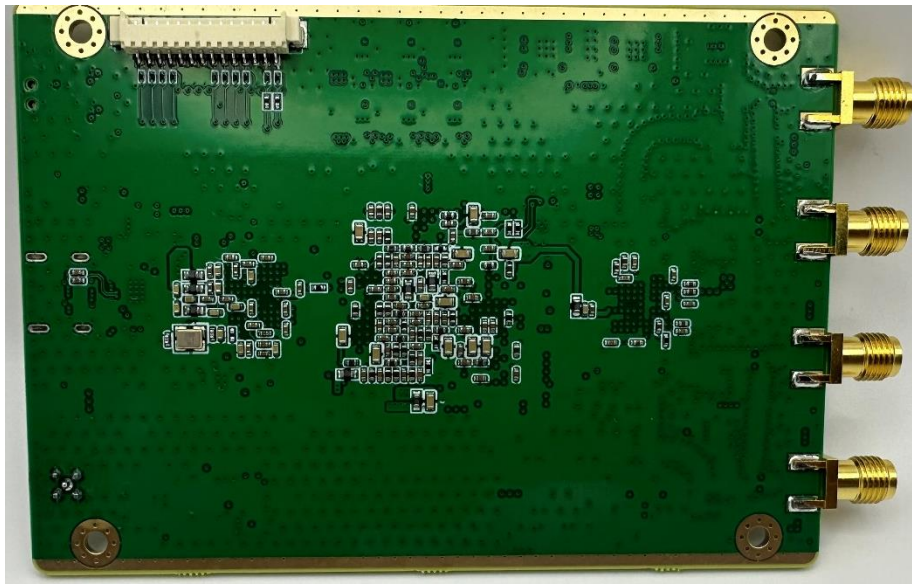


Figure 3 Interface Definition Diagram

Table 1 Interface, Indicator, Button Function Table

Type	Name	Function	Note
Interface	USB3.0 interface	Communication interface with the computer	Backward compatible with USB2.0, it is recommended to use a USB3.0 or higher interface to ensure sufficient current for the PA
	REF Interface	10M or PPS Input Interface	10M or PPS will be automatically recognized, and the indicator will show 10M or PPS. 10M can lock the local clock, and PPS can lock the local PPS and clock

	TRXA port	Transmit and Receive Interface A	This port can operate in receive or transmit mode
	RXA port	Receive Port A	Receive mode
	TRXB port	Transmit and Receive Interface B	This port can operate in receive or transmit mode
	RXB port	Receive Port B	Receive mode
	JTAG	FX3 and FPGA JTAG	For FX3 firmware and FPGA debugging
	GPIO	GPIO pins	
Indicator	LED0 Indicator	Power, configuration, clock indicator	Green -> Power normal (This indicator light means that all power rails inside the board are powered, and all power rails provide PG detection) Red -> FPGA is correctly configured with bit file Blue -> Current reference is 10M
	LED1 Indicator	PPS, clock lock work indicator	Green -> Green is the internal PPS pulse indicator,

			when an external PPS input, this PPS and external synchronization Blue -> Frequency lock signal
	LED2 Indicator	TRXA work indicator	Red -> The port is currently working in the transmission state Green -> The port is currently working in the reception state
	LED3 Indicator	RXA work indicator	Green -> The port is currently working in the reception state
	LED4 Indicator	TRXB work indicator	Red -> The port is currently working in the transmission state Green -> The port is currently working in the reception state
	LED5 Indicator	RXB work indicator	Green -> The port is currently

			working in the reception state
Button	RST Button	System reset button	Pressing will reset the system

****Start Using****

Currently, after testing, it can support the following software ecosystems:

- UHD
- GNURADIO
- SDRAngel (open-source SDR software)
- OpenAirInterface (open-source 5G protocol stack)
- MATLAB/Simulink
- DroneSecurity (DJI drone DroneID detection software)
- gnss-sdr
- Labview
- ...

The B210/B220mini uses the UHD interface to support a rich software ecosystem. No matter what system or software environment you are in, the only thing you need to do is replace the original S6 FPGA configuration file with the FPGA configuration file we provide.

It should be noted that there is a certain matching relationship between the version number of the UHD driver's FX3 firmware and the FPGA. If you encounter a prompt that the firmware version and the FPGA version do not match, please contact me to customize a lower version FPGA configuration file for you. The mainstream and latest versions do not have this problem, and you can also update your UHD driver to a higher version before using it.

****Linux UHD Driver Installation and bin File Replacement****

For first-time users, it is recommended to use the package manager and use the PATCH script to replace the bin file directly.

The steps to install UHD on Ubuntu 20.04 are as follows:

- Open the terminal.
- Add the UHD PPA (Personal Package Archive): ``sudo add-apt-repository -y ppa:ettusresearch/uhd``
- Update the list of software packages: ``sudo apt update``
- Install the UHD software package: ``sudo apt install -y libuhd-dev uhd-host``
- Install UHD firmware: ``sudo uhd_images_downloader``
- Copy the provided patch folder to any directory.
- Use the patch.sh script in the folder to update the local FPGA configuration file (you need to add execution permissions and run with sudo permissions ``chmod +x patch.sh`` ``sudo ./patch.sh``)
- Verify whether UHD is correctly installed: ``uhd_find_devices``

After installation, you can test whether the installation is successful by entering ``uhd_find_devices`` in the terminal.

For some versions of GNURADIO, the UHD driver is provided independently, not using the system UHD driver. The python-uhd is also an independent driver. If you encounter a situation where the FPGA cannot be configured after configuring the driver and running the application, run the patch.sh script again.

****Windows Installation****

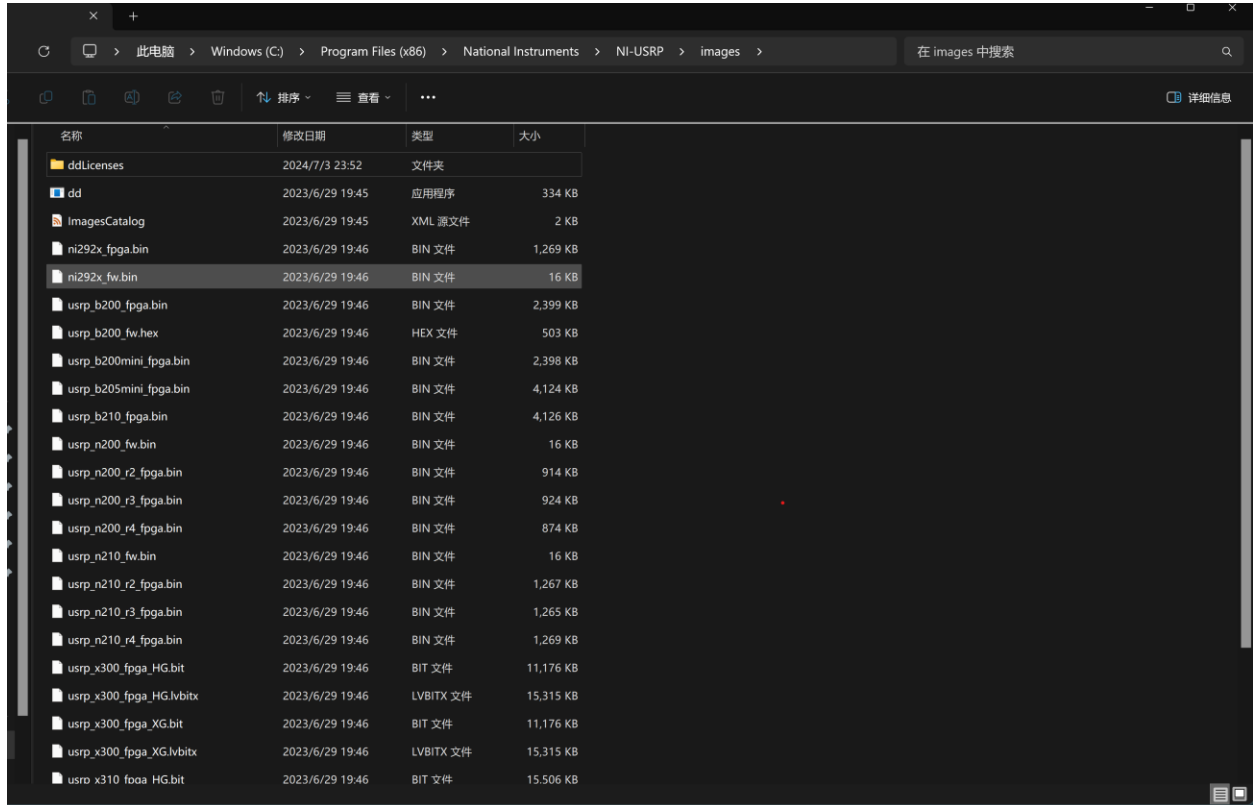
To maximize the performance of the B2x0mini series, it is recommended to use a native Linux system. Due to the performance issue of Libusb in Windows, the performance is only half of that in Linux. The performance in a virtual machine is the same as the host.

The approach in Windows is the same. Before installation and operation, use the bin file provided in the Windows folder to replace the corresponding ``usrp_b210_fpga.bin`` in the directory.

You also need to replace it for each tool independently in Windows!

****NI Software Path****

`C:\Program Files (x86)\National Instruments\NI-USRP\images`



****Figure 4 NI USRP bin file directory****

After replacement, use the UHD tool under the utilities of NI's `C:\Program Files (x86)\National Instruments\NI-USRP\utilities` to verify.

```
Windows PowerShell
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Install the latest PowerShell for new features and improvements! https://aka.ms/PSWindows

PS C:\Program Files (x86)\National Instruments\NI-USRP\utilities> .\uhd_usrp_probe.exe

-----
Device: B-Series Device
-----
Mboard: B210
revision: 4
product: 2
name: LibreSDR
serial: 7AG8U78
FW Version: 8.0
FPGA Version: 16.0

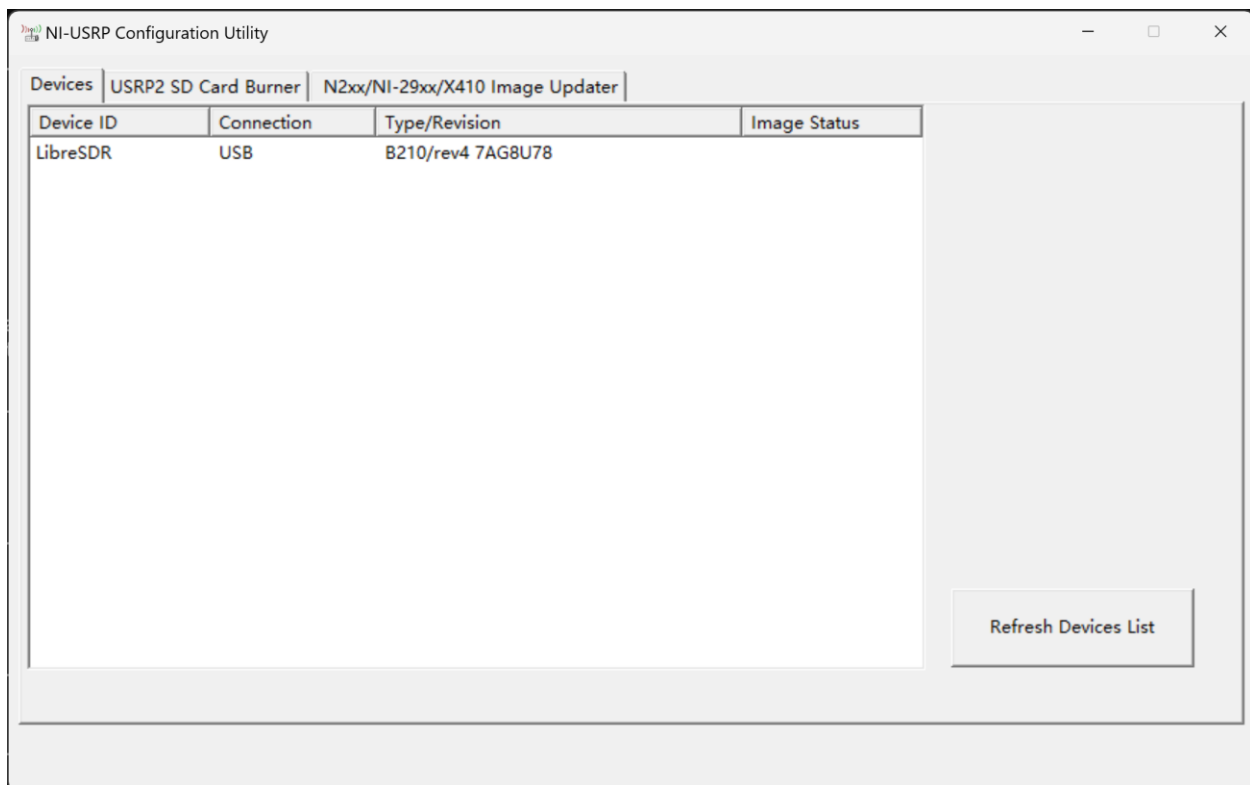
Time sources: none, internal, external, gpsdo
Clock sources: internal, external, gpsdo
Sensors: ref_locked

-----
RX DSP: 0
Freq range: -8.000 to 8.000 MHz

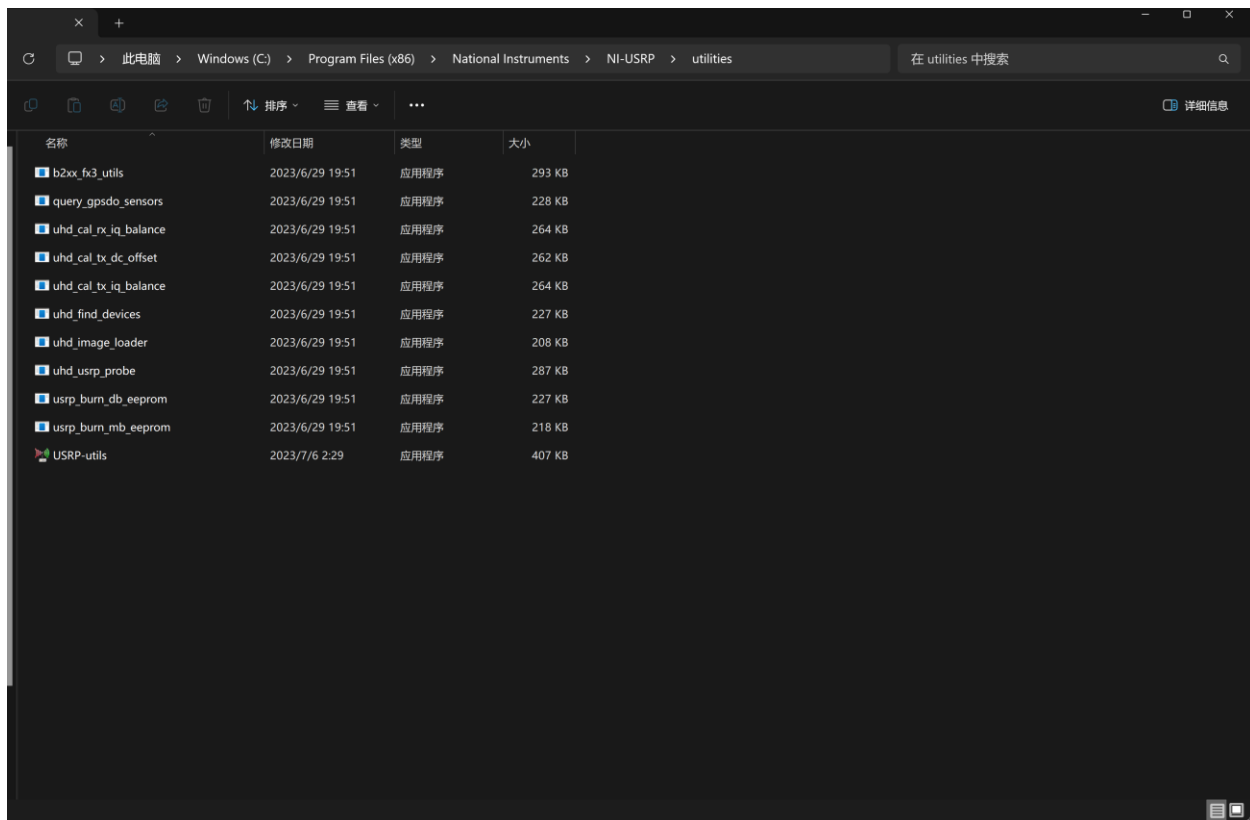
-----
RX DSP: 1
Freq range: -8.000 to 8.000 MHz

-----
RX Dboard: A
-----
RX Frontend: A
Name: FE-RX2
Antennas: TX/RX, RX2
Sensors: temp, rssi, lo_locked
Freq range: 50.000 to 6000.000 MHz
Gain range PGA: 0.0 to 76.0 step 1.0 dB
Bandwidth range: 200000.0 to 56000000.0 step 0.0 Hz
Connection Type: IQ
Uses LO offset: No
```

****Figure 5 uhd_usrp_probe****



****Figure 6 NI-USRP ConfigurationUtility****

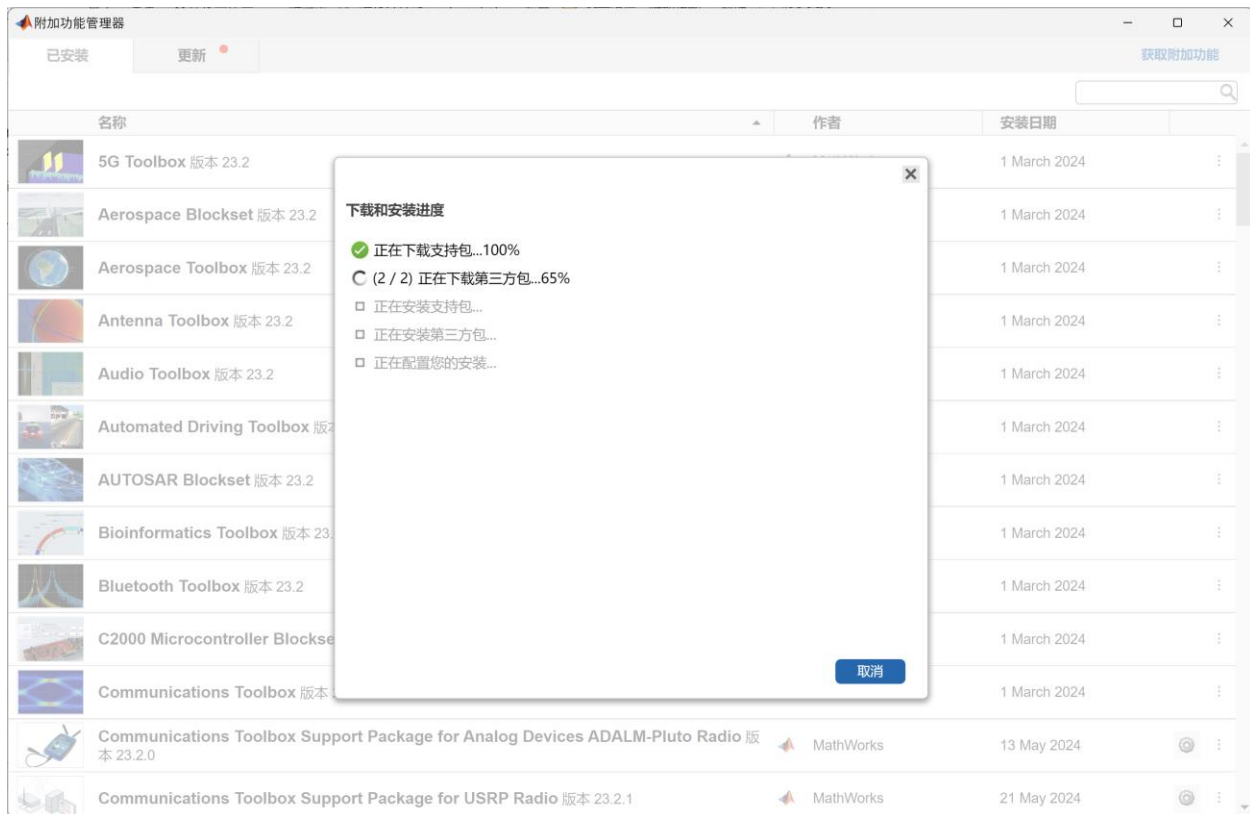


****Figure 7 NI-USRP utilities****

****MATLAB****

Before testing in MATLAB, do not connect the device. The first time, because you need to install the Winusb driver, connecting the device will be stuck. Connect the hardware in the test interface, and replace the bin file before testing.

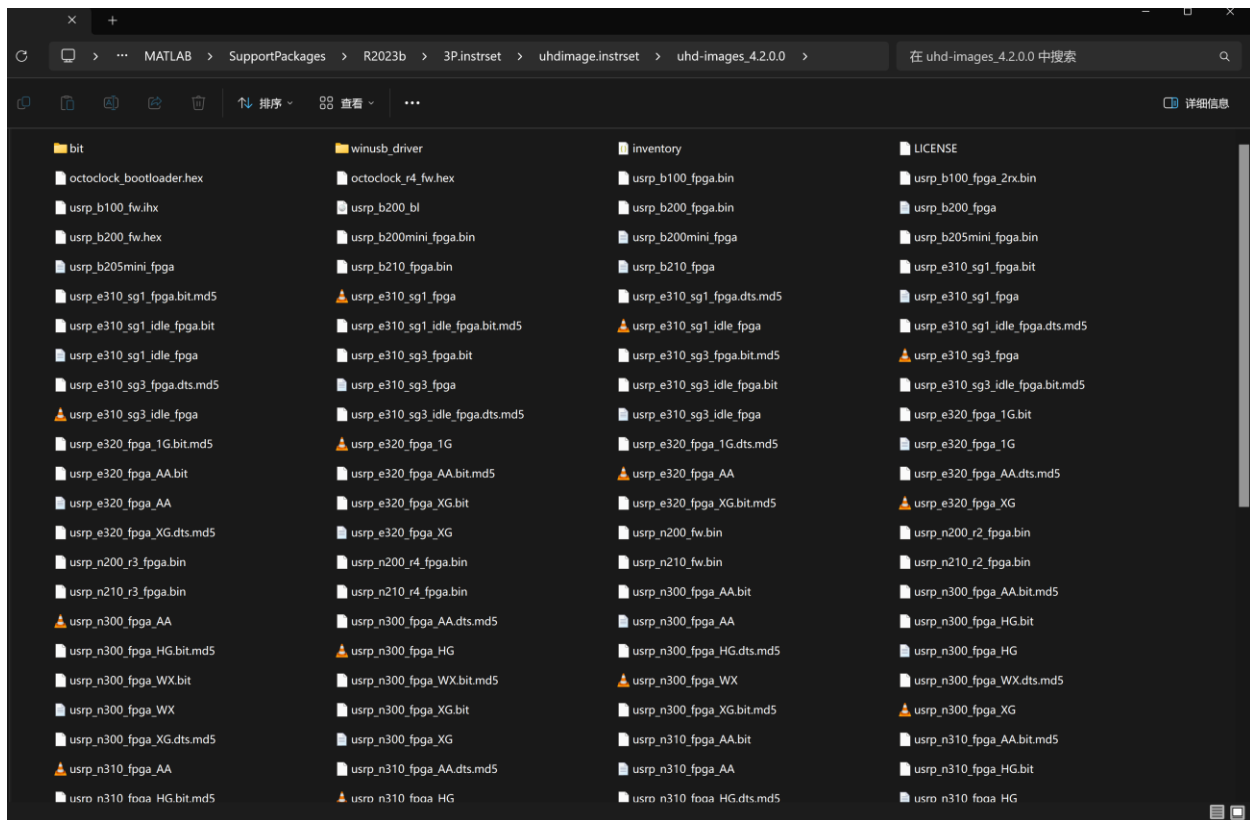
The XC7A200T has a larger logic scale and requires a longer time for configuration, please be patient.



****Figure 8 MATLAB usrp toolbox****

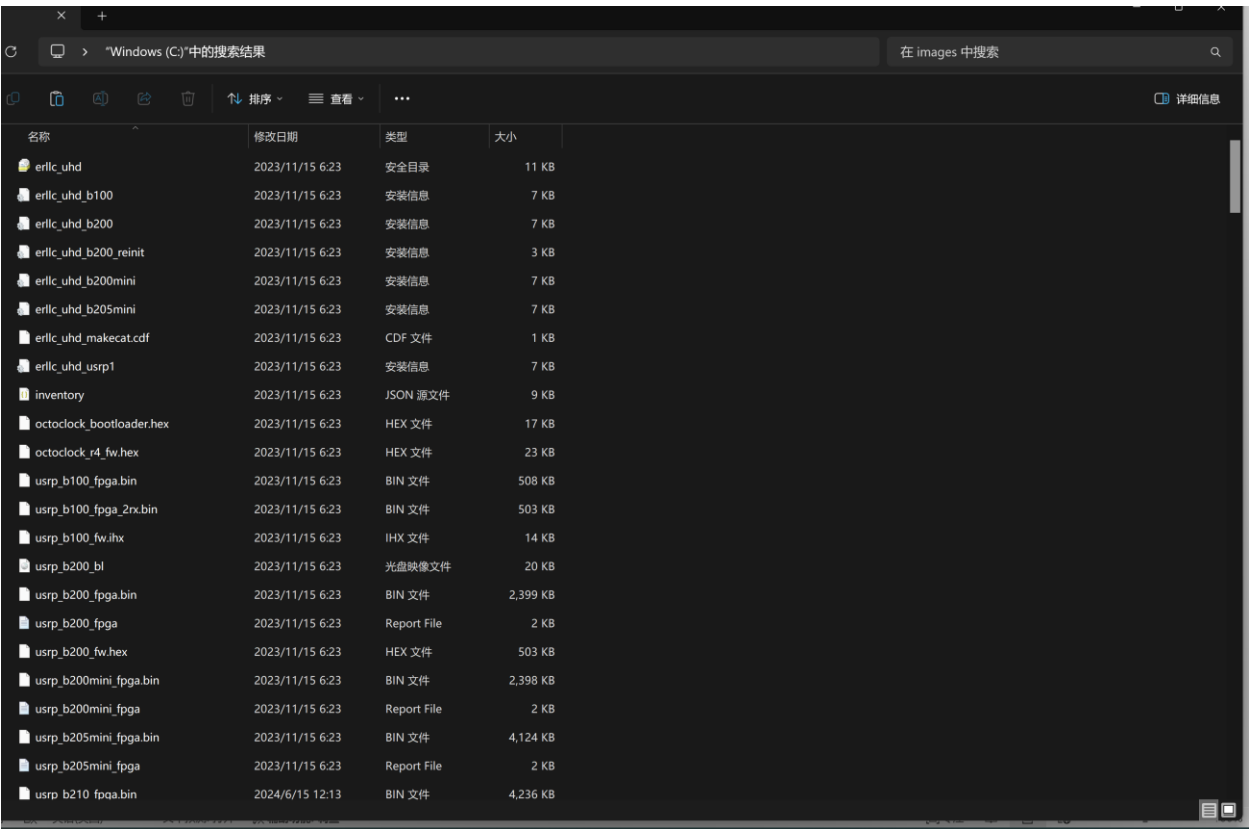
Toolbox path:

`C:\ProgramData\MATLAB\SupportPackages\R2023b\3P.instrset\uhdimage.instrset\uhd-images_4.2.0.0` (This path is hidden)



****Figure 9 MATLAB toolbox replacement path****

****UHD Driver****



名称	修改日期	类型	大小
erlfc_uhd	2023/11/15 6:23	安全目录	11 KB
erlfc_uhd_b100	2023/11/15 6:23	安装信息	7 KB
erlfc_uhd_b200	2023/11/15 6:23	安装信息	7 KB
erlfc_uhd_b200_reinit	2023/11/15 6:23	安装信息	3 KB
erlfc_uhd_b200mini	2023/11/15 6:23	安装信息	7 KB
erlfc_uhd_b205mini	2023/11/15 6:23	安装信息	7 KB
erlfc_uhd_makecat.cdf	2023/11/15 6:23	CDF 文件	1 KB
erlfc_uhd_usrp1	2023/11/15 6:23	安装信息	7 KB
inventory	2023/11/15 6:23	JSON 源文件	9 KB
octoclock_bootloader.hex	2023/11/15 6:23	HEX 文件	17 KB
octoclock_r4_fw.hex	2023/11/15 6:23	HEX 文件	23 KB
usrp_b100_fpga.bin	2023/11/15 6:23	BIN 文件	508 KB
usrp_b100_fpga_2rx.bin	2023/11/15 6:23	BIN 文件	503 KB
usrp_b100_fw.ihx	2023/11/15 6:23	IHX 文件	14 KB
usrp_b200_bl	2023/11/15 6:23	光盘映像文件	20 KB
usrp_b200_fpga.bin	2023/11/15 6:23	BIN 文件	2,399 KB
usrp_b200_fpga	2023/11/15 6:23	Report File	2 KB
usrp_b200_fw.hex	2023/11/15 6:23	HEX 文件	503 KB
usrp_b200mini_fpga.bin	2023/11/15 6:23	BIN 文件	2,398 KB
usrp_b200mini_fpga	2023/11/15 6:23	Report File	2 KB
usrp_b205mini_fpga.bin	2023/11/15 6:23	BIN 文件	4,124 KB
usrp_b205mini_fpga	2023/11/15 6:23	Report File	2 KB
usrp_b210_fpga.bin	2024/6/15 12:13	BIN 文件	4,236 KB

*****Figure 10 UHD driver replacement bin file path*****

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