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Exam 3

Q.1.

Ram access time = 30ns

TLB lookup time = 4ns

TLB miss rate = 11%

TLB Hit rate = 100-11 = 89%

Effective time = 0.89(4+30) + 0.11(4+30+30)

= 30.26 + 7.04

=37.3ns

Q.2

Hit rate = 80% = 0.8

Miss rate = 20% = 0.2

Main memory access time = 200ns

TLB access time = 80 ns

Effective time = 0.8(200 + 80) + 0.2(80+200+200)

=224 + 96 = 320ns

Q.3

TLB lookup time = 8ns

Memory Access time = 40ns

TLB miss rate to achieve memory access time of 60ns = ?

Let the hit rate to achieve the memory access time of 60ns be x.

Then miss rate = 1-hitrate

Now,

x(8+40) + (1-x)(8+40+40) = 60

48x + 88 - 88x = 60

x = 28/40

Therefore, miss rate = 1-(28/40) = 3/10 = 0.3

In percentage, 30 percent is the required miss rate.

Q.4

Given virtual address is subdivided as follows: 5|5|10|12

From here, we can see Page offset = 12.

So, Page size = 2^12 = 2^2 \* 2^10 = 4KB

Process Size to consider = 256KB

Since we know page size = frame size. So, frame size = 4KB

Now, No. of pages to run the process = 256KB/4KB

= 64 pages

We are given that each page entry size is 4B and we have 3-level page table.

So, Page table size = (No. of pages \* page entry size) + page pointer on PT1 + page pointer on PT2

= 64 \* 4 + 4 + 4

= 264B

Q.5

Given machine is a 32-bit machine and 12 higher order bits are used for page index

So,

Number of pages = 2^12

Page offset = 32-12 = 20

So, Page size = 2^20 = 1MB

We know, Page size = frame size = 1MB and we have 16GB RAM.

So, No. of frames = RAM size/frame size

=16GB/1MB

= (16 \* 2^30)/2^20

=16 \* 2^10

= 2^14 frames

Frame size = Page size = 1MB