UNIT 5

Reduced Instruction set Computer

CISC characteristics:- Complex inst'n set Computer

1) A large no. of instn's typically from 100 to 250 inst'ns.

2) Some instn's that perform specialized tasks and are used infrequently.

3) A large variety of addressing modes typically from 5 to 20 different modes.

4) Variable length instruction formats.

5) Instructions that manipulate operands in memory.

RISC characteristics: Reduced inst'n set Computer

1) Relatively few instn's

2) Relatively few addressing modes

3) Memory access limited to load & store instn's

4) All operations done with in the reg's of the CPU.

5) Fixed length, easily decoded inst'n format

6) Single cycle inst'n execution

7) Hardwired rather than microprogrammed Control.

Tightly Coupled processors & loosely Coupled processor

→ Multiprocessors are classified by the way their memory is organized.

→ A multiprocessor with common shared memory is called shared memory (or) tightly coupled multiprocessors. This doesn't preclude each processd from having its own local memory.

→ In loosely coupled (or) Distributed memory, each processd has its own local memory.

Intel Connection structures

→ The components that form a multiprocessor system are CPU's, IOP's connected to i/p-o/p devices and a memory unit may be partitioned into a no. of seperate modules.

→ The intel connections b/n the components can have different physical configurations, depending on the no. of

transfer paths that are available b/n the processors & memory in a shared memory system or among the processing elements in a loosely coupled system.

→ There are several physical forms available for establishing an interconnection network.

1. Time shared common bus
2. multiport memory
3. Crossbar switch
4. multistage switching network
5. Hypercube system.

Time shared Common Bus:

→ A common bus multiprocessor system consists of a no. of processors connected through a common path to a memory unit.

→

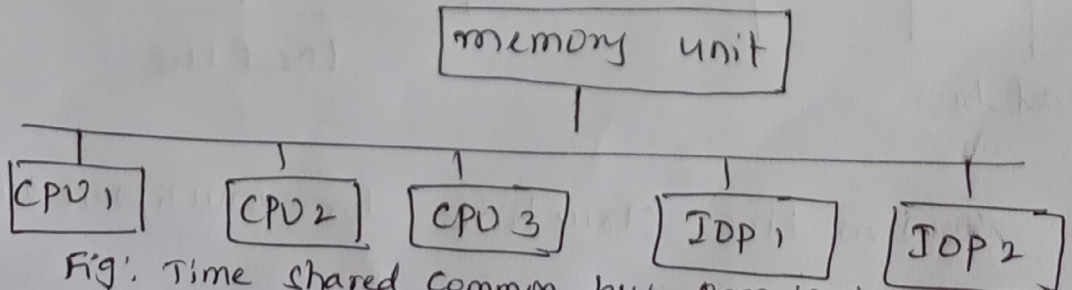


Fig: Time shared common bus organization

→ Only one processor can communicate with the memory (or) another processor at any given time.

→ Transfer operations are conducted by the processor that is in control of the bus at the time. Any other processor wishing to initiate a transfer must first determine the availability status of the bus and only after the bus becomes available can the processor address the destination unit to initiate the transfer.

→ A single common bus system is restricted to one transfer at a time.

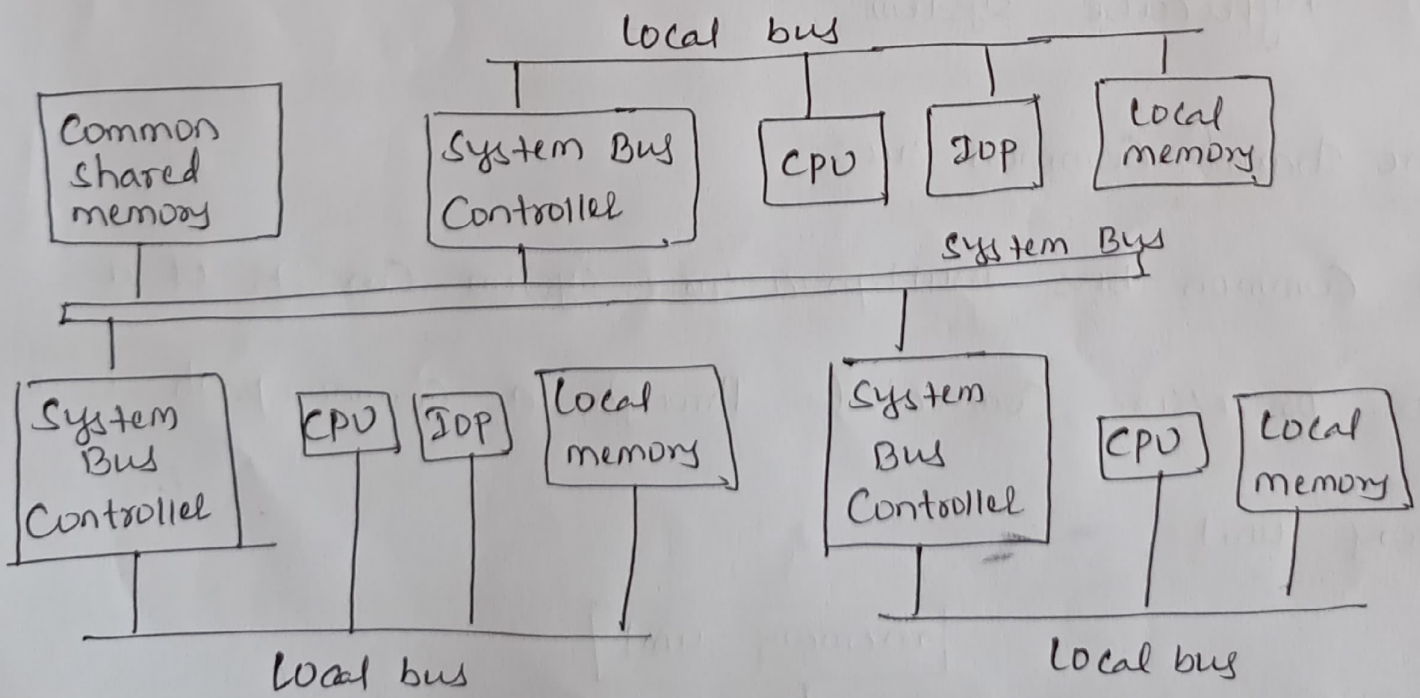
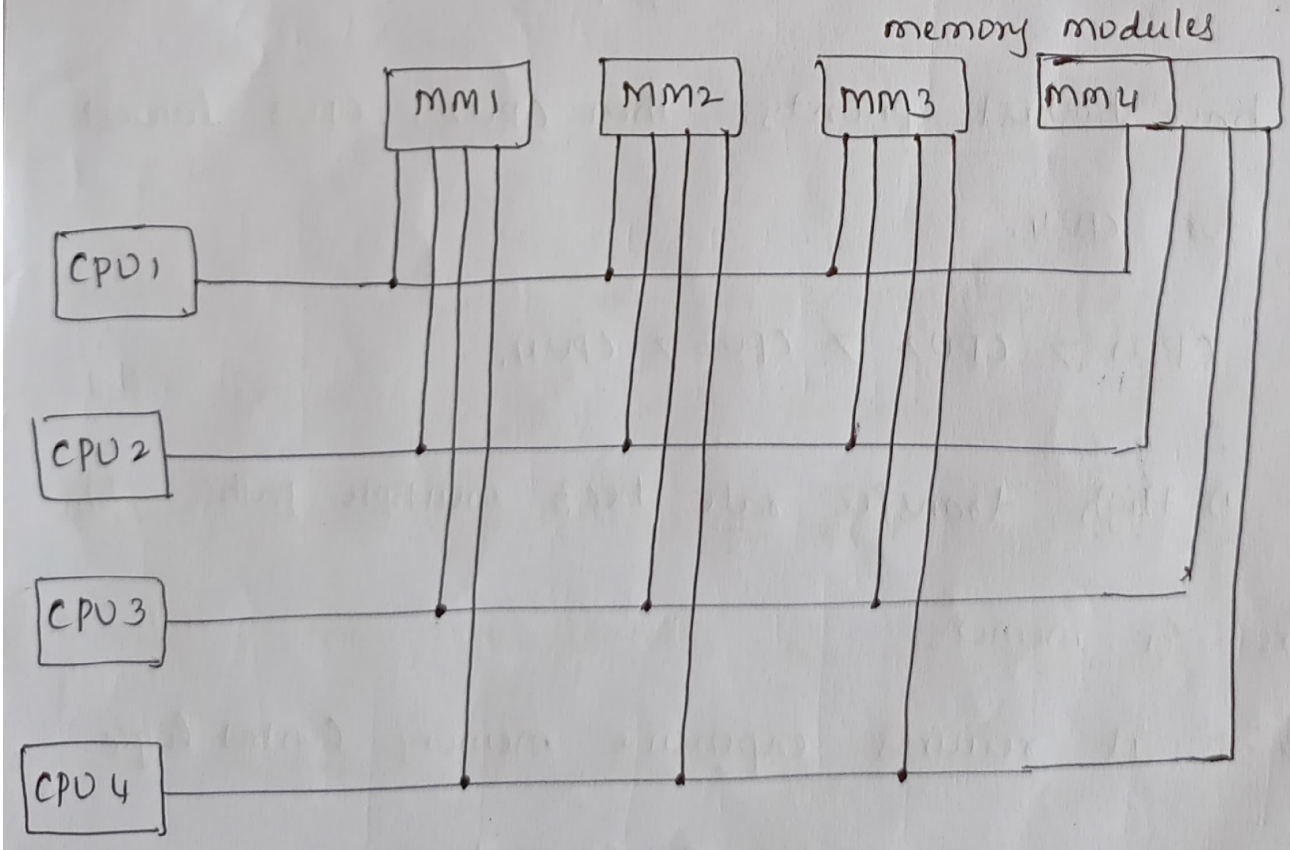


Fig: System bus structure for multiprocessors

→ No. of local buses each connected to its own local memory and to one (or) more processors. Each local bus may be connected to a CPU an IOP (or) any combination of processors. A system bus controller links each local bus to a common system bus.

2. Multiport memory

→ A multiport memory system employs seperate buses b/n each memory module and each CPU.



→ Each processor is connected to each memory module. A processor bus consists of the addr., data, control lines required to communicate with memory.

→ Each memory module have four ports & each port accommodates one of the buses. The memory module must have internal control logic to determine which port will have access to memory at any given time.

→ memory access conflicts are resolved by assigning fixed priorities to each memory port.

→ CPU1 have highest priority, then CPU2, CPU3, lowest priority for CPU4.

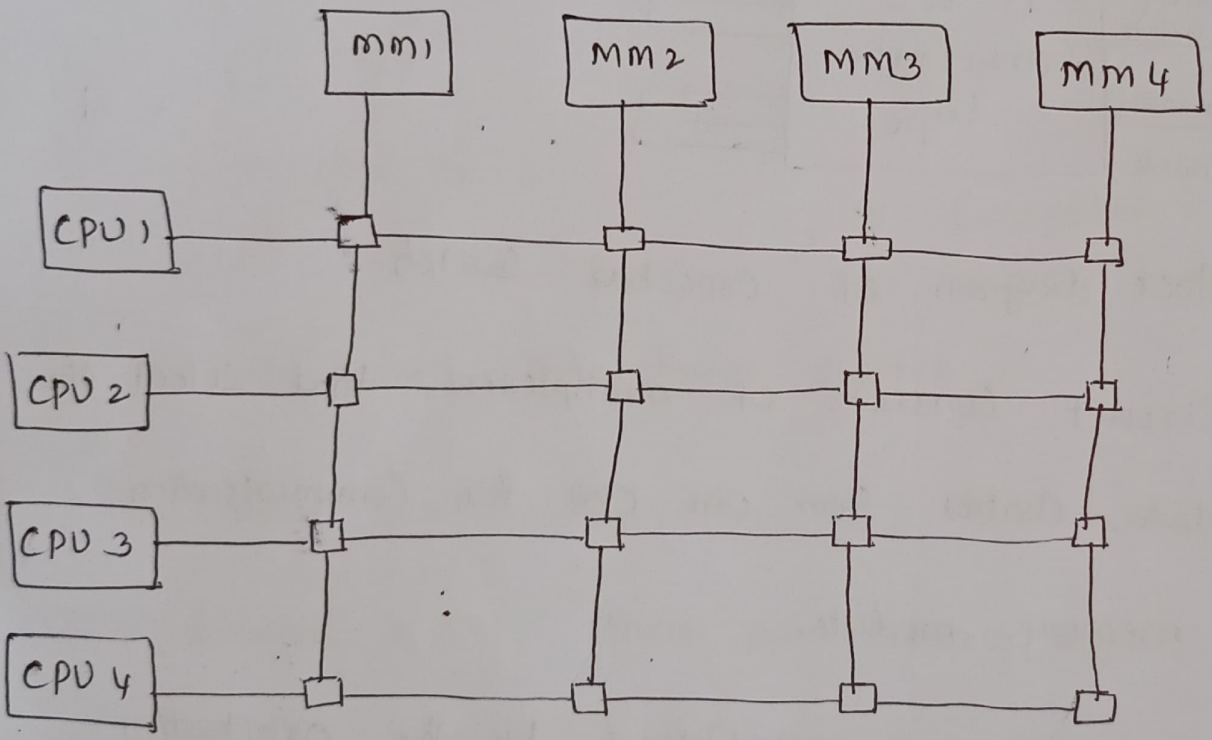
CPU1 > CPU2 > CPU3 > CPU4.

Adv:- 1) High transfer rate bec3 multiple paths b/n processors & memory.

Dis adv:- It requires expensive memory control logic and a large no. of cables & connectors.

3. Cross bar switch

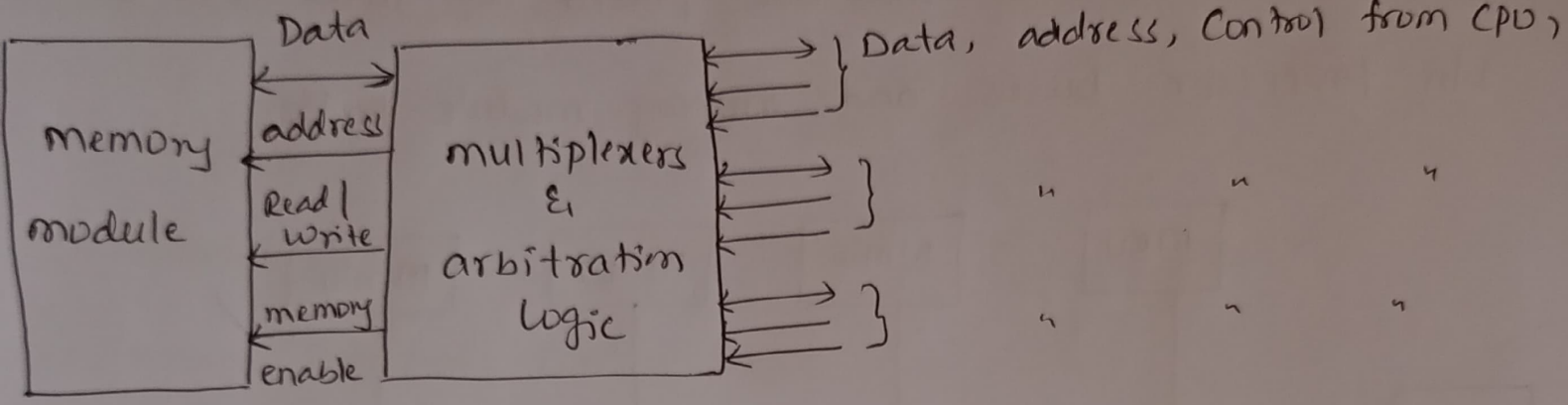
→ Cross bar switch organization consists of a no. of cross points that are placed at intersections b/n processor buses and memory module paths.



→ The small square in each cross point is a switch that determines the path from a processor to a memory module. Each switch point has control logic to setup the transfer path b/n a processor & memory.

→ It examines the address that is placed in the bus to determine whether its particular module is being addressed. It also resolves multiple requests for

access to the same memory module on a predetelmined priority basis.



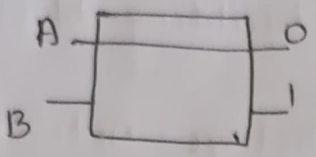
Block diagram of crossbal switch

→ The Circuit consists of multiplexers, that select the address, data, Control from one CPU for Communication with the memory module.

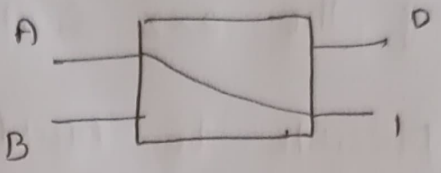
→ priority levels are established by the arbitration logic to select one CPU when two or more CPU's attempt to access the same memory.

4. Multistage Switching Network

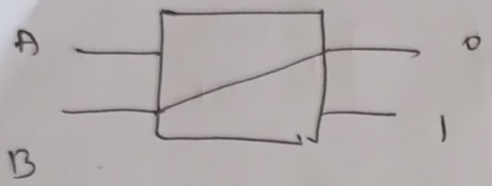
→ The basic Component of a multistage N/W is a two i/p-two o/p intelchange switch.



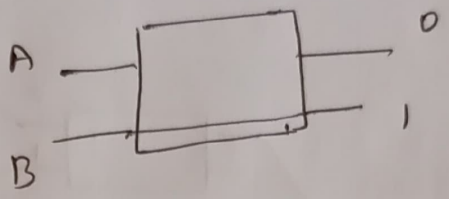
A Connected to 0



A Connected to 1



B Connected to 0



B Connected to 1

Fig: 2×2 interchange switch

→ The 2×2 switch has two i/p's labled A & B, two o/p's labeled 0 & 1. There are control signals (not shown) associated with the switch that establish the interconnection b/n the i/p & o/p terminals.

→ The switch has the capability of connecting i/p A to either of the o/p's. Terminal B of the switch behaves in a similar fashion.

→ If i/p A & B both request the same o/p terminal, only one of them will be connected & other will be blocked.

→ Using the 2×2 switch as a building block, it is possible to build a multistage network to control the comm'n b/n a no. of sources & destinations.

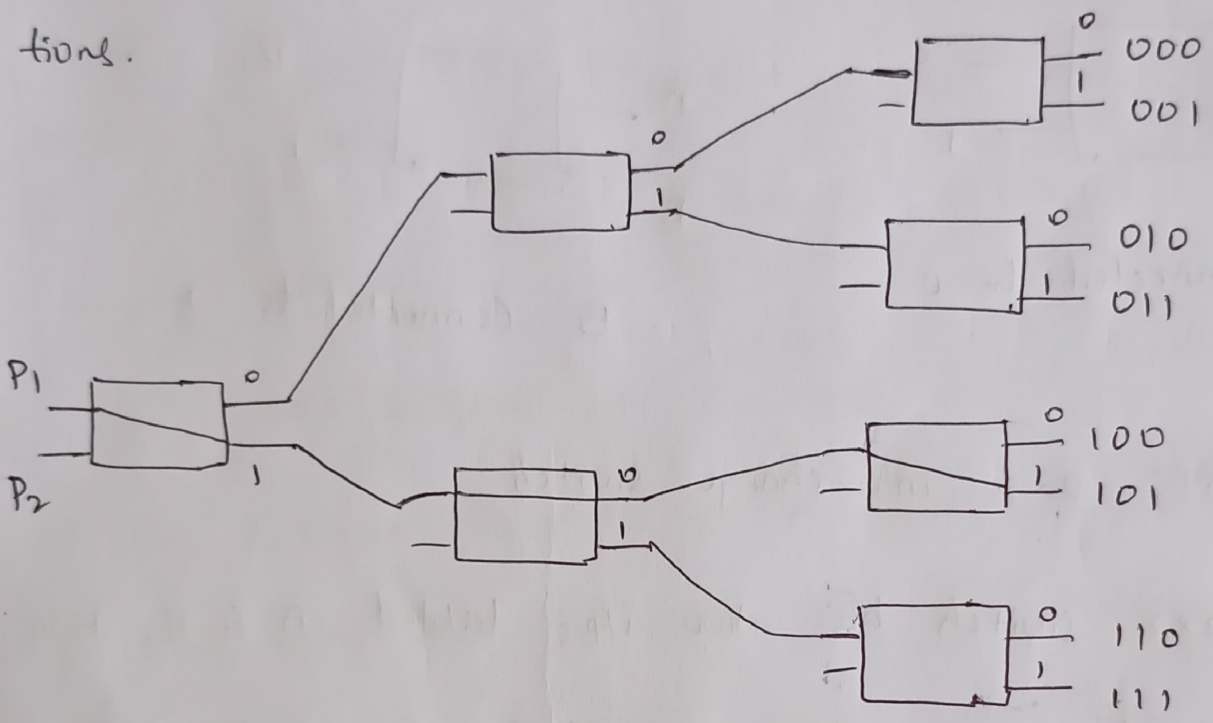


Fig: Binary tree with 2×2 switches

→ The two processors P_1 & P_2 are connected through switches to 8 memory modules marked in binary from 000 through 111.

→ The path from a source to a destination is determined from the binary bits of the destination number.

→ The first bit of the destination number determines the switch o/p in the first level.

→ The second bit specifies the o/p of the switch in the second level, and the third bit specifies the o/p of the switch in the third level.

→ for Ex.. to connect P_1 to memory 101, it is necessary to form a path from P_1 to o/p 1 in the first level switch, the o/p '0' in the second level switch, and o/p 1 in the third level switch.

→ It is clear that either P_1 or P_2 can be connected to any one of the 8 memories.

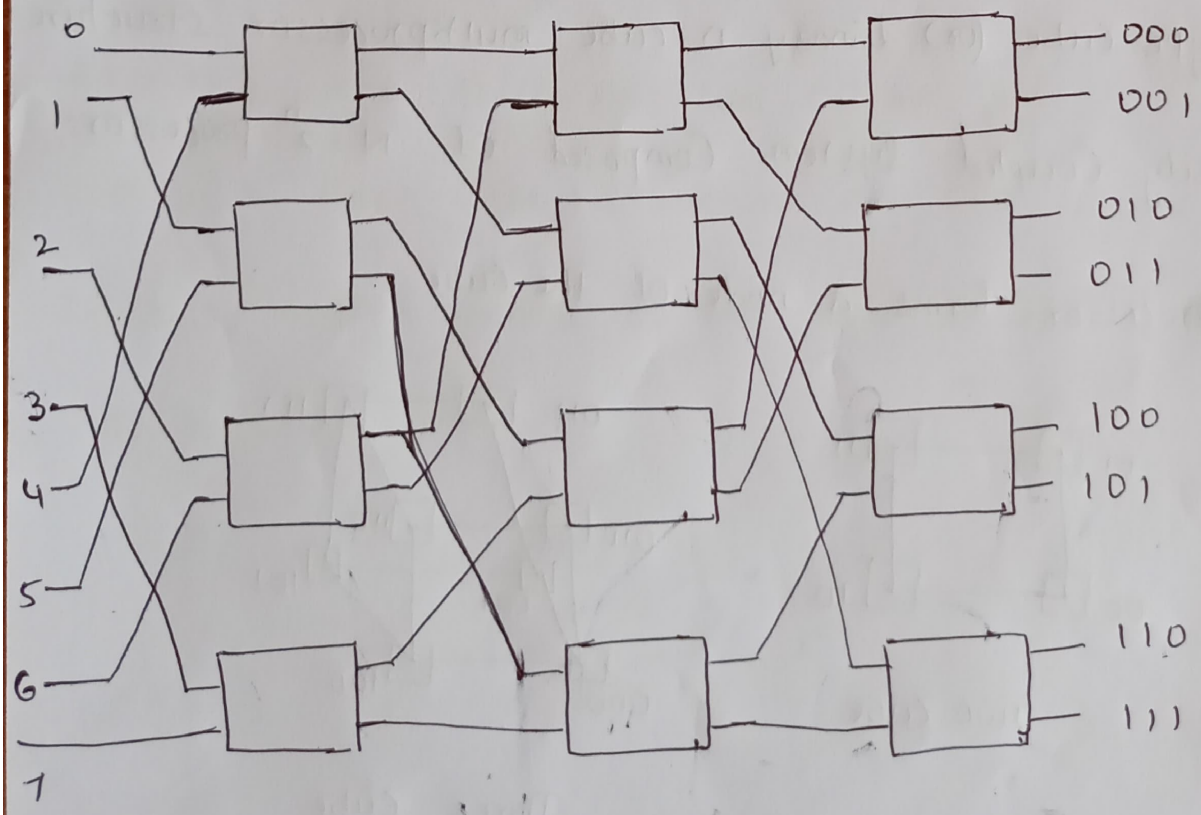


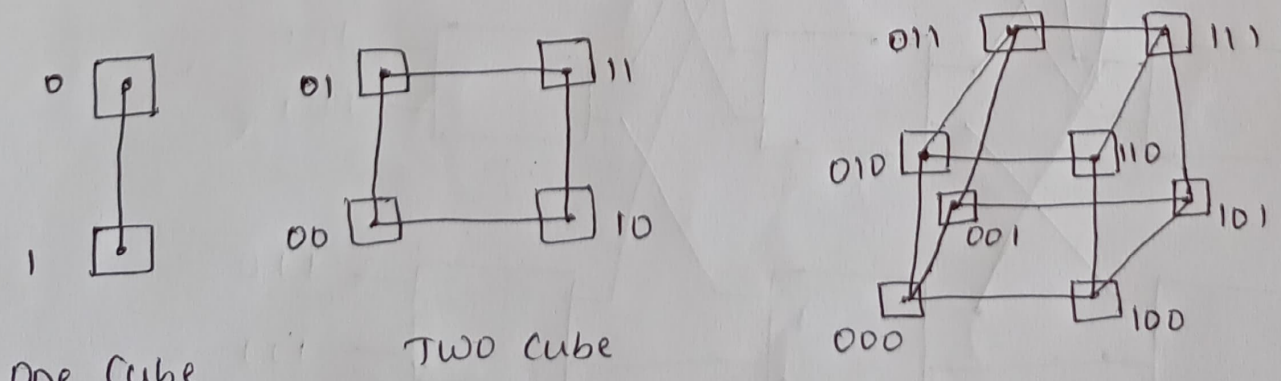
Fig: 8x8 Omega switching network

→ A particular request is initiated in the switching nlw by the source, which sends a 3-bit pattern representing the destination number. As the binary pattern moves through the nlw each level examines a different bit to determine the 2×2 switch setting. Level 1 inspects the most significant bit, level 2 inspects the middle bit, level 3 inspects the Least significant bit.

5. Hypercube interconnection

→ The hypercube (or) binary n-cube multiprocessor structure is a loosely coupled system composed of $N = 2^n$ processors.

→ Each processor forms a node of the cube.



One Cube Two Cube Three Cube

Fig: Hyper Cube structure for n=1, 2, 3

→ A one cube structure has $n=1$ and $2^n = 2$. It contains two processors interconnected by a single path.

→ A two cube structure has $n=2$ and $2^n = 4$. It contain 4 nodes interconnected as a square.

→ A three cube structure has $n=3$ and $2^n = 8$. It contain 8 nodes interconnected as a cube.

→ Each node is assigned a binary address in such away that the address of two neighbours differ in exactly one bit position.

→ for ex.., the three neighbors of the node with address 100 in a three cube structure are 000, 110, 101. Each of these binary numbers differs from address 100 by one bit value.