ECEC-355 Project 2 Write-up

Frank Tumminello & Hassan El Mghari

Experiment 4

1.

(a) How much space (in byte) does one integer occupy considering a RISC-V architecture?

Ans: 8 bytes

(b) Draw the data mapping.

We mapped out the int array of 3 unsigned ints into a 24-byte data memory table seen below.

23	0x67
22	0x45
21	0x23
20	0x01
19	0x00
18	0x00
17	0x00
16	0x00
15	0x01
14	0xEF
13	0xCD
12	0xAB
11	0x00
10	0x00
9	0x00
8	0x00
7	0x3D
6	0x2C
5	0x1B
4	0x0A
3	0x00
2	0x00
1	0x00
0	0x00

2. Continuing with 1, what is the value of x10 (assume x23 = 0)?

The value of x10 is A4 in hex or 164 in decimal.

Experiment 5

After our simulation, x9 and x11 were 128. Our code is also attached.

The code utilizes parser.c from project 1 to parse out the instruction set provided in cpu_traces/project_two and convert the instruction into a 32bit binary number. The 32bit instruction is then identified as a certain type and parsed into the RISC-V instruction format. The parsed segments of the instructions are then fed to the appropriate components in the datapath to simulate a single-cycle cpu.