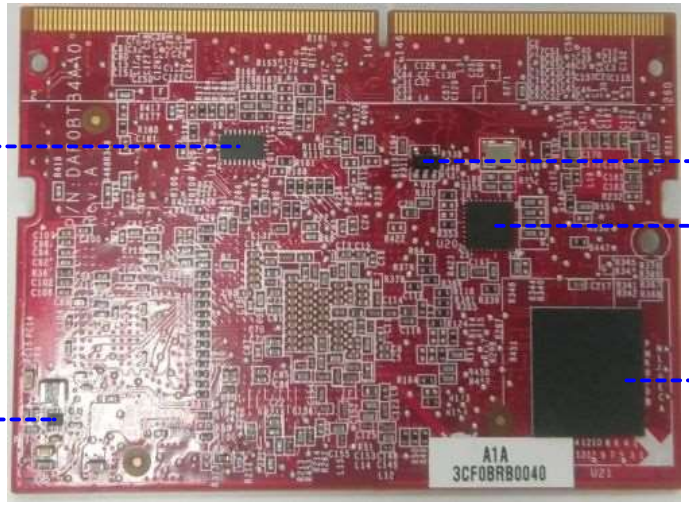
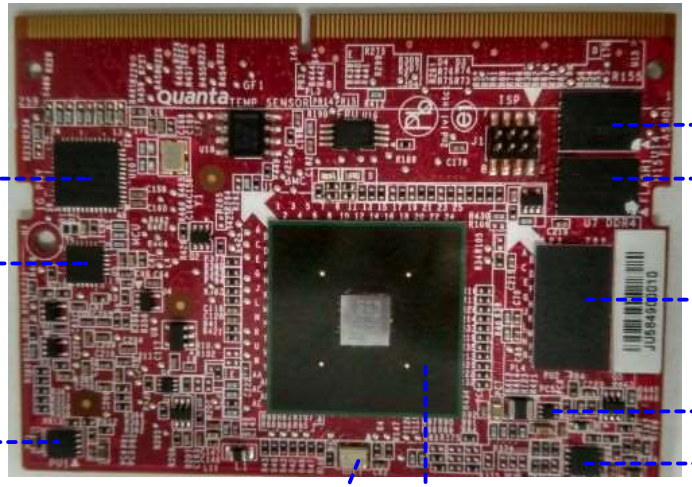
Nuvoton RunBMC NPCM7mnx-Based Module Reference Design

Nuvoton RunBMC Module Prototype - Designed by Quanta

BOTTOM



TOP



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TITLE: Cover Page			
DWG NO RunBMC Module	Wednesday, May 22, 2019	Sheet 1 / 22	Rev A.1.0

Revision Record

Revision	Date	Changes
A.1.0	May 16, 2019	First release

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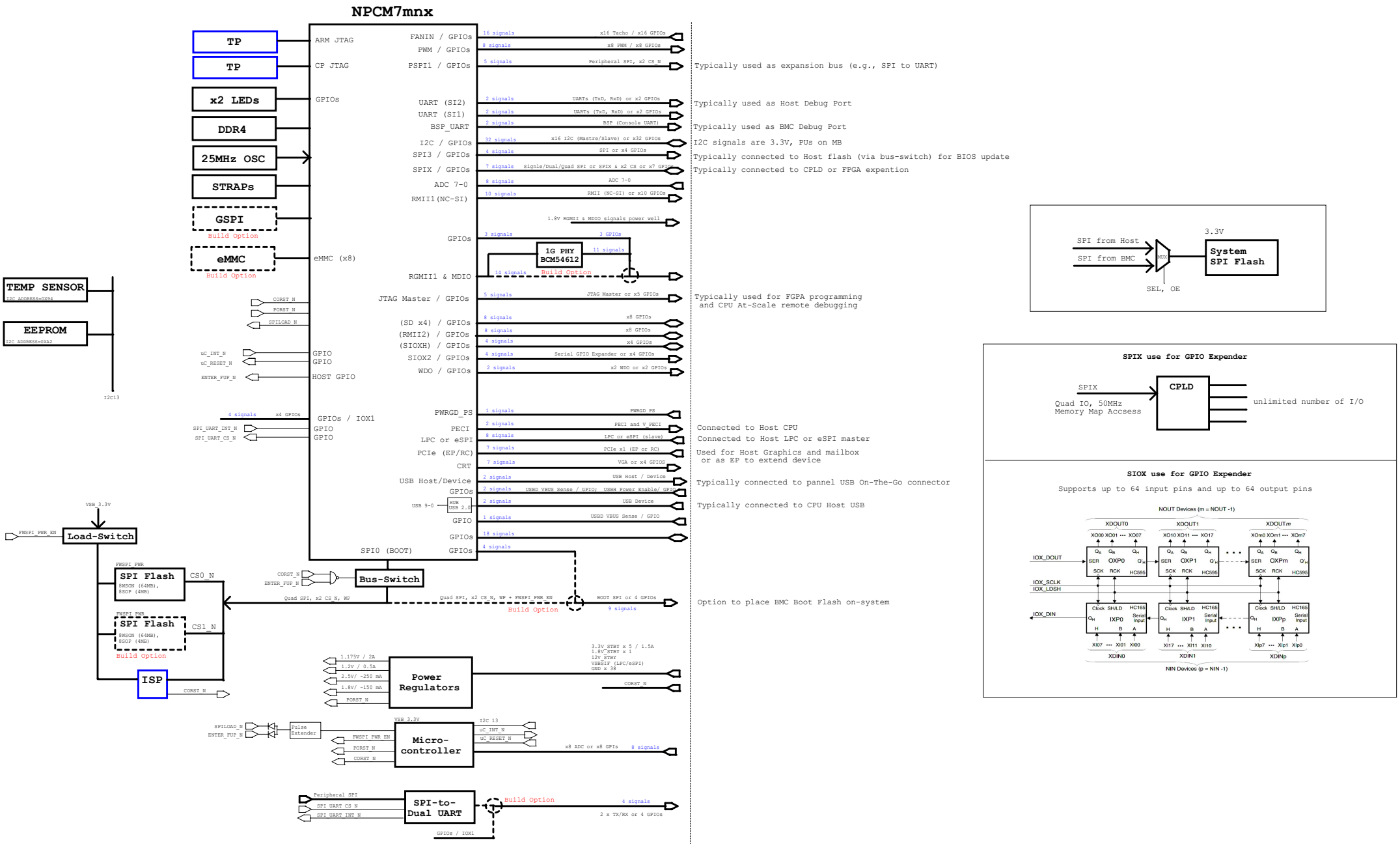
TITLE: **Revision Record**

DWG NO		Sheet	Rev
RunBMC Module	Tuesday, May 21, 2019	2 / 22	A.1.0

Connector I/F
Form Factor - 260 SO-DIMM4



SPIX use for GPIO Expender

SIOX use for GPIO Expender

Supports up to 64 input pins and up to 64 output pins

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TITLE: **Block-Diagram**

DWG NO		Sheet	Rev
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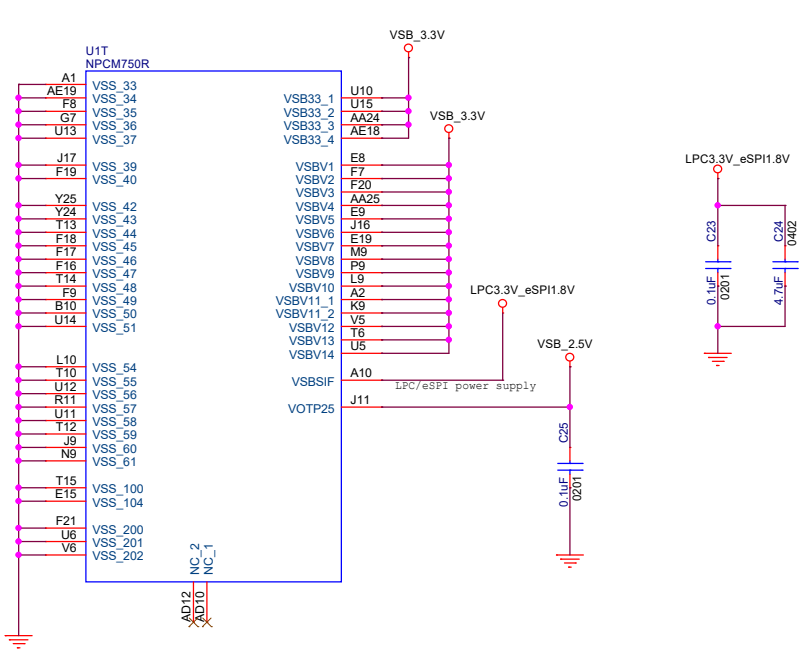
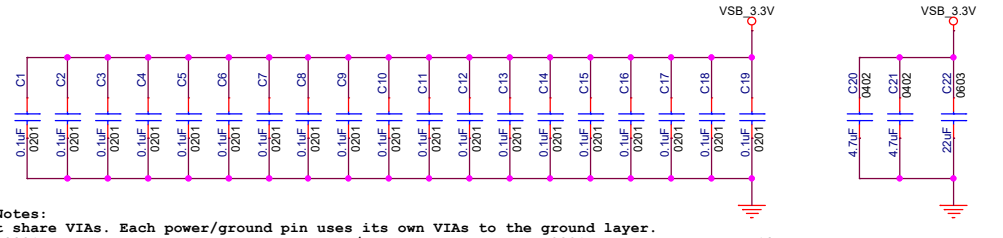
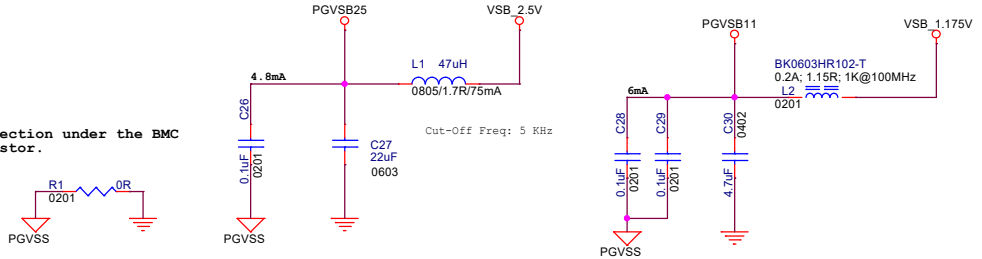




Layout Notes:
* Do not share VIAs. Each power/ground pin uses its own VIAs to the ground layer.
* Place 0201 filter capacitors under each power/ground pin pair. The 0201 capacitors can be 10nF or higher.
* Place 0402 bulk capacitors under the BMC. The 0402 capacitors can be 1uF or higher.
* Place 0603 bulk capacitors close to the BMC. The 0603 capacitors can be 10uF or higher.

Layout Notes:
One-point connection under the BMC
or use 0R resistor.



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One-point connection under the BMC
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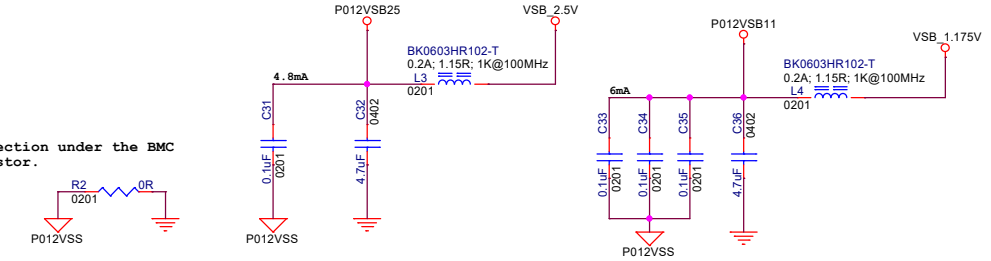

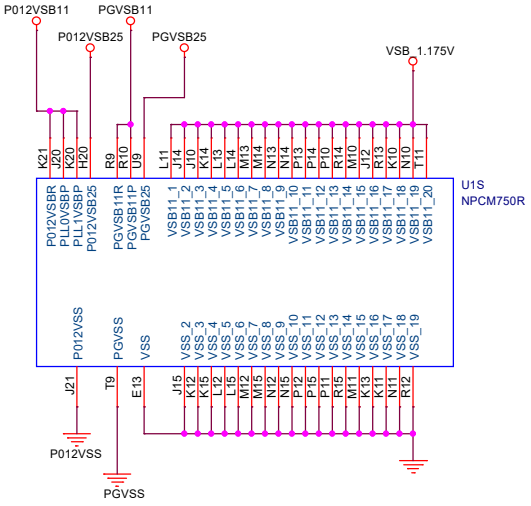

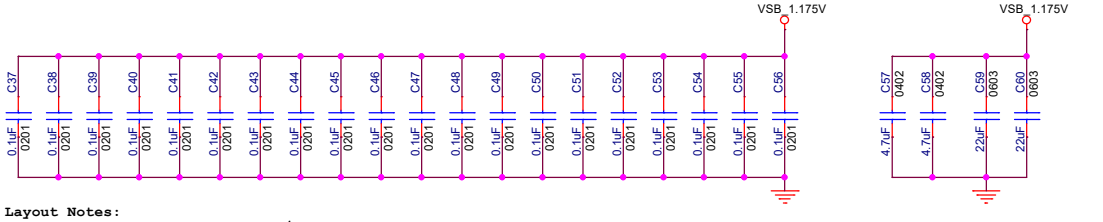

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TITLE: **BMC Power Supplies**

DWG NO		Sheet	Rev
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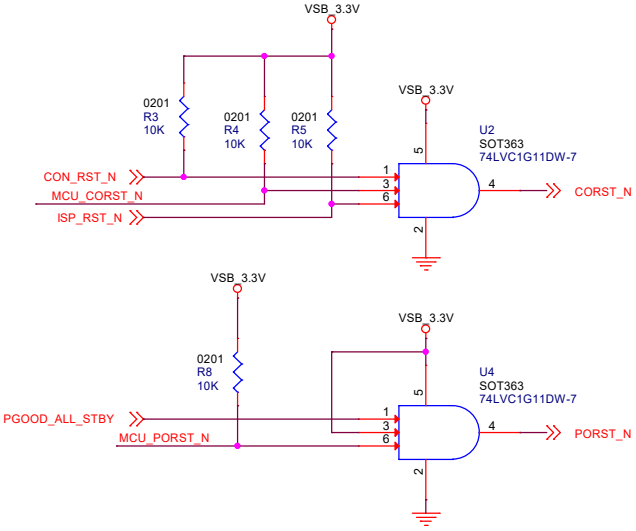
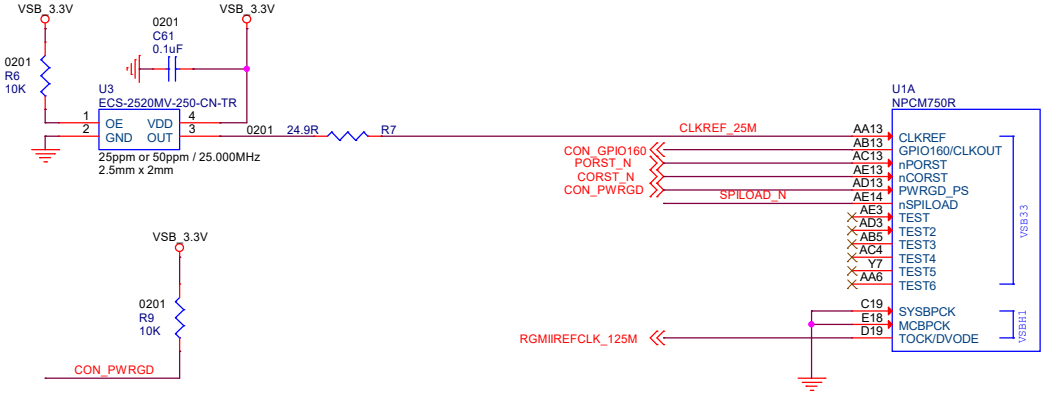
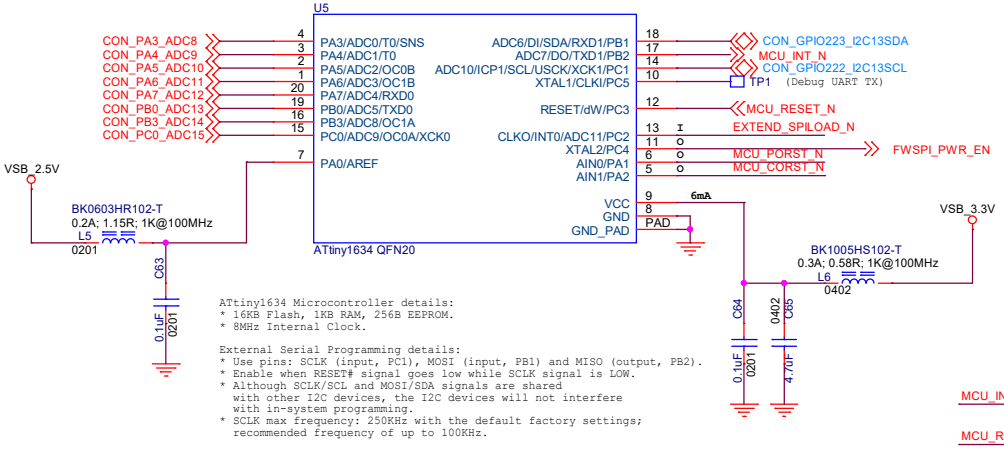
Clock and Resets



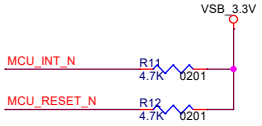


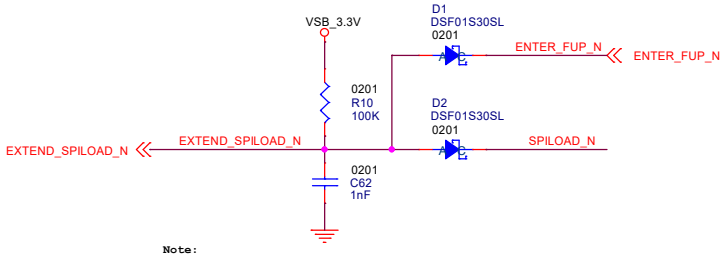
Note:
* If MCU ADCn pin is used as ADC,
  place 10nF capacitor on the baseboard close to the connector.



ATtiny1634 Microcontroller details:
* 16KB Flash, 1KB RAM, 256B EEPROM.
* 8MHz Internal Clock.

External Serial Programming details:
* Use pins: SCLK (input, PC1), MOSI (input, PB1) and MISO (output, PB2).
* Enable when RESET# signal goes low while SCLK signal is LOW.
* Although SCLK/SCL and MOSI/SDA signals are shared
  with other I2C devices, the I2C devices will not interfere
  with in-system programming.
* SCLK max frequency: 250KHz with the default factory settings;
  recommended frequency of up to 100KHz.





Note:
SPILOAD_N low pulse is 0.5 usec and the MCU may fail to detect it.
The RC circuit extends the pulse to ~10 usec.

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TITLE: **Clock and Resets**

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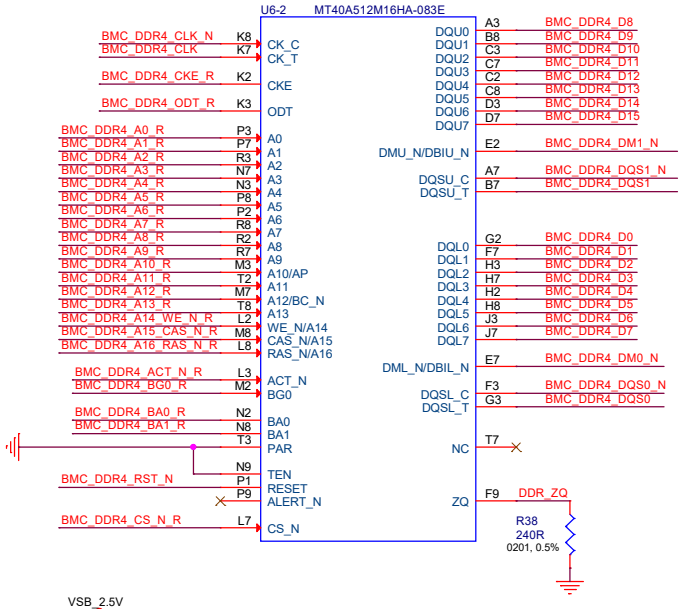
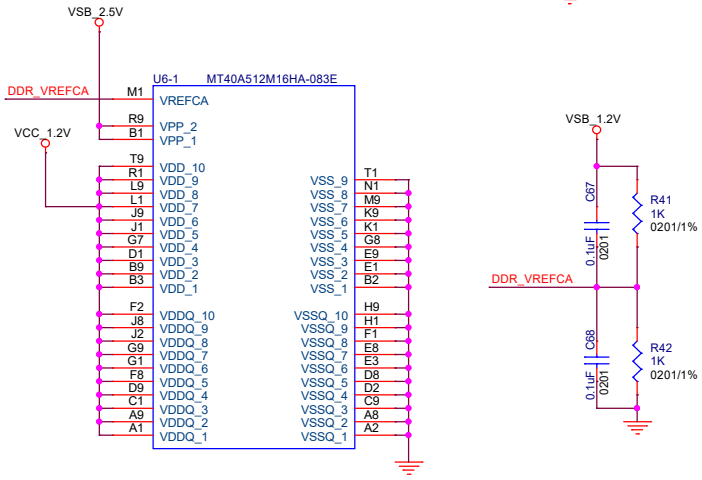
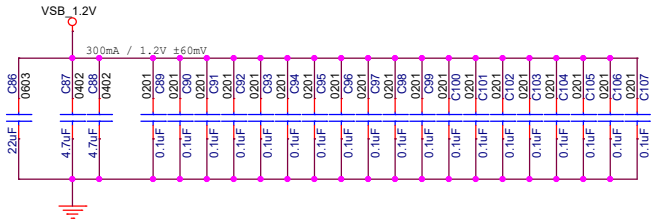
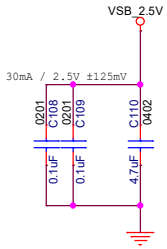
DDR4

SDRAM (DDR4-2400) 8Gbit (256Mbit x 16) Device

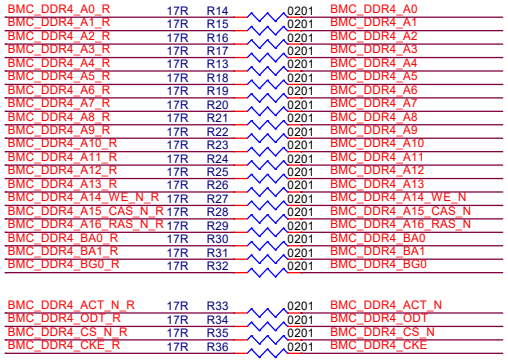




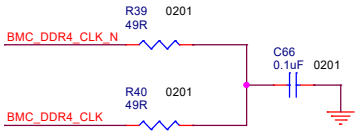




Layout Notes:
* Do not share VIAs. Each power/ground pin uses its own VIAs to the ground layer.
* Place 0201 filter capacitors under each power/ground pin pair. The 0201 capacitors can be 10nF or higher.
* Place 0402 bulk capacitors under the DDR. The 0402 capacitors can be 1uF or higher.
* Place 0603 bulk capacitors close to the DDR.The 0603 capacitors can be 10uF or higher.



Layout Note:
Place the serial terminations close to the BMC.



Layout Note:
Place the 49R and 0.1uF under the DDR device close to the PADs.

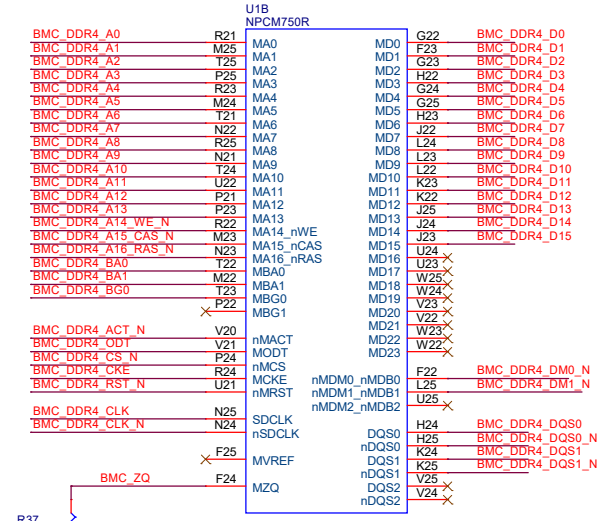
Layout Note:

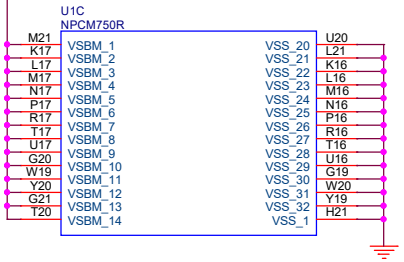
Trace Length and Skew Control:
* DQS_N to DQS (for each byte lane) : 20 mil.
* DQ and DM to DQS (within a byte lane): 100 mil.
* CLK_N to CLK: 20 mil.
* ADDR/CMD/CTL to CLK: 110 mil.

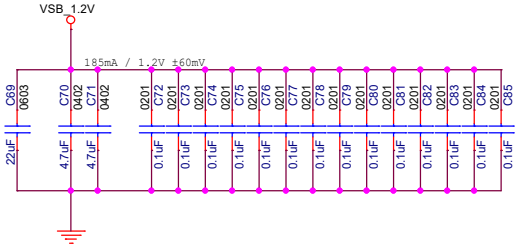
PCB Trace Impedance:
* Single-Ended: 50R
* Differential: 100R

To ease the layout:
* Data Lane 0 group can swap with Data Lane 1 group.
* The eight data signals within each byte lane can be swapped.

BMC DDR4 Interface







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TITLE: **DDR4**

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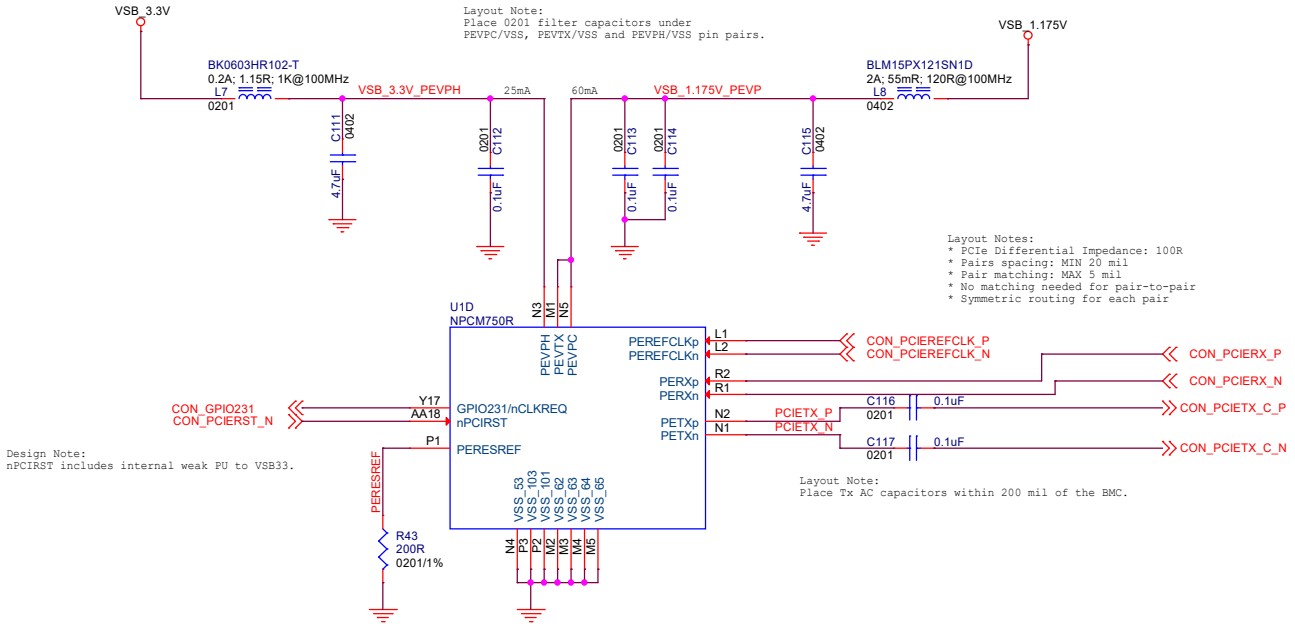
PCIe



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TITLE: **PCIe**

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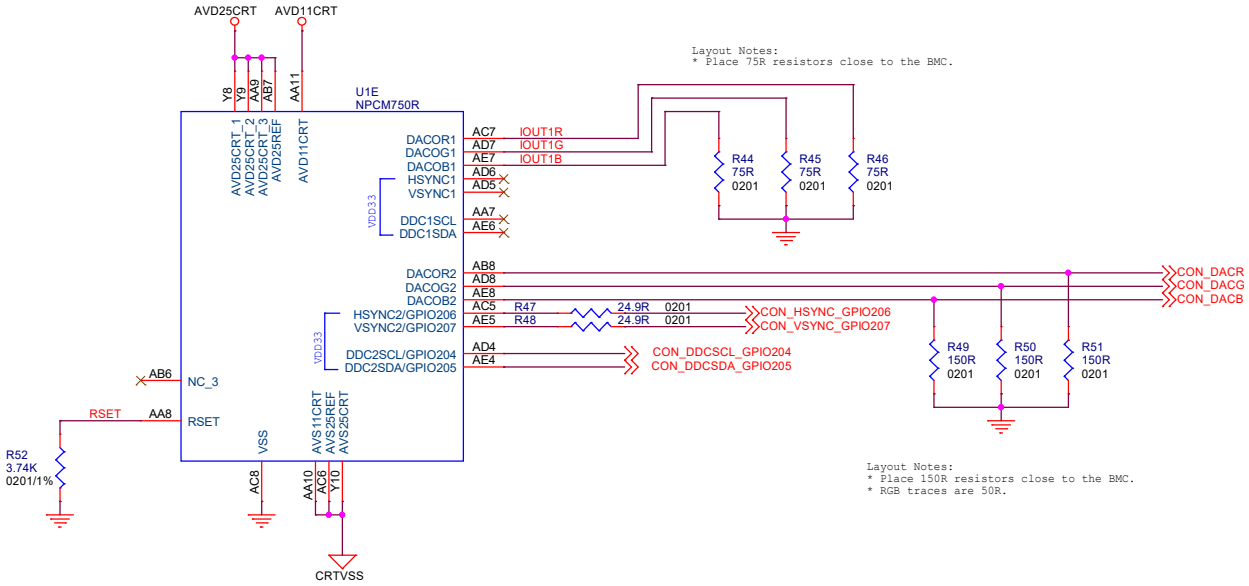
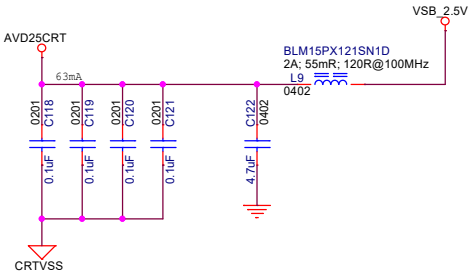
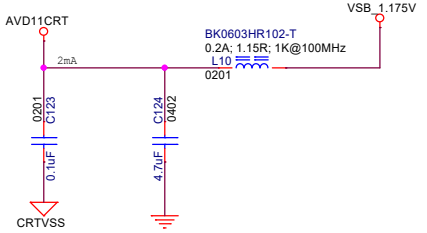
CRT Interface





Layout Note:
Place 0201 filter capacitors under BMC
AVD25CRT/AVS25CRT and AVD25REF/AVS25REF pin pairs.



Layout Note:
Place 0201 filter capacitors under BMC
AVD11CRT/AVS11CRT pin pairs.

Layout Notes:
One-point connection under the BMC
or use 0R resistor.

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TITLE: **BMC CRT**

DWG NO		Sheet	Rev
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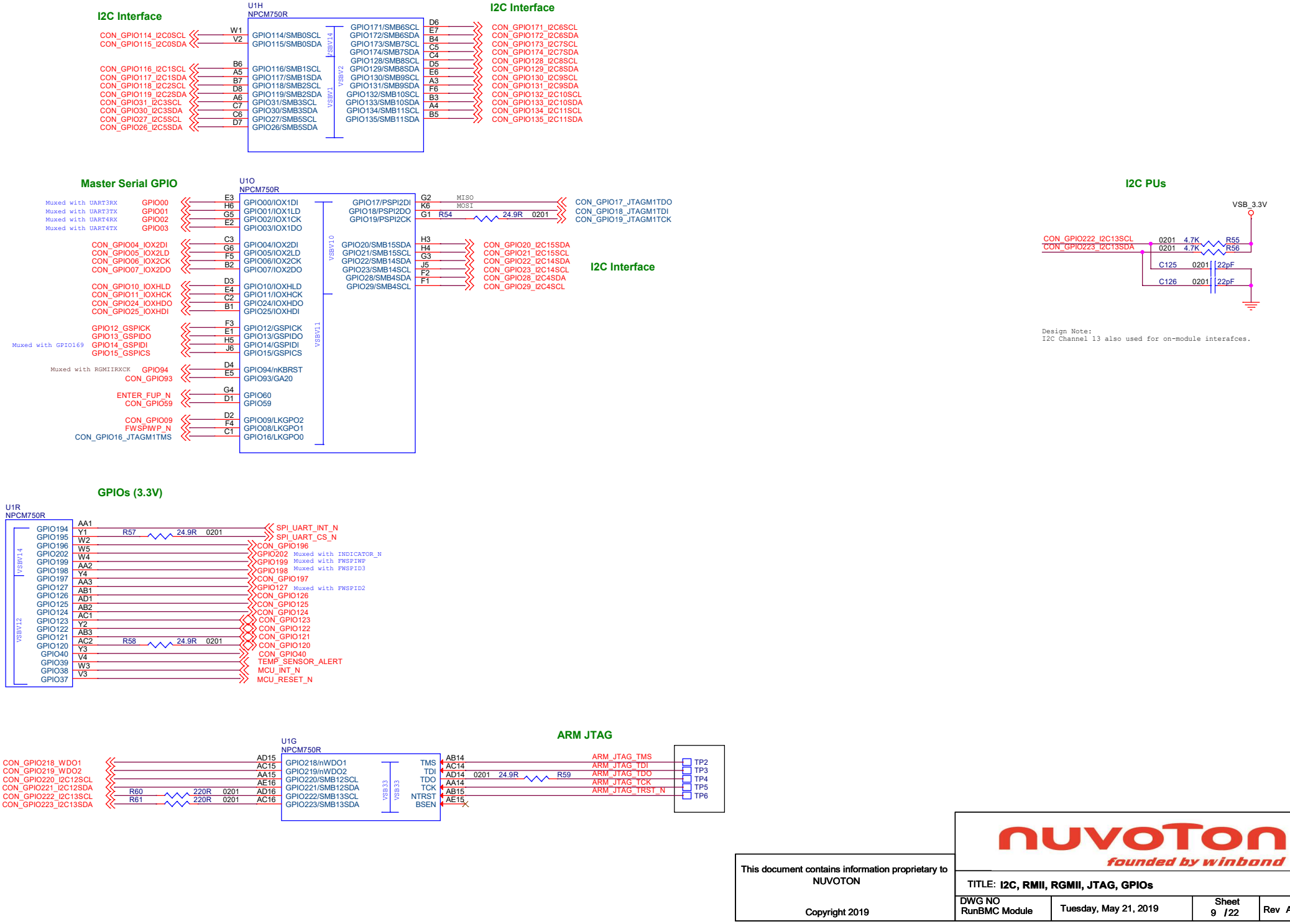
I2C Interface
U1H
NPCM750R
CON_GPIO114_I2C0SCL
CON_GPIO115_I2C0SDA
CON_GPIO116_I2C1SCL
CON_GPIO117_I2C1SDA
CON_GPIO118_I2C2SCL
CON_GPIO119_I2C2SDA
CON_GPIO31_I2C3SCL
CON_GPIO30_I2C3SDA
CON_GPIO27_I2C5SCL
CON_GPIO26_I2C5SDA
GPIO114/SMB0SCL
GPIO115/SMB0SDA
GPIO116/SMB1SCL
GPIO117/SMB1SDA
GPIO118/SMB2SCL
GPIO119/SMB2SDA
GPIO31/SMB3SCL
GPIO30/SMB3SDA
GPIO27/SMB5SCL
GPIO26/SMB5SDA
GPIO171/SMB6SCL
GPIO172/SMB6SDA
GPIO173/SMB7SCL
GPIO174/SMB7SDA
GPIO128/SMB8SCL
GPIO129/SMB8SDA
GPIO130/SMB9SCL
GPIO131/SMB9SDA
GPIO132/SMB10SCL
GPIO133/SMB10SDA
GPIO134/SMB11SCL
GPIO135/SMB11SDA
VSBV14
VSBV2
VSBV1
I2C Interface
CON_GPIO171_I2C6SCL
CON_GPIO172_I2C6SDA
CON_GPIO173_I2C7SCL
CON_GPIO174_I2C7SDA
CON_GPIO128_I2C8SCL
CON_GPIO129_I2C8SDA
CON_GPIO130_I2C9SCL
CON_GPIO131_I2C9SDA
CON_GPIO132_I2C10SCL
CON_GPIO133_I2C10SDA
CON_GPIO134_I2C11SCL
CON_GPIO135_I2C11SDA
Master Serial GPIO
U1O
NPCM750R
Muxed with UART3RX
Muxed with UART3TX
Muxed with UART4RX
Muxed with UART4TX
GPIO00
GPIO01
GPIO02
GPIO03
GPIO00/IOX1DI
GPIO01/IOX1LD
GPIO02/IOX1CK
GPIO03/IOX1DO
CON_GPIO04_IOX2DI
CON_GPIO05_IOX2LD
CON_GPIO06_IOX2CK
CON_GPIO07_IOX2DO
GPIO04/IOX2DI
GPIO05/IOX2LD
GPIO06/IOX2CK
GPIO07/IOX2DO
CON_GPIO10_IOXHLD
CON_GPIO11_IOXHCK
CON_GPIO24_IOXHDO
CON_GPIO25_IOXHDI
GPIO10/IOXHLD
GPIO11/IOXHCK
GPIO24/IOXHDO
GPIO25/IOXHDI
GPIO12_GSPICK
GPIO13_GSPIDO
Muxed with GPIO169
GPIO14_GSPIDI
GPIO15_GSPICS
GPIO12/GSPICK
GPIO13/GSPIDO
GPIO14/GSPIDI
GPIO15/GSPICS
Muxed with RGMIIRXCK
GPIO94
CON_GPIO93
GPIO94/nKBRST
GPIO93/GA20
ENTER_FUP_N
CON_GPIO59
GPIO60
GPIO59
CON_GPIO09
FWSPIWP_N
CON_GPIO16_JTAGM1TMS
GPIO009/LKGPO2
GPIO08/LKGPO1
GPIO16/LKGPO0
GPIO17/PSPI2DI
GPIO18/PSPI2DO
GPIO19/PSPI2CK
MISO
MOSI
R54
24.9R
0201
CON_GPIO17_JTAGM1TDO
CON_GPIO18_JTAGM1TDI
CON_GPIO19_JTAGM1TCK
GPIO20/SMB15SDA
GPIO21/SMB15SCL
GPIO22/SMB14SDA
GPIO23/SMB14SCL
GPIO28/SMB4SDA
GPIO29/SMB4SCL
I2C Interface
CON_GPIO20_I2C15SDA
CON_GPIO21_I2C15SCL
CON_GPIO22_I2C14SDA
CON_GPIO23_I2C14SCL
CON_GPIO28_I2C4SDA
CON_GPIO29_I2C4SCL
VSBV10
VSBV11
I2C PUs
VSB_3.3V
CON_GPIO222_I2C13SCL
CON_GPIO223_I2C13SDA
0201
4.7K
R55
R56
C125
C126
22pF
Design Note:
I2C Channel 13 also used for on-module interafces.
GPIOs (3.3V)
U1R
NPCM750R
GPIO194
GPIO195
GPIO196
GPIO202
GPIO199
GPIO198
GPIO197
GPIO127
GPIO126
GPIO125
GPIO124
GPIO123
GPIO122
GPIO121
GPIO120
GPIO40
GPIO39
GPIO38
GPIO37
R57
R58
24.9R
0201
SPI_UART_INT_N
SPI_UART_CS_N
CON_GPIO196
GPIO202
Muxed with INDICATOR_N
GPIO199
Muxed with FWSPIWP
GPIO198
Muxed with FWSPID3
CON_GPIO197
GPIO127
Muxed with FWSPID2
CON_GPIO126
CON_GPIO125
CON_GPIO124
CON_GPIO123
CON_GPIO122
CON_GPIO121
CON_GPIO120
CON_GPIO40
TEMP_SENSOR_ALERT
MCU_INT_N
MCU_RESET_N
VSBV14
VSBV12
ARM JTAG
U1G
NPCM750R
CON_GPIO218_WDO1
CON_GPIO219_WDO2
CON_GPIO220_I2C12SCL
CON_GPIO221_I2C12SDA
CON_GPIO222_I2C13SCL
CON_GPIO223_I2C13SDA
R60
R61
220R
0201
GPIO218/nWDO1
GPIO219/nWDO2
GPIO220/SMB12SCL
GPIO221/SMB12SDA
GPIO222/SMB13SCL
GPIO223/SMB13SDA
TMS
TDI
TDO
TCK
NTRST
BSEN
R59
ARM_JTAG_TMS
ARM_JTAG_TDI
ARM_JTAG_TDO
ARM_JTAG_TCK
ARM_JTAG_TRST_N
TP2
TP3
TP4
TP5
TP6
VSB33
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TITLE: I2C, RMII, RGMII, JTAG, GPIOs
DWG NO
RunBMC Module
Tuesday, May 21, 2019
Sheet
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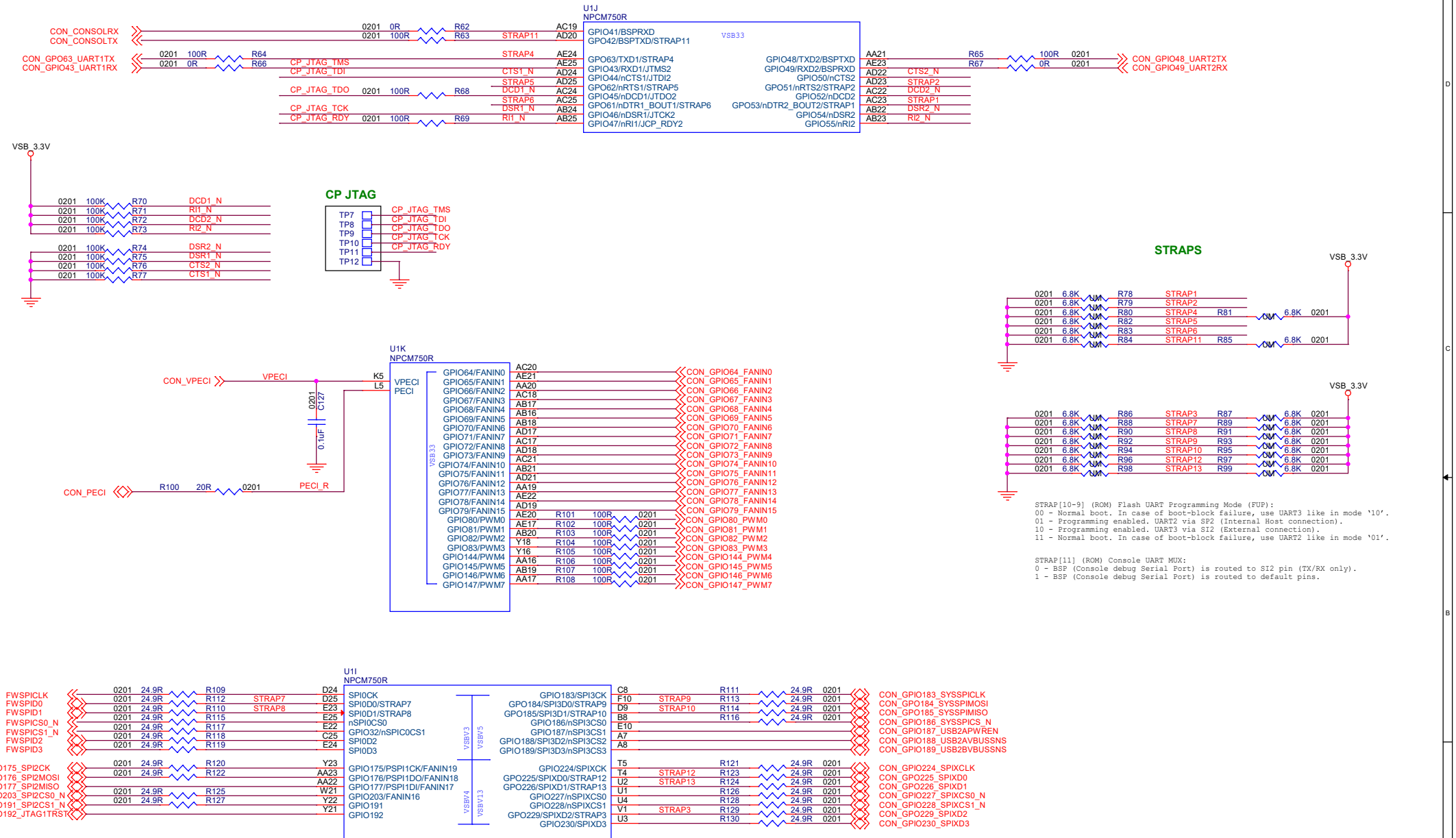
Rev A.1.0



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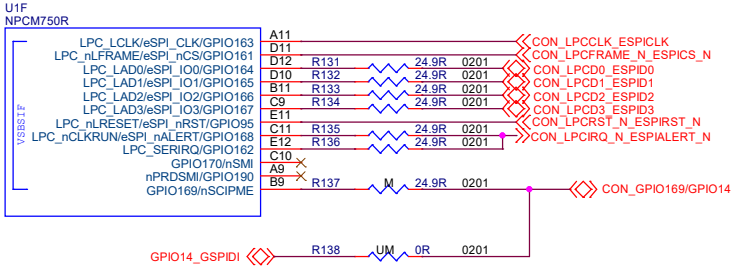
TITLE: **FAN, SPI, GPIOs, UART, CP JTAG, STRAPs**

DWG NO RunBMC Module	Tuesday, May 21, 2019	Sheet 10 / 22	Rev A.1.0

LPC / eSPI

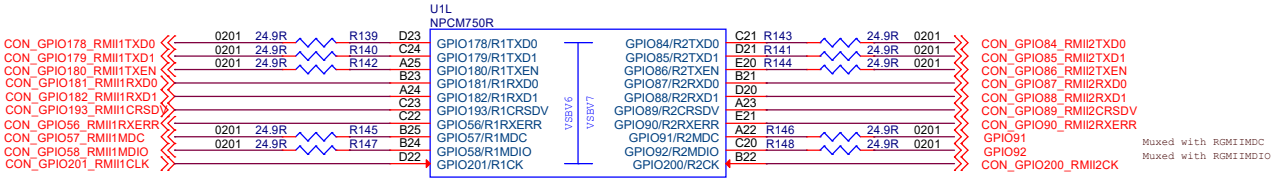


Software Notes:

If eSPI mode is used, configure pin E12 to GPIO162 input. Pin C11 is used as eSPI ALERT_N.
Else if LPC mode is used, configure pin C11 to GPIO168 input. Pin E12 is used as LPC SERIRQ_N.

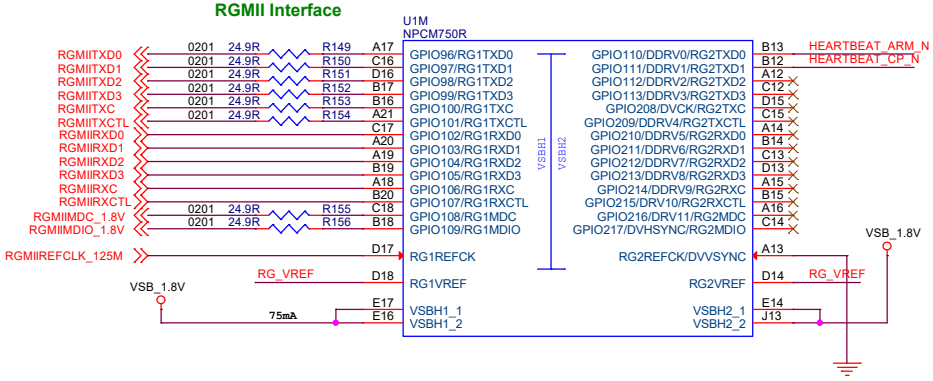
Design Note:
GPIO169 power well is VSBSIF, which can be connected to Host 3.3V or 1.8V.

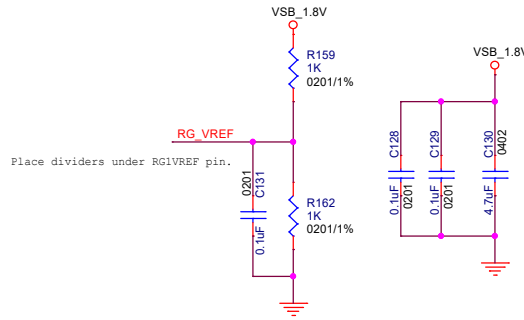
RMII Interface / GPIOs



Muxed with RGMIIMDC
Muxed with RGMIIMDIO

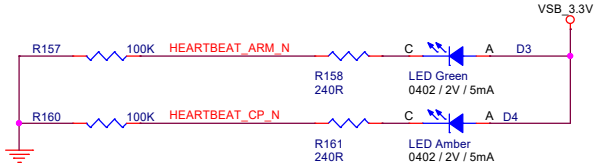
RGMII Interface





Place dividers under RG1VREF pin.

Place 0201 filter capacitors under VSBHn/VSS pin pairs.



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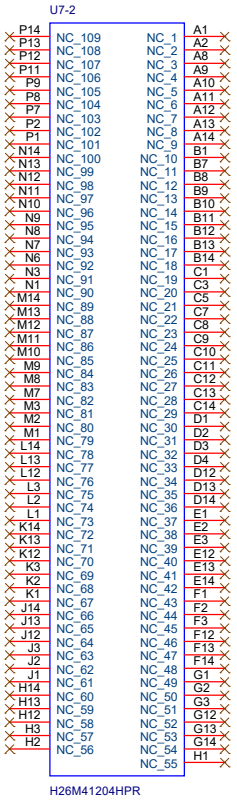
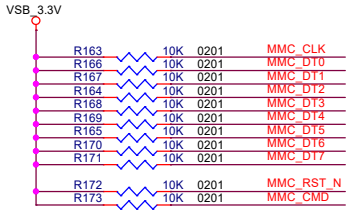
TITLE: **LPC/eSPI, RMII, RGMII**

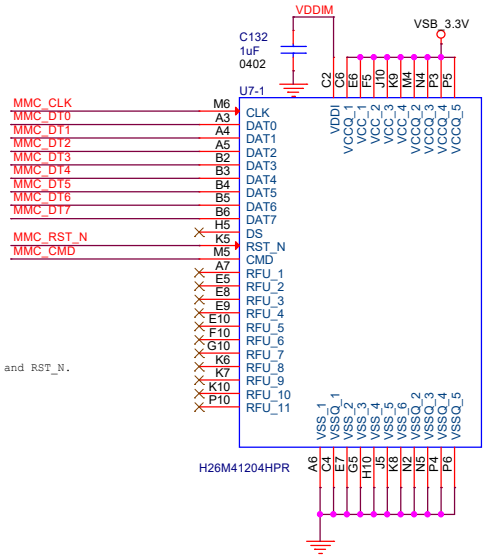
DWG NO		Sheet	Rev
RunBMC Module	Tuesday, May 21, 2019	11 / 22	A.1.0

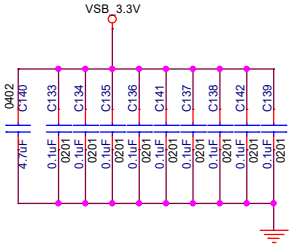
Embedded MultiMediaCard (eMMC)



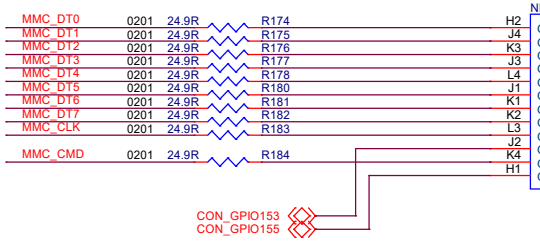


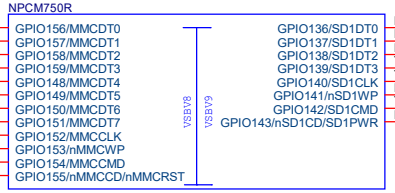
Design Notes:
* After power-up, all BMC MMC signals are floating and
  eMMC device's RST_N pin is disabled.
* eMMC device includes internal pull-up on data lines DAT[7:1] and RST_N.
* eMMC device is JEDEC/MMC standard version 5.0-compliant.



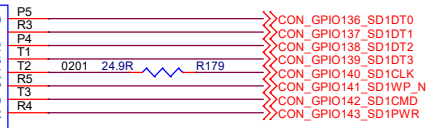


MMC





GPIOs / SD



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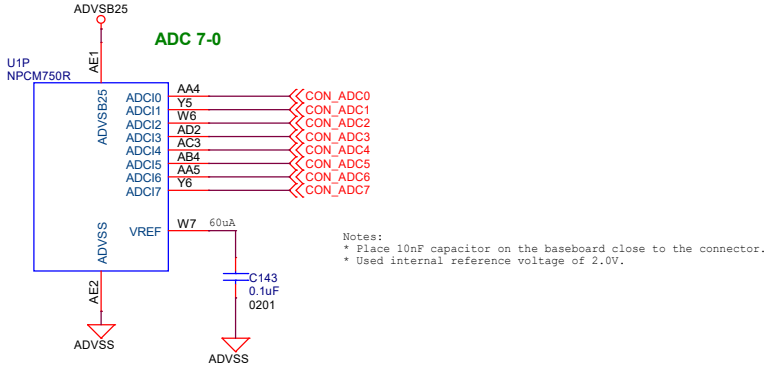
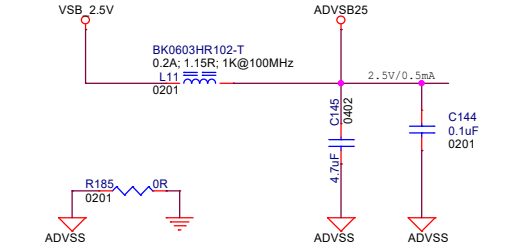
TITLE: **BMC eMMC**

DWG NO		Sheet	Rev
RunBMC Module	Tuesday, May 21, 2019	12 / 22	A.1.0





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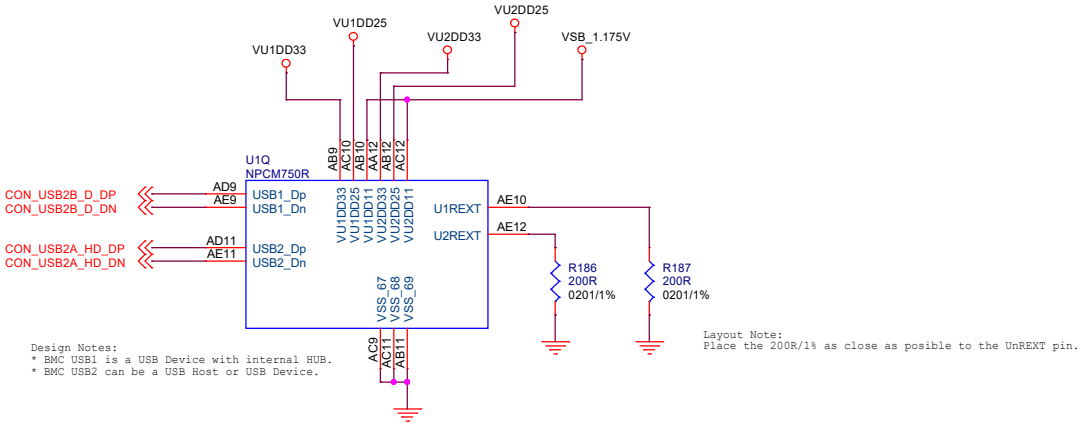
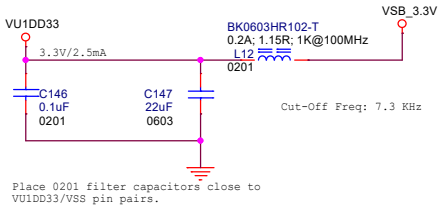
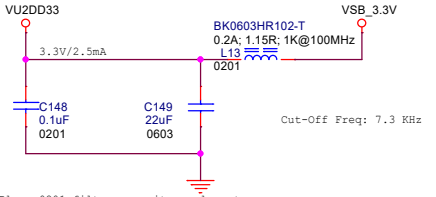
TITLE: **ADC**

DWG NO RunBMC Module	Tuesday, May 21, 2019	Sheet 13 / 22	Rev A.1.0

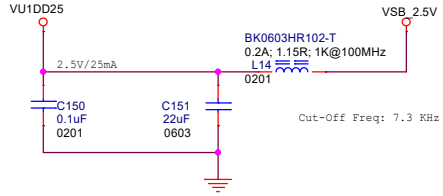




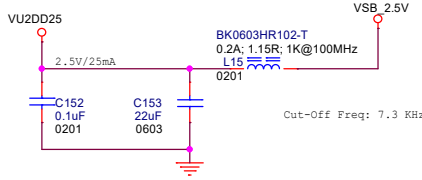
Place 0201 filter capacitors close to VU1DD33/VSS pin pairs.



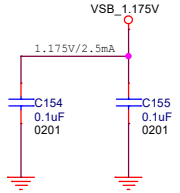
Place 0201 filter capacitors close to VU2DD33/VSS pin pairs.



Place 0201 filter capacitors close to VU1DD25/VSS pin pairs.



Place 0201 filter capacitors close to VU2DD25/VSS pin pairs.



Place 0201 filter capacitors close to VU2DD11/VSS and VU1DD11/VSS pin pairs.

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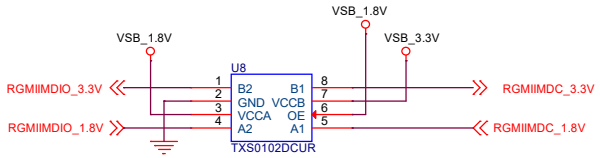
TITLE: **USB Device and Host**

DWG NO			
RunBMC Module	Tuesday, May 21, 2019	Sheet 14 / 22	Rev A.1.0

MDIO Signals Voltage Level-Shifter



RGMII MDIO Signal:
* BMC side: 1.8V swing
* PHY side: 3.3V swing
* Type: Bidirectional

RGMII MDC Signal:
* BMC side: 1.8V swing
* PHY side: 3.3V swing
* Type: Push-Pull

1 Gbit PHY

Design Notes:
* RGMII signals output impedance is 50R. Serial resistors are not needed.
* RESET, MDIO and MDC are OVDD (3.3V) power domain.
* RESET and MDIO include internal 22K (+/-50%) PU.
* MDC includes internal 22K (+/-50%) PD.

Design Note:
* TEST2, TEST3 and PHYA[0] pins include internal 22K PD.
* PHY address is 000000.

Design Notes:
* LED pins include internal 22K (+/- 50%) PU.
* LED pins configure the device on POR.
  The active polarity of each LED pin is set according to its PU/PD configuration on POR.

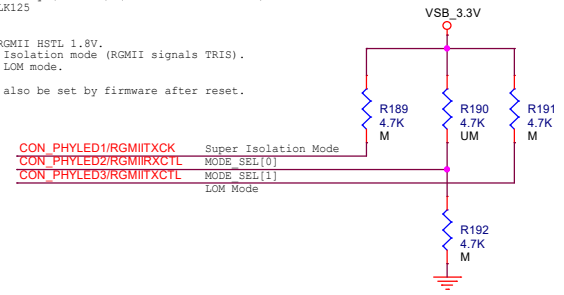
RJ45 LEDs connection:
* LED1 to Green_p Orange_n
* LED2 to Green_n Orange_p
* LED3 ro Yelloe_n; Yellow_p to 3.3V

Green/Orange LEDs Meaning:
* Green: No Link, Power-On.
* Orange: Linked @ 1000BASE-T
* Off: Linked @ 100BASE-T or Linked @ 10BASE-T

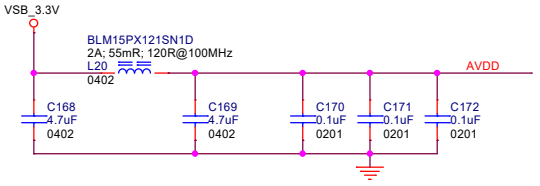
LED MUX configuration:
* LED1: Dual LED status LINKSPD[1] (default) (active low due to PU)
* LED2: Dual LED status LINKSPD[2] (default) (active high due to PD)
* LED3: Activity (default) (active low due to PU)
* LED4: CLK125

Straps:
* Set to RGMII HSTL 1.8V.
* Disable Isolation mode (RGMII signals TRIS).
* Disable LOM mode.

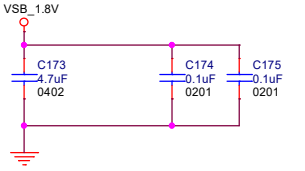
Modes can also be set by firmware after reset.



Layout Notes:
* Place 22uF bulk capacitor close to pin 3.
* Place decoupling capacitors close to pins 2 and 30.

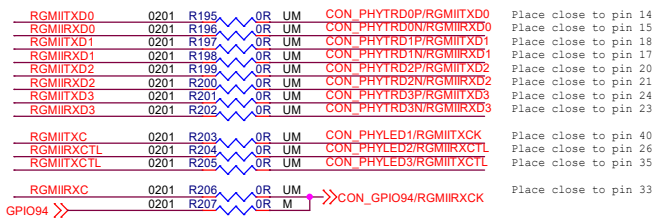


Layout Note:
Decouple each pin with 0.1uF capacitor (pins 1, 16, 22).



Layout Note:
4.7uF capacitor is common to all OVDD_RGMII pins.
Decouple each pin with 0.1uf capacitor (pins 29, 34).

Optional Mount - Bypass the PHY



Laytout Note:
Place as a group close to GMAC PHY.

Notes:
* If on-module GMAC PHY is used, select GPIOs to connector.
* If off-module GMAC PHY is used, select between MDIO 1.8V and 3.3V signals.

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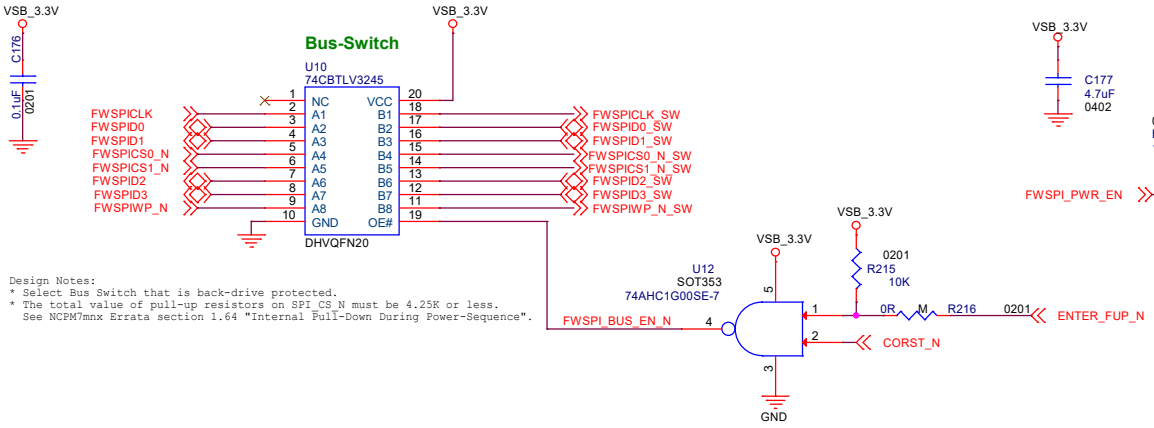
TITLE: 1 Gbit PHY

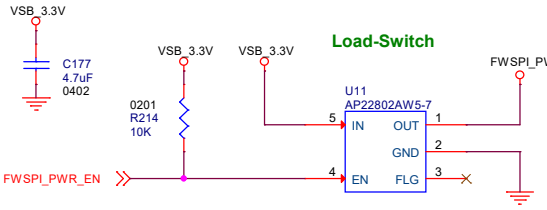
DWG NO			
RunBMC Module	Tuesday, May 21, 2019	Sheet 15 /22	Rev A.1.0

Bus-Switch



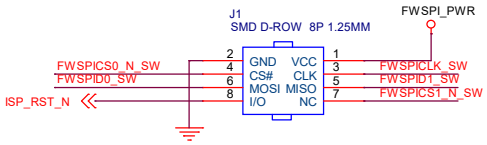
Design Notes:
* Select Bus Switch that is back-drive protected.
* The total value of pull-up resistors on SPI_CS_N must be 4.25K or less.
  See NCPM7mnx Errata section 1.64 "Internal Pull-Down During Power-Sequence".

Load-Switch



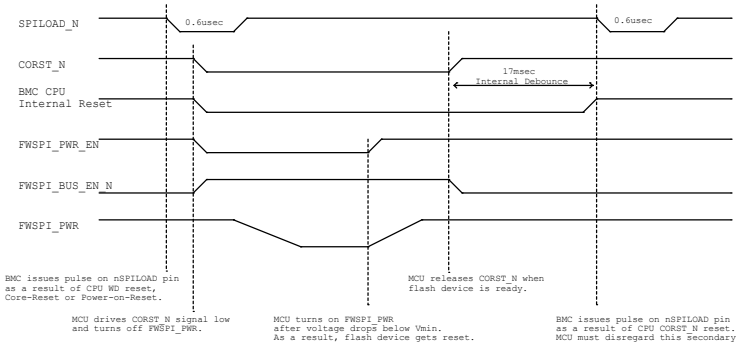
Design Notes,
* Select Load Switch with reverse current blocking.

In-System-Programming (ISP) Header



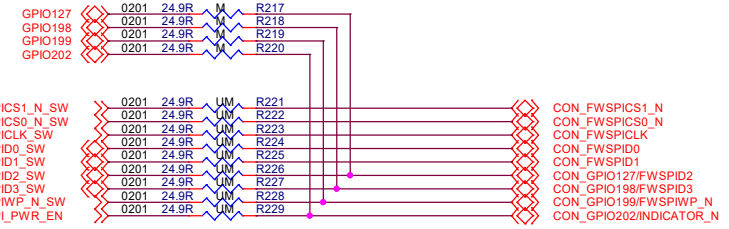
Design Notes:
* When the programmer unit is not in programming mode, I/O (pin 8) is in TRI-STATE mode.
* While programming, I/O is driven low to isolate BMC's SPI signals from flash signals.
* Make sure ISP is reverse current blocking.
* Connector type and pin assigment is TBD.
* In case ISP header is mount in the final product, make sure connector height from top PCB is up to 6 mm.
  R.A SMD type is recommanded.

FWSPI Power Cycle (Reset SPI Flash)



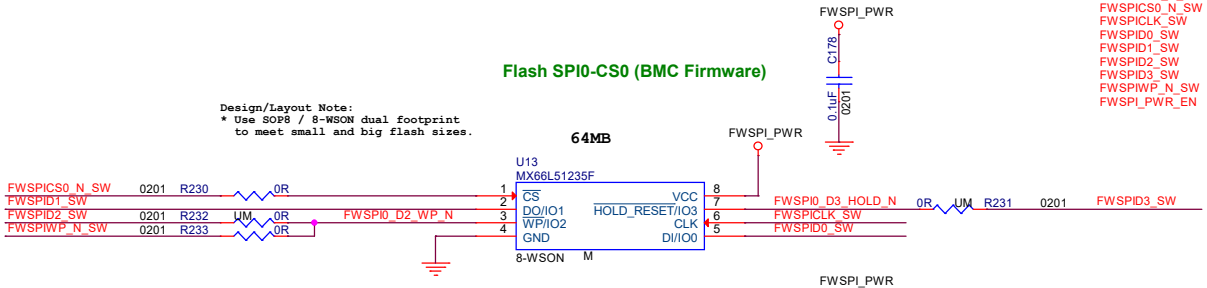
Design Notes:
* It is of utmost importance to reset the flash device connected to nSPI0CS0
  when the BMC CPU is reset (e.g., a Watchdog reset).
  This is most essential with flash devices above 16MB.
  In this case, we use flash power-cycle method to reset the flash.
* For security, FWSPIWP_N uses a lockable I/O.
* The flash contains Boot-Block, UBOOT and (optional) Linux sections.
* An external SPI flash programmer (ISP) is typically used in the production line.
  ISP can be used when the module is powered off (bare) or under power. Keep ISP_RST_N low while programming.
* FUP (Flash UART Programming) may also be used to program an empty or corrupted flash with Boot-Block and UBOOTsections.
  Later on, the Linux section can be programmed in UBOOT state through the network or USB storage device.

Layout Note:
* To avoid stubs, place flash devices,
  ISP header and the Bus-Switch close together.



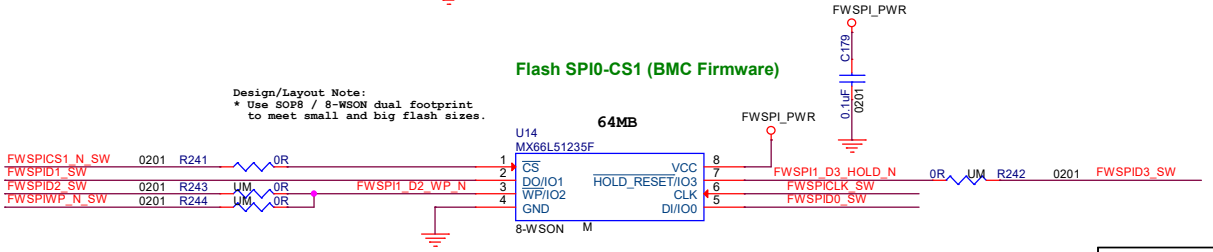
Flash SPI0-CS0 (BMC Firmware)

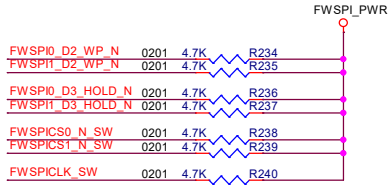
Design/Layout Note:
* Use SOP8 / 8-WSON dual footprint
  to meet small and big flash sizes.



Flash SPI0-CS1 (BMC Firmware)

Design/Layout Note:
* Use SOP8 / 8-WSON dual footprint
  to meet small and big flash sizes.





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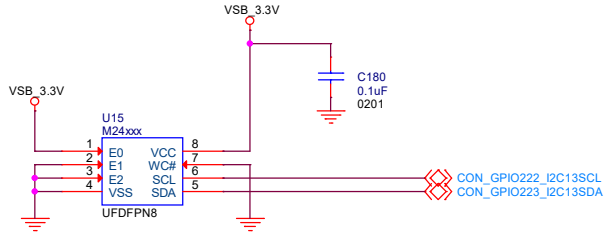
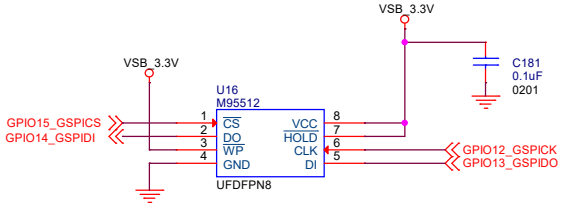
TITLE: **BMC Firmware SPI**

DWG NO		Sheet	Rev
RunBMC Module	Tuesday, May 21, 2019	16 / 22	A.1.0

I2C EEPROM (Addr=0xA2)

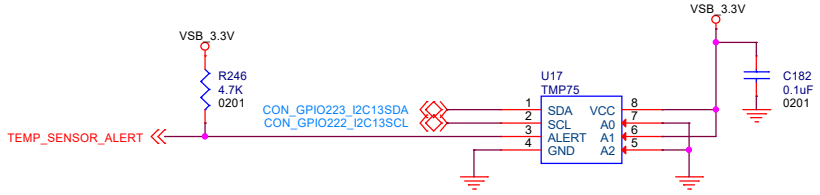


GSPI (Graphic SPI EEPROM for VGA BIOS)



Optional Mount: VBIOS EEPROM (Legacy and UEFI modes).
Note: Signals are MUXed with other optional mount functions.

I2C Temperature Sensor (Addr=0x94)



Accuracy: MAX ±3 °C, TYP ±1 °C.
Can be replaced with any temperature device with Linux support.

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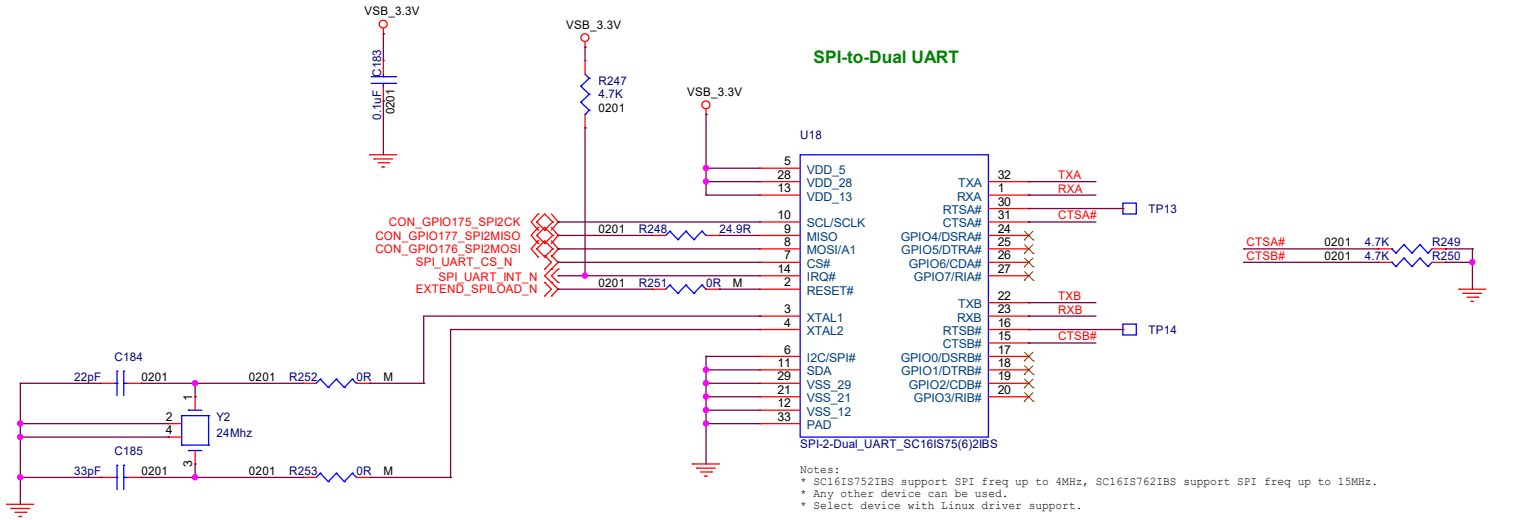
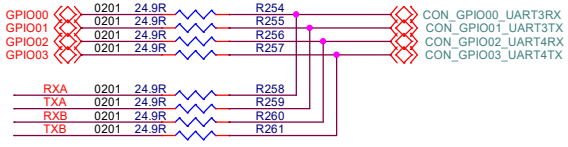
TITLE: **I2C EEPORM, I2C Temperature Sensor**

DWG NO			
RunBMC Module	Tuesday, May 21, 2019	Sheet 17 / 22	Rev A.1.0





Notes:
* After power-up-reset, GPIO00, GPIO01, GPIO02 and GPIO03 are TRIS.
* After UART device reset, TXA and RXB pins are output HIGH;
these pins are TRIS when UART device is placed in Internal Loopback.

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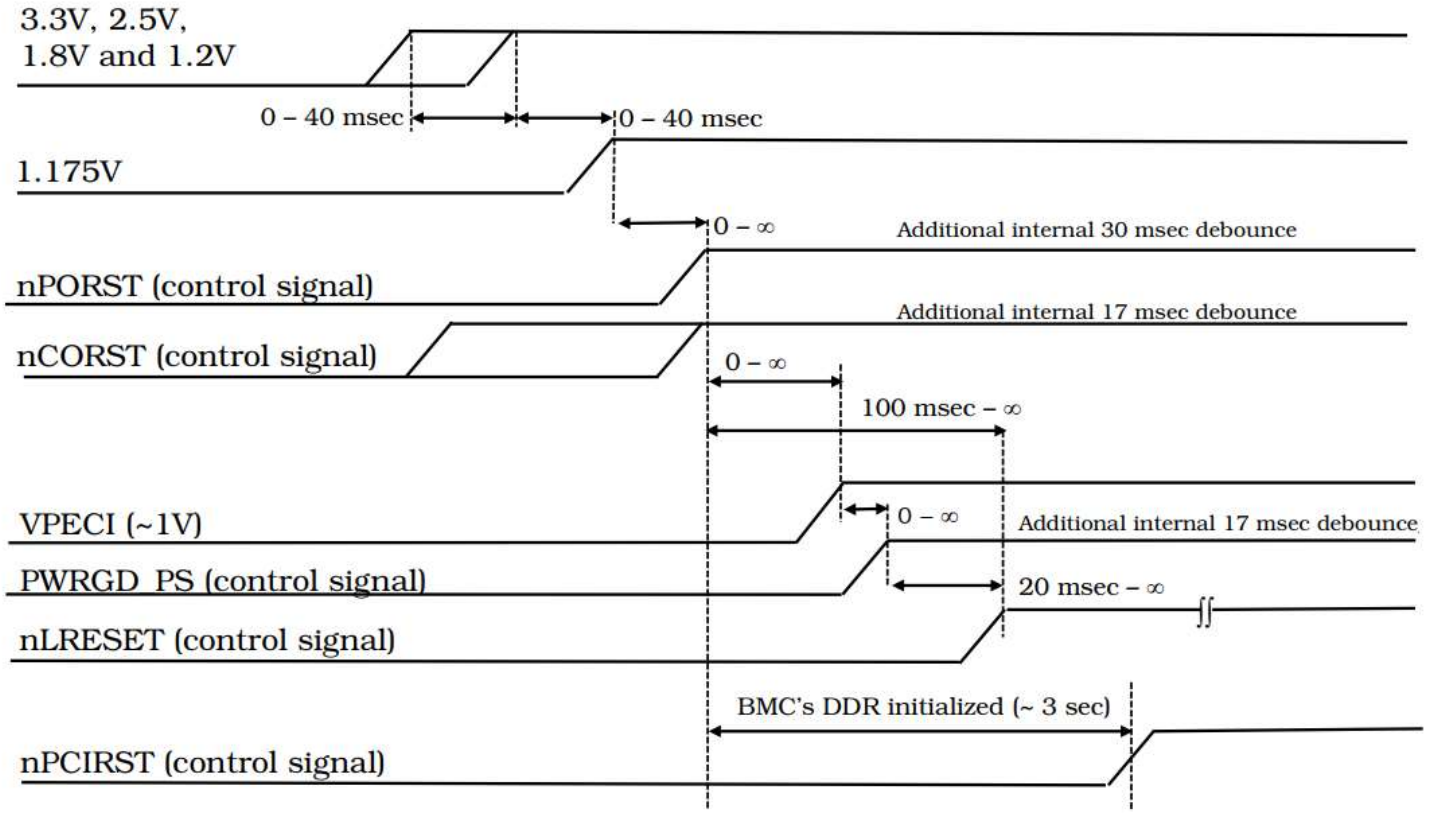
TITLE: **SPI-to-UARTs**

DWG NO RunBMC Module	Tuesday, May 21, 2019	Sheet 18 / 22	Rev A.1.0

Power-Up Sequencing



Notes (timing diagram from BDG):
When standby 3.3V, 2.5V and 1.8V are valid, and standby 1.175V is powered off, there is a ~15 K pull-down resistor on these I/O types:
- o SMB I/O type (buffer type includes C12)
- o Regular I/Os that are NOT DDR4, HSTL, ADC, DAC, PCIe PHY or USB PHY (buffer type includes ST or Ox, except for nMRST)

<Core Design>

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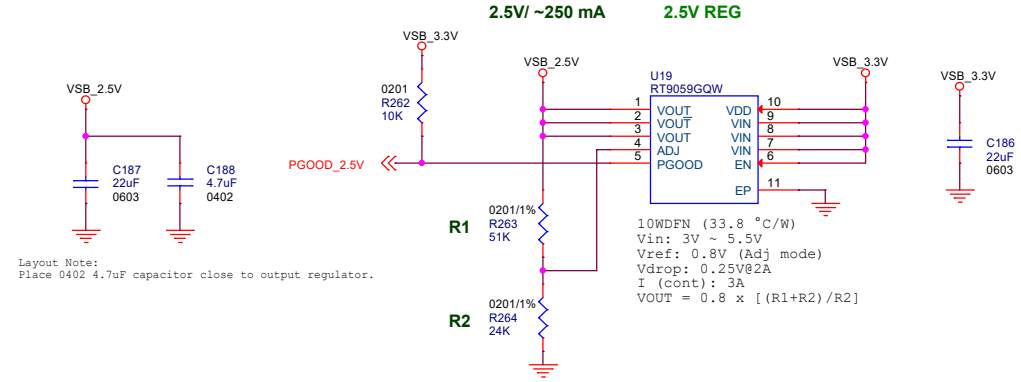
TITLE: **Power-Up Sequencing**

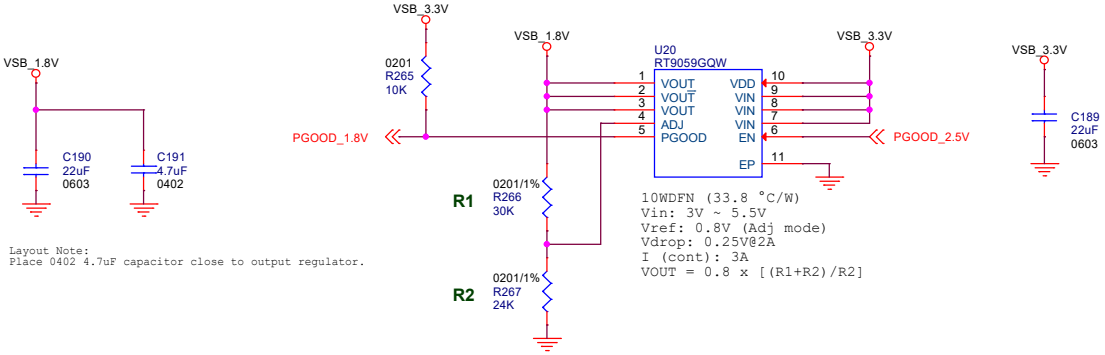
DWG NO		Sheet	Rev
RunBMC Module	Tuesday, May 21, 2019	19 / 22	A.1.0

2.5V/ ~250 mA 2.5V REG



Type: Linear / LDO
Input Voltage: 3.3V
Output Voltage: 2.5V
Max Current: 250mA
Power Dissipation: 0.2W

1.8V/ ~150 mA 1.8V REG



Type: Linear / LDO
Input Voltage: 3.3V
Output Voltage: 1.8V
Max Current: 150mA
Power Dissipation: 0.23W

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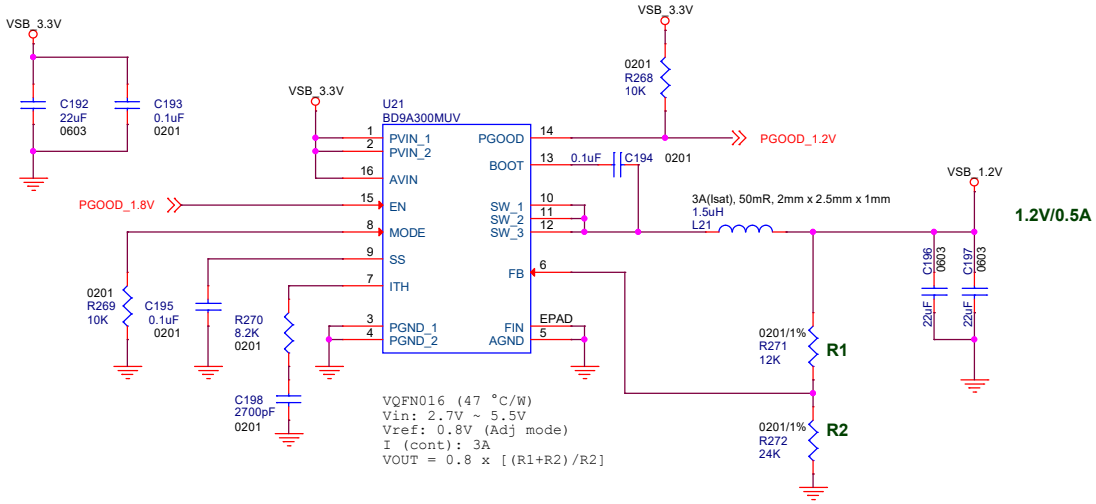
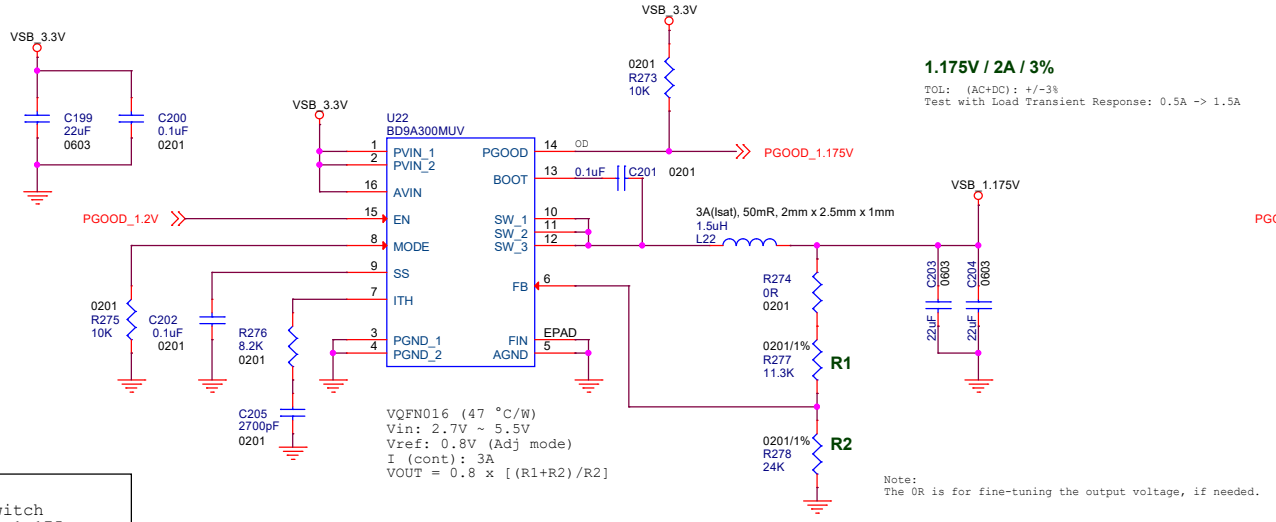
TITLE: **Power Supplies**

DWG NO RunBMC Module	Tuesday, May 21, 2019	Sheet 20 / 22	Rev A.1.0

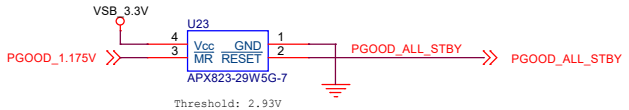


Type: Buck / Switch
Output Voltage: 1.2V
Max Current: 500mA
Power Dissipation: 0.1W



Note:
The 0R is for fine-tuning the output voltage, if needed.

Type: Buck / Switch
Output Voltage: 1.175V
Max Current: 2A
Power Dissipation: 0.4W



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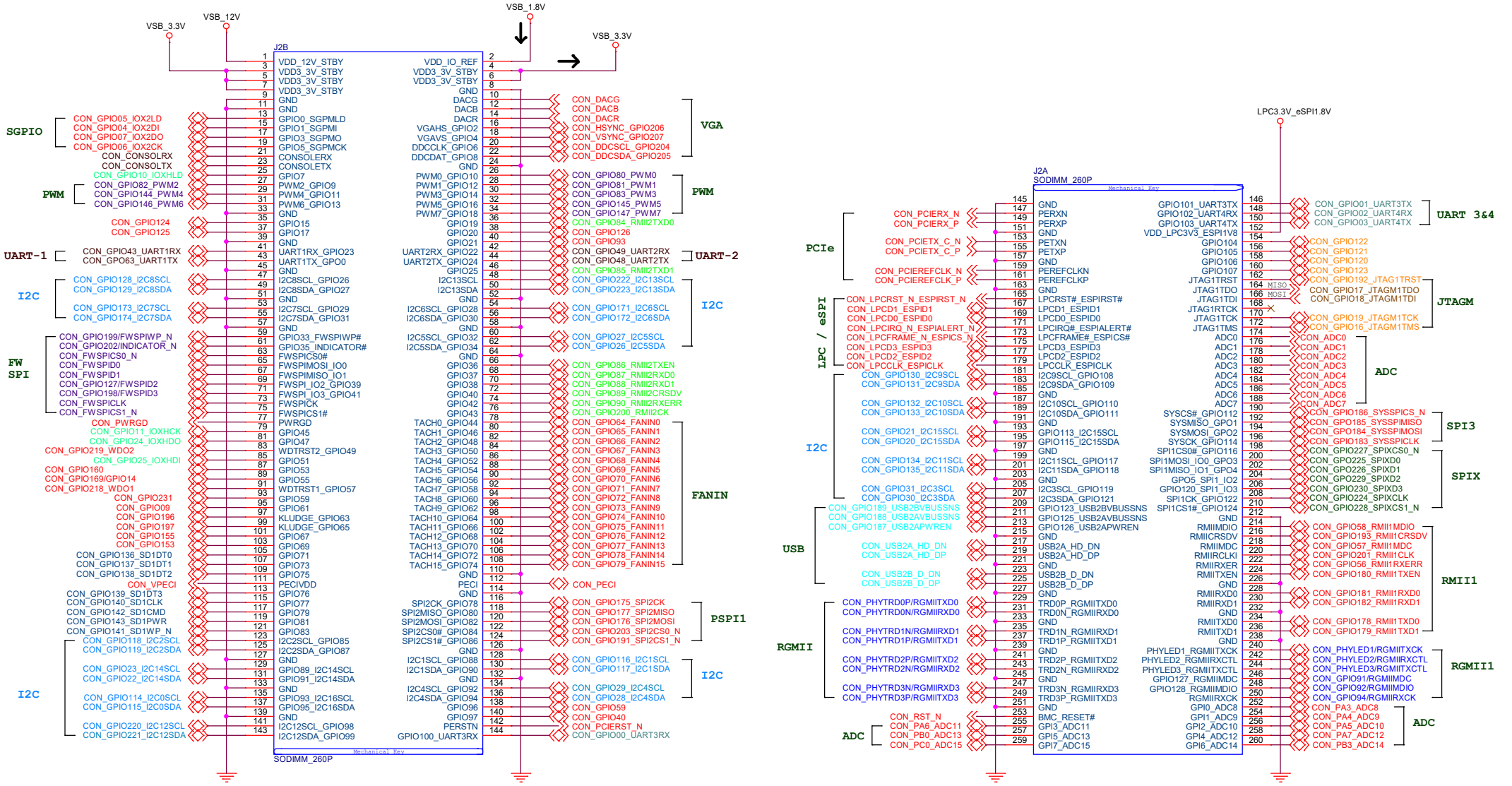
TITLE: **Power Supplies**

DWG NO		Sheet	Rev
RunBMC Module	Tuesday, May 21, 2019	21 / 22	A.1.0

SO-DIMM 260 Edge Connector



Exceptions from RunBMC Standard

RunBMC Pin Number	RunBMC Pin Name	In Func	Limitation:
168	JTAG1RTCK	JTAG	JTAG1 Return Clock is not used.

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TITLE: **SOM Connector**

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RunBMC Module	Tuesday, May 21, 2019	Sheet 22 / 22	Rev A.1.0