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NPCM750x Evaluation Board (EVB)
Quick (Standalone) Setup Guide

August 2015

This Quick Setup guide describes how to set up the NPCM750x EVB.

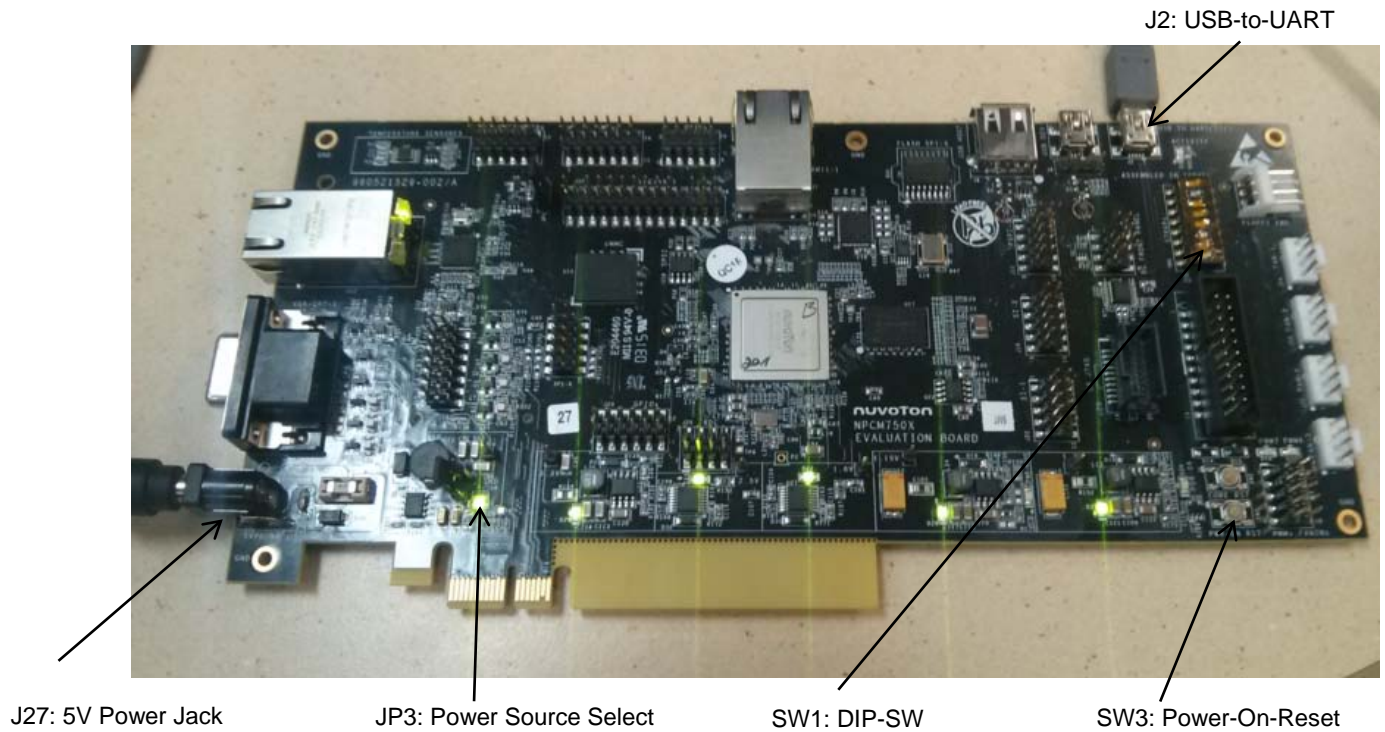J2: USB-to-UART

J27: 5V Power Jack   JP3: Power Source Select   SW1: DIP-SW   SW3: Power-On-Reset

Figure 1: Connectors, Switches and Jumpers on the EVB Board

Note: Instruction refer to Figure 1, above.

1. Power-On and Reset:

   a. Verify that jumper JP3 (power source selector) is in the 1-2 position (to select the 5V power jack).

   b. Verify that all eight dip switches (SW1) are set to the OFF position for normal operation (800 MHz CPU and 800 MHz DDR4).

   c. Connect the 5V power supply to power jack J27. The power supply should be 5V and at least 2.5A; the jack should be 2.5 mm in diameter ('+' in the center core).

   d. Verify that all six green power LEDs (D26, D29, D23, D22, D28, D27) are ON.

   e. Press and hold the PWR-ON-RST (SW3) button to issue a Power-On reset. Also verify that red LED D24 is ON.

   f. Release PWR-ON-RST (SW3) button and verify that LED D24 is OFF.

2. USB-to-UART:

   a. Download and install the USB-to-UART driver from:

      http://www.ftdichip.com/Drivers/VCP.htm

      according to the host OS.

   b. Connect a mini-USB cable between the PC host and J2. J2 is a USB-to-UART connector to the Serial Interface (SI2) of the BMC. Uboot and Linux terminal messages are sent though this port.

   c. Wait for the FTDI driver to be installed automatically. The COM port number is assigned automatically.

3. Terminal:

   a. Open a terminal (e.g., Tera Term version 4.87) and set the correct COM port number assigned by the FTDI driver (in Step 2c).

      The COM port should be configured as follows:
      115 Kbps, 8 bit, 1 stop-bit, no parity no flow control.

   b. Press and release the PWR-ON-RST (SW3) button to issue a Power-On-reset.

   c. Verify that the boot block, Uboot and Linux versions are up-to-date. Check with Nuvoton support for the most recent versions.

```
U-Boot 201310.3.6 (Jun 08 2015 - 11:04:48) by Nuvoton Technology Corp.

HAL ver : v0.3.1

Board: PolegSVB
Chip : npcm750
Core : Cortex-A9

CPU Freq:      800MHz
Memory Freq:   800MHz
SPI0 Freq:     40MHz
SPI3 Freq:     20MHz
APB1 Freq:     50MHz
APB2 Freq:     50MHz
APB3 Freq:     50MHz
APB4 Freq:     25MHz
APB5 Freq:     100MHz

RomCode   : v00.00.03.02
BootBlock : v00.10.02.19

PolegSVB Power-On Straps = 0x1ff7
Security: DISABLED, running in non-secure mode

DRAM:  496.1 MiB
WARNING: Caches not enabled
Flash: Reducing flash chip size from 32 MB to 16 MB
16 MiB
In:    serial
Out:   serial
Err:   serial
MMC:   npcmx50_sdhci: 0, npcmx50_sdhci: 1
Net:   ETH0, ETH1, ETH2, ETH3
Hit any key to stop autoboot:  0
## Booting kernel from Legacy Image at 80200000 ...
   Image Name:   Linux-3491.2.4
   Image Type:   ARM Linux Kernel Image (uncompressed)
   Data Size:    1761528 Bytes = 1.7 MiB
   Load Address: 00008000
   Entry Point:  00008000
   Verifying Checksum ... OK
   Loading Kernel Image ... OK

Starting kernel ...

Booting Linux on physical CPU 0
Linux version 3491.2.4 (ubuntu@ubuntu12) (gcc version 4.8.1 (Sourcery CodeBench Lite 2013.11-33) ) #1 Mon Jul 6 19:01:09 IDT 2015
CPU: ARMv7 Processor [414fc091] revision 1 (ARMv7), cr=18c53c7d
CPU: PIPT / VIPT nonaliasing data cache, VIPT aliasing instruction cache
Machine: NPCMX50 Chip family
Memory policy: ECC disabled, Data cache writeback
```

Figure 1: Sample Terminal Log File

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