Department of Computer Engineering
Faculty of Engineering, University of Peradeniya

CO221 : Digital Design
Lab 6

Use Proteus in this lab

1. Show how NOT and NOR can be implemented only using **NAND** gates.

2. Show how NOT and NAND can be implemented only using **NOR** gates

3. Implement the full adder circuit using NAND gates. The full adder has 3 inputs A, B and C_{in} where A and B are the input bits of the numbers and C_{in} is the Carry in. There are two outputs S and C_{out} where S is the sum bit and C_{out} is the carry out

    a. Draw the truth table for the full adder
    b. Implement using only NAND gates

Implement the above 3 tasks on the same Proteus schematic capture. Once you have finished up to task 3, show it to an instructor and get marked.

4. Implement a 7-Segment code decoder using logic gates. (To display 0-9 and A, b, C, d, E, F)
    a. Draw the truth table
    b. Try to implement the Karnaugh maps for the 7-segments
    c. Implement the decoder using logic gates. (Use 7SEG-COM-CATHODE for the 7-segment display)

Do task 4 in a new project in Proteus.