EE285
COMMON EMITTER AMPLIFIER

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SEMESTER 4
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TITLE : Common Emitter Amplifier

OBJECTIVE

1. To understand the concept of the DC load line and AC load line.
2. To understand the operation of the common emitter amplifier.
3. To understand the effect of DC blocking capacitors.

APPARATUS

BC109-NPN Transistor
Power Supply
Oscilloscope
Signal Generator
Milliammeter and Voltmeter
Potentiometer
Resistors 10kΩ, 1.2kΩ
Capacitors 0.1pF

PRE-CALCULATIONS

1. Select your operating point as V_{CE} = 6V and I_C = 5mA for the circuit shown in Figure 5. Then calculate the value of R_C (Select a suitable resistor value for R_C from EI 2 series).

Using KVL,

$$V_{CC} = V_{CE} + I_C * R_C$$

$$R_C = (V_{CC} - V_{CE}) / I_C$$
$$R_C = (12 - 6) / 0.005$$
$$R_C = 1200$$
$$R_C = 1.2\ k\Omega$$

2. Obtain an expression for I_C - V_{CE} relation and draw the DC load line.

$$V_{CC} = I_C R_C + V_{CE}$$

$$I_C = -\frac{V_{CE}}{R_C} + \frac{V_{CC}}{R_C}$$

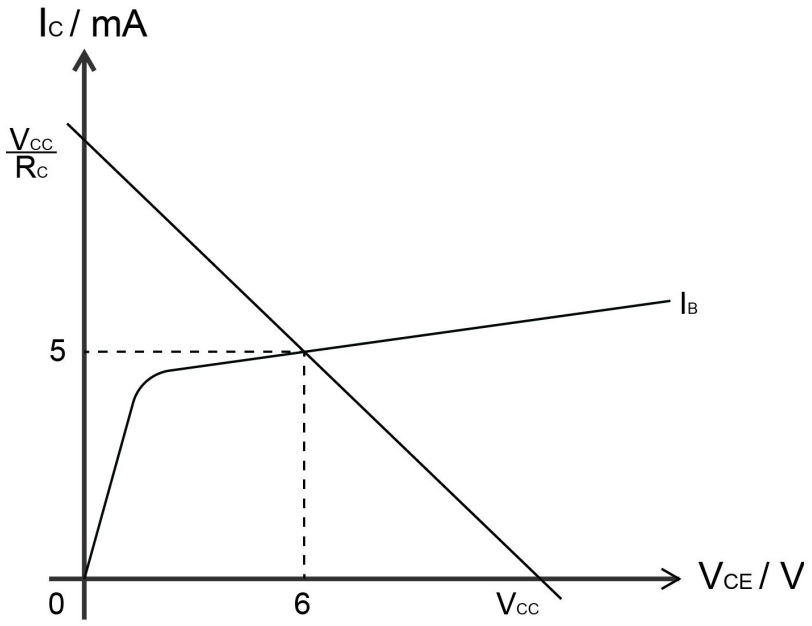

Figure 1: DC Load Line

3. Draw the AC equivalent circuit for the amplifier circuit with the load connected as shown in Figure 2. (No need to draw the small signal model of the transistor)

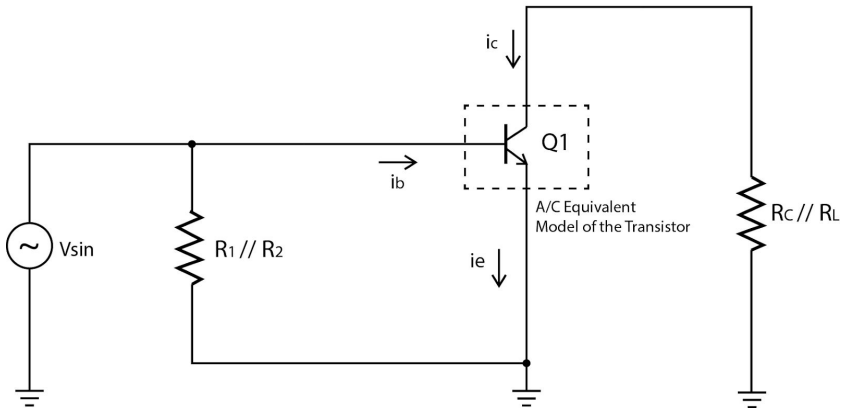

Figure 2: AC equivalent circuit for the common emitter amplifier

4. Obtain an expression for i_c - Vce relation for the amplifier (small signal relation). Then draw the AC load line (You should draw DC and AC load lines on the same graph). Also, indicate the gradients of the two load lines.

Using KVL,

$I_c \times R_{eq} + V_{ce} = 0$; $R_{eq} = (R_C \times R_L) / (R_C + R_L)$

$I_c \times R_{eq} = - V_{ce}$

$I_c = -(1/R_{EQ})\, V_{ce}$

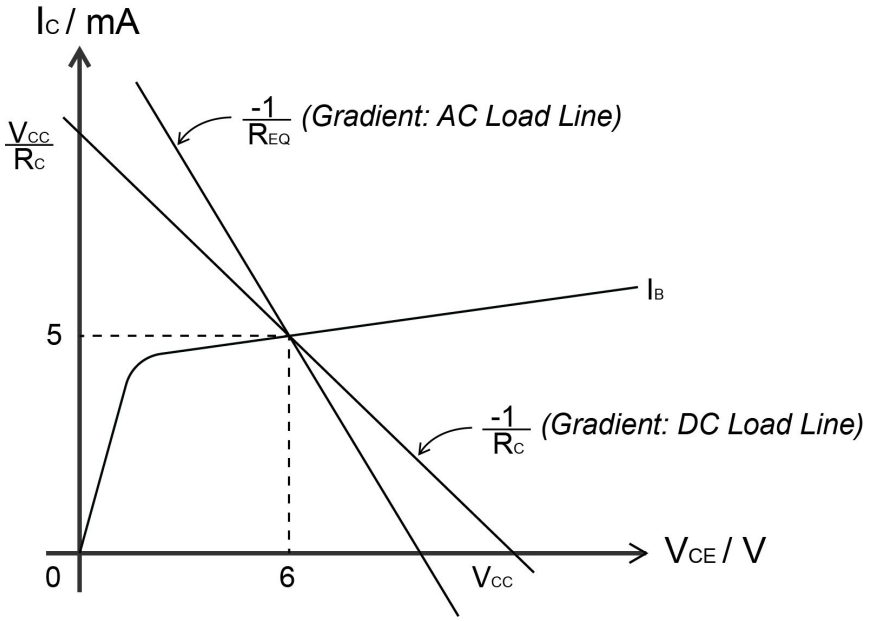

Figure 3: AC and DC load lines

$-1/R_c = - 1 / 1.2\ k\Omega$

$= - 0.833\ k\Omega^{-1}$ *(Gradient of the DC load line)*

$R_{eq} = (R_C \times R_L) / (R_C + R_L)$

$= (1.2k\Omega \times 10\ k\Omega\ ) / (1.2k\Omega + 10k\Omega)$

$= 1.071 \times 1000$

$-1/R_{EQ} = - 0.933\ k\Omega^{-1}$ *(Gradient of the AC load line)*

BRIEF PROCEDURE

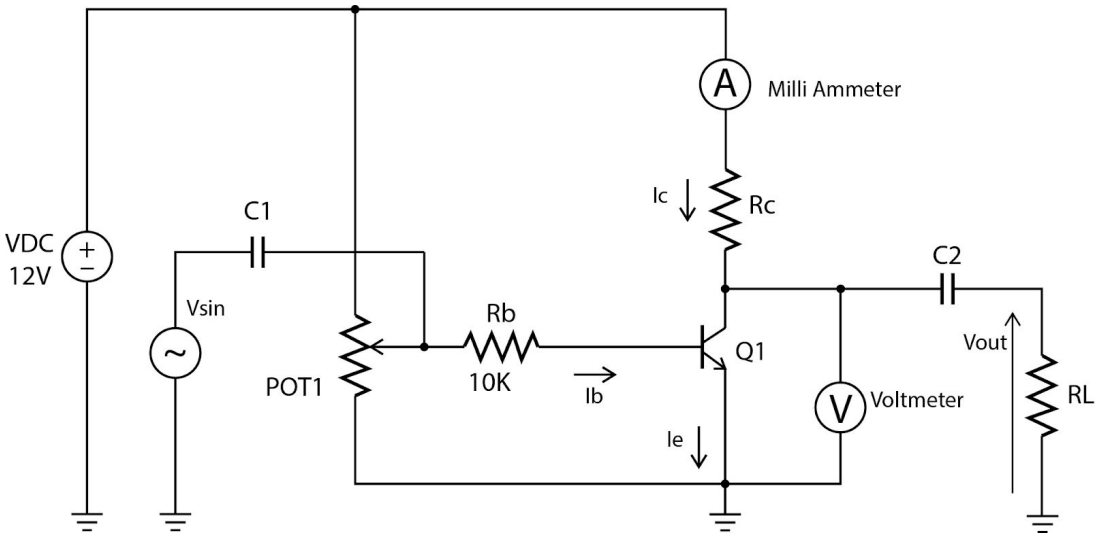

Figure 4: Circuit Diagram

First, the circuit diagram was connected as shown in Figure 4 (Without R_L). We used BC109 NPN Transistor as Q1. After power on, V_{CE} was set to 6V by adjusting the POT1. Next, a sinusoidal input signal of 1 kHz was applied using the Signal Generator.

Next, the amplitude of the input signal was increased from the Signal Generator until the output voltage V_{out} shown its maximum undistorted sinusoidal waveform from the Oscilloscope. Then the positive and negative peak voltages were observed and recorded with and without C_2 Capacitor.

Next, the load resistor, R_L (10 kOhm) was connected to the circuit. Oscilloscope indicated a distorted signal, therefore the amplitude of the input signal was reduced. Input and Output voltages were obtained and the Loaded Small Signal Voltage Gain was calculated from the observed values.

Then the operating point of the transistor was changed until V_{CE} = 2V by adjusting the POT1. The distorted sinusoidal signal was recorded with C_2 and without R_L. Again, the operating point was changed to V_{CE} = 10V by adjusting the POT1 and the distorted sinusoidal signal was observed.

OBSERVATIONS

Step 4

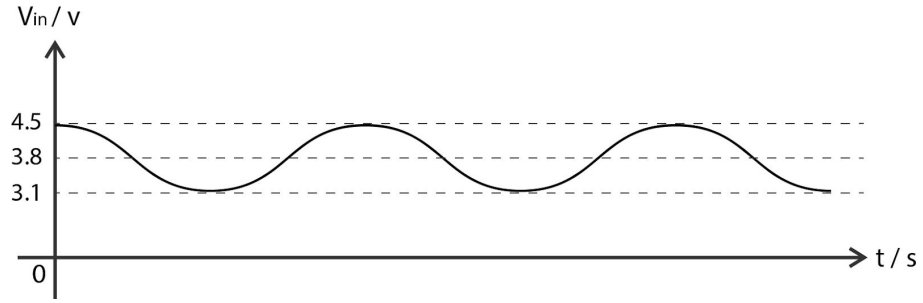

Figure 5: Intput Signal

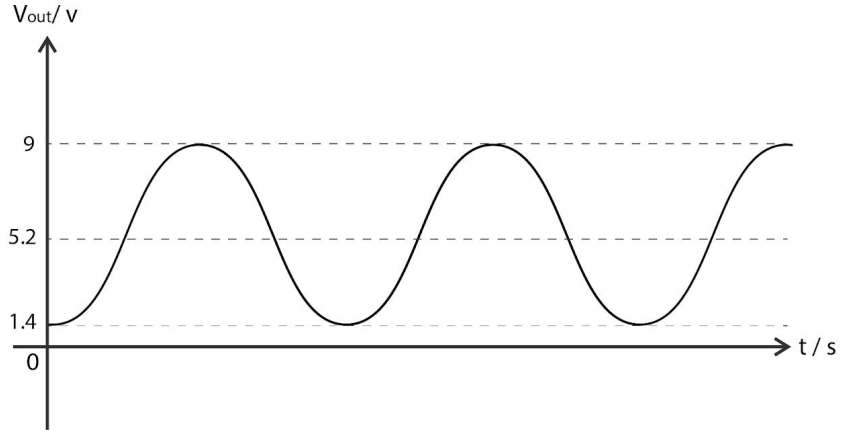

Figure 6: Output Signal without C_2

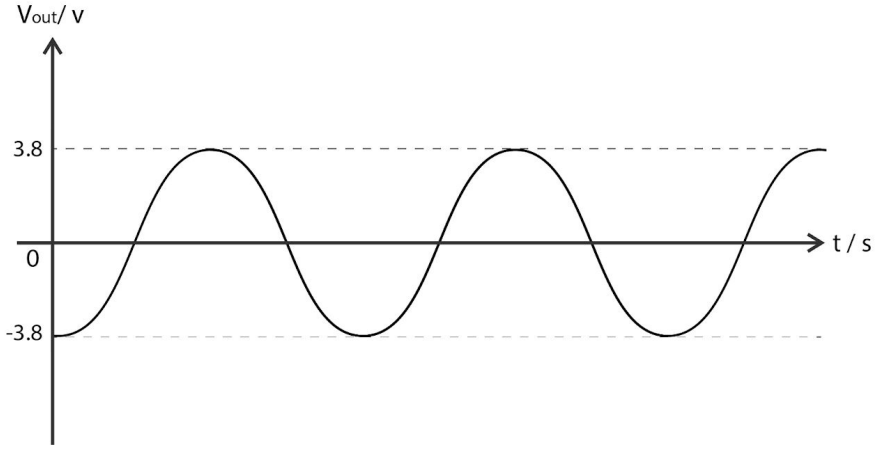

Figure 7: Output Signal with C_2

Small Signal No-load Voltage Gain = 7.6V / 1.4V
= 5.43

Step 5

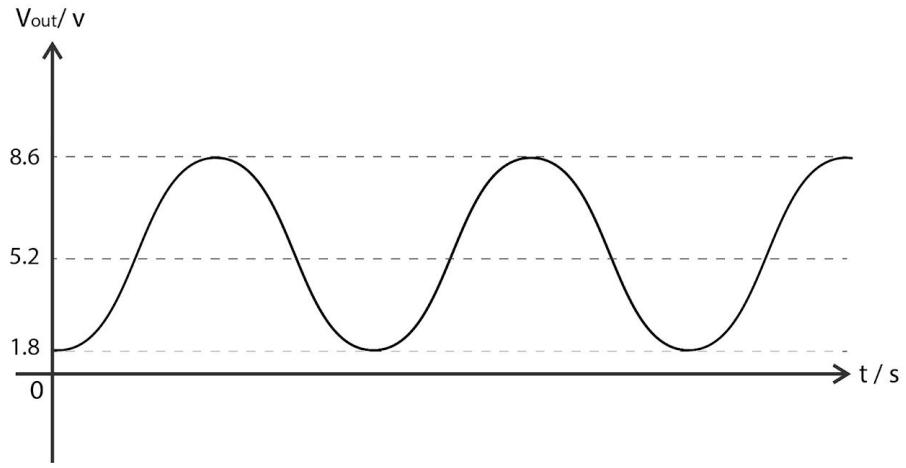

Figure 8: Output Signal without C_2

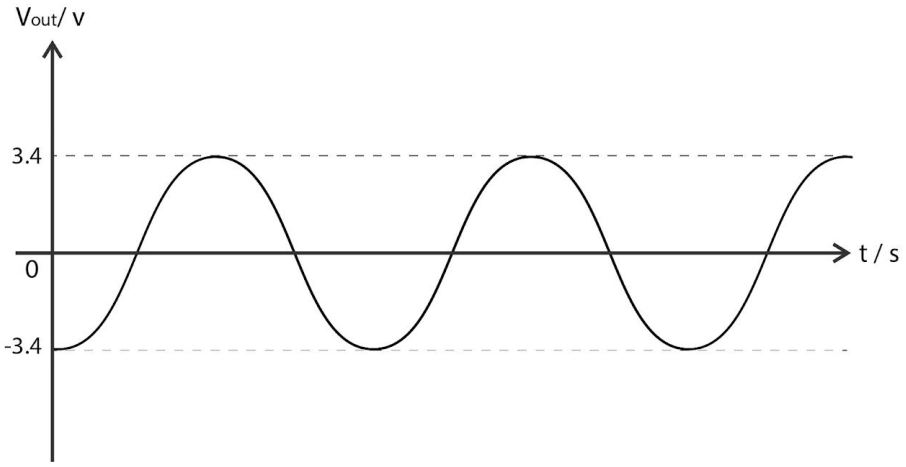

Figure 9: Output Signal with C_2

Loaded Small Signal Voltage Gain = 7.3 V / 1.4 V
= 5.21

Step 6

V_{CE} = 2V

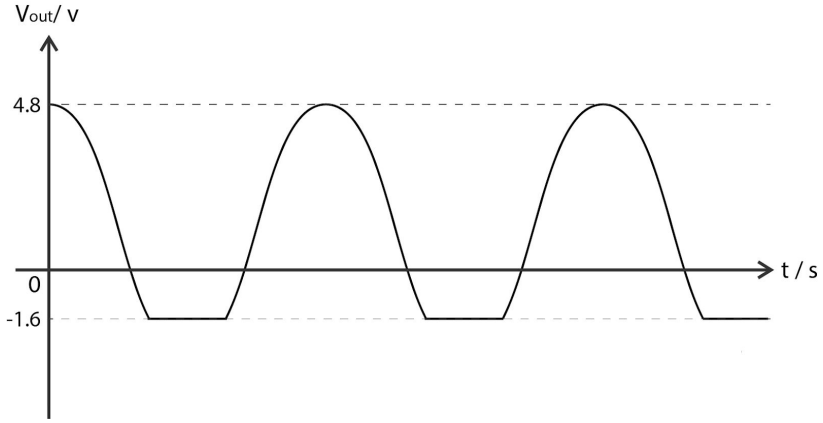

Figure 11: Output Signal with C_2, without R_L

Now Q-point is in below the mid-range of the DC load line and therefore the lower parts of the amplified signal will meet transistor's cut-off region. Due to cut-off state of the transistor, no voltage change happens to V_{out} = V_{CE} in that time period.

Step 7

V_{CE} = 10V

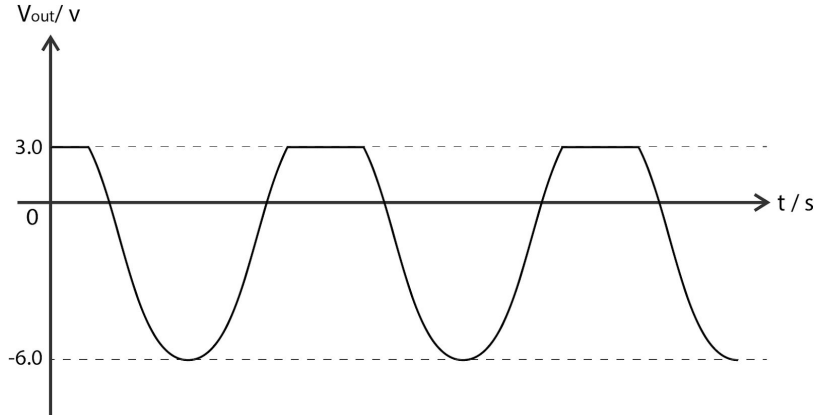

Figure 12: Output Signal with C_2, without R_L

Now Q-point is in above the mid-range of the DC load line and therefore the upper parts of the amplified signal will meet transistor's saturated region. Due to saturation state of the transistor, no voltage change happens to V_{out} = V_{CE} in that time period.

CALCULATIONS

1. Calculate the theoretical small signal voltage gain of the amplifier and compare it with the observed results.

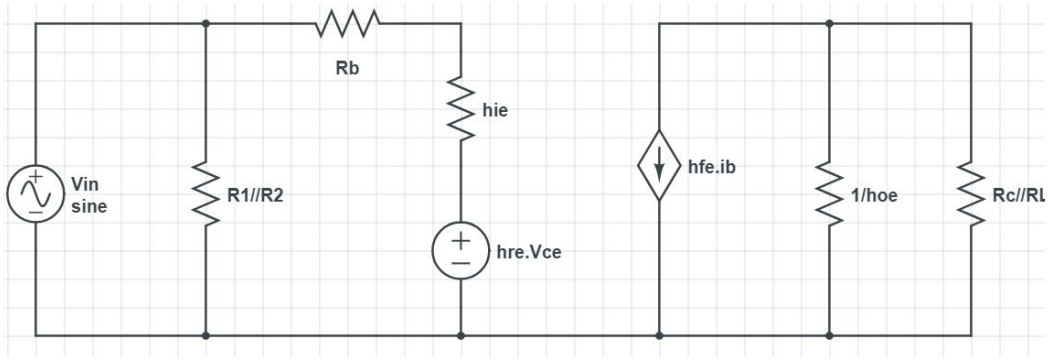

Figure 13: AC Equivalent model of the common emitter transistor amplifier

h_{fe} = 240 (Group B, min)
h_{ie} = 3.2 kΩ (Group B, min)
h_{re} = -
h_{oe} = 60 x 10-6 Ω (Group B, max)

Both h_{re} and $1/h_{oe}$ have very small values, then we can neglect them in the calculation.

With Load Resistor RL

$V_{in} = i_B \times (R_B + hie)$

$V_{out} = - (R_L // R_C) \times i_c$
$= - (R_E) \times h_{fe} \times i_b$; $R_E = R_L // R_C$

$R_E = R_L // R_C$
$= (10\ k\Omega \times 1.2\ k\Omega) / (10\ k\Omega + 1.2\ k\Omega)$
$= 1.071\ k\Omega$

$Av = V_{out} / V_{in}$
$= - (R_E \times h_{fe} \times i_b) / (i_b \times (R_B + h_{ie}))$
$= - (R_E \times h_{fe}) / (R_B + h_{ie})$
$= - (1.071 \times 240) / (3.2 + 10)$
$= - 19.473$

$Gain = | Av |$
= 19.473

Without Load Resistor RL

V_{in} = i_B x (R_B + hie)

V_{out} = - R_C x i_c
= - R_C x h_{fe} x i_b

Av = V_{out} / V_{in}
= - (R_C x h_{fe} x i_b) / (i_b x (R_B + h_{ie}))
= - (R_C x h_{fe}) / (R_B + h_{ie})
= - (1.2 x 240) / (3.2 + 10)
= - 21.818

Gain = | Av |
= 21.818

Gain	Theoretical Value	Practical Value
With Load of 10kΩ	19.5	5.21
Without Load	21.8	5.43

Here we can see a significant difference between theoretical values and practical values. Possible reasons for this difference are neglecting the values of h_{re}, $1/h_{oe}$ and neglecting the effect of the coupling capacitors.

2. Select the operating point such that V_{CE} = 6V and calculate the value β_{dc} (h_{FE}) at the Q-point

At the Q-point,

I_c = 4.2 mA
I_b = (V_{BB} - V_{BE}) / R_B
= (3.8 - 0.65) / 10 kΩ
= 0.315 mA

h_{FE} = I_c / I_b
= 4.2 mA / 0.315 mA
= 13.33

3. The h parameters are given by,

$$\beta(h_{FE}) = \left(\frac{\Delta I_C}{\Delta I_B}\right)_{V_{CE}=constant} \qquad h_{ie} = \left(\frac{\Delta V_{BE}}{\Delta I_B}\right)_{V_{CE}=constant}$$

For the operating point selected above, compute the value of h-parameters

h_{FE} = I_C / I_B
= 4.2 mA / 0.315 mA
= 13.33

h_{ie} = V_{BE} / I_B
= 0.65 x 1000 / 0.315
= 2.064 kΩ

DISCUSSIONS

1. What is the purpose of using capacitors at the input and the output? Should you change the capacitance value when your input signal's frequency ranges changes?

When we giving an AC signal into an amplifier, we should need to keep the operating point (Q-point) in the mid-range of the DC load line. Therefore we need to remove the DC part of the input signal and that is the reason that we are using the coupling capacitors at the input.

To maintain the maximum undistorted gain of the amplifier, we are fixing the Q-point at the mid-range of the DC load line, but we don't need that DC voltage as an amplified output signal. Therefore we are using a coupling capacitor at the output to filter out the DC part of the output signal.

Capacitors have big reactance at lower frequencies and they need much larger capacitance values to allow these lower-frequency signals to pass through. Therefore we should change the capacitance value when we changing the input signal frequency.

2. What is the difference between small signal amplifiers and large signal amplifiers? What are their applications?

Small signal model is used for amplifying a very small amplitude voltage signal. This model not affecting the Q-point and it linearizing all the components. Usually using as pre-amplifiers.

Large signal model is used for amplifying signals with large amplitudes. Therefore it affects the Q-point and makes the components non-linear. This model is used for power amplifiers, which are designed to give high current output.

3. What is the effect of adding an emitter resistance (with a capacitor parallel to the resistor) to the circuit? What would happen if you remove the series capacitor?

The purpose of the emitter resistor is to stabilize the bias of the amplifier. In a usual common emitter amplifier circuit, V_B is obtaining from a voltage divider circuit. But if V_{CC} is increased, V_B also increase proportionally. That affects to I_B and then for the Q-point.

But if we added a resistor between the base and the emitter of the transistor, and if V_{CC} is increased, V_B is given by $V_B = V_E + V_{BE}$. Here VB is fixed using a voltage divider and V_E also increasing. That force to reduce V_{BE} and then I_B is reducing to keep the collector current from increasing. Otherwise, we can say the emitter resistance acts as a negative feedback to control the transistors base bias.

But the emitter resistance acts as a feedback resistor, and reduce the amplifiers gain due to fluctuations in the emitter current I_E owing to the AC input signal. But adding a capacitor between ground and the emitter can solve this problem. For AC signal, capacitor short-circuits the resistor and allow the maximum gain for AC signals. Therefore this capacitor is also called as Bypass Capacitor. If the capacitor is removed, the gain of the amplifier will be reduced.

4. What is the effect of adding a load resistance (with a capacitor in series to the resistor) to the circuit? What would happen if you remove the series capacitor?

Since V_{out} is given by the equation, $V_O = (R_C // R_L) \times I_C$, (In AC model) by adding the load resistance will cause to reduce the gain of the amplifier. The capacitor in series to Load Resistor will blocks the DC signal flows through the R_L, but allows to pass AC signals through the Load Resistor.

Therefore if we removed the series capacitor, it allows reducing the gain of the amplifier and also will shift the output AC signal from some amount of DC value.

5. What is the advantage of common emitter configuration when compared with common collector and common base configuration? Explain the reasons.

S.No	Particulars	C.B	C.E	C.C
1.	Current Gain	Nearly Unity	High	Very High
2.	Voltage Gain	High	Very High	Nearly Unity
3.	Power Gain	High	High	Low
4.	Input Impedance	Low	High	Very High
5.	Output Impedance	Very High	High	Low
6.	Phase Reversal	No	Yes	No

By comparing all three types of transistor amplifiers, common collector arrangement has the highest Input Impedance. The common base arrangement has the highest output impedance. But considering both, the common emitter arrangement has moderate values. By considering the voltage and current gains, common emitter arrangement has the highest voltage gain and the current gain comparing to the other two arrangements. Thus, we can say the common emitter arrangement is the best choice for a general purpose amplifier.

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