Radial Multistage Thermoelectric Cooling for 3D Integrated Circuits: Mathematical Modelling and Thermal Network Formulation

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***Abstract*—This paper presents a mathematical model for a radial, multi-stage thermoelectric cooler (TEC) integrated with a stacked microelectronic chip. Heat is extracted laterally from a central hotspot through a coupled two-layer thermal network consisting of a silicon "chip layer" and an active TEC layer, and rejected at the package perimeter to a micro-channel heat sink. We derive: (i) element-level TEC relations including Peltier, Joule and conductive terms; (ii) equivalent radial and vertical thermal resistances for wedge-shaped sectors and through-silicon via (TSV) bundles; and (iii) a global block-matrix formulation for the coupled silicon–TEC network. The formulation is extended with an additional central node that aggregates volumetric heat generation in the innermost cylinder. The resulting sparse, asymmetric linear system is suitable for optimization of TEC geometry and operating currents.**

I. Introduction

Modern high-power 3D integrated circuits (3D-ICs) can reach power densities on the order of $100\,\mathrm{W\,cm^{-2}}$ and total powers of $400\,\mathrm{W}$ or more. Conventional cooling solutions relying on vertical heat extraction and top-side heatsinks are challenged by strong vertical temperature gradients and limited heat removal from deeply buried dies.

This work considers an alternative architecture in which heat from a central hotspot is transported *radially* towards the chip perimeter using a multistage radial TEC, where the rejected heat is removed by a micro-channel heat sink. Each radial wedge behaves as a one-dimensional multistage TEC in the radial direction; the full device consists of N_θ identical wedges arranged azimuthally.

We focus on the mathematical formulation of a single representative wedge, whose solution can be scaled to the full 2π device. All derivations are carried out for a steady-state operating point with prescribed stage currents.

II. Nomenclature

For clarity, the main symbols and subscripts used throughout this paper are summarized in the boxed, two-column list below.

III. Geometry of the Radial TEC Wedge

Figure 1 illustrates the cross-sectional layout of a single radial TEC element (one wedge segment) used in this work. The main components are:

- **(Red arrow)** ceramic interconnect / substrate (dark grey),
- **(Blue arrows)** thermoelectric legs: blue = p-type, red = n-type,
- **(Green arrow)** azimuthal copper wiring (pink) connecting this TEC element to the next element on the same stage,
- **(Black arrow)** copper interconnect (yellow) between the p and n legs of the same TEC couple.

The geometry of each wedge is parameterised to support optimisation (see the parameter list in Section II). Below we summarise the role and dimensional parameters of each sub-component.

A. Central Cylinder and Wedge Angle

The radial TEC surrounds a central cylindrical heat spreader of radius R_{cyl} (silicon), which collects heat from the stacked dies and feeds it into the radial stages. The representative wedge spans an angle $\theta = 2\pi/N_\theta$ and all radial dimensions are measured from $r = R_{\text{cyl}}$ outwards.

The first TEC stage has radial length L_1 so that its outer radius is $R_{\text{cyl}} + L_1$. Subsequent stages expand radially according to the geometric ratio k_r ("radial expansion factor"),

$$\frac{L_{i+1}}{L_i} = k_r, \tag{1}$$

giving stage boundaries

$$r_{\text{start},1} = R_{\text{cyl}}, \qquad r_{\text{end},1} = R_{\text{cyl}} + L_1, \tag{2}$$

$$r_{\text{start},2} = r_{\text{end},1}, \qquad r_{\text{end},2} = r_{\text{end},1} + k_r L_1, \text{ etc.} \tag{3}$$

The central region $0 \le r \le R_{\text{cyl}}$ is modelled as node T_0, with internal thermal resistance $R_{\text{int,chip}}$ and volumetric heat generation $Q_{\text{gen},0}$ as described in Section V.

B. Ceramic Interconnect (Radial Support)

The ceramic interconnect (dark grey in Fig. 1) provides a mechanically robust and electrically insulating base between neighbouring p and n legs, while also acting as a controlled thermal "dam" between stages. Its key roles are:

- maintaining electrical isolation between legs and TSVs,
- providing a high-conductivity radial path where desired (e.g., AlN),
- shaping the effective series resistance R_{is} between stages (Sec. III-F).

Symbols			
Q	Heat flow rate [W]	R	Thermal / electrical resistance [K/W, Ω]
K	Thermal conductance [W/K]	k	Thermal conductivity [W/(m K)]
T	Temperature [K]	I	Electrical current [A]
A	Area [m^2]	L	Length (radial leg length) [m]
t	Thickness (out-of-plane) [m]	w	In-plane width (radial or azimuthal) [m]
N	Count of repeated elements (e.g., wedges, TSVs)	P	Pitch (TSV spacing) [m]
S	Seebeck coefficient term [V/K]	x	Generic state vector entry
α	Seebeck coefficient per leg [V/K]	ρ	Electrical resistivity [Ω m]
θ	Wedge angle [rad]		
q''	Heat flux [W/m^2]		
Subscripts and Superscripts			
i	Radial ring / TEC stage index	0	Central cylinder node
Si	Silicon chip layer	c	Cold side of TEC element
h	Hot side of TEC element	TE	Thermoelectric leg quantity
TSV	Through-silicon via quantity	ic	Copper interconnect or wiring
oc	Outer copper connection	is	Radial ceramic/insulator quantity
az	Azimuthal insulator quantity	w	Coolant (water) boundary
lat	Lateral (in-plane) conduction path	vert	Vertical (chip-to-TEC) path
tot	Parallel aggregate of identical elements	global	Effective (combined) quantity
gen	Generated heat source	conv	Convection-related quantity

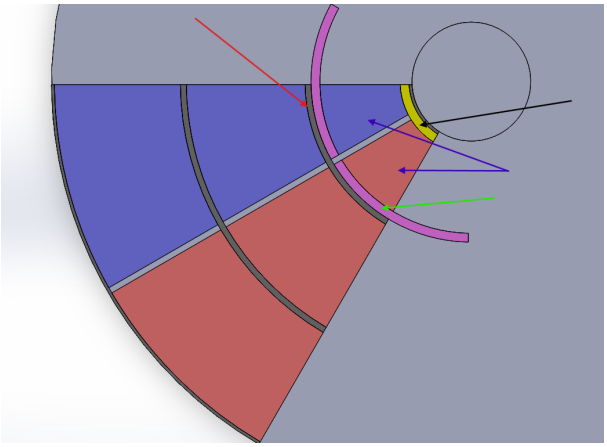

Fig. 1. Top-view schematic of a single radial TEC element showing ceramic interconnect, p/n thermoelectric legs, azimuthal copper wiring to neighbouring elements, and local p–n interconnect.

We characterise the radial ceramic by its thermal conductivity k_{is} and effective radial width w_{is}. For a stage of radial length L_i the radial-insulator contribution to the total series resistance is given by Eq. (32) and contributes to $R_{\text{eff,series}}$ and ultimately to K_i.

C. Thermoelectric Legs

Each TEC element consists of a p-type and an n-type leg (red-blue pair in Fig. 1) connected in series electrically and in parallel thermally. Their material is typically Bi_2Te_3 with properties given in the parameter table. The legs are arranged azimuthally over an angle θ per element and radially over the stage length L_i.

The leg geometry determines the stage conductance $K_{\text{total,TE}}$, Seebeck term S_i, and electrical resistance $R_{TE,i}$ used in the nodal equations:

- L_i: radial length of legs in stage i,
- θ: Azimuthal span of both TE legs
- t: out-of-plane thickness.

Stage-to-stage length variation is governed by the expansion factor k_r as above.

D. Copper Interconnect and Outerconnect

The copper p–n interconnect (yellow, black arrow) links the p and n legs in the same TEC element. Its radial length and thickness are denoted $w_{\text{ic},i}$ and $t_{\text{ic},i}$, and its azimuthal span by $\beta_{\text{ic},i}$. These parameters control both the vertical resistance to TSVs (through the contact area and TSV count) and the in-plane electrical resistance $R_{e,\text{ic}}$.

An outer copper connection ("outerconnect") of radial width $w_{\text{oc},i}$, thickness $t_{\text{oc},i}$, and azimuthal span $\beta_{\text{oc},i}$ completes the current loop at the hot side of stage i and interfaces with either the next stage or with the cooling manifold.

E. Azimuthal Insulators

The green arrow in Fig. 1 indicates azimuthal insulators that electrically insulate a given TEC element from the next element along the stage. These traces are dimensioned by their arc length w_{az}, thickness (layer thickness t) and length which is equal to TEC length L_i. Their thermal conductance contributes to the back conduction and is implicitly included in K_{global} where appropriate.

F. Radial Insulators

Radial insulators of width w_{is} separate successive TEC stages to suppress direct conduction while still allowing radial conduction. Their radial resistance R_{is} is given by Eq. (32). This resistance is added in series to the TEC-leg resistance $1/K_{\text{total,TE}}$ to form $R_{\text{eff,series}}$.

G. Thermal TSVs and Vertical Path

Thermal TSVs (copper cylinders of radius $R_{\text{TSV},i}$ and pitch $P_{\text{TSV},i}$) establish the vertical thermal path between selected chip rings and the TEC cold junctions in the evaporator zone. Their count per ring is controlled by the interconnect width $w_{\text{ic},i}$ and the radial clearance g_{rad}, using the relations in Eq. (30).

The equivalent TSV resistance $R_{\text{TSV,tot}}$ and interconnect resistance R_{ic} combine into the vertical resistance $R_{v,i}$ (Eq. (31)), which appears as the coupling element in the block matrices. In the pumping zone, we set $R_{v,i}$ to a very large value to emulate the absence of TSVs.

IV. TEC Element-Level Model

Consider a single thermoelectric stage with cold-side temperature T_c and hot-side temperature T_h operated at current I. Using standard lumped-parameter notation,

- K [W/K]: thermal conductance of the leg pair (including effective series/parallel contributions of ceramic and azimuthal insulator),
- S [V/K]: Seebeck coefficient multiplied by the number of couples in the stage,
- R_e [Ω]: total electrical resistance of the stage, including interconnects as appropriate.

The steady-state heat balance at the cold side can be written as

$$Q_c = SIT_c - K(T_h - T_c) - Q_{\text{J,c}}, \tag{4}$$

where Q_c is the net heat absorbed at the cold junction (positive when cooling) and $Q_{\text{J,c}}$ is the fraction of Joule heat deposited at the cold side. For a symmetric leg pair with interconnects concentrated at the cold junction, the Joule contribution can be expressed as

$$Q_{\text{J,c}} = \frac{1}{2} I^2 R_{\text{TE}} + I^2 R_{e,\text{ic}} + \frac{1}{2} I^2 R_{e,\text{w}}, \tag{5}$$

where R_{TE} is the electrical resistance of the TE legs, $R_{e,\text{ic}}$ is the cold-side interconnect resistance, and $R_{e,\text{w}}$ accounts for any series wiring between isothermal nodes.

The corresponding hot-side heat is

$$Q_h = SIT_h - K(T_h - T_c) + (I^2 R_e - Q_{\text{J,c}}), \tag{6}$$

so that energy conservation ($Q_h - Q_c = I^2 R_e$) is satisfied.

For a multistage one-dimensional TEC stack indexed by $i = 1, \ldots, M$ (increasing temperature from cold to hot), we will later make use of the interface relation $Q_{h,i} = Q_{c,i+1}$ at each internal stage boundary.

A. Variable Cross-Section TEC Legs and Geometric Factor

In the radial TEC, each leg pair occupies a wedge of constant angle θ and out-of-plane thickness t, but the available cross-section for heat and current flow varies with radius r due to: (i) trapezoidal leg shape, (ii) embedded copper interconnect and outerconnect, (iii) radial ceramic gaps w_{is}, and (iv) azimuthal insulation width w_{az}. Instead of carrying all of these details explicitly in the network, we encapsulate them into a single geometric factor G_i for stage i.

We subdivide a single leg in stage i into three radial regions between inner radius r_1 and outer radius $r_1 + L_i$:

- inner copper interconnect region: $r \in [r_{\text{start}},\, r_1 + w_{\text{ic},i}]$,
- full TE material region: $r \in [r_1 + w_{\text{ic},i},\, r_1 + L_i - w_{\text{oc},i}]$,
- outer copper connect region: $r \in [r_1 + L_i - w_{\text{oc},i},\, r_{\text{end}}]$,

with effective start and end radii corrected for the radial ceramic gap,

$$r_{\text{start}} = r_1 + \frac{w_{\text{is}}}{2}, \qquad r_{\text{end}} = r_1 + L_i - \frac{w_{\text{is}}}{2}, \tag{7}$$

for interior stages ($i = 2, \ldots, N-1$). For the first and last stages, the full width w_{is} is attributed to the single adjacent TEC, so $w_{\text{is}}/2$ is replaced by w_{is}.

The baseline area available to a single leg accounting for a constant azimuthal insulation width w_{az} is

$$A_{\text{base}}(r) = t\left(r\,\tfrac{\theta}{2} - w_{\text{az}}\right), \tag{8}$$

which reduces to $t(\theta r/2)$ when $w_{\text{az}} = 0$. In the wire regions, the copper footprint further subtracts area so that the local cross-section can be written generically as

$$A_j(r) = C_j r - D, \qquad j = 1, 2, 3, \tag{9}$$

with region-dependent slopes C_j and a common offset $D = t w_{\text{az}}$. Integrals of the form

$$\int \frac{\mathrm{d}r}{A_j(r)} = \int \frac{\mathrm{d}r}{C_j r - D} = \frac{1}{C_j} \ln\!\left(\frac{C_j r - D}{\cdot}\right) \tag{10}$$

lead to logarithmic contributions from each region. Summing the three pieces and collecting geometry-only terms yields a stage-dependent geometric factor G_i:

$$\begin{aligned} G_i = {} & \frac{1}{t\frac{\theta}{2} - t_{\text{ic},i}\frac{\beta_{\text{ic},i}}{2}} \ln\!\left(\frac{(r_1 + w_{\text{ic},i})(t\frac{\theta}{2} - t_{\text{ic},i}\frac{\beta_{\text{ic},i}}{2}) - t w_{\text{az}}}{r_{\text{start}}(t\frac{\theta}{2} - t_{\text{ic},i}\frac{\beta_{\text{ic},i}}{2}) - t w_{\text{az}}}\right) \\ & + \frac{1}{t\frac{\theta}{2}} \ln\!\left(\frac{(r_1 + L_i - w_{\text{oc},i})(t\frac{\theta}{2}) - t w_{\text{az}}}{(r_1 + w_{\text{ic},i})(t\frac{\theta}{2}) - t w_{\text{az}}}\right) \\ & + \frac{1}{t\frac{\theta}{2} - t_{\text{oc},i}\frac{\beta_{\text{oc},i}}{2}} \ln\!\left(\frac{r_{\text{end}}(t\frac{\theta}{2} - t_{\text{oc},i}\frac{\beta_{\text{oc},i}}{2}) - t w_{\text{az}}}{(r_1 + L_i - w_{\text{oc},i})(t\frac{\theta}{2} - t_{\text{oc},i}\frac{\beta_{\text{oc},i}}{2}) - t w_{\text{az}}}\right). \end{aligned} \tag{11}$$

For a single p-type leg in stage i the electrical and thermal resistances then reduce to

$$R_{e,p,i} = \rho_p\, G_i, \qquad R_{k,p,i} = \frac{G_i}{k_p}, \tag{12}$$

and similarly for the n-type leg,

$$R_{e,n,i} = \rho_n\, G_i, \qquad R_{k,n,i} = \frac{G_i}{k_n}. \tag{13}$$

Because the p and n legs are in series electrically and in parallel thermally, the stage-level electrical resistance and TEC-leg thermal conductance become

$$R_{\mathrm{TE},i} = R_{e,p,i} + R_{e,n,i} = (\rho_p + \rho_n) G_i, \tag{14}$$

$$K_{\mathrm{total,TE},i} = \frac{1}{R_{k,p,i}} + \frac{1}{R_{k,n,i}} = \frac{k_p + k_n}{G_i}, \tag{15}$$

The copper interconnect and outerconnect themselves add azimuthal series resistance to the current loop. Approximating each as a conductive sheet of thickness $t_{\mathrm{ic},i}$ or $t_{\mathrm{oc},i}$ and azimuthal spans $\beta_{\mathrm{ic},i}$ and $\beta_{\mathrm{oc},i}$, their resistances along the azimuth are

$$R_{e,\mathrm{ic},i} = \frac{\rho_c \, \beta_{\mathrm{ic},i}}{t_{\mathrm{ic},i} \, \ln\!\left(\dfrac{r_1 + w_{\mathrm{ic},i}}{r_1}\right)}, \tag{16}$$

$$R_{e,\mathrm{oc},i} = \frac{\rho_c \, \beta_{\mathrm{oc},i}}{2 t_{\mathrm{oc},i} \, \ln\!\left(\dfrac{r_1 + L_i}{r_1 + L_i - w_{\mathrm{oc},i}}\right)}, \tag{17}$$

so that the total electrical resistance for stage i used in the Joule terms is

$$R_{e,i} = R_{\mathrm{TE},i} + R_{e,\mathrm{ic},i} + 2R_{e,\mathrm{oc},i}. \tag{18}$$

In the nodal TEC balance, Eqs. (41)–(42), the half-split Joule term $\frac{1}{2} I_i^2 R_{e,i}$ therefore includes the full contribution of both legs and all azimuthal wiring in stage i, while the stage conductance K_i appearing in the conductive terms is identified with the global conductance

$$K_i = K_{\mathrm{global},i} = K_{\mathrm{eff,series},i} + K_{\mathrm{az},i}, \tag{19}$$

where $K_{\mathrm{eff,series},i}$ is constructed from $K_{\mathrm{total,TE},i}$ via Eqs. (33)–(35).

V. Radial Wedge Geometry and Resistances

We now restrict attention to a single wedge of azimuthal span θ (rad), representing an angle $\theta = 2\pi/N_\theta$ of the full circular device.

A. Chip Layer: Radial Conduction and Heat Generation

The bottom silicon die is modelled as a solid cylindrical wedge of thickness t_{chip} and thermal conductivity k_{Si}. Radial heat transport occurs between concentric radii r_a and r_b within the wedge. The cross-sectional area normal to the radial heat flow at radius r is

$$A_{\mathrm{Si}}(r) = r \, \theta \, t_{\mathrm{chip}}. \tag{20}$$

The corresponding radial thermal resistance between r_a and r_b is obtained by integration,

$$R_{\mathrm{lat}}(r_a, r_b) = \int_{r_a}^{r_b} \frac{\mathrm{d}r}{k_{\mathrm{Si}} A_{\mathrm{Si}}(r)} = \frac{1}{k_{\mathrm{Si}} t_{\mathrm{chip}} \theta} \ln\!\left(\frac{r_b}{r_a}\right). \tag{21}$$

The chip layer also hosts volumetric power dissipation. We model this as a uniform heat flux q'' [W/m^2] applied over the top surface of each radial segment. For a segment spanning radii r_{i-1} to r_i, the top area is the sector area

$$A_{\mathrm{top},i} = \frac{\theta}{2}(r_i^2 - r_{i-1}^2), \tag{22}$$

and the corresponding generated heat assigned to node i is

$$Q_{\mathrm{gen},i} = q'' A_{\mathrm{top},i}. \tag{23}$$

At the very centre, $0 \le r \le R_{\mathrm{cyl}}$, we approximate the hotspot as a cylinder with total generation obtained from a prescribed heat flux q''_{flux} as

$$Q_{\mathrm{gen},0} = q''_{\mathrm{flux}} \, \frac{1}{2} R_{\mathrm{cyl}}^2 \, \theta, \tag{24}$$

where q''_{flux} denotes the chip-side heat flux for the *full* device and the factor θ accounts for the fact that a single wedge occupies only a fraction $\theta/(2\pi)$ of the total circumference. Equivalently, one may prescribe a total chip power Q_{tot} and scale it to the representative wedge as $Q_{\mathrm{gen},0} = Q_{\mathrm{tot}}/N_\theta$.

The effective thermal resistance from the peak temperature at the cylinder centre to its outer surface can be written as

$$R_{\mathrm{int,chip}} = \frac{1}{2 \, \theta \, k_{\mathrm{Si}} \, t_{\mathrm{chip}}}, \tag{25}$$

which we identify with $R_{\mathrm{Si},0\to1}$ in the network.

B. Vertical Resistance: TSV Bundle and Interconnect

Vertical coupling between the chip and the TEC cold junction is provided by a bundle of TSVs in parallel, plus metal interconnect in series. The resistance of a single TSV of radius R_{TSV} and length t_{SOI} is

$$R_{\mathrm{TSV}} = \rho_{\mathrm{TSV}} \frac{t_{\mathrm{SOI}}}{\pi R_{\mathrm{TSV}}^2}, \tag{26}$$

and with N_{TSV} identical vias in parallel the equivalent becomes

$$R_{\mathrm{TSV,tot}} = \frac{R_{\mathrm{TSV}}}{N_{\mathrm{TSV}}}. \tag{27}$$

The via count is determined geometrically from available interconnect width w_{ic}, TSV pitch P_{TSV}, radial clearance g_{rad}, and local radius r, e.g.,

$$N_{\mathrm{row}} = \left\lfloor \frac{w_{\mathrm{ic}}}{2R_{\mathrm{TSV}} + g_{\mathrm{rad}}} \right\rfloor, \tag{28}$$

$$N_{\mathrm{per\text{-}row}} = \left\lfloor \frac{r \, \beta_{\mathrm{ic}}}{P_{\mathrm{TSV}}} \right\rfloor, \tag{29}$$

$$N_{\mathrm{TSV}} = N_{\mathrm{row}} N_{\mathrm{per\text{-}row}}. \tag{30}$$

We consider the middle of the copper interconnect as the cold junction. Between it and the TSV endpoint there is the dielectric electrical insulation layer and half of the thickness of the copper interconnect layer. Then the total vertical resistance is given by,

$$R_v = R_{TSV} \tag{31}$$

For now we can assume that the thermal resistance of dielectric layer and the copper interconnect is zero. This can be attributed very thin (500nm) dielectric layer and the higher conductivity of copper.

C. TEC Leg Effective Conductance with Insulator

Between neighbouring TEC stages there exists a radial ceramic or dielectric insulator. Its radial thermal resistance from $r_1 + L - w_{\text{is}}$ to $r_1 + L$ is

$$R_{\text{is}} = \frac{1}{k_{\text{is}} t\theta} \ln\left(\frac{r_1 + L}{r_1 + L - w_{\text{is}}}\right). \tag{32}$$

Combining this series resistance with the intrinsic leg conductance $K_{\text{total,TE}}$ yields an effective series resistance

$$R_{\text{eff,series}} = R_{\text{is}} + \frac{1}{K_{\text{total,TE}}}, \tag{33}$$

with corresponding conductance $K_{\text{eff,series}} = 1/R_{\text{eff,series}}$.

In addition, azimuthal leakage through an insulator strip of width w_{az} and thickness t gives a parallel conductance

$$K_{\text{az}} = k_{\text{az}} \frac{w_{\text{az}} t}{L}, \tag{34}$$

so that the net conductance of a TEC unit becomes

$$K_{\text{global}} = K_{\text{eff,series}} + K_{\text{az}}. \tag{35}$$

This K_{global} is used as the stage conductance K_i in the network equations.

VI. Two-Layer Radial Network and Nodal Equations

We discretize the radial direction into N active rings. For $i = 1, \ldots, N$ we define:

- $T_{\text{Si},i}$: chip temperature at ring i,
- $T_{c,i}$: TEC cold-side node temperature at interface between TEC stages $i-1$ and i.

An additional central node T_0 represents the lumped central cylinder where the chip and TEC are thermally merged.

A. Chip-Layer Nodes $T_{Si,i}$

For a generic chip node i ($1 \le i \le N$), applying steady-state energy conservation with lateral conduction to neighbours, vertical coupling to TEC, and local generation $Q_{\text{gen},i}$ gives

$$\frac{T_{\text{Si},i-1} - T_{\text{Si},i}}{R_{\text{lat},i-1}} + \frac{T_{\text{Si},i+1} - T_{\text{Si},i}}{R_{\text{lat},i}} - \frac{T_{\text{Si},i} - T_{c,i}}{R_{v,i}} + Q_{\text{gen},i} = 0. \tag{36}$$

Rearranging Eq. (36) into the standard linear form yields

$$\left(\frac{1}{R_{\text{lat},i-1}}\right) T_{\text{Si},i-1} - \left(\frac{1}{R_{\text{lat},i-1}} + \frac{1}{R_{\text{lat},i}} + \frac{1}{R_{v,i}}\right) T_{\text{Si},i} + \left(\frac{1}{R_{\text{lat},i}}\right) T_{\text{Si},i+1} + \left(\frac{1}{R_{v,i}}\right) T_{c,i} = -Q_{\text{gen},i}. \tag{37}$$

At the outermost chip ring $i = N$, an additional convective term couples the silicon to cooling water at temperature T_{w} through resistance R_{conv}, modifying the diagonal coefficient and right-hand side accordingly:

$$A_{\text{Si}}(N,N) \leftarrow A_{\text{Si}}(N,N) - \frac{1}{R_{\text{conv}}}, \tag{38}$$

$$B_{\text{Si}}(N) \leftarrow B_{\text{Si}}(N) - \frac{T_{\text{w}}}{R_{\text{conv}}}. \tag{39}$$

B. TEC-Layer Nodes $T_{c,i}$

The TEC node $T_{c,i}$ represents the thermal mass at the junction between radial stages $i-1$ and i. It receives vertical heat from the chip, stage-to-stage pumped heat from $i-1$, and rejects heat to stage i.

The vertical heat input from the chip is

$$Q_{\text{vert},i} = \frac{T_{\text{Si},i} - T_{c,i}}{R_{v,i}}. \tag{40}$$

Using the element-level expressions, the hot-side heat from stage $i-1$ and cold-side heat into stage i are

$$Q_{h,i-1} = S_{i-1} I_{i-1} T_{c,i} + \tfrac{1}{2} I_{i-1}^2 R_{e,i-1} - K_{i-1}(T_{c,i} - T_{c,i-1}), \tag{41}$$

$$Q_{c,i} = S_i I_i T_{c,i} - \tfrac{1}{2} I_i^2 R_{e,i} + K_i (T_{c,i+1} - T_{c,i}). \tag{42}$$

Imposing energy balance at node i,

$$Q_{\text{vert},i} + Q_{h,i-1} - Q_{c,i} = 0, \tag{43}$$

and collecting coefficients of $T_{c,i-1}$, $T_{c,i}$, $T_{c,i+1}$ and $T_{\text{Si},i}$ yields

$$(S_{i-1} I_{i-1} + K_{i-1})\, T_{c,i-1} - \left(\frac{1}{R_{v,i}} + K_{i-1} - S_{i-1} I_{i-1} + S_i I_i + K_i\right) T_{c,i} + K_i T_{c,i+1} + \left(\frac{1}{R_{v,i}}\right) T_{\text{Si},i} = -\frac{1}{2} I_{i-1}^2 R_{e,i-1} - \frac{1}{2} I_i^2 R_{e,i}. \tag{44}$$

At the outermost TEC node $i = N$, the final stage rejects heat to the water boundary, which is imposed by eliminating $T_{c,N+1}$ in favour of T_{w} using $T_{c,N+1} = T_{\text{w}}$ in Eq. (42), thereby modifying the diagonal of A_{TEC} and the corresponding entry in B_{TEC} by a term $-K_N T_{\text{w}}$.

C. Central Node T_0 with Volumetric Generation

The central node T_0 represents the common temperature of the merged chip and TEC region within radius R_{cyl}. Heat generated in this cylinder flows radially to the first silicon ring and to the first TEC node through effective resistances $R_{\text{Si},0\to1}$ and $R_{\text{TEC},0\to1}$, respectively. The nodal equation is

$$Q_{\text{gen},0} = \frac{T_0 - T_{\text{Si},1}}{R_{\text{Si},0\to1}} + \frac{T_0 - T_{c,1}}{R_{\text{TEC},0\to1}}, \tag{45}$$

or equivalently (multiplying by -1 to match the negative-diagonal convention of the other blocks),

$$-\left(\frac{1}{R_{\text{Si},0\to1}} + \frac{1}{R_{\text{TEC},0\to1}}\right) T_0 + \frac{1}{R_{\text{Si},0\to1}} T_{\text{Si},1} + \frac{1}{R_{\text{TEC},0\to1}} T_{c,1} = -Q_{\text{gen},0}. \tag{46}$$

For the silicon side, $R_{\text{Si},0\to1}$ is identified with the internal resistance of a wedge with volumetric generation, Eq. (25). For the TEC side, adding the central radial insulator layer of width w_{is} and conductivity k_{is} to the internal cylinder resistance gives

$$R_{\text{TEC},0\to1} = \frac{1}{t\theta}\left[\frac{1}{2k_{\text{Si}}} + \frac{1}{k_{\text{is}}} \ln\left(\frac{R_{\text{cyl}}}{R_{\text{cyl}} + w_{\text{is}}}\right)\right]. \tag{47}$$

Including T_0 increases the dimension of the global system by one, but preserves sparsity since it connects only to $T_{\text{Si},1}$ and $T_{c,1}$.

VII. Global Block-Matrix Formulation

Block Notation

Collecting all unknowns into a single vector

$$\mathbf{x} = \begin{bmatrix} T_0 & T_{\mathrm{Si},1} & \cdots & T_{\mathrm{Si},N} & T_{c,1} & \cdots & T_{c,N} \end{bmatrix}^{\mathsf{T}}, \quad (48)$$

the linear system can be expressed compactly as

$$\mathbf{M}\,\mathbf{x} = \mathbf{b}. \quad (49)$$

The matrix $\mathbf{M}$ has the block structure

$$\mathbf{M} = \begin{bmatrix} M_{00} & \mathbf{m}_{0,\mathrm{Si}}^{\mathsf{T}} & \mathbf{m}_{0,\mathrm{TEC}}^{\mathsf{T}} \\ \mathbf{m}_{0,\mathrm{Si}} & \mathbf{A}_{\mathrm{Si}} & \mathbf{A}_{\mathrm{Coup}} \\ \mathbf{m}_{0,\mathrm{TEC}} & \mathbf{A}_{\mathrm{Coup}} & \mathbf{A}_{\mathrm{TEC}} \end{bmatrix}, \quad (50)$$

where

- $M_{00} = -\left(\frac{1}{R_{\mathrm{Si},0\to1}} + \frac{1}{R_{\mathrm{TEC},0\to1}}\right)$,
- $\mathbf{m}_{0,\mathrm{Si}}$ has a single non-zero entry $+1/R_{\mathrm{Si},0\to1}$ in position corresponding to $T_{\mathrm{Si},1}$,
- $\mathbf{m}_{0,\mathrm{TEC}}$ has a single non-zero entry $+1/R_{\mathrm{TEC},0\to1}$ in position corresponding to $T_{c,1}$,
- $\mathbf{A}_{\mathrm{Si}}$ is tridiagonal with entries given by Eq. (37) plus boundary modifications in Eq. (39),
- $\mathbf{A}_{\mathrm{TEC}}$ is tridiagonal with entries given by Eq. (44) and the outer boundary correction described below Eq. (44),
- $\mathbf{A}_{\mathrm{Coup}}$ is diagonal with entries $1/R_{v,i}$.

Expanded Block Form

For clarity, the structure in Eq. (50) can be written in expanded form. Because this matrix is wide, we render it in single-column mode: where the non-zero entries of $\mathbf{A}_{\mathrm{Si}}$, $\mathbf{A}_{\mathrm{TEC}}$ and $\mathbf{A}_{\mathrm{Coup}}$ are given explicitly by Eqs. (37), (44) and the definition of $R_{v,i}$, respectively.

The right-hand side vector collects heat sources and boundary contributions as

$$\mathbf{b} = \begin{bmatrix} -Q_{\mathrm{gen},0} & -Q_{\mathrm{gen},1} & \cdots & -Q_{\mathrm{gen},N} & b_{\mathrm{TEC},1} & \cdots & b_{\mathrm{TEC},N} \end{bmatrix}^{\mathsf{T}}, \quad (51)$$

where

$$b_{\mathrm{TEC},i} = -\tfrac{1}{2} I_{i-1}^2 R_{e,i-1} - \tfrac{1}{2} I_i^2 R_{e,i} + b_{\mathrm{bc},i}, \quad (52)$$

and $b_{\mathrm{bc},i}$ collects contributions from fixed-temperature boundaries (e.g., $-K_N T_{\mathrm{w}}$ at $i = N$).

For completeness, the expanded forms of $\mathbf{x}$ and $\mathbf{b}$ are

$$\mathbf{x} = \begin{bmatrix} T_0 & T_{\mathrm{Si},1} & T_{\mathrm{Si},2} & \dots & T_{\mathrm{Si},N} & T_{c,1} & T_{c,2} & \dots & T_{c,N} \end{bmatrix}^{\mathsf{T}}, \quad (53)$$

and

$$\mathbf{b} = \begin{bmatrix} -Q_{\mathrm{gen},0} & -Q_{\mathrm{gen},1} & -Q_{\mathrm{gen},2} & \dots & -Q_{\mathrm{gen},N} & b_{\mathrm{TEC},1} & b_{\mathrm{TEC},2} & \dots & b_{\mathrm{TEC},N} \end{bmatrix}^{\mathsf{T}}. \quad (54)$$

The assembled matrix is sparse, tridiagonal within each block, and slightly asymmetric due to the convective Peltier terms $S_i I_i$. It can be solved efficiently using standard sparse linear solvers, and differentiable with respect to geometric and operating parameters for gradient-based optimization.

Boundary Conditions and Wedge Scaling

Centre ($r = 0$ to R_{cyl}): The internal cylinder is represented by node T_0 and Eq. (46). All chip-layer and TEC-layer temperatures within this radius are assumed equal to T_0, so no additional degrees of freedom are introduced in this region.

Outer radius ($r = r_N$): At the chip outer radius, heat is rejected to a coolant at temperature T_{w} through R_{conv}, implemented via Eq. (39). On the TEC side, the last stage rejects heat directly to T_{w} by substituting $T_{c,N+1} = T_{\mathrm{w}}$ into Eq. (42), which modifies the last row of $\mathbf{A}_{\mathrm{TEC}}$ and $\mathbf{b}$.

Representative wedge: Rather than solving the full 2π annulus, we model a single wedge of angle $\theta = 2\pi/N_\theta$. All radial resistances and cross-sectional areas are derived for this wedge, and chip-side heat generation is scaled either from a global flux q''_{flux} (Eqs. (23)–(24)) or from a total power Q_{tot} divided by the wedge count N_θ. Electrical currents I_i are likewise interpreted as the current per wedge or per leg pair.

TSV zones: Regions without TSVs are enforced by assigning a very large vertical resistance $R_{v,i}$ (e.g., $R_{v,i} \to 10^9$ K/W), which effectively decouples $T_{\mathrm{Si},i}$ from $T_{c,i}$ and leaves heat to flow purely laterally in the silicon layer in those rings.

VIII. Conclusion

We have developed a consistent mathematical model for a radial multistage TEC coupled to a 3D-IC hotspot through a two-layer thermal network. Starting from element-level TEC physics, we derived equivalent resistances for radial conduction in the silicon die, TSV bundles and interconnects, and TEC legs including ceramic and azimuthal leakage paths. These ingredients were assembled into a block-structured linear system augmented with a central node that explicitly represents volumetric heat generation in the innermost cylinder.

This formulation is directly compatible with finite-difference style discretization and can be implemented in MATLAB or Python using sparse matrices. Future work will integrate electrical constraints, current-sharing strategies among stages, and geometric optimization of TEC leg dimensions and TSV layouts to minimise hotspot temperature under power and footprint constraints.

$$
\mathbf{M} = \begin{bmatrix}
M_{00} & \dfrac{1}{R_{\mathrm{Si},0\to1}} & 0 & \cdots & 0 & \dfrac{1}{R_{\mathrm{TEC},0\to1}} & 0 & \cdots & 0 \\
\dfrac{1}{R_{\mathrm{Si},0\to1}} & (\mathbf{A}_{\mathrm{Si}})_{11} & (\mathbf{A}_{\mathrm{Si}})_{12} & \cdots & 0 & (\mathbf{A}_{\mathrm{Coup}})_{11} & 0 & \cdots & 0 \\
0 & (\mathbf{A}_{\mathrm{Si}})_{21} & (\mathbf{A}_{\mathrm{Si}})_{22} & \cdots & 0 & 0 & (\mathbf{A}_{\mathrm{Coup}})_{22} & \cdots & 0 \\
\vdots & \vdots & \vdots & \ddots & \vdots & \vdots & \vdots & \ddots & \vdots \\
0 & 0 & 0 & \cdots & (\mathbf{A}_{\mathrm{Si}})_{NN} & 0 & 0 & \cdots & (\mathbf{A}_{\mathrm{Coup}})_{NN} \\
\dfrac{1}{R_{\mathrm{TEC},0\to1}} & (\mathbf{A}_{\mathrm{Coup}})_{11} & 0 & \cdots & 0 & (\mathbf{A}_{\mathrm{TEC}})_{11} & (\mathbf{A}_{\mathrm{TEC}})_{12} & \cdots & 0 \\
0 & 0 & (\mathbf{A}_{\mathrm{Coup}})_{22} & \cdots & 0 & (\mathbf{A}_{\mathrm{TEC}})_{21} & (\mathbf{A}_{\mathrm{TEC}})_{22} & \cdots & 0 \\
\vdots & \vdots & \vdots & \ddots & \vdots & \vdots & \vdots & \ddots & \vdots \\
0 & 0 & 0 & \cdots & (\mathbf{A}_{\mathrm{Coup}})_{NN} & 0 & 0 & \cdots & (\mathbf{A}_{\mathrm{TEC}})_{NN}
\end{bmatrix}
$$

Fig. 2. Expanded block structure of the coupled silicon–TEC system matrix $\mathbf{M}$.