Appendix A

1 Introduction

The radial TEC cooler can be modeled using a thermal network, reducing the system to whats known as a **Compact Thermal Model (CTM)**. This reduces the problem to a linear system and it can be used for preliminary design decisions and optimization. The thermal network is configured as a single stage occupies a cocentric ring around the chip, with multiple stages stacked radially outward for increased performance. This asymmetric feature can be exploited to model only a single as a one dimensional radial network. However, the presence of the chip layer, which emulates the heat flux from the chip, converts the system into a two dimensional network.

Nomenclature

Symbols

θ	Wedge Angle [rad]
r	radius [m]
L	Length [m]
W	width [m]
N	No. of Stages [$\mathbb{Z}^+$]
t	thickness [m]
f	Fractions use for dimensional reduction [$-$]
Q	Heat Load [W]
κ	Thermal Conductivity [W/(m K)]
ρ	Electrical Resistivity [Ωm]
T	Temperature [K]
A	Cross Sectional Area [m^2]
κ	Thermal Conductivity [W/(m K)]
ρ	Electrical Resistivity [Ωm]
S	Seebeck Coefficient [V/K]

Subscripts and Superscripts

chip	Chip Layer
base	Base of radial TEC array
ins	Insulator Layer
TEC	TEC Layer
cyl	Cylinder
i	i^{th} stage
in	Inner
out	Outer
is	Radial Insulator
az	Azimuthal Insulator
p	p type leg
n	n type leg
ic	Interconnection
oc	Outerconnection
e	Electrical
t	Thermal
ins	Insulator Layer
ve	Vertical

2 Geometry Parametrization

To allow a robust optimization framework, each and all the geometric elements of the radial TEC array must be parametrized. The radius of the TEC array is defined by r_{base} such that it covers the entire rectangular chip area. The chip is assumed to be square with side length L_{chip}, and width W_{chip}. Therefore, the base radius is defined as:

$$r_{\text{base}} = \frac{1}{2}\sqrt{L_{\text{chip}}^2 + W_{\text{chip}}^2} \tag{1}$$

2.1 Wedge

Wedges are the fundamental repeating unit of the radial TEC structure. Each wedge contains a single element for each stage arranged radially. The innermost TEC element is belongs the to first stage and the outermost element belongs to the last stage. The wedge is mainly parametrized by the wedge angle θ and the base radius r_{base}, as shown in fig. 1. The wedge angle is determined by the number of wedges N in the full 360 degree array, such that $\theta = 2\pi/N$. The base radius is defined as the radial distance from the center of the chip to the inner edge of the first stage TEC element.

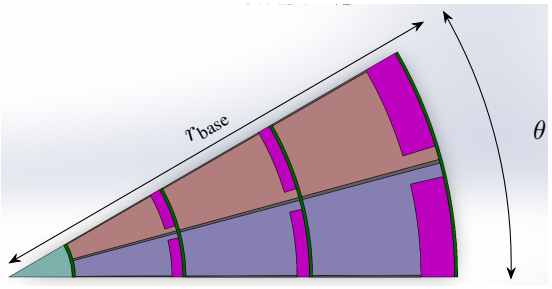


Figure 1: Top view of a single wedge showing the base radius r_{base} and wedge angle θ.

2.2 Layer System

Radial TEC array consists of 3 main layers stacked vertically, namely the chip layer, insulator layer, and the radial TEC array layer. The chip layer is modeled as a heat source with a constant heat flux boundary condition. The insulator layer provides electrical isolation between the chip and the TEC array. The radial TEC array layer contains the TEC elements and radial insulators arranged in a wedge pattern. Each layer is defined mainly by its thickness, denoted as t_{chip}, t_{ins}, and t_{TEC} respectively.

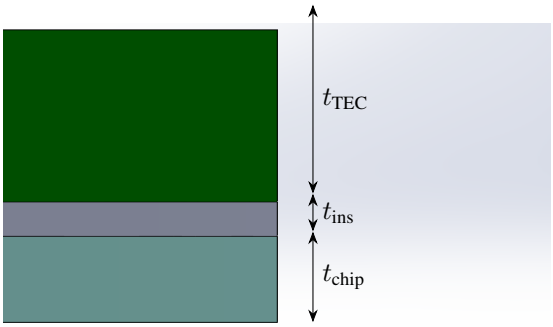


Figure 2: Side view of the layer system.

2.3 Central Cylinder

In the center of the radial TEC array lies a cylindrical region that represents the area not covered by the TEC elements. This central cylinder is defined by its radius r_{cyl}. This cylinder spans all 3 layers of the system, from the chip layer to the radial TEC array layer.

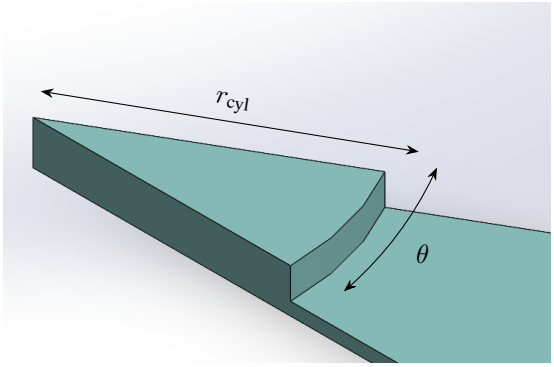


Figure 3: Isometric view of the central cylinder

2.4 TEC Element

TEC elements are sandwiched between radial insulators from both radial direction and azimuthal direction. Each TEC element is defined by its inner and outer radius, r_{in} and r_{out} respectively, as well as its thickness t_{TEC}.

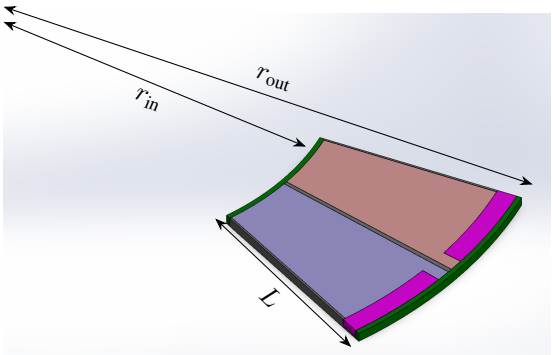


Figure 4: A Single TEC element

2.5 Thermoelectric Legs

The wedge is divided into two separate regions in the azimuthal direction, one consisting of p type semiconductor material and other consisting of n type semiconductor material. They are shown in fig. 4 in light violet and light red colours respectively. Each leg in the stage can have arbitary lengths as long as they all add up to the final length. However, this increases the number of independant variables in the optimization problem. Therefore, we can perform a dimensional reduction by assuming that lengths of stages vary by some ratio. So let's define leng length ratio f_L as,

$$f_L = \frac{L_{i+1}}{L_i} \tag{2}$$

where L_i is the length of the TEC legs in stage i. Therefore, the length of each stage can be defined as:

$$L_i = L_1 \cdot f_L^{(i-1)} \tag{3}$$

where L_1 is the length of the TEC legs in the first stage. Since the radial insulator isn't included in the length, we can get a relationship between stage lengths and radius of the TEC array as:

$$\begin{aligned} r_{\text{base}} &= r_{\text{cyl}} + \sum_{i=1}^{N} L_i + (N+1) \cdot W_{\text{is}} \\ &= r_{\text{cyl}} + \sum_{i=1}^{N} L_1 \cdot f_L^{(i-1)} + (N+1) \cdot W_{\text{is}} \\ &= r_{\text{cyl}} + L_1 \cdot \frac{1 - f_L^N}{1 - f_L} + (N+1) \cdot W_{\text{is}} \end{aligned}$$

Solving for L_1 gives:

$$L_1 = \frac{(r_{\text{base}} - r_{\text{cyl}} - (N+1) \cdot W_{\text{is}}) \cdot (1 - f_L)}{1 - f_L^N} \tag{4}$$

This means that the lengths of all stages can be defined using only two independant variables, f_L and r_{cyl}.

2.6 Radial Insulator

Radial insulators separate each TEC element in the radial direction. Each radial insulator is defined by its width W_{is} which is constant throughout the entire radial TEC array. It has the same thickness as the TEC elements, t_{TEC}. Its indicated in dark green colour in figs. 4 and 5

2.7 Azimuthal Insulator

Azimuthal insulators separate the p-type and n-type legs in each TEC element, as well as between adjacent wedges. Each azimuthal insulator is defined by its with along the arc in the azimuthal direction, denoted as W_{az}. It also has the same thickness as the TEC elements, t_{TEC}. It is indicated in dark gray colour in figs. 4 and 5.

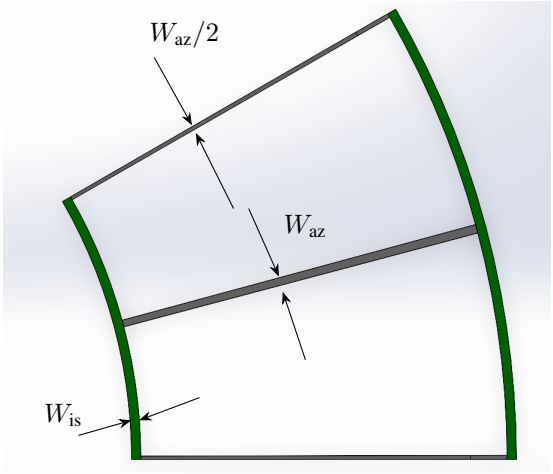


Figure 5: Radial and Azimuthal Insulators Top View

2.8 Interconnector

Interconnector provides electrical contact between TEC elements within each stage. Its located near the cold side of the TE unit and connects the n-type leg of a wedge to the p-type leg of the same wedge.

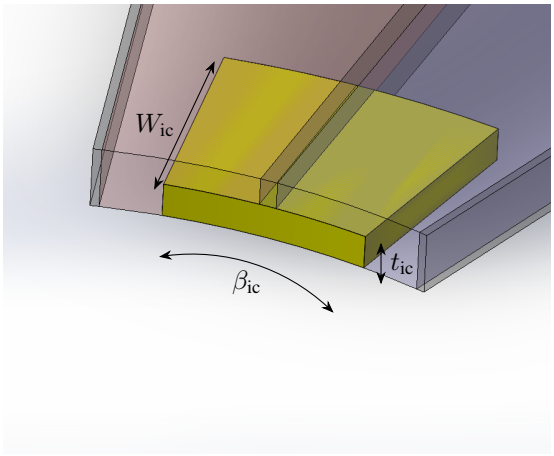


Figure 6: Isometric view of Interconnector

Interconnector is parametrized by its width W_{ic}, thickness t_{ic}, and angle β_{ic} it subtends at the center of the wedge, as shown in fig. 6. For the optmization purposes, all the interconnector dimensions are defined as fractions of the TEC element dimensions. Therefore, we can define:

$$W_{\text{ic}} = f_{\text{ic,W}} \cdot L_{\text{TEC}} \quad ; \quad f_{\text{ic,W}} \in (0,1) \tag{5}$$

$$t_{\text{ic}} = f_{\text{ic,t}} \cdot t_{\text{TEC}} \quad ; \quad f_{\text{ic,t}} \in (0,1) \tag{6}$$

$$\beta_{\text{ic}} = f_{\text{ic},\beta} \cdot \theta \quad ; \quad f_{\text{ic},\beta} \in (0,1) \tag{7}$$

The thickness is measured from the bottom of the TEC element to the top of the TEC array surface. Therefore it's not visible from the top view when $t_{\text{ic}} < t_{\text{TEC}}$.

2.9 Outerconnector

Outerconnector refeers to the electrical contact between TEC elements of adjacent wedges. Its located near the hot side of the TEC unit and connects the p-type leg of a wedge to the n-type leg of the adjacent wedge.

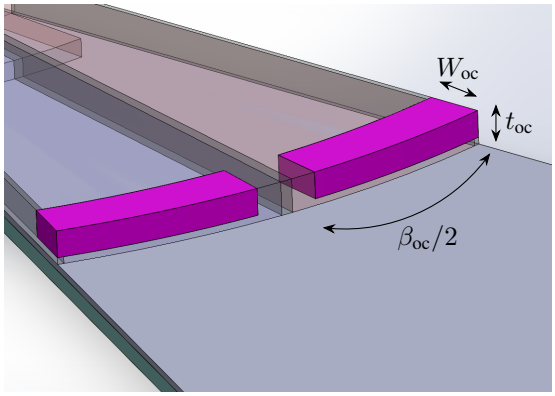


Figure 7: Isometric view of Outerconnector

Outerconnector is parametrized similarly to the interconnector, with width W_{oc}, thickness t_{oc}, and angle β_{oc} it subtends at the center of the wedge, as shown in fig. 7. For the optmization purposes, all the outerconnector dimensions are defined as fractions of the TEC element dimensions. Therefore, we can define:

$$W_{\text{oc}} = f_{\text{oc,W}} \cdot L_{\text{TEC}} \quad ; \quad f_{\text{oc,W}} \in (0,1) \tag{8}$$

$$t_{\text{oc}} = f_{\text{oc,t}} \cdot t_{\text{TEC}} \quad ; \quad f_{\text{oc,t}} \in (0,1) \tag{9}$$

$$\beta_{\text{oc}} = f_{\text{oc},\beta} \cdot \theta \quad ; \quad f_{\text{oc},\beta} \in (0,1) \tag{10}$$

The thickness is measured from the top of the TEC element to the bottom of the TEC array surface, in contrast to the interconnector.

3 Resistance Calculation

To build the thermal network, the thermal resistances of each component must be calculated. Apart from that, the electrical resistances of the TEC elements must also be calculated to account for Joule heating effects.

3.1 Resistor Arrangement

3.1.1 TEC Layer

The calculation of thermal resistances depends on the direction of heat flow and the arrangement of components in that direction. In the radial TEC array, heat flows radially outward from the center of the chip to the outer edge of the TEC array.

Since there are many components, we need to pick a point to be used as a node in each TEC element. For convenience, we pick the junction between radial insulator, and central azimuthal insulator as the node point. This means that all components between two such points will be absorbed into a single thermal resistance. This resistance is used mainly to calculate the back conduction. The arrangement of resistors between two such nodes is shown in fig. 8.

3.1.2 Chip Layer

Nodes in the chip layer are designated to be directly below the nodes in the TEC layer in order to ease the vertical resistance calculation. The arrangement of resistors between two such nodes in the chip layer is shown in fig. 9. Two main resistors are shown here: vertical resistance (R_{ve}) which represents the heat transfer between chip layer and TEC layer, and the horizontal resistance (R_{chip}) which represents the heat transfer in between the chip nodes.

Since there is a heat generation term for the chip layer nodes, and this heat generation is characterized by a heat flux value, an area is require to calculate the generated heat per node. Apart from that, an area is also required to calculate the vertical resistance values. For both of these area values, it was decided to use the complete area of the corresponding TEC element. This decision was based on the boundaries.

Realistically, the annular segment surrounding the chip node should be used to calculate the area, so that each chip node gets half of the area from connecting TEC elements. However, this will result in the edge node not accounting for outermost area fraction. Apart from that, since the central node is modeled as a cylinder, its convenient to use the area of the corresponding circle to calculate the heat generation for the node 0. Similar issues exists when calculating the vertical resistance as well. Therefore, in the chosen method, resistance values and heat generation and resistance values corresponding to i^{th} node and resistors will be calculated using the area covered by the i^{th} TEC element.

This wrong area calculation will likely result in sightly off Temperature values for TEC and chip nodes, but the overall result of central Temperature and other metrics such as COP would not be affected as much. Therefore this compromise is tolerable because the main use of the model is to be used in the optimization process.

3.2 Thermal Resistances

The thermal resistance of each component will be calculated based on geometry and material properties. The general formula for thermal resistance is given by:

$$R_{\text{t}} = \frac{L}{\kappa \cdot A} \tag{11}$$

For a variables cross sectional area, the thermal resistance can be calculated using:

$$R_{\text{t}} = \int_{x=0}^{L} \frac{dx}{\kappa \cdot A(x)} \tag{12}$$

3.2.1 Thermoelectric Legs

Due to the presence of multiple components within the area of a Thermoelectric leg, the Calculation must be carried out accounting for the area reduction caused by those components. They include, the azimuthal insulators, interconnector, and outerconnector. Since the heat is carried in the radial direction, the cross sectional area is given by:

$$A(r) = S(r) \cdot t_{\text{TEC}} \tag{13}$$

Since we consider only one thermoelectric leg, the associated azimuthal angle is $\theta/2$ and since $S(r) = r \cdot \frac{\theta}{2}$,

$$A(r) = r \cdot \frac{\theta}{2} \cdot t_{\text{TEC}} \tag{14}$$

When going radially outward starting from r_{in} to r_{out} based on the fraction of area belongs to the TE material, we can divide TE leg into 3 regions.

Region with interconnect occupying a fraction of cross section area

This region spans from $r = r_{\text{in}}$ to $r = (r_{\text{in}} + W_{\text{ic}})$ In this region, the cross section area becomes,

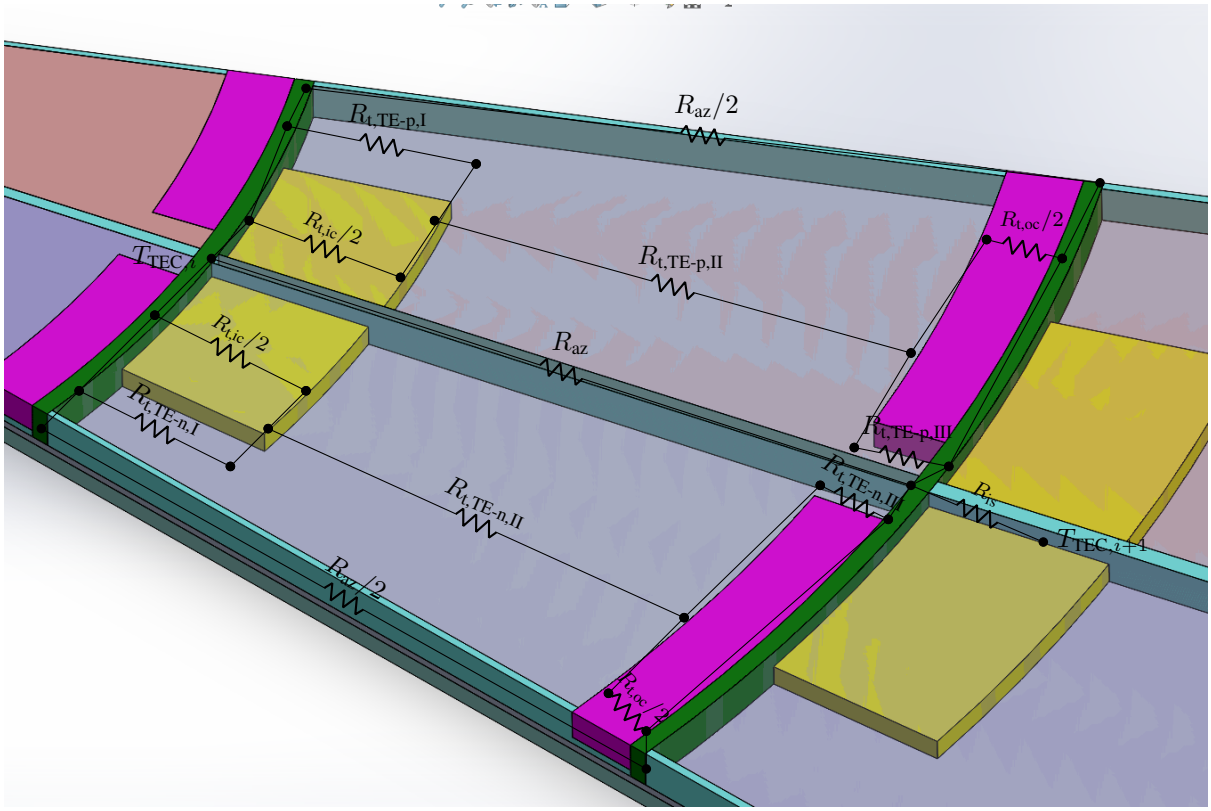
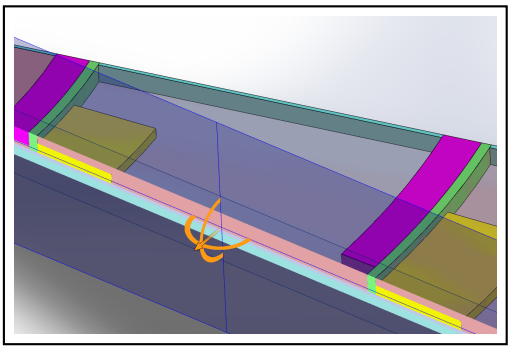


Figure 8: Thermal resistance network between two adjacent interconnector nodes showing parallel paths through p-type leg, n-type leg, and radial insulator.



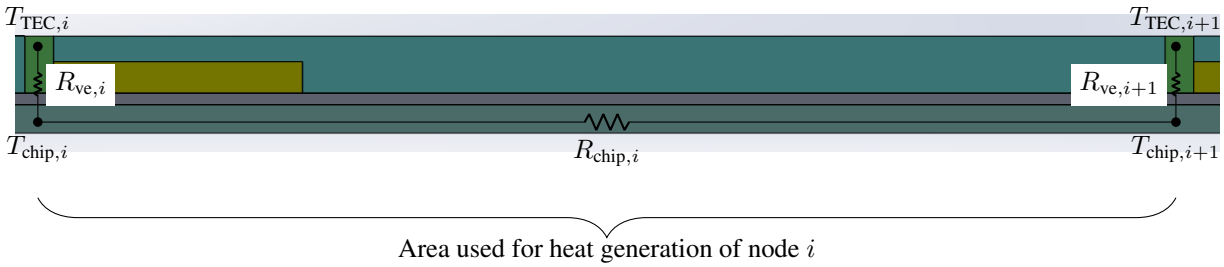


Figure 9: Resistor diagram in the chip layer between 2 nodes.

$$A(r) = r \cdot \frac{\theta}{2} \cdot t_{\text{TEC}} - r \cdot \frac{\beta_{\text{ic}}}{2} \cdot t_{\text{ic}} = \frac{r}{2}(\theta \cdot t_{\text{TEC}} - \beta_{\text{ic}} \cdot t_{\text{ic}}) \tag{15}$$

From this, we need to subtract the cross sectional area occupied by the azimuthal insulator. This area is equal to the arc length of the azimuthal insulator at radius r multiplied by the thickness of the TEC layer. Since the azimuthal insulator width is W_{az} is constant for all r values, the area occupied by the azimuthal insulator is given by:

$$A_{\text{az}} = W_{\text{az}} \cdot t_{\text{TEC}} \tag{16}$$

Here we consider single TEC leg, so the azimuthal insulator occupies half the width, two times and it adds upto W_{az}. Therefore, the effective cross sectional area in this region becomes:

$$A(r) = \frac{r}{2}(\theta \cdot t_{\text{TEC}} - \beta_{\text{ic}} \cdot t_{\text{ic}}) - W_{\text{az}} \cdot t_{\text{TEC}} = \frac{1}{2}\left[r(\theta \cdot t_{\text{TEC}} - \beta_{\text{ic}} \cdot t_{\text{ic}}) - 2W_{\text{az}} \cdot t_{\text{TEC}}\right]$$

Since r is the variable of integration, let's write in $ax+b$ form.

$$A(r) = \frac{\theta \cdot t_{\text{TEC}} - \beta_{\text{ic}} \cdot t_{\text{ic}}}{2} \cdot r - W_{\text{az}} \cdot t_{\text{TEC}} \tag{17}$$

Then the integration in the eq. (12) becomes,

$$R_{\text{t,TE,I}} = \int_{r_{\text{in}}}^{r_{\text{in}}+W_{\text{ic}}} \frac{dr}{\kappa_{\text{TE}}\left(\frac{\theta \cdot t_{\text{TEC}} - \beta_{\text{ic}} \cdot t_{\text{ic}}}{2} \cdot r - W_{\text{az}} \cdot t_{\text{TEC}}\right)}$$

Since a solution to a integral in the form of $\int_{x_1}^{x_2} \frac{dx}{ax+b}$ is given by,

$$\int_{x_1}^{x_2} \frac{dx}{ax+b} = \frac{1}{a}\int_{x_1}^{x_2} \frac{d(ax+b)}{ax+b} = \frac{1}{a}\left[\ln|ax+b|\right]_{x_1}^{x_2} = \frac{1}{a}\left[\ln\left|\frac{ax_2+b}{ax_1+b}\right|\right] \tag{18}$$

Applying the definite integral limits gives:

$$R_{\text{t,TE,I}} = \frac{2}{\kappa_{\text{TE}}(\theta \cdot t_{\text{TEC}} - \beta_{\text{ic}} \cdot t_{\text{ic}})} \cdot \ln\left|\frac{(\theta \cdot t_{\text{TEC}} - \beta_{\text{ic}} \cdot t_{\text{ic}})(r_{\text{in}} + W_{\text{ic}}) - 2W_{\text{az}} \cdot t_{\text{TEC}}}{(\theta \cdot t_{\text{TEC}} - \beta_{\text{ic}} \cdot t_{\text{ic}})r_{\text{in}} - 2W_{\text{az}} \cdot t_{\text{TEC}}}\right| \tag{19}$$

Region without any other geometry sharing a fraction of cross section area

This region spans from $r = (r_{\text{in}} + W_{\text{ic}})$ to $r = (r_{\text{out}} - W_{\text{oc}})$. In this region, the cross section area remains the same as eq. (14).

$$A(r) = r \cdot \frac{\theta}{2} \cdot t_{\text{TEC}}$$

When the correction for azimuthal insulator area is applied, the effective cross sectional area becomes:

$$A(r) = r \cdot \frac{\theta}{2} \cdot t_{\text{TEC}} - W_{\text{az}} \cdot t_{\text{TEC}}$$

Rearranging into $ax + b$ form gives:

$$A(r) = \frac{1}{2}\theta \cdot t_{\text{TEC}} \cdot r - W_{\text{az}} \cdot t_{\text{TEC}} \tag{20}$$

Then the integration in the eq. (12) becomes,

$$R_{\text{t,TE,II}} = \int_{r_{\text{in}}+W_{\text{ic}}}^{r_{\text{out}}-W_{\text{oc}}} \frac{dr}{\kappa_{\text{TE}}\left(\frac{1}{2}\theta \cdot t_{\text{TEC}} \cdot r - W_{\text{az}} \cdot t_{\text{TEC}}\right)}$$

According to eq. (18), applying the definite integral limits gives:

$$R_{\text{t,TE,II}} = \frac{2}{\kappa_{\text{TE}}\theta \cdot t_{\text{TEC}}} \cdot \ln\left|\frac{\theta \cdot t_{\text{TEC}}(r_{\text{out}} - W_{\text{oc}}) - 2W_{\text{az}} \cdot t_{\text{TEC}}}{\theta \cdot t_{\text{TEC}}(r_{\text{in}} + W_{\text{ic}}) - 2W_{\text{az}} \cdot t_{\text{TEC}}}\right| \tag{21}$$

Region with outerconnect sharing a fraction of cross section area

This region spans from $r = (r_{\text{out}} - W_{\text{oc}})$ to $r = r_{\text{out}}$. In this region, the cross section area becomes,

$$A(r) = r \cdot \frac{\theta}{2} \cdot t_{\text{TEC}} - r \cdot \frac{\beta_{\text{oc}}}{2} \cdot t_{\text{oc}} = \frac{r}{2}(\theta \cdot t_{\text{TEC}} - \beta_{\text{oc}} \cdot t_{\text{oc}})$$

After subtracting the azimuthal insulator area, the effective cross sectional area in this region becomes:

$$A(r) = \frac{r}{2}(\theta \cdot t_{\text{TEC}} - \beta_{\text{oc}} \cdot t_{\text{oc}}) - W_{\text{az}} \cdot t_{\text{TEC}} = \frac{1}{2}\left[r(\theta \cdot t_{\text{TEC}} - \beta_{\text{oc}} \cdot t_{\text{oc}}) - 2W_{\text{az}} \cdot t_{\text{TEC}}\right]$$

Rearranging into $ax + b$ form gives:

$$A(r) = \frac{\theta \cdot t_{\text{TEC}} - \beta_{\text{oc}} \cdot t_{\text{oc}}}{2} \cdot r - W_{\text{az}} \cdot t_{\text{TEC}} \tag{22}$$

Then the integration in the eq. (12) becomes,

$$R_{\text{t,TE,III}} = \int_{r_{\text{out}}-W_{\text{oc}}}^{r_{\text{out}}} \frac{dr}{\kappa_{\text{TE}}\left(\frac{\theta\cdot t_{\text{TEC}}-\beta_{\text{oc}}\cdot t_{\text{oc}}}{2}\cdot r - W_{\text{az}}\cdot t_{\text{TEC}}\right)}$$

According to eq. (18), applying the definite integral limits gives:

$$R_{\text{t,TE,III}} = \frac{2}{\kappa_{\text{TE}}(\theta\cdot t_{\text{TEC}} - \beta_{\text{oc}}\cdot t_{\text{oc}})}\cdot \ln\left|\frac{(\theta\cdot t_{\text{TEC}} - \beta_{\text{oc}}\cdot t_{\text{oc}})r_{\text{out}} - 2W_{\text{az}}\cdot t_{\text{TEC}}}{(\theta\cdot t_{\text{TEC}} - \beta_{\text{oc}}\cdot t_{\text{oc}})(r_{\text{out}}-W_{\text{oc}}) - 2W_{\text{az}}\cdot t_{\text{TEC}}}\right| \quad (23)$$

The same way we divided the TEC element into 3 regions in the radial direction, we can perform division based integrals for azimuthal and vertical directions as well.

However, this would create total of 27 regions for each TEC element, making the calculations cumbersome.

Therefore, we make the assumption that the heat flow is uniform across the entire cross sectional area of the TEC leg, and we apply area correction only in the radial direction. This simplification is valid as long as the azimuthal and vertical dimensions of the TEC leg are small compared to the radial dimension, Which is the case in our design.

3.2.2 Interconnect

The interconnect transfers heat in radial direction. Therefore, the thermal resistance of the interconnect can be calculated similarly to the thermoelectric leg, using the same cross sectional area calculations. The cross sectional area of the interconnect is given by:

$$\begin{aligned} A_{\text{ic}}(r) &= S(r)\cdot t_{\text{ic}} \\ &= r\cdot\beta_{\text{ic}}\cdot t_{\text{ic}} \end{aligned}$$

The eq. (12) becomes:

$$R_{\text{t,ic}} = \int_{r_{\text{in}}}^{r_{\text{in}}+W_{\text{ic}}} \frac{dr}{\kappa_{\text{TE}}\cdot r\cdot\beta_{\text{ic}}\cdot t_{\text{ic}}}$$

Evaluating the integral assuming constant thermal conductivity κ_{TE} gives:

$$R_{\text{t,ic}} = \frac{1}{\kappa_{\text{TE}}\cdot\beta_{\text{ic}}\cdot t_{\text{ic}}} ln\left(\frac{r_{\text{in}}+W_{\text{ic}}}{r_{\text{in}}}\right) \quad (24)$$

3.2.3 Outerconnect

The outerconnect transfers heat in radial direction. Therefore, the thermal resistance of the outerconnect can be calculated similarly to the interconnect. The only difference is that there are two outerconnects per TEC element, one on each side. However, since they are subtending only half the angle of the interconnect, their combined resistance is equal to that of a single interconnect. Therefore, the thermal resistance of the outerconnect for a single TEC element is given by:

$$R_{\text{t,oc}} = \frac{1}{\kappa_{\text{TE}}\cdot\beta_{\text{oc}}\cdot t_{\text{oc}}} ln\left(\frac{r_{\text{out}}}{r_{\text{out}}-W_{\text{oc}}}\right) \quad (25)$$

3.2.4 Radial Insulators

As per the resistor arrangement shown in fig. 8, the radial insulator after the current stage is the one that gets added currnt lumped resistor. Therefore, the integral limits are from $r = (r_{\text{out}})$ to $r = (r_{\text{out}} + W_{\text{is}}$. The cross sectional area of the radial insulator is given by:

$$\begin{aligned} A_{\text{is}}(r) &= S(r)\cdot t_{\text{TEC}} \\ &= r\cdot\theta\cdot t_{\text{TEC}} \end{aligned}$$

Then the eq. (12) becomes:

$$R_{\text{is}} = \int_{r_{\text{out}}}^{r_{\text{out}}+W_{\text{is}}} \frac{dr}{\kappa_{\text{is}}\cdot r\cdot\theta\cdot t_{\text{TEC}}}$$

Evaluating the integral assuming constant thermal conductivity κ_{is} gives:

$$R_{\text{is}} = \frac{1}{\kappa_{\text{is}}\cdot\theta\cdot t_{\text{TEC}}} ln\left(\frac{r_{\text{out}}+W_{\text{is}}}{r_{\text{out}}}\right) \quad (26)$$

3.2.5 Azimuthal Insulator

Since the azimuthal insulator is characterized by the constant by the constant arc length W_{az}, the thermal resistance can be calculated directly without integration. The cross sectional area of the azimuthal insulator is given by:

$$A_{\text{az}} = W_{\text{az}}\cdot t_{\text{TEC}}$$

Therefore, eq. (11) becomes:

$$R_{\text{az}} = \frac{L}{\kappa_{\text{az}}\cdot W_{\text{az}}\cdot t_{TEC}} \quad (27)$$

3.2.6 Vertical Resistance

Heat generated through the chip layer will be transferred vertically upward to the TEC layer through the insulator layer. While this insulator layer can be something like SOI which is weakly thermally conductive, the conductivity cannot be ignored because the thin layer would decrease the thermal resistance significantly. The are area heat travels through can be calculated using the area of the corresponding TEC element. Therefore, the cross sectional area for vertical resistance is given by:

$$A_{\text{TEC}} = \frac{\theta}{2}(r_{\text{out}}^2 - r_{\text{in}}^2) \tag{28}$$

Then eq. (11) becomes,

$$R_{\text{ve}} = \frac{2t_{\text{ins}}}{\kappa_{\text{ins}}\theta\left(r_{\text{out}}^2 - r_{\text{in}}^2\right)} \tag{29}$$

3.2.7 Chip Layer Resistance

Chip layer node to node thermal resistance can be calculated by performing the integration shown in eq. (12). Here the area is calculated for the whole span of the wedge, therefore $S(r) = r \cdot \theta$, and eq. (14) becomes,

$$A(r) = r \cdot \theta \cdot t_{\text{chip}}$$

Then the integral in eq. (12) becomes,

$$R_{\text{chip}} = \int_{r_{\text{in}}}^{r_{\text{out}}} \frac{dr}{\kappa_{\text{chip}} \cdot r \cdot \theta \cdot t_{\text{chip}}}$$

Evaluating the integral and applying the limits gives,

$$R_{\text{chip}} = \frac{1}{\kappa_{\text{chip}} \cdot \theta \cdot t_{\text{chip}}} ln\left(\frac{r_{\text{out}}}{r_{\text{in}}}\right) \tag{30}$$

3.2.8 Central Cylinder Resistance

In the resistor network, the central cylinder acts as a common node for both layers, denoted by **Node 0**. This is because it's a single block spanning all 3 layers as shown in fig. 3. Therefore, it is required to calculated the resistance between node 0 and node 1 of both TEC layer and the chip layer.

The standard solution for a cylinder with volumetric generation is $T_{\text{center}} - T_{\text{surf}} = \frac{Q}{4\pi kt}$. Adjusting for the wedge angle θ (where the full circle is 2π), the factor becomes 2θ. From this, the thermal resistance between node 0 and node 1 in the TEC layer can be derived as:

$$R_{\text{cyl}} = \frac{1}{2\theta\kappa t} \tag{31}$$

For the Chip Layer

For the chip layer, this can be directly used as the resistance between node 0 and node 1. Therefore, the thermal resistance between node 0 and node 1 in the chip layer becomes:

$$R_{\text{chip},0\to1} = \frac{1}{2\theta\kappa_{\text{chip}}t_{\text{chip}}} \tag{32}$$

For the TEC Layer

For the TEC layer, $t \to t_{\text{TEC}}$ and $\kappa \to \kappa_{\text{TEC}}$. However, between the central cylinder and the first node on the TEC layer, there is a radial insulator layer which wasn't accounted for during the TEC layer resistance calculation because its position is before the first node. Therefore, the radial insulator resistance must be added to the above resistance, which is given by eq. (26). Since the resistors are in series, the thermal resistance between node 0 and node 1 in the TEC layer becomes:

$$R_{\text{TEC},0\to1} = \frac{1}{2\theta\kappa_{\text{chip}}t_{\text{TEC}}} + R_{\text{is},0} \tag{33}$$

3.3 Lumping Resistors Together

Now we need to lump all the resistors between two adjacent interconnect nodes together.The resistor arrangement is shown in fig. 8 is shown in a simplified manner in fig. 10.

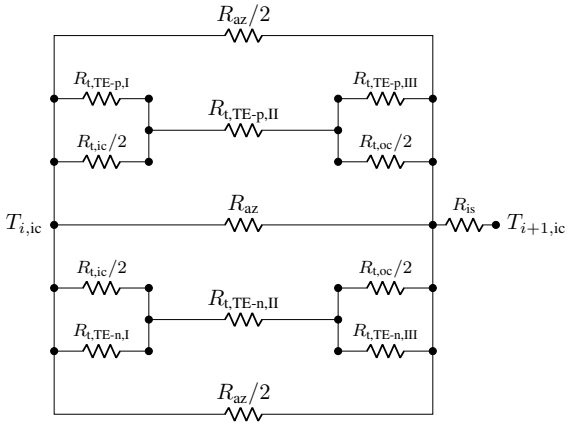


Figure 10: Resistor network between two adjacent interconnector nodes.

Now all the resistors can be lumped together to a single resistor. First, let's lump together the parallel resistors in the regions I and III together.

$$\frac{1}{R_{\text{t,TE-p,I,combined}}} = \frac{1}{R_{\text{t,TE-p,I}}} + \frac{1}{R_{\text{t,ic}}/2} \tag{34}$$

$$\frac{1}{R_{\text{t,TE-p,III,combined}}} = \frac{1}{R_{\text{t,TE-p,III}}} + \frac{1}{R_{\text{t,oc}}/2} \tag{35}$$

Similarly for n-TE side,

$$\frac{1}{R_{\text{t,TE-n,I,combined}}} = \frac{1}{R_{\text{t,TE-n,I}}} + \frac{1}{R_{\text{t,ic}}/2} \tag{36}$$

$$\frac{1}{R_{\text{t,TE-n,III,combined}}} = \frac{1}{R_{\text{t,TE-n,III}}} + \frac{1}{R_{\text{t,oc}}/2} \tag{37}$$

These combined resistors are in series with the region II resistors. Therefore, the total thermoelectric leg resistors for both p-type and n-type legs become:

$$\begin{aligned} R_{\text{t,TE-p,combined}} = {} & R_{\text{t,TE-p,I,combined}} + R_{\text{t,TE-p,II}} \\ & + R_{\text{t,TE-p,III,combined}} \end{aligned} \tag{38}$$

$$\begin{aligned} R_{\text{t,TE-n,combined}} = {} & R_{\text{t,TE-n,I,combined}} + R_{\text{t,TE-n,II}} \\ & + R_{\text{t,TE-n,III,combined}} \end{aligned} \tag{39}$$

These combined resistances are in parallel with the azimuthal resistances. Therefore,

$$\begin{aligned} \frac{1}{R_{\text{TE,combined}}} = {} & \frac{1}{R_{\text{az}}/2} + \frac{1}{R_{\text{t,TE-p,combined}}} \\ & + \frac{1}{R_{\text{az}}} + \frac{1}{R_{\text{t,TE-n,combined}}} + \frac{1}{R_{\text{az}}/2} \end{aligned} \tag{40}$$

Finally, the above resistor is in series with the radial insulator resistor, and the total lumped resistance between two adjacent interconnect nodes becomes,

$$R_{\text{TEC}} = R_{\text{TE,combined}} + R_{\text{is}} \tag{41}$$

3.4 Electrical Resistances

The electrical resistance of each component will be calculated based on geometry and material properties. The general formula for electrical resistance is given by:

$$R_{\text{e}} = \frac{\rho_{\text{TE}} \cdot L}{A} \tag{42}$$

For a variables cross sectional area, the electrical resistance can be calculated using:

$$R_{\text{e}} = \int_{x=0}^{L} \frac{\rho_{\text{TE}} \cdot dx}{A(x)} \tag{43}$$

3.4.1 Thermoelectric Legs

The electrical resistance of the thermoelectric leg can be calculated similarly to the thermal resistance, using the same cross sectional area calculations. However, the effect of considering areas such as I and III similar to thermal resistance is negligable because electricity flows from interconnect to the outerconnect directly through the region II only. There is no lateral / azimuthal charge transfer. Therefore, the electrical resistance of the thermoelectric leg for a single TEC element is given by the same expression from eq. (21), wtih κ_{TE} replaced by $\frac{1}{\rho_{\text{TE}}}$. Therefore, the electrical resistance of a single thermoelectric leg becomes:

$$\begin{aligned} R_{\text{e,TE,II}} = {} & \frac{2\rho_{\text{TE}}}{\theta \cdot t_{\text{TEC}}} \cdot \\ & \ln \left| \frac{\theta \cdot t_{\text{TEC}}(r_{\text{out}} - W_{\text{oc}}) - 2W_{\text{az}} \cdot t_{\text{TEC}}}{\theta \cdot t_{\text{TEC}}(r_{\text{in}} + W_{\text{ic}}) - 2W_{\text{az}} \cdot t_{\text{TEC}}} \right| \end{aligned} \tag{44}$$

3.4.2 Interconnects

The interconnects transfer electricity mainly in azimuthal direction. Because of this, the variable of integration is the angle. Therefore, we can substitute $dx = rd\phi$ to'' eq. (43) and it becomes:

$$R_{\text{e,ic}} = \int_{\phi_1}^{\phi_2} \frac{\rho_{\text{TE}} \cdot r}{A(\phi)} \cdot d\phi \tag{45}$$

These interconnects have a rectangular cross section area, with width W_{ic} and thickness t_{ic}. Since both dimensional are independant of the angle ϕ, the cross sectional integration becomes:

$$R_{\text{e,ic}} = \int_{\phi_1}^{\phi_2} \frac{\rho_{\text{TE}} \cdot r}{W_{\text{ic}} \cdot t_{\text{ic}}} \cdot d\phi$$

Assuming constant resistivity ρ_{TE}, and using the average radius value for r as $r_{\text{avg}} = r_{\text{in}} + \frac{1}{2}W_{\text{ic}}$ they can be taken outside the integral:

$$R_{\text{e,ic}} = \frac{\rho_{\text{TE}} \cdot r_{\text{avg}}}{W_{\text{ic}} \cdot t_{\text{ic}}} \int_{\phi_1}^{\phi_2} d\phi$$

Assuming that interconnect start at some arbitrary angle ϕ_1 and ends at $\phi_2 = \phi_1 + \beta_{\text{ic}}$, the integral evaluates to:

$$
\begin{aligned}
R_{\text{e,ic}} &= \frac{\rho_{\text{TE}} \cdot r_{\text{avg}}}{W_{\text{ic}} \cdot t_{\text{ic}}} \int_{\phi_1}^{\phi_1+\beta_{\text{ic}}} d\phi \\
&= \frac{\rho_{\text{TE}} \cdot r_{\text{avg}}}{W_{\text{ic}} \cdot t_{\text{ic}}} (\phi_1 + \beta_{\text{ic}} - \phi_1) \\
&= \frac{\rho_{\text{TE}} \cdot r_{\text{avg}} \cdot \beta_{\text{ic}}}{W_{\text{ic}} \cdot t_{\text{ic}}}
\end{aligned}
$$

Therefore, the electrical resistance of the interconnect for a single TEC element is given by:

$$
R_{\text{e,ic}} = \frac{\rho_{\text{TE}} \cdot r_{\text{avg}} \cdot \beta_{\text{ic}}}{W_{\text{ic}} \cdot t_{\text{ic}}} \tag{46}
$$

3.4.3 outerconnect

Interconnect and outerconnect have similar geometry and current flow direction. Therefore, the electrical resistance of the outerconnect can be calculated similarly to the interconnect. The only difference is that there are two outerconnects per TEC element, one on each side. However, since they are subtending only half the angle of the interconnect, their combined resistance is equal to that of a single interconnect. Therefore, the electrical resistance of the outerconnect for a single TEC element is given by:

$$
R_{\text{e,oc}} = \frac{\rho_{\text{TE}} \cdot r_{\text{avg}} \cdot \beta_{\text{oc}}}{W_{\text{oc}} \cdot t_{\text{oc}}} \tag{47}
$$

Where $r_{\text{avg}} = r_{\text{out}} - \frac{1}{2} W_{\text{oc}}$.

4 Formation of the Linear System

To find the temperature values at each node in the thermal network, we can set up a system of linear equations based on the lumped resistances and heat sources. Each node will have an equation representing the balance of heat flow into and out of that node. Here we write the energy balance available 3 types of nodes: chip layer nodes, TEC layer nodes and central node.

4.1 Chip Layer

A general node in this layer has 4 terms: 2 lateral heat transfer, 1 vertical heat transfer to the TEC layer and the heat generation from the heat flux applied. Writing the energy balance equation,

$$
\underbrace{\frac{T_{\text{chip},i-1} - T_{\text{chip},i}}{R_{\text{chip},i-1}}}_{\text{Lateral In}} + \underbrace{\frac{T_{\text{chip},i+1} - T_{\text{chip},i}}{R_{\text{chip},i}}}_{\text{Lateral Out}} - \underbrace{\frac{T_{\text{chip},i} - T_{\text{TEC},i}}{R_{\text{ve},i}}}_{\text{Vertical Loss}} + Q_{\text{gen},i} = 0
$$

Isolating the unknown temperature terms in the above equation gives,

$$
\begin{aligned}
&\frac{1}{R_{\text{chip},i-1}} T_{\text{chip},i-1} - \left(\frac{1}{R_{\text{chip},i-1}} + \frac{1}{R_{\text{chip},i}} + \frac{1}{R_{\text{ve},i}} \right) T_{\text{chip},i} \\
&+ \frac{1}{R_{\text{chip},i}} T_{\text{chip},i+1} + \frac{1}{R_{\text{ve},i}} T_{\text{TEC},i} = -Q_{\text{gen},i}.
\end{aligned} \tag{48}
$$

This layer doesn't have any boundary conditions due to its closed nature. However, it should be noted that when writing the equation for the 1st node, the term $R_{\text{chip},i-1} = R_{\text{chip},0}$ is equal to $R_{\text{chip},0\to1}$ which is given by eq. (32).

4.2 TEC Layer

The nodes in the TEC layer are governed by thermoelectric effect. The standard equation for the TEC module is as follows.

$$
Q_c = SIT_c - \tfrac{1}{2} I^2 R - K_t \left(T_h - T_c \right), \tag{49}
$$

The terms represents heat pump through thermoelectric effects, joule heating due to electrical resistance, and back conduction respectively. Note that we have derived thermal resistance values instead of conductance values, so we need to use their reciprocals when substituting into the equation.

4.2.1 Resistance Heat generation Assignment

The 0.5 term in the joule heating term is to divide the heating from the TE legs to both cold side and hot side equally. However here we have interconnect and outerconnect that generates the heat. But their heat doesn't get added to both sides equally. So instead of a single lumped $R_{e,i}$, we have to split the electrical resistance of Stage i into three distinct physical components:

- $R_{e,ic,i}$ (Inner/Cold Interconnect):The resistance of the copper trace at the cold junction (the node itself).
- $R_{e,TE-p,i}$ and $R_{e,TE-n,i}$ (TE Legs): The resistance of the P and N semiconductor pillars.

- $R_{e,oc,i}$ (Outer/Hot Interconnect): The resistance of the copper trace at the hot junction (the outer rim of this stage).

We assign Joule heating based on where the component is located relative to the node $T_{c,i}$.

- At Node $T_{c,i}$: We have the Interconnect of Stage i.

  Contribution: 100% of $I_i^2 R_{e,ic,i}$ adds heat to this node.

- Between Node $T_{c,i}$ and Outer Boundary: We have the Legs of Stage i.

  Contribution: 50% of $I_i^2 R_{e,TE-p,i}$ + 50% of $I_i^2 R_{e,TE-n,i}$ flows back to this node (the cold side).

- Coming from the Previous Stage $(i-1)$: The previous stage rejects heat into current node. This rejected heat includes the generation from its own legs and its own outer interconnect.

  Contribution: 100% of $I_{i-1}^2 R_{e,oc,i-1}$ (Outerconnect of prev stage) + 50% of $I_{i-1}^2 R_{e,TE-p,i-1}$ + 50% of $I_{i-1}^2 R_{e,TE-n,i-1}$.

Note that at the edge boundary, the heat generated from the outerconnect, and the half of p and n TE leg heating of the last stage will not be added to any node, as it is assumed to be dissipated to the boundary condition.

4.2.2 Writing Energy Balance

Writing the energy balance equation for a general TEC layer node,

$$\underbrace{\frac{T_{\text{chip},i} - T_{c,i}}{R_{\text{ve},i}}}_{\text{From Chip}} + \underbrace{Q_{h,i-1}}_{\text{From Stage } i-1} - \underbrace{Q_{c,i}}_{\text{Into Stage } i} = 0 \tag{50}$$

Heat Rejected from Stage $i-1$ - $Q_{h,i-1}$ This is the heat exiting the hot side of the inner ring. It includes the Peltier heat, the back conduction, and Specific Joule Terms:

$$\begin{aligned} Q_{h,i-1} &= S_{i-1} I_{i-1} T_{\text{TEC},i-1} - K_{t,i-1}(T_{\text{TEC},i} - T_{\text{TEC},i-1}) \\ &\quad + \underbrace{\left[\frac{1}{2} I_{i-1}^2 (R_{\text{TE-p},i-1} + R_{\text{TE-n},i-1}) + I_{i-1}^2 R_{e,\text{oc},i-1}\right]}_{\text{Joule Heat at Hot Side}} \end{aligned} \tag{51}$$

Heat Absorbed by stage i - $Q_{c,i}$ This is the heat entering the cold side of the inner ring. It includes the Peltier heat, the back conduction, and Specific Joule Terms:

$$\begin{aligned} Q_{c,i} &= S_i I_i T_{c,i} - K_{t,i}(T_{\text{TEC},i+1} - T_{\text{TEC},i}) \\ &\quad - \underbrace{\left[\frac{1}{2} I_i^2 (R_{\text{TE-p},i} + R_{\text{TE-n},i}) + I_i^2 R_{e,\text{ic},i}\right]}_{\text{Joule Heat at Cold Side}} \end{aligned} \tag{52}$$

Note that we subtracted the Joule heating term because, in the context of the current node, the jouel heating term should be added to final equation. Since we are subtracting the Q_c term, the sign of the jouel heating term must be negative to be added as a generation term in the final equation. Substituting eq. (51) and eq. (52) into eq. (50) and isolating the unknown temperature terms gives:

$$\begin{aligned} &(S_{i-1} I_{i-1} + K_{t,i-1})\, T_{\text{TEC},i-1} - \left(\frac{1}{R_{\text{ve},i}} + K_{t,i-1} + S_i I_i + K_{t,i}\right) T_{\text{TEC},i} \\ &+ K_{t,i} T_{\text{TEC},i+1} + \frac{1}{R_{\text{ve},i}} T_{\text{chip},i} \\ &= -I_{i-1}^2 \left(\frac{(R_{\text{TE-p},i-1} + R_{\text{TE-n},i-1})}{2} + R_{\text{oc},i-1}\right) \\ &\quad - I_i^2 \left(\frac{(R_{\text{TE-p},i} + R_{\text{TE-n},i})}{2} + R_{\text{ic},i}\right) \end{aligned} \tag{53}$$

Similar to chip layer, when writing the equation for the 1st node, the term $K_{t,i-1} = K_{t,0}$ is equal to $\frac{1}{R_{\text{TEC},0\to1}}$ which is given by eq. (33). It should also be noted that the K_t values are calculated using the lumped thermal resistance values derived in eq. (41).

4.2.3 Boundary Condition

We assume a constant temperature boundary condition at the outer edge of the TEC layer to ease the modelling process. Since the micro channel characteristics aren't a part of the mathematical model, this boundary condition is justified. Therefore, for the last TEC layer node, the therm $T_{\text{TEC}ni+1}$ becomes a known value equal to the boundary temperature T_{w}. The energy balance equation for the last TEC layer node becomes:

$$\begin{aligned} &(S_{N-1} I_{N-1} + K_{t,N-1})\, T_{\text{TEC},N-1} \\ &- \left(\frac{1}{R_{\text{ve},N}} + K_{t,N-1} + S_N I_N + K_{t,N}\right) T_{\text{TEC},N} + K_{t,N} T_{\text{w}} + \frac{1}{R_{\text{ve},N}} T_{\text{chip},N} \\ &= -I_{N-1}^2 \left(\frac{(R_{\text{TE-p},N-1} + R_{\text{TE-p},N-1})}{2} + R_{\text{oc},N-1}\right) \\ &\quad - I_N^2 \left(\frac{(R_{\text{TE-p},N} + R_{\text{TE-n},N})}{2} + R_{\text{ic},N}\right) \end{aligned}$$

Where N is the number of stages in the radial TEC. Since T_{w} is known, it can be carried out to the right hand side of the equation. Then the above equation becomes,

$$\begin{aligned}
&(S_{N-1}I_{N-1} + K_{t,N-1})\,T_{\text{TEC},N-1} \\
&- \left(\frac{1}{R_{\text{ve},N}} + K_{t,N-1} + S_N I_N + K_{t,N}\right) T_{\text{TEC},N} + \frac{1}{R_{\text{ve},N}} T_{\text{chip},N} \\
&= -I_{N-1}^2 \left(\frac{(R_{\text{TE-p},N-1} + R_{\text{TE-p},N-1})}{2} + R_{\text{oc},N-1}\right) \\
&\quad - I_N^2 \left(\frac{(R_{\text{TE-p},N} + R_{\text{TE-n},N})}{2} + R_{\text{ic},N}\right) - K_{t,N} T_{\text{w}}
\end{aligned} \tag{54}$$

4.3 Central Node

At the exact center ($r = 0$ to $r = r_{\text{cyl}}$), the "Chip Layer" and "TEC Layer" are mechanically and thermally merged by the heat spreader/via bundle. Therefore, they share the same temperature. Denoting this temperature as T_0, we can write the energy balance equation for this central node as:

$$\frac{T_{\text{chip},1} - T_0}{R_{\text{chip},0\to1}} + \frac{T_{\text{TEC},1} - T_0}{R_{\text{TEC},0\to1}} - Q_{\text{gen},0} = 0$$

Isolating the unknown temperature terms in the above equation gives,

$$\begin{aligned}
&- \left(\frac{1}{R_{\text{chip},0\to1}} + \frac{1}{R_{\text{TEC},0\to1}}\right) T_0 + \frac{1}{R_{\text{chip},0\to1}} T_{\text{chip},1} \\
&+ \frac{1}{R_{\text{TEC},0\to1}} T_{\text{TEC},1} = -Q_{\text{gen},0}
\end{aligned} \tag{55}$$

The above equation will work as the first equation in the linear system.

5 Matrix Formulation

The system of linear equations derived from the energy balance equations can be represented in matrix form as:

$$\mathbf{A} \cdot \mathbf{T} = \mathbf{B} \tag{56}$$

Where $\mathbf{T}$ is the vector of unknown temperatures at each node, $\mathbf{A}$ is the coefficient matrix derived from the lumped resistances and thermoelectric parameters, and $\mathbf{B}$ is the vector representing the known terms including heat generation and boundary conditions.

5.1 Block Notation

The unknown vector $\mathbf{T}$ can be organized in a block notation as follows:

$$\mathbf{T} = \begin{bmatrix} T_0 \\ \mathbf{T}_{\text{chip}} \\ \mathbf{T}_{\text{TEC}} \end{bmatrix} \tag{57}$$

with,

$$\mathbf{T}_{\text{chip}} = \begin{bmatrix} T_{\text{chip},1} \\ T_{\text{chip},2} \\ \vdots \\ T_{\text{chip},N} \end{bmatrix} \quad \text{and} \quad \mathbf{T}_{\text{TEC}} = \begin{bmatrix} T_{\text{TEC},1} \\ T_{\text{TEC},2} \\ \vdots \\ T_{\text{TEC},N} \end{bmatrix} \tag{58}$$

The coefficient matrix $\mathbf{A}$ can be organized in a block notation as follows:

$$\mathbf{A} = \begin{bmatrix} \mathbf{A_{00}} & \mathbf{Link_{0\to Si}} & \mathbf{Link_{0\to TEC}} \\ \mathbf{Link_{Si\to 0}} & \mathbf{A_{chip}} & \mathbf{A_{ve}} \\ \mathbf{Link_{TEC\to 0}} & \mathbf{A_{ve}} & \mathbf{A_{TEC}} \end{bmatrix} \tag{59}$$

Where:

- $\mathbf{A_{00}}$ (Scalar): The sum of conductances leaving Node 0.
- $\mathbf{Link_{0\to Si}}$: Coupling to the first chip ring.
- $\mathbf{Link_{0\to TEC}}$: Coupling to the first TEC ring.
- $\mathbf{A_{chip}}$: a Tridiagonal matrix representing lateral conduction in the Chip.
- $\mathbf{A_{TEC}}$: a Tridiagonal matrix representing the active TEC network.
- $\mathbf{A_{ve}}$: a Diagonal matrix representing the vertical conduction between the Chip and TEC layers.

The known vector $\mathbf{B}$ can be organized in a block notation as follows:

$$\mathbf{B} = \begin{bmatrix} \mathbf{B_0} \\ \mathbf{B}_{\text{chip}} \\ \mathbf{B}_{\text{TEC}} \end{bmatrix} \tag{60}$$

Where :

- $\mathbf{B_0}$ (Scalar): The heat generation at Node 0
- $\mathbf{B}_{\text{chip}}$: A vector representing heat generation in the chip layer.
- $\mathbf{B}_{\text{TEC}}$: A vector representing the Joule heating in the TEC layer.

5.2 Expanded Notation

5.2.1 $\mathbf{A_{00}}$ - Center Scalar

$$\mathbf{A_{00}} = \left[-\left(\frac{1}{R_{\text{chip},0\to1}} + \frac{1}{R_{\text{TEC},0\to1}} \right) \right]$$

Description: This scalar represents the sum of all thermal conductances leaving the center node (T_0). It connects to the first Silicon ring and the first TEC node.

5.2.2 $\mathbf{Link_{0\to Si}}$ - Center to Silicon

$$\mathbf{Link_{0\to Si}} = \begin{bmatrix} \frac{1}{R_{\text{chip},0\to1}} & 0 & \dots & 0 \end{bmatrix}_{1\times N}$$

Description: A row vector of size $1 \times N$. Only the first element is non-zero, representing the connection to $T_{\text{chip},1}$.

5.2.3 $\mathbf{Link_{0\to TEC}}$ - Center to TEC

$$\mathbf{Link_{0\to TEC}} = \begin{bmatrix} \frac{1}{R_{\text{TEC},0\to1}} & 0 & \dots & 0 \end{bmatrix}_{1\times N}$$

Description: A row vector of size $1 \times N$. Only the first element is non-zero, representing the connection to $T_{\text{TEC},1}$.

5.2.4 $\mathbf{Link_{Si\to 0}}$ - Silicon to Center

$$\mathbf{Link_{Si\to 0}} = \begin{bmatrix} \frac{1}{R_{\text{chip},0\to1}} \\ 0 \\ \vdots \\ 0 \end{bmatrix}_{N\times 1}$$

Description: A column vector of size $N \times 1$. This is the transpose of Region 2.

5.2.5 $\mathbf{A_{chip}}$ - Lateral Conduction Matrix

Description: A symmetric **Tridiagonal** matrix representing passive heat spreading.

- **Diagonal** (i, i)**:** The negative sum of all conductances leaving the node.
- *Boundary:* Note that at $i = 1$, the term connects to T_0. At $i = N$, the term assumes an adiabatic edge (no $R_{\text{chip},N}$).
- **Off-Diagonals:** Represents the lateral resistance R_{chip} between rings.

5.2.6 $\mathbf{A_{ve}}$ - Vertical Coupling

$$\mathbf{A_{ve}} = \begin{bmatrix} \frac{1}{R_{\text{ve},1}} & 0 & \dots & 0 \\ 0 & \frac{1}{R_{\text{ve},2}} & \dots & 0 \\ \vdots & \vdots & \ddots & \vdots \\ 0 & 0 & \dots & \frac{1}{R_{\text{ve},N}} \end{bmatrix}_{N\times N}$$

Description: A **Diagonal** matrix.

- This matrix appears twice in the global system: once connecting Silicon to TEC (Region 6), and once connecting TEC to Silicon (Region 8).

5.2.7 $\mathbf{Link_{TEC\to 0}}$ - TEC to Center

$$\mathbf{Link_{TEC\to 0}} = \begin{bmatrix} \frac{1}{R_{\text{TEC},0\to1}} \\ 0 \\ \vdots \\ 0 \end{bmatrix}_{N\times 1}$$

Description: A column vector of size $N \times 1$. This is the transpose of Region 3.

5.2.8 $\mathbf{A_{TEC}}$ - Active Pumping Matrix

Description: An **Asymmetric Tridiagonal** matrix.

- **Diagonal** (i, i)**:** Negative sum of Vertical Loss + Back conduction IN + Peltier OUT + Back conduction OUT.
- **Lower Off-Diagonal** $(i, i-1)$**:** Heat arriving from the previous stage. This contains the Peltier term $S_{i-1}I_{i-1}$ and the back conduction $K_{t,i-1}$.
- **Upper Off-Diagonal** $(i, i+1)$**:** Only back conduction $K_{t,i}$ comes from the hotter stage. The Peltier term does not flow "backwards".

5.2.9 Vector $\mathbf{B}$ - Source Vector

Description:

- $\mathbf{B_0}$: Heat generation at the center.
- $\mathbf{B}_{\text{chip}}$: Heat generation in the Silicon rings (inverted sign).
- $\mathbf{B}_{\text{TEC}}$: Contains the Joule heating terms.
- Current Node heating: $I_i^2 R_{\text{ic},i}$ (Interconnect) + $0.5 \cdot I_i^2 (R_{\text{TE-p},i} + R_{\text{TE-n},i})$ (Half leg).
- Previous Stage heating: $I_{i-1}^2 R_{\text{oc},i-1}$ (Outerconnect) + $0.5 \cdot I_{i-1}^2 (R_{\text{TE-p},i-1} + R_{\text{TE-n},i-1})$ (Half leg).
- **Last Row:** Includes the boundary condition term $-K_{t,N} T_{\text{w}}$.

6 Validation

The developed Compact Thermal Model (CTM) has been validated against a high-fidelity COMSOL Multiphysics simulation. The comparison focuses on the maximum temperature achieved within the radial TEC structure under identical operating conditions.

For all the test cases, a 3 stage radial TEC model was used. The CAD geometry was created in SolidWorks using a parametric model, allowing for easy adjustments of design parameters such as wedge angle, TEC thickness, and leg length. The CAD model was then live linked with COMSOL, and the MATLAB API for COMSOL was used to automate the simulation process and extract results. This workflow is illustrated below:

$$\begin{array}{c}\text{Parametric} \\ \text{SolidWorks} \\ \text{model}\end{array} \longleftrightarrow \begin{array}{c}\text{COMSOL} \\ \updownarrow \\ \text{MATLAB}\end{array}$$

Table 1: Validation Cases: CTM vs COMSOL Comparison

Case ID	Name	θ (°)	t_{TEC} (μm)	f_L	L_1 (μm)	I (mA)	q (W/m²)	MATLAB $T_{\max}$ (°C)	COMSOL $T_{\max}$ (°C)	Error (°C)	Error (%)
1	Thin TEC Low Current	30	100	1.00	1957.02	50	500	36.04	20.48	-15.56	-43.2
2	Moderate Current	30	150	1.15	1690.73	100	500	31.81	20.25	-11.56	-36.4
3	Length Ratio Test	30	150	1.20	1612.93	80	500	30.68	20.32	-10.36	-33.8
4	High Heat Flux	30	200	1.15	1690.73	120	2000	58.23	22.42	-35.81	-61.5
5	Wide Wedge Angle	45	150	1.15	1690.73	80	1000	44.85	21.33	-23.52	-52.4

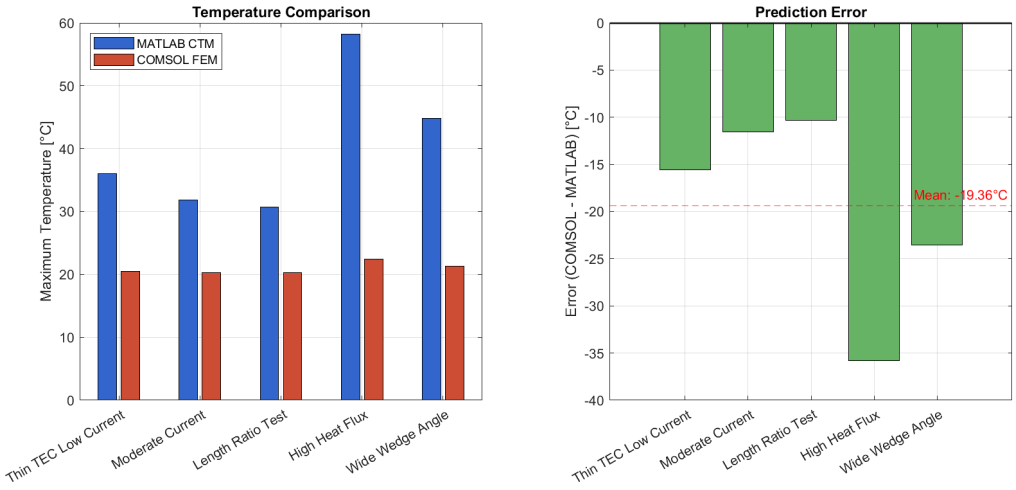


Figure 11: Maximum Temperature between CTM and COMSOL (left) and Prediction Error (right)

The validation results show systematic overprediction of maximum temperature in the CTM compared to COMSOL. This discrepancy may stem from simplified assumptions in the compact model, particularly regarding heat spreading efficiency and the dimensional reduction approach. Nevertheless, the CTM provides a computationally efficient tool for rapid design iteration and optimization, with simulation times significantly faster than COMSOL.

7 Summary

The complete thermal behavior of the radial TEC array is encapsulated in the linear system $\mathbf{A} \cdot \mathbf{T} = \mathbf{B}$. Solving this system yields the temperature distribution vector $\mathbf{T}$, providing a computationally efficient metric for evaluating and optimizing the cooling performance of the radial TEC design. While validation against high-fidelity COMSOL simulations reveals systematic overprediction of maximum temperatures, the Compact Thermal Model (CTM) remains a valuable tool for preliminary optimization due to its significantly reduced computational cost.