Department of Electrical,
Computer, & Biomedical Engineering
Faculty of Engineering
& Architectural Science

Course Title:	Computer Organization and Architecture
Course Number:	COE608
Semester/Year:	Winter 2023

Instructor:	Dr. Demetres Kostas

Assignment/Lab Number:	6
Assignment/Lab Title:	The Complete CPU

Submission Date:	12 April 2023
Due Date:	12 April 2023

LAST NAME	**FIRST NAME**	**Student Number**	**Section**	**Signature**	**Email**
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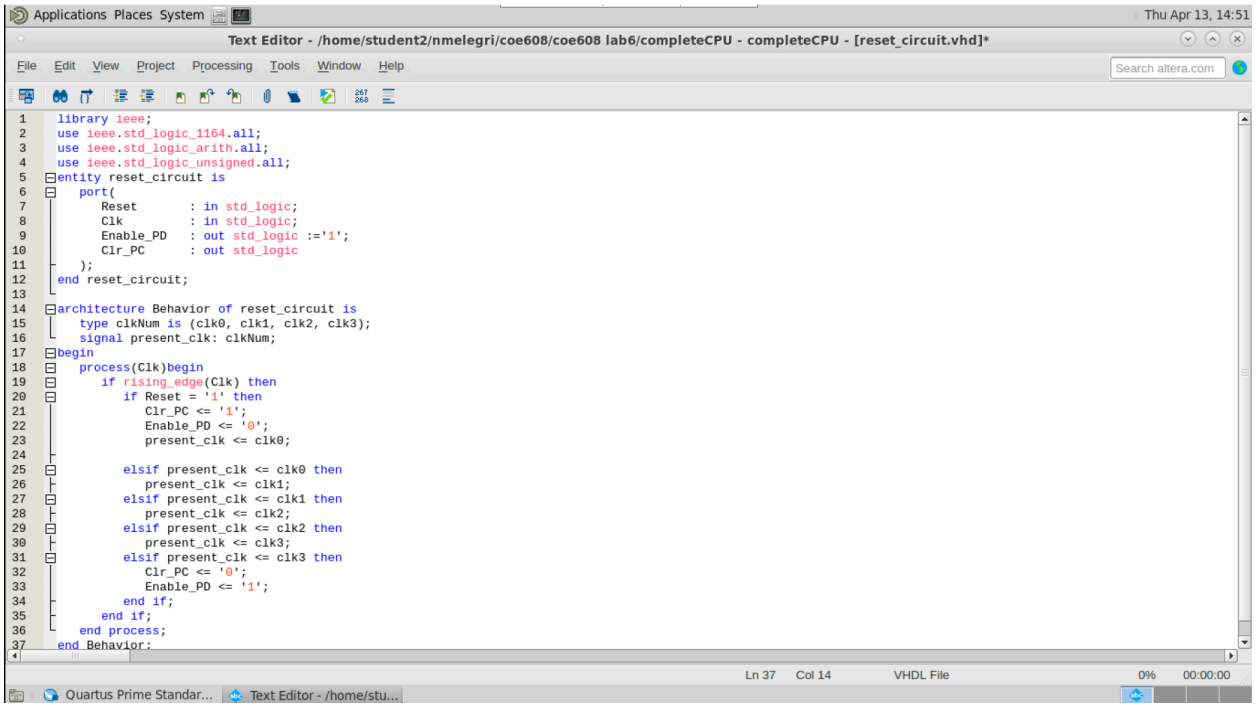
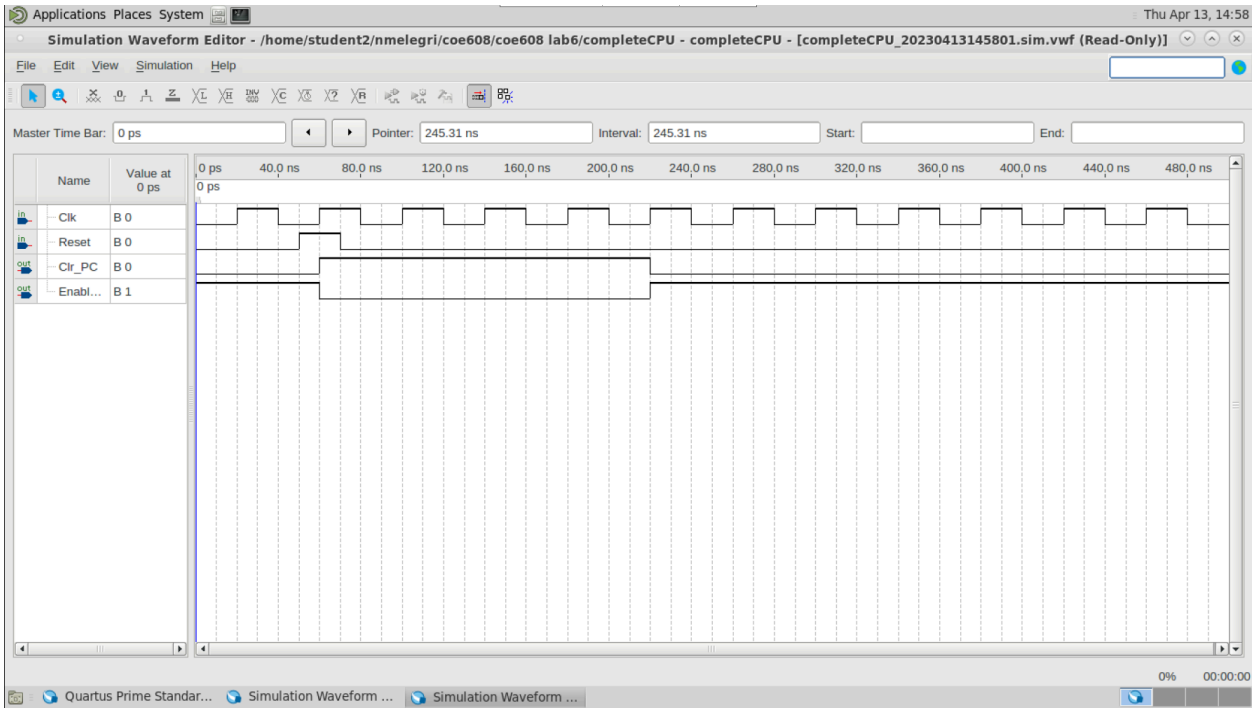
Part I

Reset Circuitry

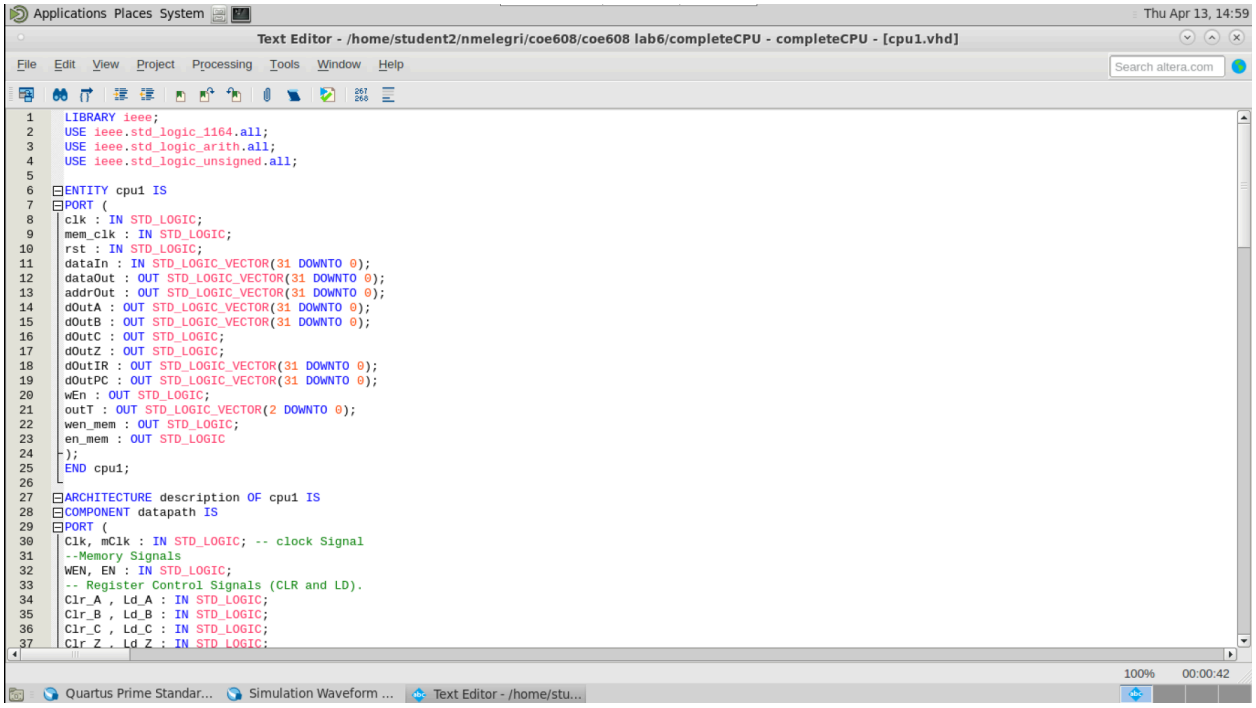


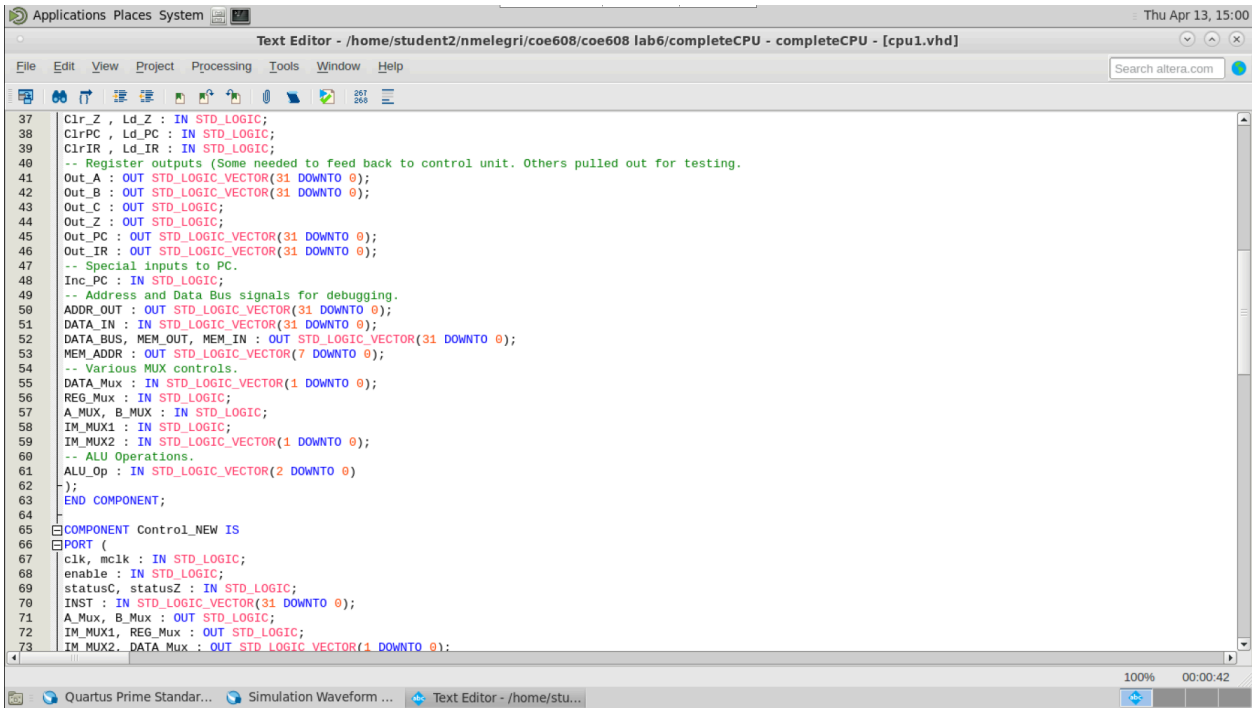
Waveform

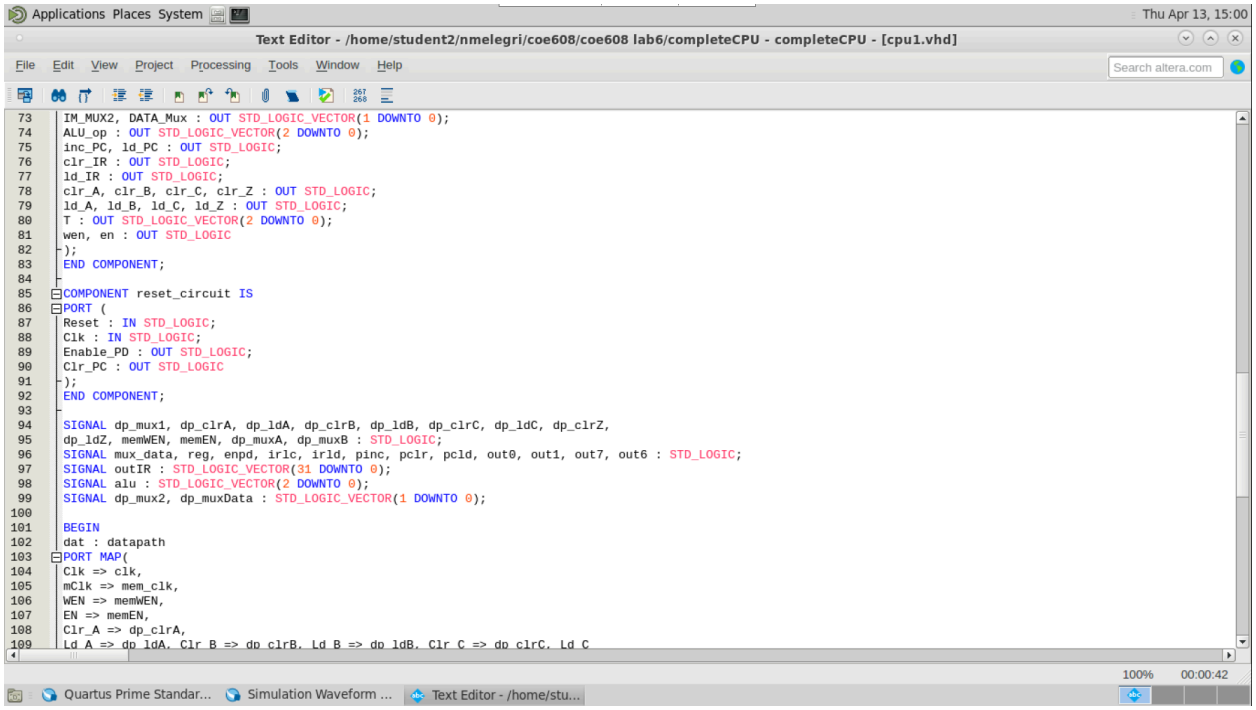


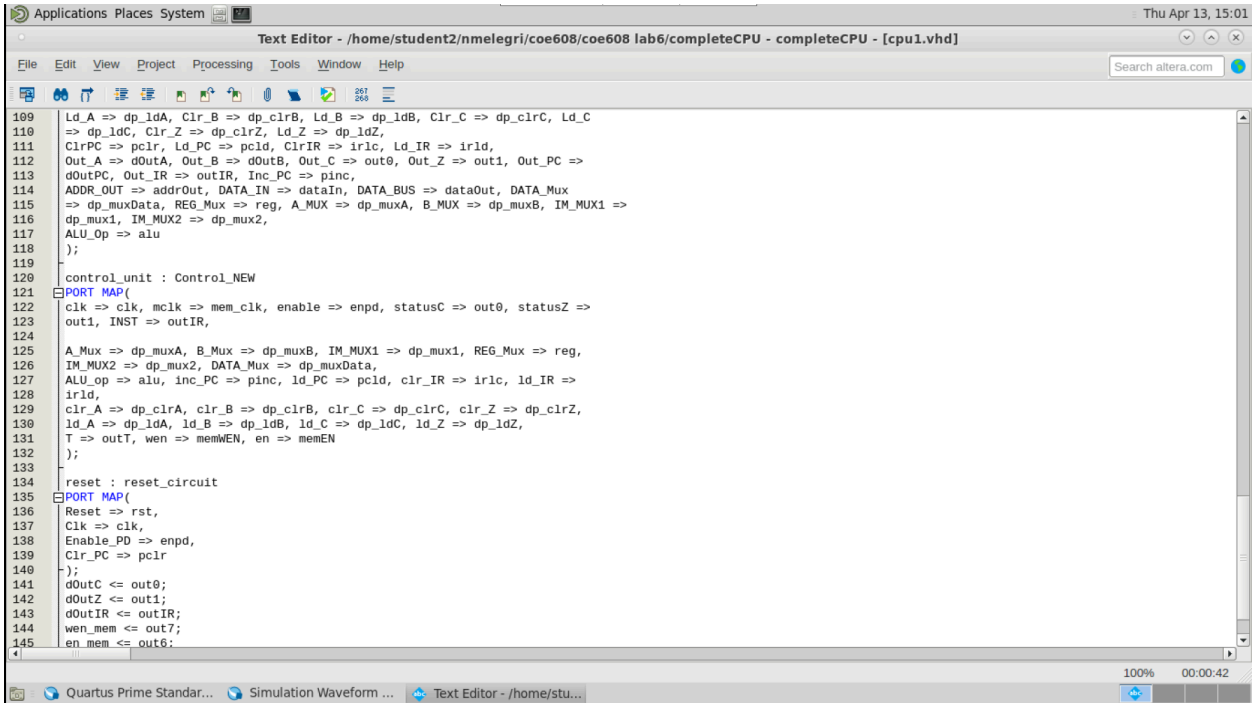
Part II

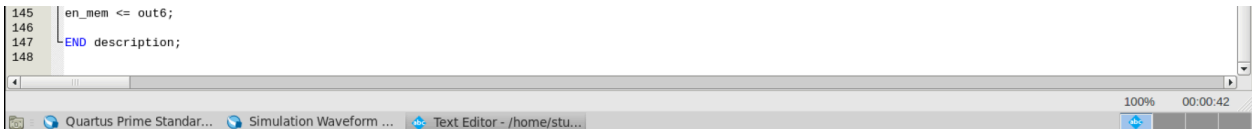
CPU


Applications Places System
Thu Apr 13, 14:59
Text Editor - /home/student2/nmelegri/coe608/coe608 lab6/completeCPU - completeCPU - [cpu1.vhd]
File Edit View Project Processing Tools Window Help
Search altera.com
LIBRARY ieee;
USE ieee.std_logic_1164.all;
USE ieee.std_logic_arith.all;
USE ieee.std_logic_unsigned.all;
ENTITY cpu1 IS
PORT (
clk : IN STD_LOGIC;
mem_clk : IN STD_LOGIC;
rst : IN STD_LOGIC;
dataIn : IN STD_LOGIC_VECTOR(31 DOWNTO 0);
dataOut : OUT STD_LOGIC_VECTOR(31 DOWNTO 0);
addrOut : OUT STD_LOGIC_VECTOR(31 DOWNTO 0);
dOutA : OUT STD_LOGIC_VECTOR(31 DOWNTO 0);
dOutB : OUT STD_LOGIC_VECTOR(31 DOWNTO 0);
dOutC : OUT STD_LOGIC;
dOutZ : OUT STD_LOGIC;
dOutIR : OUT STD_LOGIC_VECTOR(31 DOWNTO 0);
dOutPC : OUT STD_LOGIC_VECTOR(31 DOWNTO 0);
wEn : OUT STD_LOGIC;
outT : OUT STD_LOGIC_VECTOR(2 DOWNTO 0);
wen_mem : OUT STD_LOGIC;
en_mem : OUT STD_LOGIC
);
END cpu1;
ARCHITECTURE description OF cpu1 IS
COMPONENT datapath IS
PORT (
Clk, mClk : IN STD_LOGIC; -- clock Signal
--Memory Signals
WEN, EN : IN STD_LOGIC;
-- Register Control Signals (CLR and LD).
Clr_A , Ld_A : IN STD_LOGIC;
Clr_B , Ld_B : IN STD_LOGIC;
Clr_C , Ld_C : IN STD_LOGIC;
Clr_Z , Ld_Z : IN STD_LOGIC;
100%
00:00:42
Quartus Prime Standar...
Simulation Waveform ...
Text Editor - /home/stu...


Applications Places System
Thu Apr 13, 15:00
Text Editor - /home/student2/nmelegri/coe608/coe608 lab6/completeCPU - completeCPU - [cpu1.vhd]
File Edit View Project Processing Tools Window Help
Search altera.com
Clr_Z , Ld_Z : IN STD_LOGIC;
ClrPC , Ld_PC : IN STD_LOGIC;
ClrIR , Ld_IR : IN STD_LOGIC;
-- Register outputs (Some needed to feed back to control unit. Others pulled out for testing.
Out_A : OUT STD_LOGIC_VECTOR(31 DOWNTO 0);
Out_B : OUT STD_LOGIC_VECTOR(31 DOWNTO 0);
Out_C : OUT STD_LOGIC;
Out_Z : OUT STD_LOGIC;
Out_PC : OUT STD_LOGIC_VECTOR(31 DOWNTO 0);
Out_IR : OUT STD_LOGIC_VECTOR(31 DOWNTO 0);
-- Special inputs to PC.
Inc_PC : IN STD_LOGIC;
-- Address and Data Bus signals for debugging.
ADDR_OUT : OUT STD_LOGIC_VECTOR(31 DOWNTO 0);
DATA_IN : IN STD_LOGIC_VECTOR(31 DOWNTO 0);
DATA_BUS, MEM_OUT, MEM_IN : OUT STD_LOGIC_VECTOR(31 DOWNTO 0);
MEM_ADDR : OUT STD_LOGIC_VECTOR(7 DOWNTO 0);
-- Various MUX controls.
DATA_Mux : IN STD_LOGIC_VECTOR(1 DOWNTO 0);
REG_Mux : IN STD_LOGIC;
A_MUX, B_MUX : IN STD_LOGIC;
IM_MUX1 : IN STD_LOGIC;
IM_MUX2 : IN STD_LOGIC_VECTOR(1 DOWNTO 0);
-- ALU Operations.
ALU_Op : IN STD_LOGIC_VECTOR(2 DOWNTO 0)
);
END COMPONENT;
COMPONENT Control_NEW IS
PORT (
clk, mclk : IN STD_LOGIC;
enable : IN STD_LOGIC;
statusC, statusZ : IN STD_LOGIC;
INST : IN STD_LOGIC_VECTOR(31 DOWNTO 0);
A_Mux, B_Mux : OUT STD_LOGIC;
IM_MUX1, REG_Mux : OUT STD_LOGIC;
IM_MUX2, DATA_Mux : OUT STD_LOGIC_VECTOR(1 DOWNTO 0);
100%
00:00:42
Quartus Prime Standar...
Simulation Waveform ...
Text Editor - /home/stu...


Applications Places System
Thu Apr 13, 15:00
Text Editor - /home/student2/nmelegri/coe608/coe608 lab6/completeCPU - completeCPU - [cpu1.vhd]
File Edit View Project Processing Tools Window Help
Search altera.com
IM_MUX2, DATA_Mux : OUT STD_LOGIC_VECTOR(1 DOWNTO 0);
ALU_op : OUT STD_LOGIC_VECTOR(2 DOWNTO 0);
inc_PC, ld_PC : OUT STD_LOGIC;
clr_IR : OUT STD_LOGIC;
ld_IR : OUT STD_LOGIC;
clr_A, clr_B, clr_C, clr_Z : OUT STD_LOGIC;
ld_A, ld_B, ld_C, ld_Z : OUT STD_LOGIC;
T : OUT STD_LOGIC_VECTOR(2 DOWNTO 0);
wen, en : OUT STD_LOGIC
);
END COMPONENT;
COMPONENT reset_circuit IS
PORT (
Reset : IN STD_LOGIC;
Clk : IN STD_LOGIC;
Enable_PD : OUT STD_LOGIC;
Clr_PC : OUT STD_LOGIC
);
END COMPONENT;
SIGNAL dp_mux1, dp_clrA, dp_ldA, dp_clrB, dp_ldB, dp_clrC, dp_ldC, dp_clrZ,
dp_ldZ, memWEN, memEN, dp_muxA, dp_muxB : STD_LOGIC;
SIGNAL mux_data, reg, enpd, irlc, irld, pinc, pclr, pcld, out0, out1, out7, out6 : STD_LOGIC;
SIGNAL outIR : STD_LOGIC_VECTOR(31 DOWNTO 0);
SIGNAL alu : STD_LOGIC_VECTOR(2 DOWNTO 0);
SIGNAL dp_mux2, dp_muxData : STD_LOGIC_VECTOR(1 DOWNTO 0);
BEGIN
dat : datapath
PORT MAP(
Clk => clk,
mClk => mem_clk,
WEN => memWEN,
EN => memEN,
Clr_A => dp_clrA,
Ld_A => dp_ldA, Clr_B => dp_clrB, Ld_B => dp_ldB, Clr_C => dp_clrC, Ld_C
100%
00:00:42
Quartus Prime Standar...
Simulation Waveform ...
Text Editor - /home/stu...


Applications Places System
Thu Apr 13, 15:01
Text Editor - /home/student2/nmelegri/coe608/coe608 lab6/completeCPU - completeCPU - [cpu1.vhd]
File Edit View Project Processing Tools Window Help
Search altera.com
Ld_A => dp_ldA, Clr_B => dp_clrB, Ld_B => dp_ldB, Clr_C => dp_clrC, Ld_C
=> dp_ldC, Clr_Z => dp_clrZ, Ld_Z => dp_ldZ,
ClrPC => pclr, Ld_PC => pcld, ClrIR => irlc, Ld_IR => irld,
Out_A => dOutA, Out_B => dOutB, Out_C => out0, Out_Z => out1, Out_PC =>
dOutPC, Out_IR => outIR, Inc_PC => pinc,
ADDR_OUT => addrOut, DATA_IN => dataIn, DATA_BUS => dataOut, DATA_Mux
=> dp_muxData, REG_Mux => reg, A_MUX => dp_muxA, B_MUX => dp_muxB, IM_MUX1 =>
dp_mux1, IM_MUX2 => dp_mux2,
ALU_Op => alu
);
control_unit : Control_NEW
PORT MAP(
clk => clk, mclk => mem_clk, enable => enpd, statusC => out0, statusZ =>
out1, INST => outIR,
A_Mux => dp_muxA, B_Mux => dp_muxB, IM_MUX1 => dp_mux1, REG_Mux => reg,
IM_MUX2 => dp_mux2, DATA_Mux => dp_muxData,
ALU_op => alu, inc_PC => pinc, ld_PC => pcld, clr_IR => irlc, ld_IR =>
irld,
clr_A => dp_clrA, clr_B => dp_clrB, clr_C => dp_clrC, clr_Z => dp_clrZ,
ld_A => dp_ldA, ld_B => dp_ldB, ld_C => dp_ldC, ld_Z => dp_ldZ,
T => outT, wen => memWEN, en => memEN
);
reset : reset_circuit
PORT MAP(
Reset => rst,
Clk => clk,
Enable_PD => enpd,
Clr_PC => pclr
);
dOutC <= out0;
dOutZ <= out1;
dOutIR <= outIR;
wen_mem <= out7;
en_mem <= out6;
100%
00:00:42
Quartus Prime Standar...
Simulation Waveform ...
Text Editor - /home/stu...


en_mem <= out6;
END description;
100%
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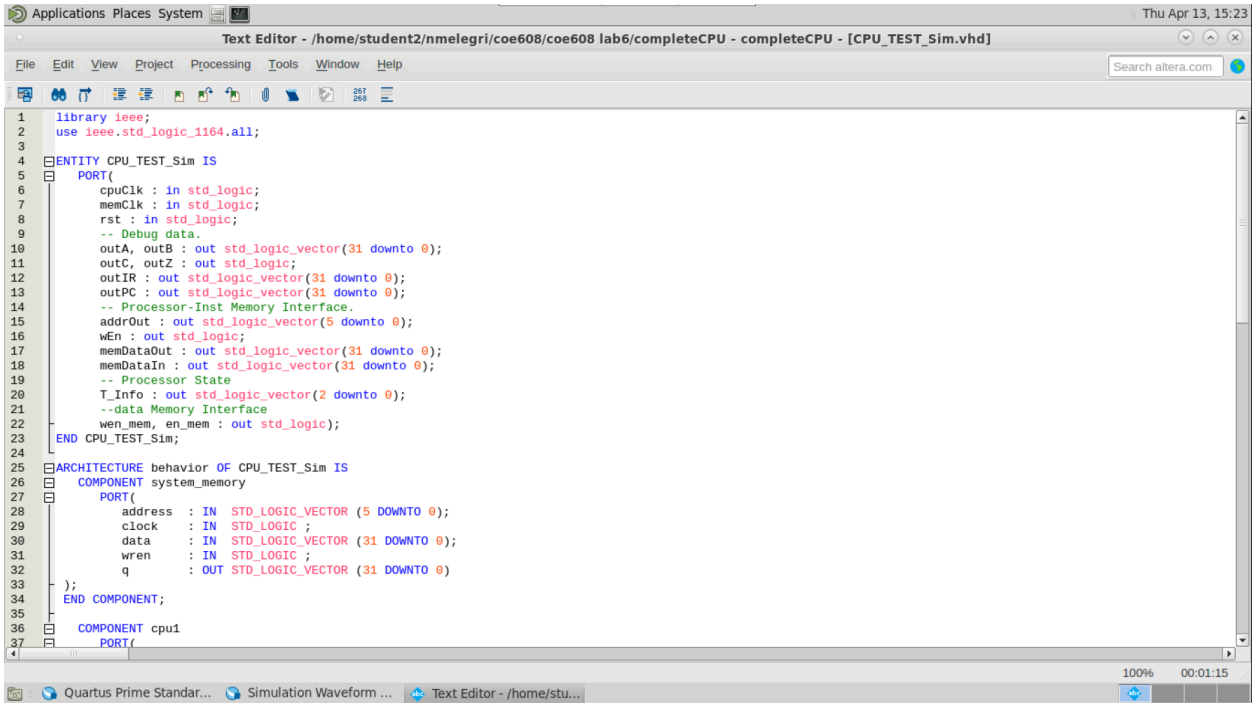
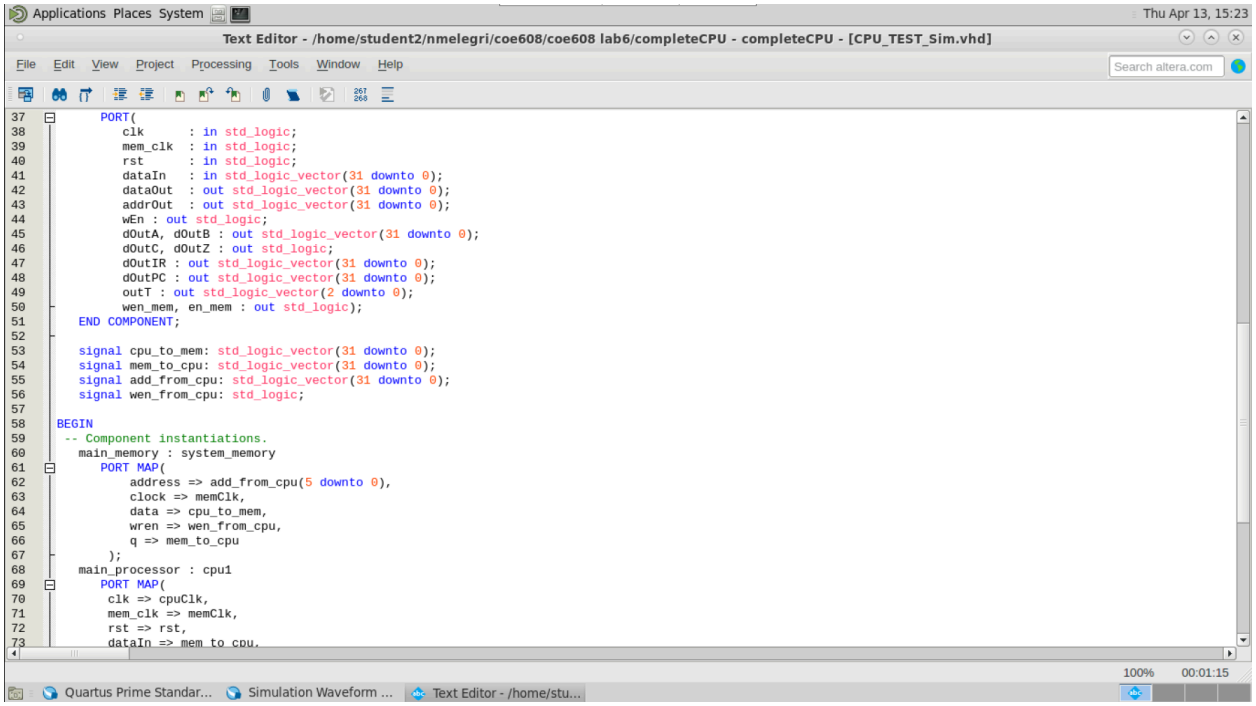
Quartus Prime Standar...
Simulation Waveform ...
Text Editor - /home/stu...

CPU Tester (connects CPU to instruction memory)



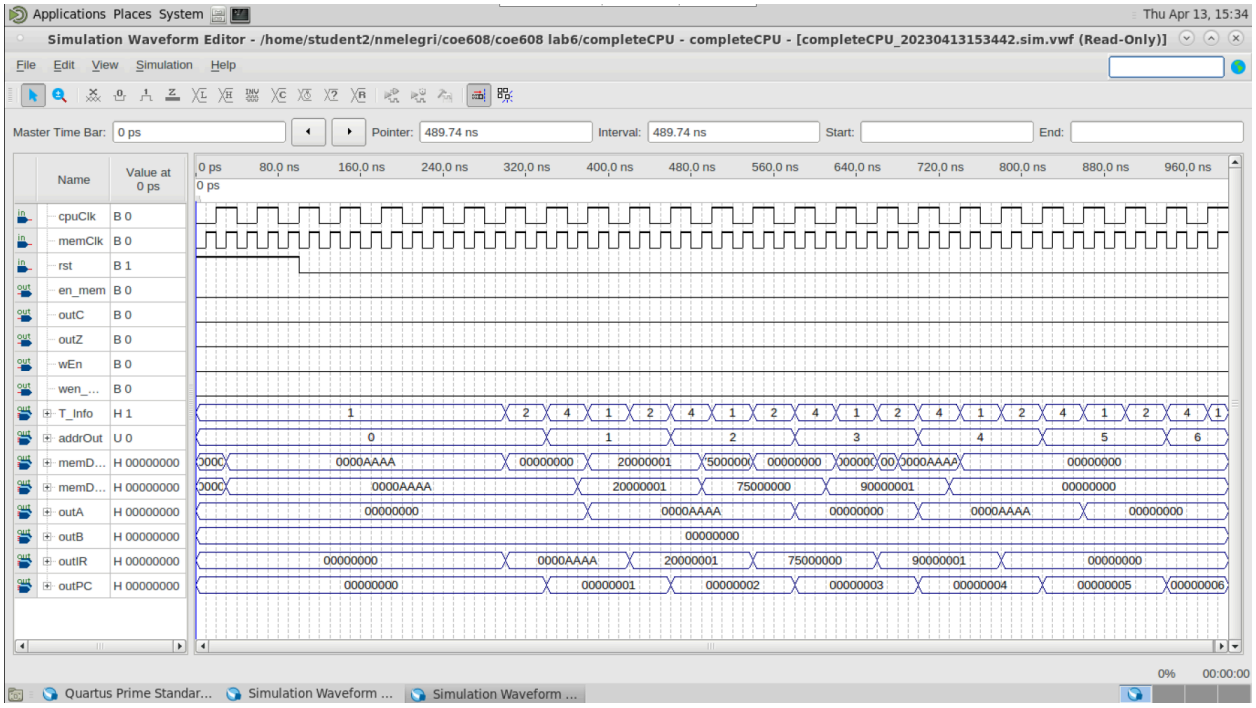

```
1  library ieee;
2  use ieee.std_logic_1164.all;
3
4  ENTITY CPU_TEST_Sim IS
5     PORT(
6        cpuClk : in std_logic;
7        memClk : in std_logic;
8        rst : in std_logic;
9        -- Debug data.
10       outA, outB : out std_logic_vector(31 downto 0);
11       outC, outZ : out std_logic;
12       outIR : out std_logic_vector(31 downto 0);
13       outPC : out std_logic_vector(31 downto 0);
14       -- Processor-Inst Memory Interface.
15       addrOut : out std_logic_vector(5 downto 0);
16       wEn : out std_logic;
17       memDataOut : out std_logic_vector(31 downto 0);
18       memDataIn : out std_logic_vector(31 downto 0);
19       -- Processor State
20       T_Info : out std_logic_vector(2 downto 0);
21       --data Memory Interface
22       wen_mem, en_mem : out std_logic);
23 END CPU_TEST_Sim;
24
25 ARCHITECTURE behavior OF CPU_TEST_Sim IS
26    COMPONENT system_memory
27       PORT(
28          address  : IN  STD_LOGIC_VECTOR (5 DOWNTO 0);
29          clock    : IN  STD_LOGIC ;
30          data     : IN  STD_LOGIC_VECTOR (31 DOWNTO 0);
31          wren     : IN  STD_LOGIC ;
32          q        : OUT STD_LOGIC_VECTOR (31 DOWNTO 0)
33 );
34  END COMPONENT;
35
36    COMPONENT cpu1
37       PORT(
```


Applications Places System
Thu Apr 13, 15:23
Text Editor - /home/student2/nmelegri/coe608/coe608 lab6/completeCPU - completeCPU - [CPU_TEST_Sim.vhd]
File Edit View Project Processing Tools Window Help
Search altera.com
37 PORT(
38 clk : in std_logic;
39 mem_clk : in std_logic;
40 rst : in std_logic;
41 dataIn : in std_logic_vector(31 downto 0);
42 dataOut : out std_logic_vector(31 downto 0);
43 addrOut : out std_logic_vector(31 downto 0);
44 wEn : out std_logic;
45 dOutA, dOutB : out std_logic_vector(31 downto 0);
46 dOutC, dOutZ : out std_logic;
47 dOutIR : out std_logic_vector(31 downto 0);
48 dOutPC : out std_logic_vector(31 downto 0);
49 outT : out std_logic_vector(2 downto 0);
50 wen_mem, en_mem : out std_logic);
51 END COMPONENT;
52
53 signal cpu_to_mem: std_logic_vector(31 downto 0);
54 signal mem_to_cpu: std_logic_vector(31 downto 0);
55 signal add_from_cpu: std_logic_vector(31 downto 0);
56 signal wen_from_cpu: std_logic;
57
58 BEGIN
59 -- Component instantiations.
60 main_memory : system_memory
61 PORT MAP(
62 address => add_from_cpu(5 downto 0),
63 clock => memClk,
64 data => cpu_to_mem,
65 wren => wen_from_cpu,
66 q => mem_to_cpu
67);
68 main_processor : cpu1
69 PORT MAP(
70 clk => cpuClk,
71 mem_clk => memClk,
72 rst => rst,
73 dataIn => mem_to_cpu,
100%
00:01:15
Quartus Prime Standar...
Simulation Waveform ...
Text Editor - /home/stu...

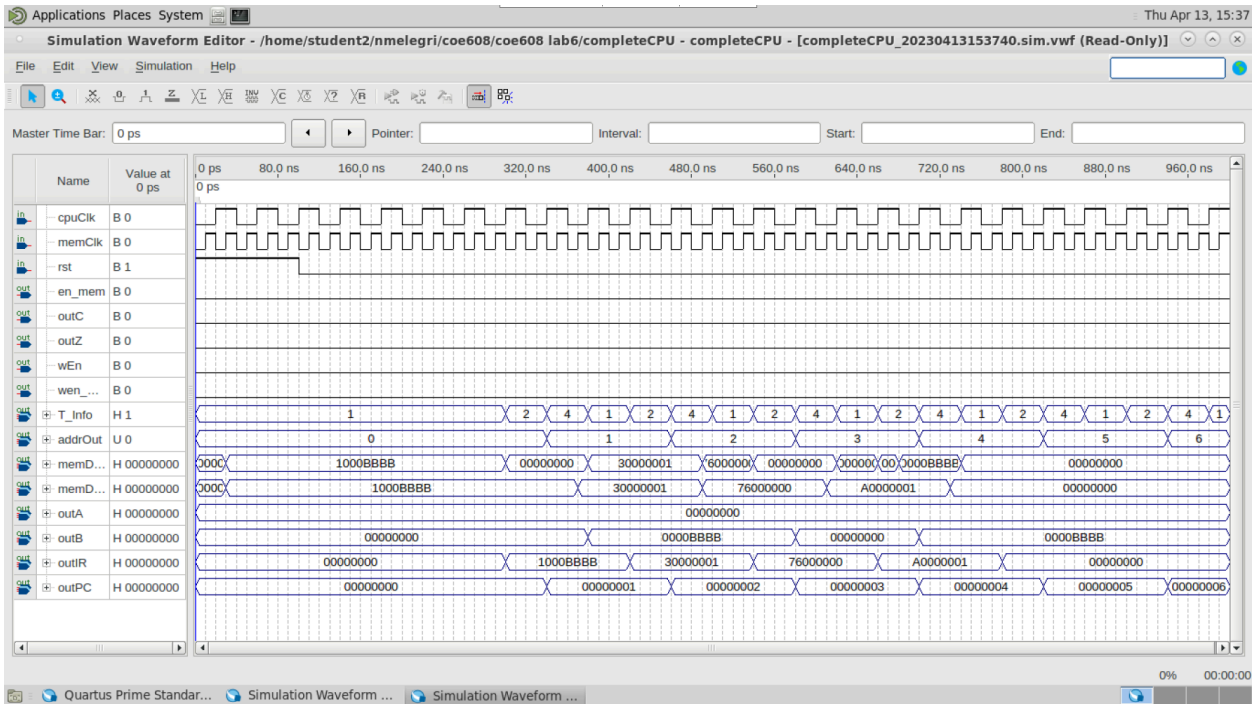

73 dataIn => mem_to_cpu,
74 dataOut => cpu_to_mem,
75 addrOut => add_from_cpu,
76 wEn => wen_from_cpu,
77 dOutA => outA,
78 dOutB => outB,
79 dOutC => outC,
80 dOutZ => outZ,
81 dOutIR => outIR,
82 dOutPC => outPC,
83 outT => T_Info,
84 wen_mem => wen_mem,
85 en_mem => en_mem
86);
87
88 addrOut <= add_from_cpu(5 downto 0);
89 wEn <= wen_from_cpu;
90 memDataOut <= mem_to_cpu;
91 memDataIn <= cpu_to_mem;
92 END behavior;
100%
00:01:15
Quartus Prime Standar...
Simulation Waveform ...
Text Editor - /home/stu...

Waveforms

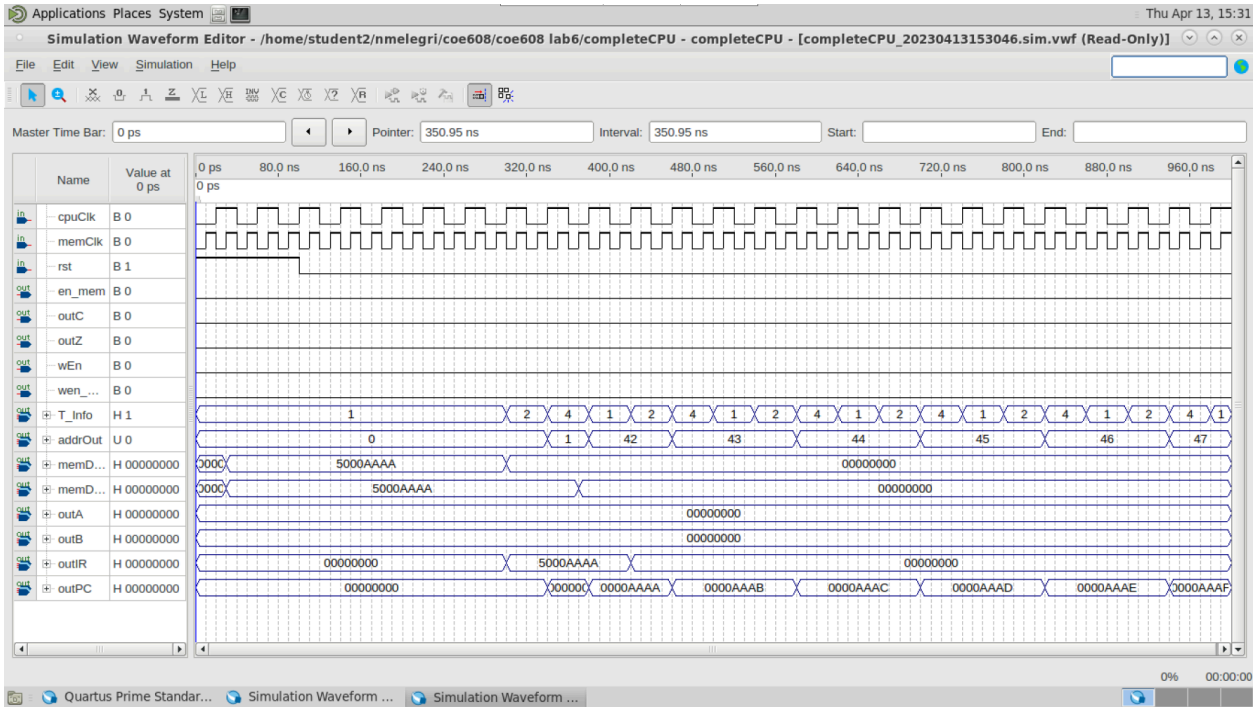
LDAI, STA, CLRA, LDA



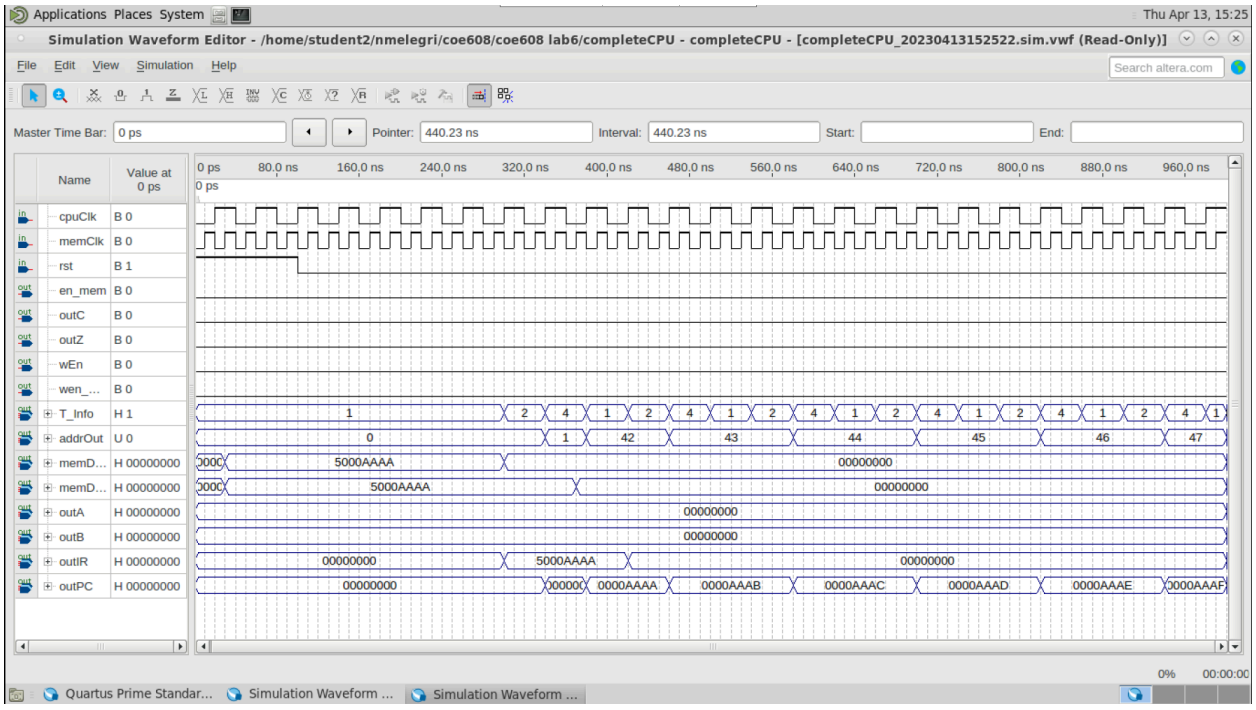
LDBI, STB, CLRB, LDB



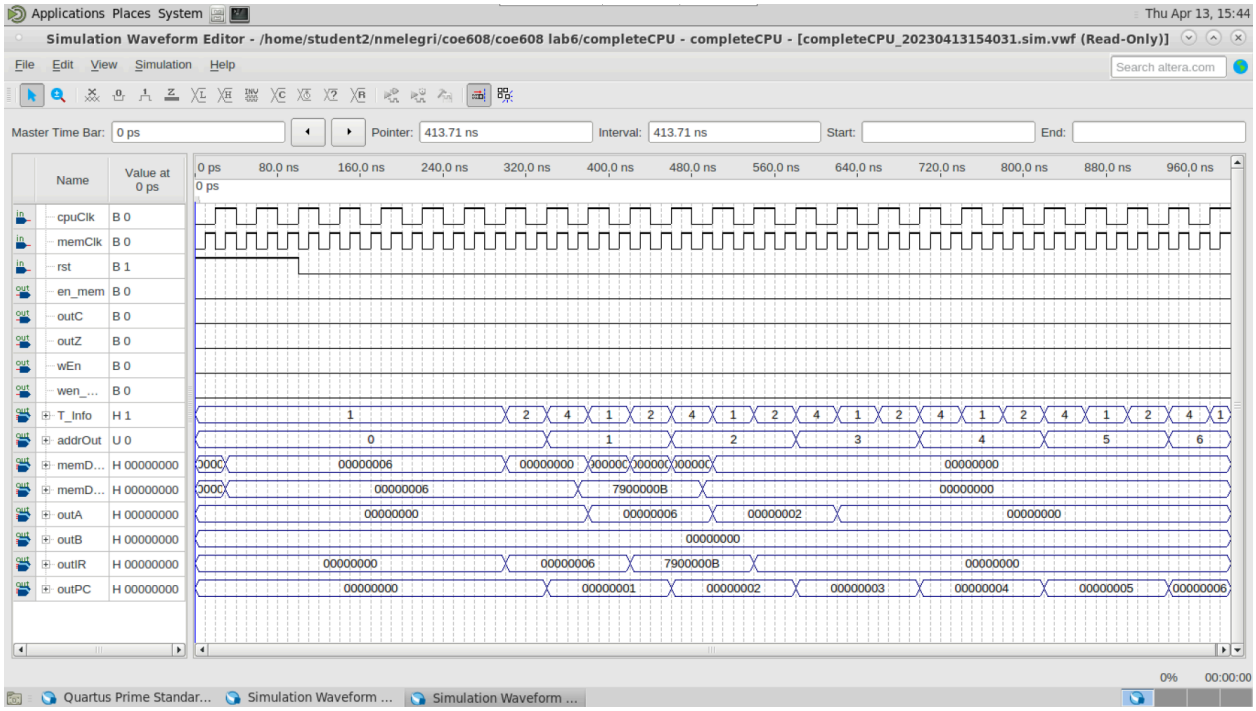
LUI


Applications Places System
Thu Apr 13, 15:31
Simulation Waveform Editor - /home/student2/nmelegri/coe608/coe608 lab6/completeCPU - completeCPU - [completeCPU_20230413153046.sim.vwf (Read-Only)]
File Edit View Simulation Help
Master Time Bar: 0 ps
Pointer: 350.95 ns
Interval: 350.95 ns
Start:
End:
Name
Value at 0 ps
cpuClk B 0
memClk B 0
rst B 1
en_mem B 0
outC B 0
outZ B 0
wEn B 0
wen_... B 0
T_Info H 1
addrOut U 0
memD... H 00000000
memD... H 00000000
outA H 00000000
outB H 00000000
outIR H 00000000
outPC H 00000000
0 ps 80.0 ns 160.0 ns 240.0 ns 320.0 ns 400.0 ns 480.0 ns 560.0 ns 640.0 ns 720.0 ns 800.0 ns 880.0 ns 960.0 ns
0 ps
5000AAAA
00000000
0000AAAA
0000AAAB
0000AAAC
0000AAAD
0000AAAE
0000AAAF
0%
00:00:00
Quartus Prime Standar...
Simulation Waveform ...
Simulation Waveform ...

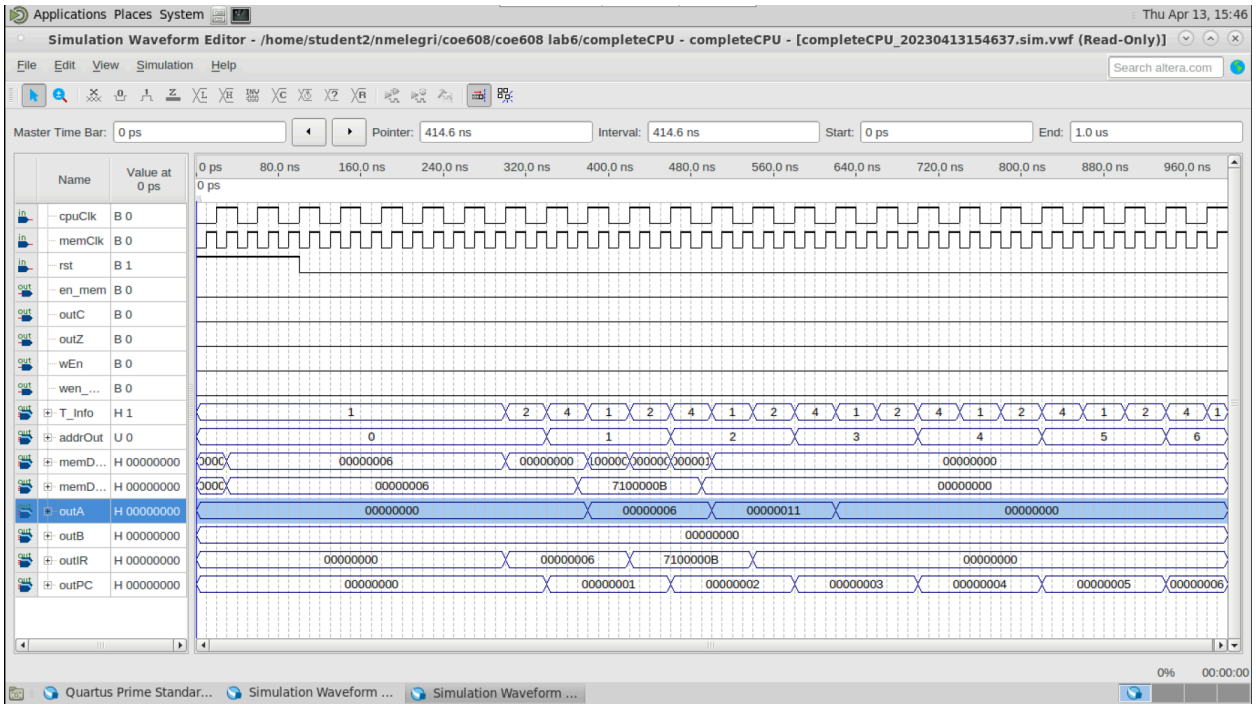
JMP


Applications Places System
Thu Apr 13, 15:25
Simulation Waveform Editor - /home/student2/nmelegri/coe608/coe608 lab6/completeCPU - completeCPU - [completeCPU_20230413152522.sim.vwf (Read-Only)]
File Edit View Simulation Help
Search altera.com
Master Time Bar: 0 ps
Pointer: 440.23 ns
Interval: 440.23 ns
Start:
End:
Name
Value at 0 ps
cpuClk B 0
memClk B 0
rst B 1
en_mem B 0
outC B 0
outZ B 0
wEn B 0
wen_... B 0
T_Info H 1
addrOut U 0
memD... H 00000000
memD... H 00000000
outA H 00000000
outB H 00000000
outIR H 00000000
outPC H 00000000
0 ps 80.0 ns 160.0 ns 240.0 ns 320.0 ns 400.0 ns 480.0 ns 560.0 ns 640.0 ns 720.0 ns 800.0 ns 880.0 ns 960.0 ns
0 ps
5000AAAA
00000000
0000AAAA
0000AAAB
0000AAAC
0000AAAD
0000AAAE
0000AAAF
0%
00:00:00
Quartus Prime Standar...
Simulation Waveform ...
Simulation Waveform ...

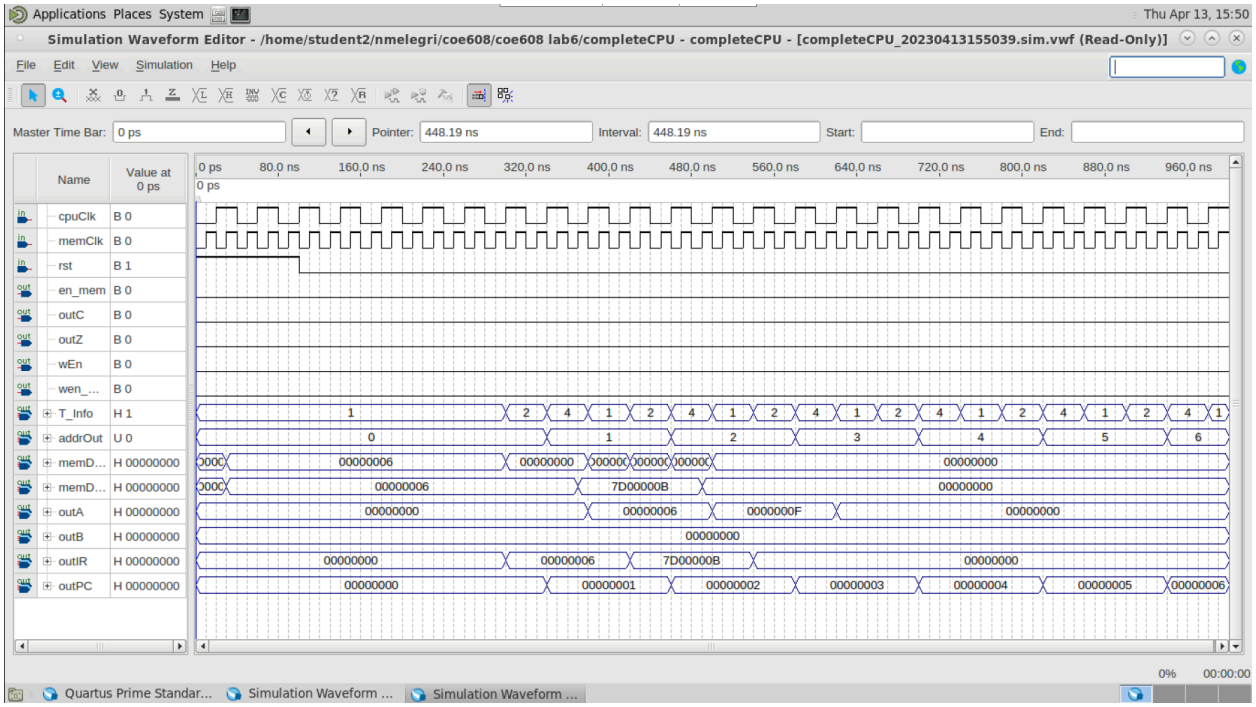
ANDI


Applications Places System
Thu Apr 13, 15:44
Simulation Waveform Editor - /home/student2/nmelegri/coe608/coe608 lab6/completeCPU - completeCPU - [completeCPU_20230413154031.sim.vwf (Read-Only)]
File Edit View Simulation Help
Search altera.com
Master Time Bar: 0 ps
Pointer: 413.71 ns
Interval: 413.71 ns
Start:
End:
Name
Value at 0 ps
cpuClk B 0
memClk B 0
rst B 1
en_mem B 0
outC B 0
outZ B 0
wEn B 0
wen_... B 0
T_Info H 1
addrOut U 0
memD... H 00000000
memD... H 00000000
outA H 00000000
outB H 00000000
outIR H 00000000
outPC H 00000000
0 ps 80,0 ns 160,0 ns 240,0 ns 320,0 ns 400,0 ns 480,0 ns 560,0 ns 640,0 ns 720,0 ns 800,0 ns 880,0 ns 960,0 ns
0%
00:00:00
Quartus Prime Standar...
Simulation Waveform ...
Simulation Waveform ...

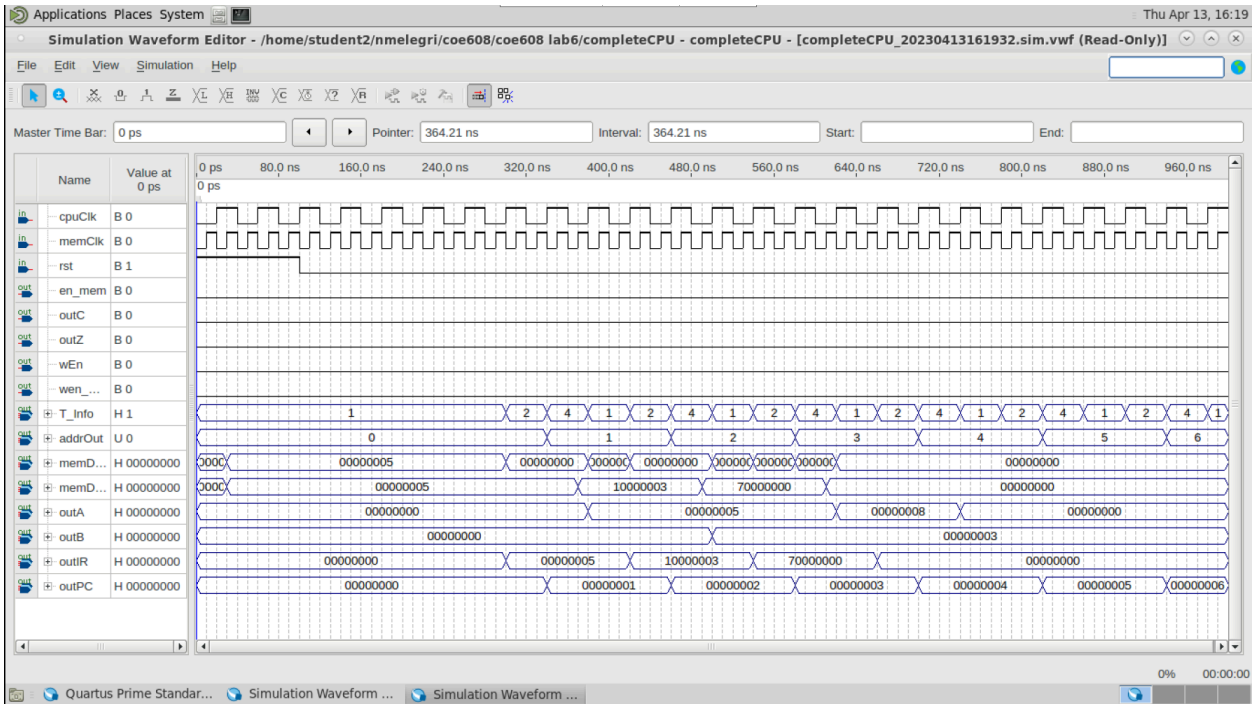
ADDI


Applications Places System
Thu Apr 13, 15:46
Simulation Waveform Editor - /home/student2/nmelegri/coe608/coe608 lab6/completeCPU - completeCPU - [completeCPU_20230413154637.sim.vwf (Read-Only)]
File Edit View Simulation Help
Search altera.com
Master Time Bar: 0 ps
Pointer: 414.6 ns
Interval: 414.6 ns
Start: 0 ps
End: 1.0 us
Name
Value at 0 ps
cpuClk B 0
memClk B 0
rst B 1
en_mem B 0
outC B 0
outZ B 0
wEn B 0
wen_... B 0
T_Info H 1
addrOut U 0
memD... H 00000000
memD... H 00000000
outA H 00000000
outB H 00000000
outIR H 00000000
outPC H 00000000
0 ps 80,0 ns 160,0 ns 240,0 ns 320,0 ns 400,0 ns 480,0 ns 560,0 ns 640,0 ns 720,0 ns 800,0 ns 880,0 ns 960,0 ns
0%
00:00:00
Quartus Prime Standar...
Simulation Waveform ...
Simulation Waveform ...

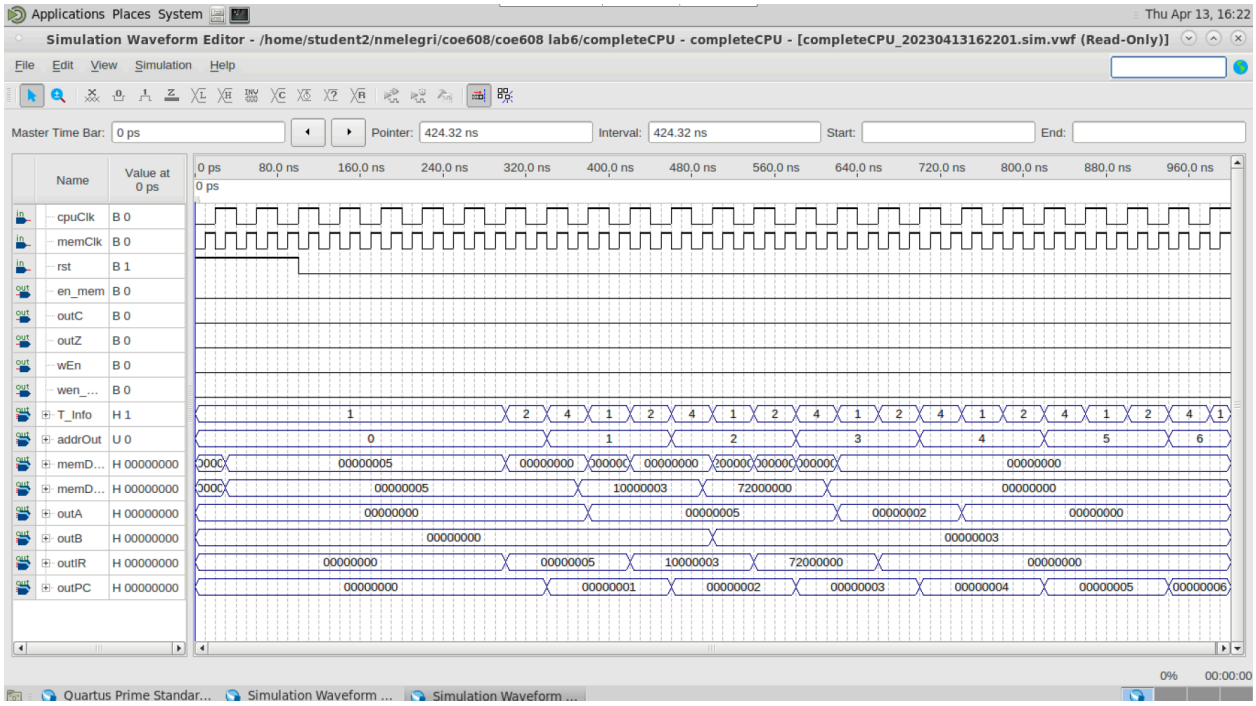
ORI


Applications Places System
Thu Apr 13, 15:50
Simulation Waveform Editor - /home/student2/nmelegri/coe608/coe608 lab6/completeCPU - completeCPU - [completeCPU_20230413155039.sim.vwf (Read-Only)]
File Edit View Simulation Help
Master Time Bar: 0 ps
Pointer: 448.19 ns
Interval: 448.19 ns
Start:
End:
Name
Value at 0 ps
cpuClk B 0
memClk B 0
rst B 1
en_mem B 0
outC B 0
outZ B 0
wEn B 0
wen_... B 0
T_Info H 1
addrOut U 0
memD... H 00000000
memD... H 00000000
outA H 00000000
outB H 00000000
outIR H 00000000
outPC H 00000000
0 ps 80,0 ns 160,0 ns 240,0 ns 320,0 ns 400,0 ns 480,0 ns 560,0 ns 640,0 ns 720,0 ns 800,0 ns 880,0 ns 960,0 ns
Quartus Prime Standar...
Simulation Waveform ...
Simulation Waveform ...
0%
00:00:00

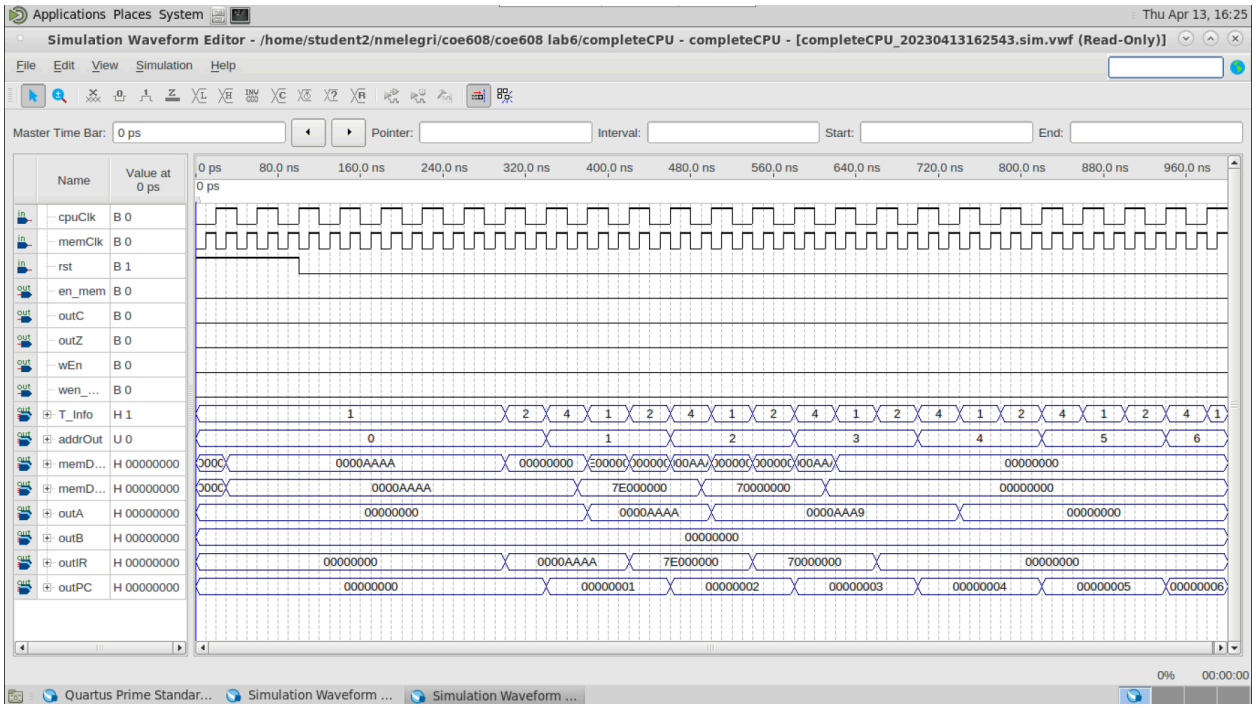
ADD


Applications Places System
Thu Apr 13, 16:19
Simulation Waveform Editor - /home/student2/nmelegri/coe608/coe608 lab6/completeCPU - completeCPU - [completeCPU_20230413161932.sim.vwf (Read-Only)]
File Edit View Simulation Help
Master Time Bar: 0 ps
Pointer: 364.21 ns
Interval: 364.21 ns
Start:
End:
Name
Value at 0 ps
cpuClk B 0
memClk B 0
rst B 1
en_mem B 0
outC B 0
outZ B 0
wEn B 0
wen_... B 0
T_Info H 1
addrOut U 0
memD... H 00000000
memD... H 00000000
outA H 00000000
outB H 00000000
outIR H 00000000
outPC H 00000000
0 ps 80,0 ns 160,0 ns 240,0 ns 320,0 ns 400,0 ns 480,0 ns 560,0 ns 640,0 ns 720,0 ns 800,0 ns 880,0 ns 960,0 ns
Quartus Prime Standar...
Simulation Waveform ...
Simulation Waveform ...
0%
00:00:00

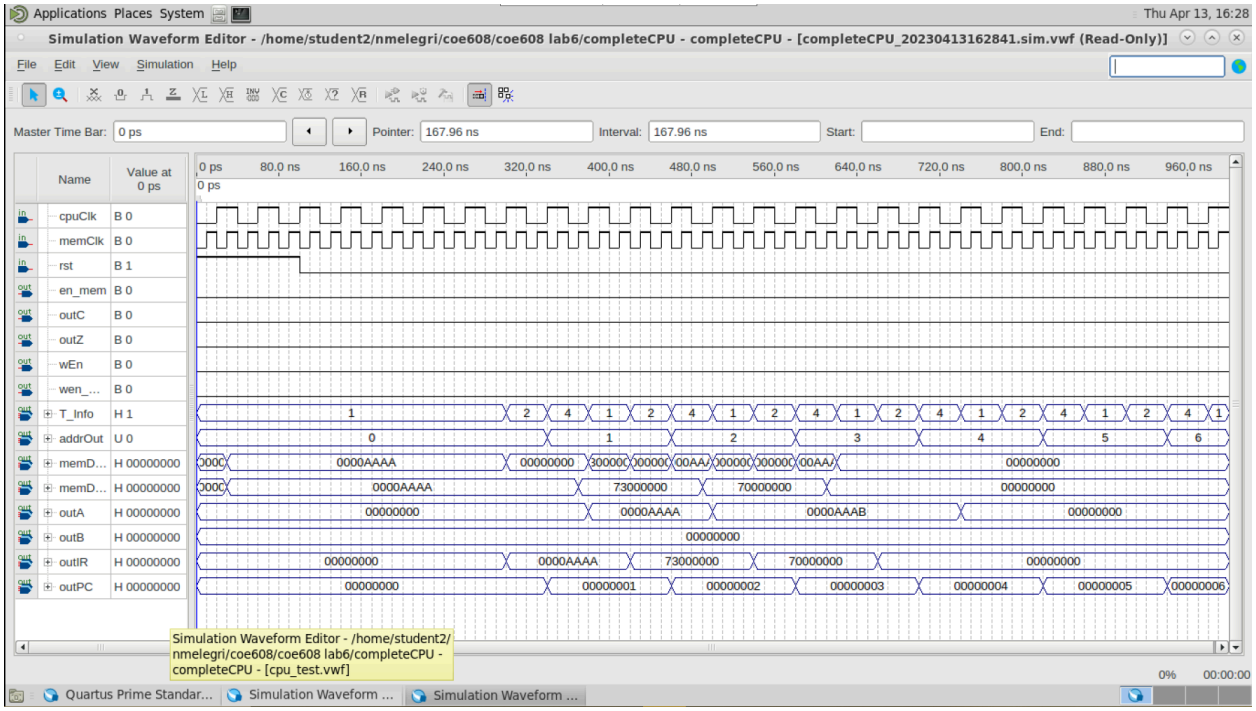
SUB


Applications Places System
Thu Apr 13, 16:22
Simulation Waveform Editor - /home/student2/nmelegri/coe608/coe608 lab6/completeCPU - completeCPU - [completeCPU_20230413162201.sim.vwf (Read-Only)]
File Edit View Simulation Help
Master Time Bar: 0 ps
Pointer: 424.32 ns
Interval: 424.32 ns
Start:
End:
Name
Value at 0 ps
cpuClk B 0
memClk B 0
rst B 1
en_mem B 0
outC B 0
outZ B 0
wEn B 0
wen_... B 0
T_Info H 1
addrOut U 0
memD... H 00000000
memD... H 00000000
outA H 00000000
outB H 00000000
outIR H 00000000
outPC H 00000000
0 ps 80,0 ns 160,0 ns 240,0 ns 320,0 ns 400,0 ns 480,0 ns 560,0 ns 640,0 ns 720,0 ns 800,0 ns 880,0 ns 960,0 ns
Quartus Prime Standar...
Simulation Waveform ...
Simulation Waveform ...
0%
00:00:00

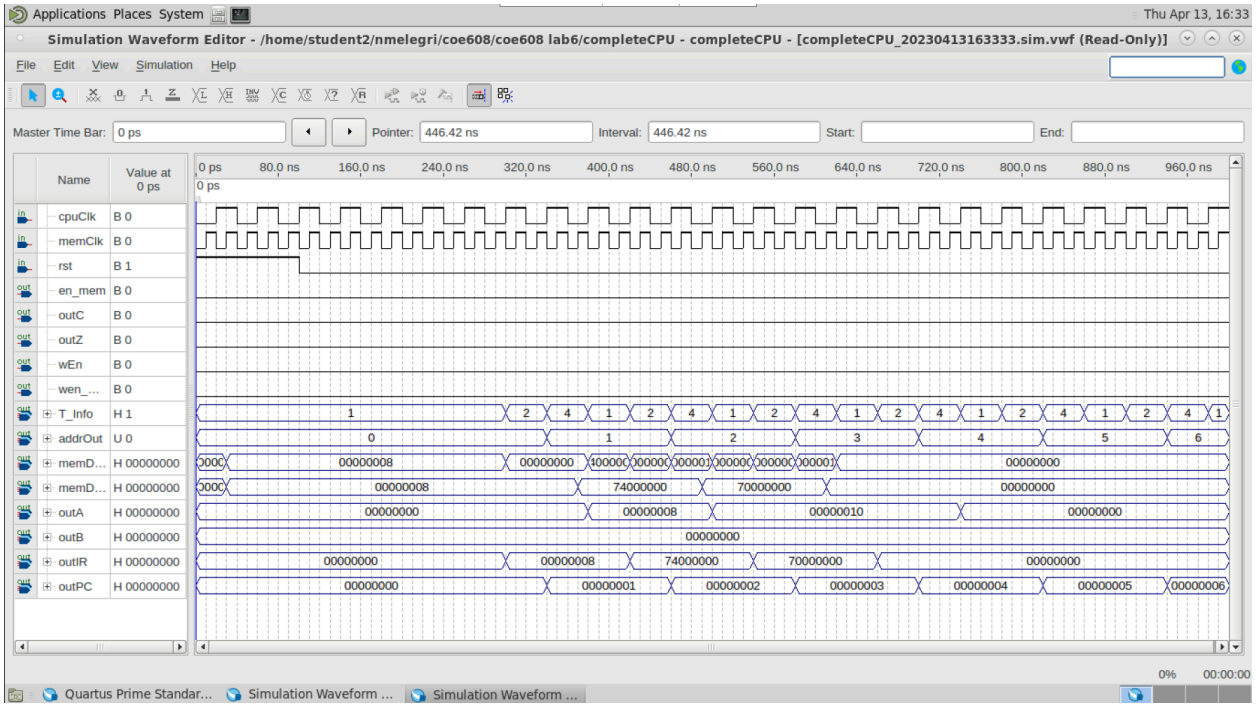
DECA


Applications Places System
Thu Apr 13, 16:25
Simulation Waveform Editor - /home/student2/nmelegri/coe608/coe608 lab6/completeCPU - completeCPU - [completeCPU_20230413162543.sim.vwf (Read-Only)]
File Edit View Simulation Help
Master Time Bar: 0 ps
Pointer:
Interval:
Start:
End:
Name
Value at 0 ps
cpuClk B 0
memClk B 0
rst B 1
en_mem B 0
outC B 0
outZ B 0
wEn B 0
wen_... B 0
T_Info H 1
addrOut U 0
memD... H 00000000
memD... H 00000000
outA H 00000000
outB H 00000000
outIR H 00000000
outPC H 00000000
0 ps 80,0 ns 160,0 ns 240,0 ns 320,0 ns 400,0 ns 480,0 ns 560,0 ns 640,0 ns 720,0 ns 800,0 ns 880,0 ns 960,0 ns
Quartus Prime Standar...
Simulation Waveform ...
Simulation Waveform ...
0%
00:00:00

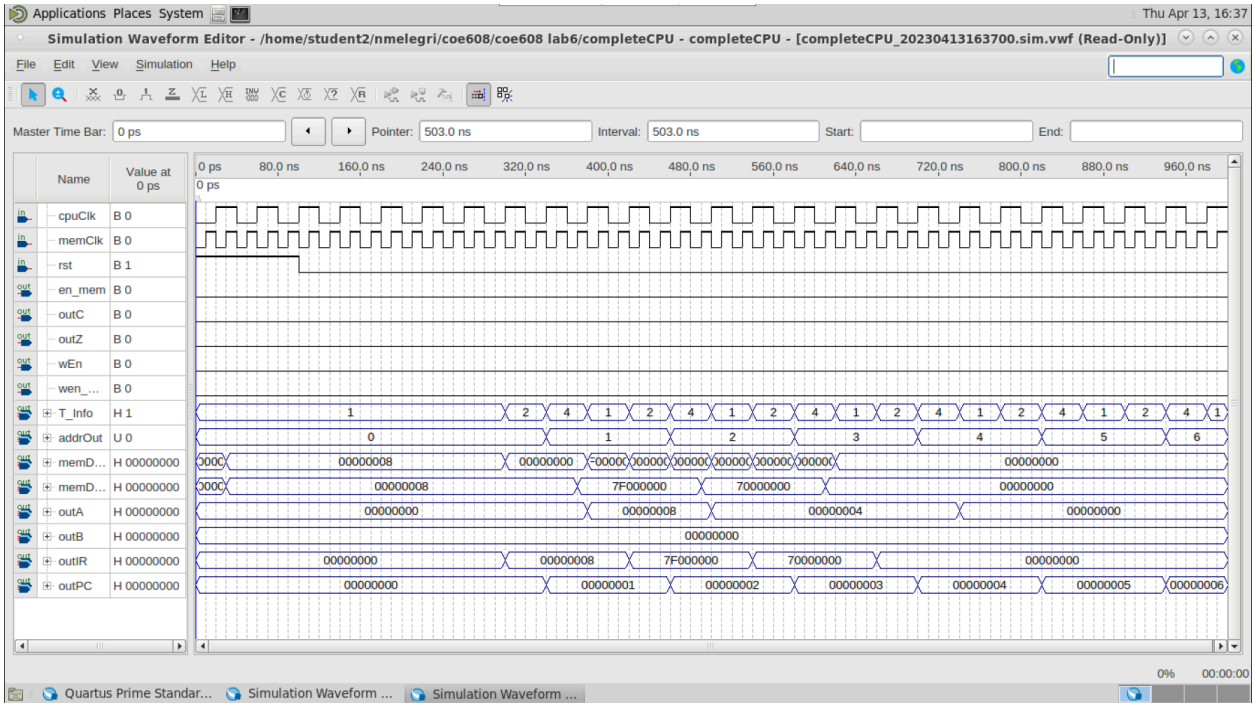
INCA


Applications Places System
Thu Apr 13, 16:28
Simulation Waveform Editor - /home/student2/nmelegri/coe608/coe608 lab6/completeCPU - completeCPU - [completeCPU_20230413162841.sim.vwf (Read-Only)]
File Edit View Simulation Help
Master Time Bar: 0 ps
Pointer: 167.96 ns
Interval: 167.96 ns
Start:
End:
Name
Value at 0 ps
cpuClk B 0
memClk B 0
rst B 1
en_mem B 0
outC B 0
outZ B 0
wEn B 0
wen_... B 0
T_Info H 1
addrOut U 0
memD... H 00000000
memD... H 00000000
outA H 00000000
outB H 00000000
outIR H 00000000
outPC H 00000000
0 ps 80.0 ns 160.0 ns 240.0 ns 320.0 ns 400.0 ns 480.0 ns 560.0 ns 640.0 ns 720.0 ns 800.0 ns 880.0 ns 960.0 ns
Simulation Waveform Editor - /home/student2/nmelegri/coe608/coe608 lab6/completeCPU - completeCPU - [cpu_test.vwf]
0%
00:00:00
Quartus Prime Standar...
Simulation Waveform ...
Simulation Waveform ...

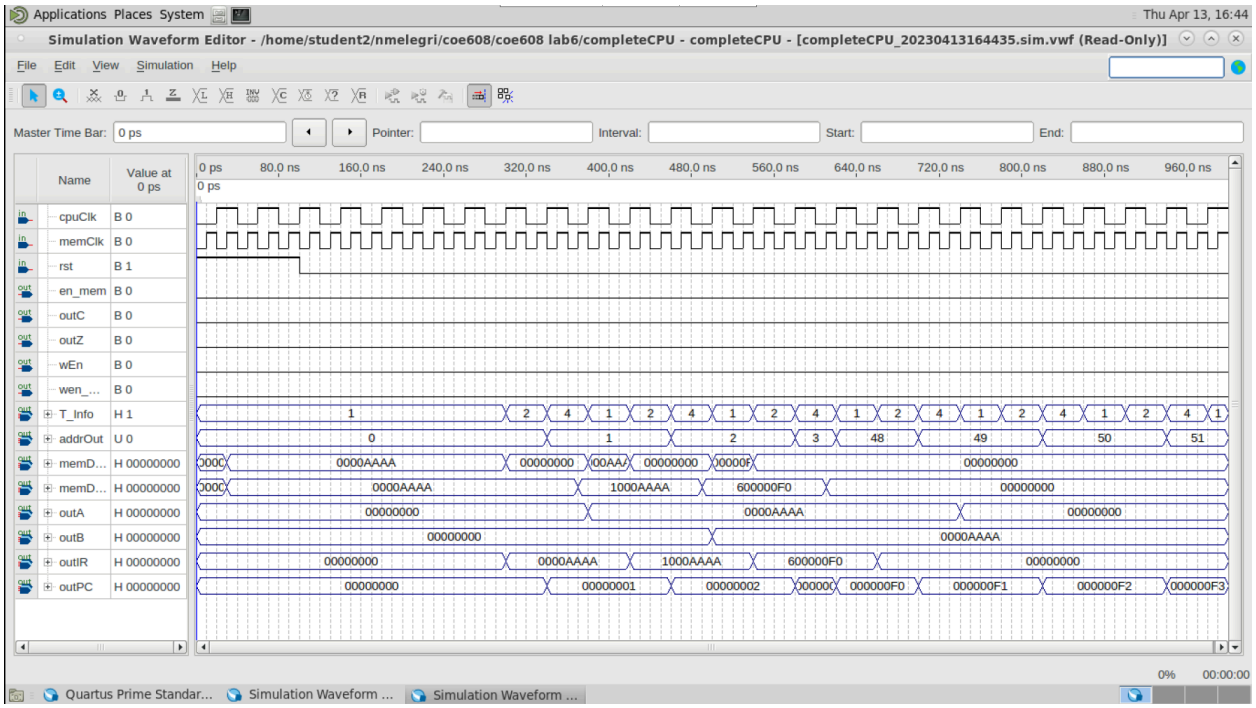
ROL


Applications Places System
Thu Apr 13, 16:33
Simulation Waveform Editor - /home/student2/nmelegri/coe608/coe608 lab6/completeCPU - completeCPU - [completeCPU_20230413163333.sim.vwf (Read-Only)]
File Edit View Simulation Help
Master Time Bar: 0 ps
Pointer: 446.42 ns
Interval: 446.42 ns
Start:
End:
Name
Value at 0 ps
cpuClk B 0
memClk B 0
rst B 1
en_mem B 0
outC B 0
outZ B 0
wEn B 0
wen_... B 0
T_Info H 1
addrOut U 0
memD... H 00000000
memD... H 00000000
outA H 00000000
outB H 00000000
outIR H 00000000
outPC H 00000000
0 ps 80.0 ns 160.0 ns 240.0 ns 320.0 ns 400.0 ns 480.0 ns 560.0 ns 640.0 ns 720.0 ns 800.0 ns 880.0 ns 960.0 ns
0%
00:00:00
Quartus Prime Standar...
Simulation Waveform ...
Simulation Waveform ...

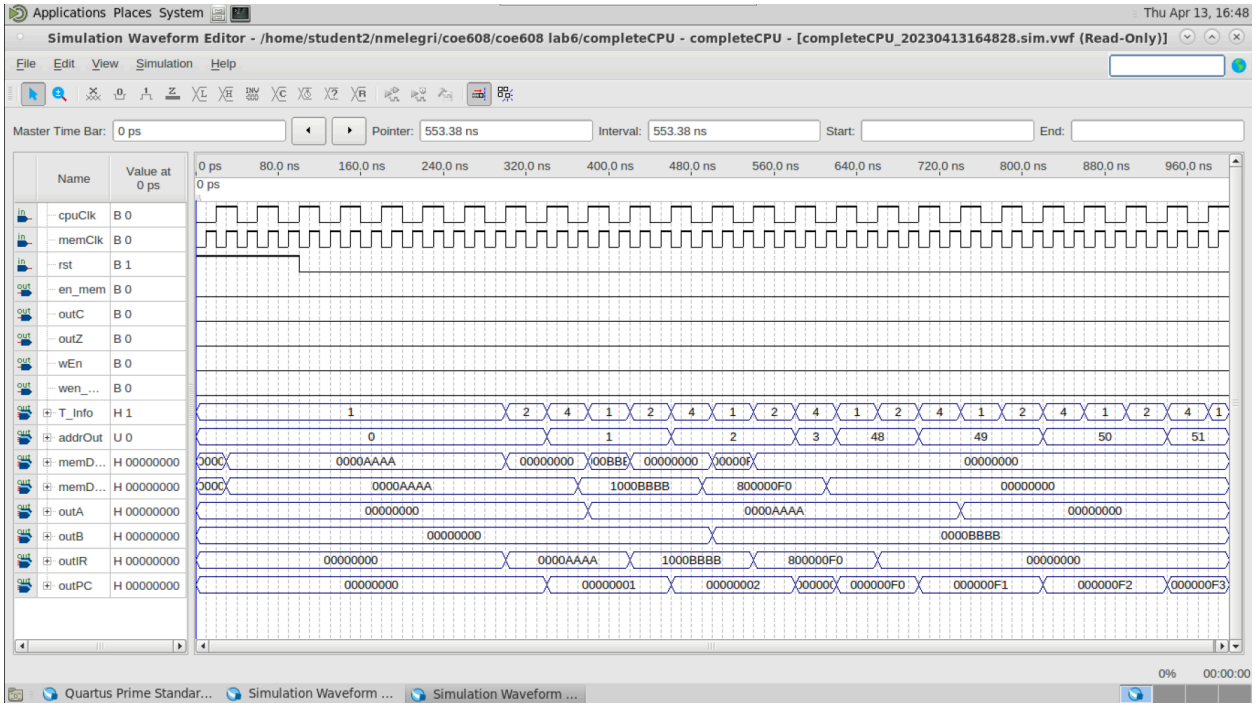
ROR


Applications Places System
Thu Apr 13, 16:37
Simulation Waveform Editor - /home/student2/nmelegri/coe608/coe608 lab6/completeCPU - completeCPU - [completeCPU_20230413163700.sim.vwf (Read-Only)]
File Edit View Simulation Help
Master Time Bar: 0 ps
Pointer: 503.0 ns
Interval: 503.0 ns
Start:
End:
Name
Value at 0 ps
cpuClk B 0
memClk B 0
rst B 1
en_mem B 0
outC B 0
outZ B 0
wEn B 0
wen_... B 0
T_Info H 1
addrOut U 0
memD... H 00000000
memD... H 00000000
outA H 00000000
outB H 00000000
outIR H 00000000
outPC H 00000000
0 ps 80.0 ns 160.0 ns 240.0 ns 320.0 ns 400.0 ns 480.0 ns 560.0 ns 640.0 ns 720.0 ns 800.0 ns 880.0 ns 960.0 ns
0%
00:00:00
Quartus Prime Standar...
Simulation Waveform ...
Simulation Waveform ...

BEQ


Applications Places System
Thu Apr 13, 16:44
Simulation Waveform Editor - /home/student2/nmelegri/coe608/coe608 lab6/completeCPU - completeCPU - [completeCPU_20230413164435.sim.vwf (Read-Only)]
File Edit View Simulation Help
Master Time Bar: 0 ps
Pointer:
Interval:
Start:
End:
Name
Value at 0 ps
cpuClk B 0
memClk B 0
rst B 1
en_mem B 0
outC B 0
outZ B 0
wEn B 0
wen_... B 0
T_Info H 1
addrOut U 0
memD... H 00000000
memD... H 00000000
outA H 00000000
outB H 00000000
outIR H 00000000
outPC H 00000000
0 ps 80.0 ns 160.0 ns 240.0 ns 320.0 ns 400.0 ns 480.0 ns 560.0 ns 640.0 ns 720.0 ns 800.0 ns 880.0 ns 960.0 ns
0%
00:00:00
Quartus Prime Standar...
Simulation Waveform ...
Simulation Waveform ...

BNE


Applications Places System
Thu Apr 13, 16:48
Simulation Waveform Editor - /home/student2/nmelegri/coe608/coe608 lab6/completeCPU - completeCPU - [completeCPU_20230413164828.sim.vwf (Read-Only)]
File Edit View Simulation Help
Master Time Bar: 0 ps
Pointer: 553.38 ns
Interval: 553.38 ns
Start:
End:
Name
Value at 0 ps
cpuClk B 0
memClk B 0
rst B 1
en_mem B 0
outC B 0
outZ B 0
wEn B 0
wen_... B 0
T_Info H 1
addrOut U 0
memD... H 00000000
memD... H 00000000
outA H 00000000
outB H 00000000
outIR H 00000000
outPC H 00000000
0 ps 80,0 ns 160,0 ns 240,0 ns 320,0 ns 400,0 ns 480,0 ns 560,0 ns 640,0 ns 720,0 ns 800,0 ns 880,0 ns 960,0 ns
0 ps
0%
00:00:00
Quartus Prime Standar...
Simulation Waveform ...
Simulation Waveform ...