MBARARA UNIVERSITY OF SCIENCE &
TECHNOLOGY.
FACULTY OF COMPUTING & INFORMATICS
END OF SEMESTER II EXAMINATION 2021/2022

PROGRAMME: BSE
YEAR OF STUDY: I
COURSE NAME: Computer Organization & Architecture
COURSE CODE: SWE1206
DURATION: Three Hours
TIME: 9:00 P.M. – 12:00 NOON.
DATE: $11^{th}$ OCTOBER 2022

## EXAMINATION INSTRUCTIONS

1. THE PAPER CONTAINS TWO SECTIONS: SECTION A AND B.
2. ATTEMPT ALL QUESTIONS IN SECTION A (40 MARKS).
3. ATTEMPT ANY THREE (03) QUESTIONS IN SECTION B (60 MARKS).
4. BEGIN EACH QUESTION OF SECTION B ON A NEW PAGE.
5. THIS IS NOT AN OPEN BOOK EXAMINATION- CANDIDATES SHOULD NOT CONSULT ANY REFERENCE MATERIAL DURING THIS SITTING.
6. ANY FORM OF EXAMINATION MALPRACTICE IS PROHIBITED AND WHEN COMMITTED, EXAMINATION REGULATIONS SECTION 2.4.9 SHALL BE APPLIED.
7. DO NOT OPEN THIS EXAM UNTIL YOU ARE TOLD TO DO SO.
8. ALL ROUGH WORK SHOULD BE IN YOUR ANSWER BOOKLET, DO NOT WRITE ANYTHING ON THIS QUESTION PAPER.

## Section A (40 marks)

1. Distinguish between Computer Organization and Computer Architecture? (2 Marks)
2. What do you understand by each of the following concepts? (2 Marks each)
   (i) Transducer.
   (ii) Memory Management Unit.
   (iii) Integrated circuits.
   (iv) Instruction set design.
3. Computer Memory is said to be made of a hierarchy; with the help of a diagram briefly describe what this hierarchy is. (3 Marks)
4. What is the difference between a cache hit and a cache miss? What happens when a cache hit occurs. (4 Marks)
5. Suppose that the tag of the address of the word stored in cache memory is 1011 while the index of the word is 011. Calculate the main memory address from which this word was obtained. (3 Marks)
6. How is EPROM different from EEPROM? (2 Marks)
7. Mention two salient features each of the second and third generation computers invented in 1957 and 1958 respectively. (4 Marks)
8. Explain Amdahl's and Moore's law as used in computer evolution and performance. (4 Marks)
9. What is the distinction between computer structure and computer function? (2 Marks)
10. Using Venn diagrams, briefly explain how the hamming code algorithm can be used for error detection and error correction. (4 Marks)
11. When designing computers, why can't one just connect the peripheral devices directly to the system bus? (4 Marks)

## Section B (60 marks)

### Question 1

(a) Explain the differences between the following concepts

(i) Direct addressing mode & Register addressing. (2 Marks)

(ii) Cylinder, sector, track & RAID as used in external memory. (4 Marks)

(b) Suppose an 8-bit data word stored in memory is 11001011. Using the Hamming algorithm, determine the check bits that would be stored in memory along with the data word. Show how you got your answer. (8 Marks)

(c) For the 8-bit word 00111001, the check bits stored with it would be 0111. Suppose when the word is read from memory, the check bits are calculated to be 1101. What is the data word that was read from memory? (6 Marks)

### Question 2

(a) Write-through cache policy solves the problem of inconsistency by forcing all writes to update both the cache and the main memory. However, there is still a problem with this technique.

(i) Briefly discuss what the problem with the write-through cache policy.(3 Marks)

(ii) Explain a solution to this problem based on the write back approach.(3 Marks)

(b) If cache memory contains 8 blocks and is using the 2-way set associative mapping, in which set and block would data from main memory address 20 be placed. (6 Marks)

(c) Why are replacement algorithms needed when using associative and set-associative techniques to write data to cache memory? (4 Marks)

(d) Explain the difference between the least recently used and the least frequently used replacement algorithms. (4 Marks)

### Question 3

(a) In a computer structure, there can be multiple I/O modules attached to the processor. When a processor receives multiple interrupts, discuss two ways in which the processor can determine which device issued the interrupt. (4 Marks)

(b) Explain the problems with Interrupt-driven I/O over DMA. (4 Marks)

(c) When a DMA module takes control of a bus, and while it retains control of the bus, what does the processor do? (6 Marks)

(d) When the processor wishes to read or write a block of data, it issues a command to the DMA module by sending it information. Discuss what is contained in the information sent to the DMA module. (6 Marks)

## Question 4

(a) With the help of a diagram, explain the main elements of a machine instruction. (6 Marks)

(b) Discuss four areas where source and result operands can be located. (4 Marks)

(c) Consider a high-level language instruction

$$Z = \frac{A + B}{C - (D * E)}$$

expressed in a language such as FORTRAN. Write a two-address machine instruction that can be used to compute the value of $Z$. (Use appropriate temporary locations where needed.) (10 Marks)

## Question 5

(a) Distinguish between Associative Mapping and Set Associative Mapping. (4 Marks)

(b) Using Cache-Memory Mapping, Consider a memory of 32 blocks (labeled 0 through 31) and a cache of 8 blocks (labeled 0 through 7).

(i) Under direct mapping, which blocks of memory contend for block 2 of the cache? (3 Marks)

(ii) Under 4-way set associativity, to which blocks of cache may element 31 of memory go? (4 Marks).

(c) Discuss the Four memory types of accessing units of data in a computer system. (4 Marks)

(d) A PDP-11 instruction $ADDA, B$ results in the following sequence of states: $iac, if, iod, oac, of, oac, of, do, oac, os$. Where *iac* stands for instruction address calculation, *if*; instruction fetch, *iod*; instruction operation decoding, *oac*; operation address calculation, *of*; operand fetch, *do*; data operation and *os*; operand store. Draw the instruction state cycle diagram for the PDP processor. (5 Marks)