CHAPTER 4: CACHE MEMORY

TRUE OR FALSE

T F 1. No single technology is optimal in satisfying the memory requirements for a computer system.

T F 2. A typical computer system is equipped with a hierarchy of memory subsystems, some internal to the system and some external.

T F 3. External memory is often equated with main memory.

T F 4. The processor requires its own local memory.

T F 5. Cache is not a form of internal memory.

T F 6. The *unit of transfer* must equal a word or an addressable unit.

T F 7. Both sequential access and direct access involve a shared read-write mechanism.

T F 8. In a volatile memory, information decays naturally or is lost when electrical power is switched off.

T F 9. To achieve greatest performance the memory must be able to keep up with the processor.

T F 10. Secondary memory is used to store program and data files and is usually visible to the programmer only in terms of individual bytes or words.

T F 11. The L1 cache is slower than the L3 cache.

T F 12. With *write back* updates are made only in the cache.

T F 13. It has become possible to have a cache on the same chip as the processor.

T F 14. All of the Pentium processors include two on-chip L1 caches, one for data and one for instructions.

T F 15. Cache design for HPC is the same as that for other hardware platforms and applications.

MULTIPLE CHOICE

1. _____ refers to whether memory is internal or external to the computer.

   A. Location B. Access

   C. Hierarchy D. Tag

2. Internal memory capacity is typically expressed in terms of _____.

   A. hertz B. nanos

   C. bytes D. LOR

3. For internal memory, the _____ is equal to the number of electrical lines into and out of the memory module.

   A. access time B. unit of transfer

   C. capacity D. memory ratio

4. "Memory is organized into records and access must be made in a specific linear sequence" is a description of _____.

   A. sequential access B. direct access

   C. random access D. associative

5. individual blocks or records have a unique address based on physical location with _____.

   A. associative B. physical access

   C. direct access D. sequential access

6. For random-access memory, _____ is the time from the instant that an address is presented to the memory to the instant that data have been stored or made available for use.

   A. memory cycle time B. direct access

   C. transfer rate D. access time

7. The _____ consists of the access time plus any additional time required before a second access can commence.

   A. latency B. memory cycle time

   C. direct access D. transfer rate

8. A portion of main memory used as a buffer to hold data temporarily that is to be read out to disk is referred to as a _____.

   A. disk cache B. latency

   C. virtual address D. miss

9. A line includes a _____ that identifies which particular block is currently being stored.

   A. cache B. hit

   C. tag D. locality

10. _____ is the simplest mapping technique and maps each block of main memory into only one possible cache line.

    A. Direct mapping B. Associative mapping

    C. Set associative mapping D. None of the above

11. When using the _____ technique all write operations made to main memory are made to the cache as well.

    A. write back B. LRU

    C. write through D. unified cache

12. The key advantage of the _____ design is that it eliminates contention for the cache between the instruction fetch/decode unit and the execution unit.

    A. logical cache B. split cache

    C. unified cache D. physical cache

13. The Pentium 4 _____ component executes micro-operations, fetching the required data from the L1 data cache and temporarily storing results in registers.

    A. fetch/decode unit B. out-of-order execution logic

    C. execution unit D. memory subsystem

14. In reference to access time to a two-level memory, a _____ occurs if an accessed word is not found in the faster memory.

    A. miss B. hit

    C. line D. tag

15. A logical cache stores data using _____.

    A. physical addresses B. virtual addresses

    C. random addresses D. none of the above

SHORT ANSWER

1. _____ memory consists of peripheral storage devices, such as disk and tape.

2. One byte equals _____ bits.

3. From a user's point of view the two most important characteristics of memory are capacity and _____.

4. The three performance parameters for memory are: access time, transfer rate, and _____.

5. _____ is a random access type of memory that enables one to make a comparison of desired bit locations within a word for a specified match, and to do this for all words simultaneously, thus retrieving a word based on a portion of its contents rather than its address.

6. The _____ rate is the rate at which data can be transferred into or out of a memory unit.

7. The most commonly used physical types of memory are: semiconductor memory, _____ memory (used for disk and tape), and optical and magneto-optical.

8. The three key characteristics of memory are capacity, access time, and _____.

9. External, nonvolatile memory is referred to as _____ or auxiliary memory.

10. The cache consists of blocks called _____.

11. _____ computing deals with super computers and their software.

12. The Pentium 4 processor core consists of four major components: fetch/decode unit, out-of-order execution logic, memory subsystem, and _____.

13. An interesting feature of the _____ architecture is the use of a small first-in-first-out (FIFO) write buffer to enhance memory write performance.

14. _____ memory is a facility that allows programs to address memory from a logical point of view, without regard to the amount of main memory physically available.

15. For set-associative mapping the cache control logic interprets a memory address as three fields: Set, Word, and _____.

TRUE OR FALSE

1. T	2. T
3. F	4. T
5. F	6. F
7. T	8. T
9. T	10. F
11. F	12. T
13. T	14. T
15. F	16.

MULTIPLE CHOICE

1. A	2. C
3. B	4. A
5. C	6. D
7. B	8. A
9. C	10. A
11. C	12. B
13. C	14. A
15. B	16.

SHORT ANSWER

1.	External	2.	8
3.	performance	4.	memory cycle time
5.	Associative	6.	transfer
7.	magnetic surface	8.	cost
9.	secondary	10.	lines
11.	High-performance	12.	execution units
13.	ARM	14.	Virtual
15.	Tag	16.	