Final Exam – 2021-2022 – Model2

1. The _____ stores data.
(a) system bus (b) I/O (c) main memory (d) control unit

2. The _____ moves data between the computer and its external environment.
(a) data transport (b) I/O (c) register (d) CPU interconnection

3. _____ provide storage internal to the CPU.
(a) Control units (b) ALUs (c) Main memory (d) Registers

4. The _____ performs the computer's data processing functions.
(a) Register (b) CPU interconnection (c) ALU (d) system bus

5. A _____ is a mechanism that provides for communication among CPU, main memory, and I/O.
(a) system interconnection (b) CPU interconnection (c) peripheral (d) processor

6. Computer technology is changing at a _____ pace.
(a) slow (b) slow to medium (c) rapid (d) non-existent

7. It is a(n) _____ design issue whether a computer will have a multiply instruction.
(a) architectural (b) memory (c) elementary (d) organizational

8. It is a(n) _____ issue whether the multiply instruction will be implemented by a special multiply unit or by a mechanism that makes repeated use of the add unit of the system.
(a) architectural (b) memory (c) mechanical (d) organizational

9. _____ attributes include hardware details transparent to the programmer.
(a) Interface (b) Organizational (c) Memory (d) Architectural

10. When data are moved over longer distances, to or from a remote device, the process is known as_____.
(a) data communications (b) registering (c)structuring (d) data transport

11. The _____ is a relatively small fast memory interposed between a larger, slower memory and the logic that accesses the larger memory.
(a) peripheral (b) cache (c) processor (d) arithmetic and logic unit

12. An increase in clock rate means that individual operations are executed _____.
(a) the same (b) slower (c) with very little change (d) faster

13. A _____ is a core designed to perform parallel operations on graphics data.
(a) MIC (b) ALU (c) GPU (d) PGD

14. A(n) _____ mean is a good candidate for comparing the execution time performance of several systems.
(a) Geometric (b) Arithmetic (c) Harmonic (d) Evaluation

15. _____ law deals with the potential speedup of a program using multiple processors compared to a single processor.
(a) Moore's (b) Amdahl's (c) Little's (d) Murphy's

16. The ____ register is used to hold the word received from the memory.
(a) MBR (b) MAR (c) IR (d) IBR

17. The ____ register specifies the address in the memory of the word to be read or written.
(a) MBR (b) MAR (c) IR (d) IBR

18. The ____ register contains the address of the next instruction to be fetched
(a) IR (b) IBR (c) PC (d) AC

19. The ____ register is used to temporarily hold operands and results of the ALU
(a) IR (b) AC (c) IBR (d) MBR

20. The desktop application(s) that require the great power of today's microprocessor-based systems include_____.
(a) image processing (b) speech recognition (c) videoconferencing (d) all of the above

21. The von Neumann general-purpose architecture IAS is based on which concept?
(a) data and instructions are stored in a single read-write memory
(b) the contents of this memory are addressable by location
(c) execution occurs in a sequential fashion
(d) all of the above

22. A sequence of codes or instructions is called _____.

(a) a program (b) memory (c) an interconnect (d) a register

23. The processing required for a single instruction is called the _____ cycle.

(a) execute (b) fetch (c) storing (d) packet

Instructuion

24. A(n) _____ is generated by a failure such as power failure or memory parity error.

(a) timer interrupt (b) I/O interrupt (c) program interrupt (d) hardware failure interrupt

25. A(n) _____ is generated by some condition that occurs as a result of an instruction execution.

(a) timer interrupt (b) I/O interrupt (c) program interrupt (d) hardware failure interrupt

26. One increment, or pulse, of a clock is referred to as a _____.

(a) clock cycle (b) clock rate (c) clock speed (d) cycle time

clock speed

27. The number of clock cycles per second is known as _____.

(a) clock cycle (b) clock rate (c) performance (d) cycle time

28. The use of multiple processors on the same chip is referred to as _____ and provides the potential to increase performance without increasing the clock rate.

(a) multicore (b) GPU (c) data channels (d) MPC

29. Consider a task in which 40% of its time is consumed by operations that [illegible] takes 1 second on a single processor machine. Then the same task takes ____ seconds on an 8-processors machine.

(a) 0.6 (b) 0.4 (c) 0.6 + 0.4/8 (d) 0.4 + 0.6/8

$$\frac{1}{0.6 + \frac{0.4}{8}}$$

30. _____ enables a processor to work simultaneously on multiple instructions by performing a different phase for each of the multiple instructions at the same time.

(a) Pipelining (b) cashing (c) overclocking (d) programming

31. _____ refers to whether memory is internal or external to the computer.

(a) Location (b) Access (c) Hierarchy (d) Tag

32. Internal memory capacity is typically expressed in terms of _____.

(a) hertz (b) nanos (c) bytes (d) LOR

33. For internal memory, the _____ is equal to the number of electrical lines into and out of the memory module.

(a) access time (b) unit of transfer (c) capacity (d) memory ratio

34. "Memory is organized into records and access must be made in a specific linear sequence" is a description of _____.

(a) sequential access (b) direct access (c) random access (d) associative access

35. A cash line includes a _____ that identifies which particular block is currently being stored.

(a) register (b) hit (c) tag (d) locality

36. The interrupt that allows the operating system to perform functions on a regular basis is called_____.

(a) timer interrupt (b) I/O interrupt (c) program interrupt (d) hardware failure interrupt

[illegible] to designate the source or destination of the data on the data bus.

(c) control lines (d) address lines

37. The _____ are used to designate the source or destination of the data on the data bus.
(a) system lines (b) data lines (c) control lines (d) address lines

38. The data lines provide a path for moving data among system modules and are collectively called the
(a) control bus (b) address bus (c) data bus (d) system bus

39. The first part of the instruction cycle is called
(a) Fetch cycle (b) execution cycle (c) optimization cycle (d) cashing cycle

40. The interrupt is generated by an I/O controller to signal normal completion of an operation, request service from the processor, or to signal a variety of error conditions is called.
(a) timer interrupt (b) I/O interrupt (c) program interrupt (d) hardware failure interrupt

41. _____ is the simplest mapping function and maps each block of main memory into only one possible cache line.
(a) Direct mapping (b) Associative mapping
(c) Set associative mapping (d) None of the above

42. The mapping function that maps each block into any available cache line is called
(a) Direct mapping (b) Associative mapping
(c) Set associative mapping (d) None of the above

43. In the _____ policy all write operations made to main memory are made to the cache as well.
(a) write back (b) LRU (c) write through (d) unified cache

44. The _____ specifies the operation to be performed.
(a) source operand reference (b) opcode (c) next instruction reference
(d) processor register

45. If the instruction set of a computer includes 64 instructions, then the width of the opcode in the instruction format is at least 2^6
(a) 2 bits (b) 4 bits (c) 6 bits (d) 8 bits

46._____ instructions provide computational capabilities for processing number data.
(a) Boolean (b) Logic (c) Memory (c) Arithmetic

47. The collection of different instructions that the processor can execute is called the processor's _____.
(a) registers (b) memory (c) architecture (d) instruction set

48. In_____ the operands reside in the stack.
(a) 3-address instruction (b) 2-address instruction (c) 1-address instruction (d) 0-address instruction

49. The advantage of _____ addressing is that no memory reference other than the instruction fetch is required to obtain the operand.
(a) direct (b) immediate (c) register (d) stack

50. In the _____ addressing the instruction contains the address of the operand in the main memory.
(a) direct (b) immediate (c) register (d) stack

the operand is fetched using two memory references.
(d) stack

(c) register (d) stack

51. In the _____ addressing the operand is fetched using two memory references.
(a) direct (b) indirect (c) register (d) stack

52. In_____ the operands reside in the stack.
(a) 3-address instruction (b) 2-address instruction (c) 1-address instruction (d) 0-address instruction

53. The basic function of a computer is to execute programs. (a) true (b) false
54. Interrupts do not improve processing efficiency. (a) true (b) false
55. An I/O module cannot exchange data directly with the processor. (a) true (b) false
56. Program execution consists of repeating the process of instruction fetch and instruction execution. (a) true (b) false

DMA 57. The function of the address bus is to transfer data between CPU and I/O. (a) true (b) false
58. The instruction that causes a division by zero generates an I/O interrupt (a) true (b) false
59. Without using interrupts the program execution halts until the I/O operation is done. (a) true (b) false

60. The PC register is used to store the fetched instruction. (a) true (b) false
61. While an interrupt is handled, no other interrupts can be handled. (a) true (b) false
62. The speed of external memory is often equal to that of the internal memory. (a) true (b) false
63. Cache is a form of internal memory. (a) true (b) false
64. The address of the next instruction to be fetched must be explicit in the current instruction. (a) true (b) false

65. Memory references are slower than register references. (a) true (b) false
66. The computer memory is responsible of storing the data (a) true (b) false
67. The CPU consists only of the control unit (a) true (b) false
68. The registers exist in the main memory

69. Moving the data from the computer to the memory is done by I/O. (a) true (b) false

70. The multiplication operation is done by the I/O (a) true (b) false

71. The number of bits used to represent a data types an architectural attribute. (a) true (b) false

72. The first-generation computers were implemented using Transistors Vacuum (a) true (b) false

73. The 3rd -generation computers were implemented using integrated circuits. (a) true (b) false

74. Over years the cost of computer systems continues to rise. (a) true (b) false

75. Workstation systems cannot support highly sophisticated engineering and scientific applications. (a) true (b) false

76. The cache holds recently accessed data. (a) true (b) false

77. MIPS is a measure for the performance of a processor. (a) true (b) false

78. The overall execution time of a program is independent of the clock rate. (a) true (b) false

79. Operations performed by a processor, such as fetching an instruction, decoding the instruction, performing an arithmetic operation, and so on, are governed by a system clock. (a) true (b) false

80. According to Amdahl's law, using multiple processors instead of one slows down the execution. (a) true (b) false

Best wishes!