CHAPTER 3:
A TOP-LEVEL VIEW OF COMPUTER FUNCTION AND INTERCONNECTION

TRUE OR FALSE

T F 1. At a top level, a computer consists of CPU, memory, and I/O components.

T F 2. The basic function of a computer is to execute programs.

T F 3. Program execution consists of repeating the process of instruction fetch and instruction execution.

T F 4. Interrupts do not improve processing efficiency.

T F 5. An I/O module cannot exchange data directly with the processor.

T F 6. A key characteristic of a bus is that it is not a shared transmission medium.

T F 7. Computer systems contain a number of different buses that provide pathways between components at various levels of the computer system hierarchy.

T F 8. In general, the more devices attached to the bus, the greater the bus length and hence the greater the propagation delay.

T F 9. It is not possible to connect I/O controllers directly onto the system bus.

T F 10. The method of using the same lines for multiple purposes is known as *time multiplexing*.

T F 11. Timing refers to the way in which events are coordinated on the bus.

T F 12. With asynchronous timing the occurrence of events on the bus is determined by a clock.

T F 13. Because all devices on a synchronous bus are tied to a fixed clock rate, the system cannot take advantage of advances in device performance.

T F 14. The unit of transfer at the link layer is a *phit* and the unit transfer

at the physical layer is a *flit.*

T F 15. A key requirement for PCIe is high capacity to support the needs of higher data rate I/O devices such as Gigabit Ethernet.

MULTIPLE CHOICE

1. Virtually all contemporary computer designs are based on concepts developed by _____ at the Institute for Advanced Studies, Princeton.

   A. John Maulchy B. John von Neumann

   C. Herman Hollerith D. John Eckert

2. The von Neumann architecture is based on which concept?

   A. data and instructions are stored in a single read-write memory

   B. the contents of this memory are addressable by location

   C. execution occurs in a sequential fashion

   D. all of the above

3. A sequence of codes or instructions is called _____.

   A. software B. memory

   C. an interconnect D. a register

4. The processing required for a single instruction is called a(n) _____ cycle.

   A. execute B. fetch

   C. instruction D. packet

5. A(n) _____ is generated by a failure such as power failure or memory parity error.

   A. I/O interrupt B. hardware failure interrupt

   C. timer interrupt D. program interrupt

6. A(n) _____ is generated by some condition that occurs as a result of an instruction execution.

A. timer interrupt B. I/O interrupt

C. program interrupt D. hardware failure interrupt

7. The interconnection structure must support which transfer?

   A. memory to processor

   B. processor to memory

   C. I/O to or from memory

   D. all of the above

8. A bus that connects major computer components (processor, memory, I/O) is called a _____.

   A. system bus B. address bus

   C. data bus D. control bus

9. The _____ are used to designate the source or destination of the data on the data bus.

   A. system lines B. data lines

   C. control lines D. address lines

10. The data lines provide a path for moving data among system modules and are collectively called the _____.

    A. control bus B. address bus

    C. data bus D. system bus

11. A _____ is the high-level set of rules for exchanging packets of data between devices.

    A. bus B. protocol

    C. packet D. QPI

12. Each data path consists of a pair of wires (referred to as a _____) that transmits data one bit at a time.

A. lane B. path

C. line D. bus

13. The _____ receives read and write requests from the software above the TL and creates request packets for transmission to a destination via the link layer.

A. transaction layer B. root layer

C. configuration layer D. transport layer

14. The TL supports which of the following address spaces?

A. memory

B. I/O

C. message

D. all of the above

15. The QPI _____ layer is used to determine the course that a packet will traverse across the available system interconnects.

A. link B. protocol

C. routing D. physical

SHORT ANSWER

1. A _____ register specifies the address in memory for the next read or write.

2. A _____ register contains the data to be written into memory or receives the data read from memory.

3. The most common classes of interrupts are: program, timer, I/O and _____.

4. A(n) _____ interrupt is generated by a timer within the processor and allows the operating system to perform certain functions on a regular basis.

5. A(n) _____ interrupt is generated by an I/O controller to signal normal completion of an operation, request service from the processor, or to signal a variety of error conditions.

6. A _____ interrupt simply means that the processor can and will ignore that interrupt request signal.

7. The collection of paths connecting the various modules is called the _____ structure.

8. A _____ is a communication pathway connecting two or more devices.

9. The _____ lines are used to control the access to and the use of the data and address lines.

10. Bus lines can be separated into two generic types: _____ and multiplexed.

11. With _____ timing the occurrence of one event on a bus follows and depends on the occurrence of a previous event.

12. With _____ transmission signals are transmitted as a current that travels down one conductor and returns on the other.

13. The QPI link layer performs two key functions: flow control and _____ control.

14. The _____ is a popular high-bandwidth, processor-independent bus that can function as a mezzanine or peripheral bus.

15. The _____ function is needed to ensure that a sending QPI entity does not overwhelm a receiving QPI entity by sending data faster than the receiver can process the data and clear buffers for more incoming data.

Answers

TRUE OR FALSE

1.	T	2.	T
3.	T	4.	F
5.	F	6.	F
7.	T	8.	T
9.	F	10.	T
11.	T	12.	F
13.	T	14.	F
15.	T		

MULTIPLE CHOICE

1.	B	2.	D

3.	A	4.	C
5.	B	6.	C
7.	D	8.	A
9.	D	10.	C
11.	B	12.	A
13.	A	14.	D
15.	C	16.	

SHORT ANSWER

1.	memory address (MAR)	2.	memory buffer (MBR)
3.	hardware failure	4.	timer
5.	I/O	6.	disabled
7.	interconnection	8.	bus
9.	control	10.	dedicated
11.	asynchronous	12.	balanced
13.	error	14.	peripheral component interconnect (PCI)
15.	flow control		