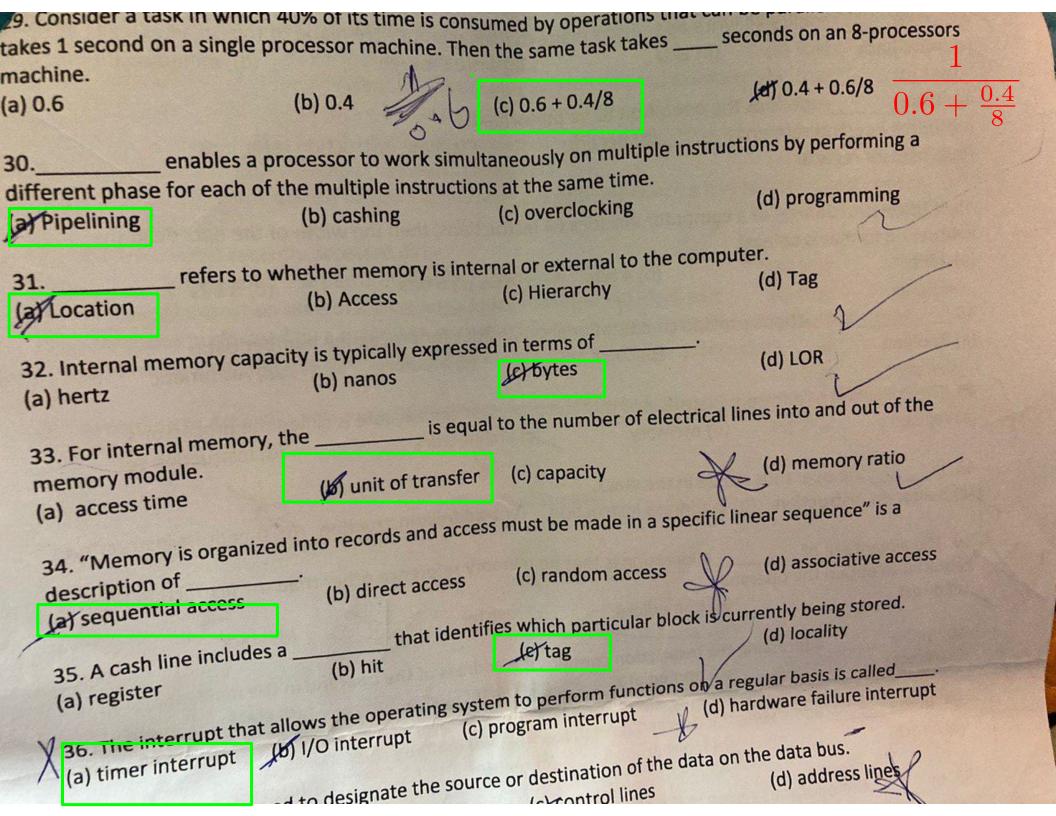
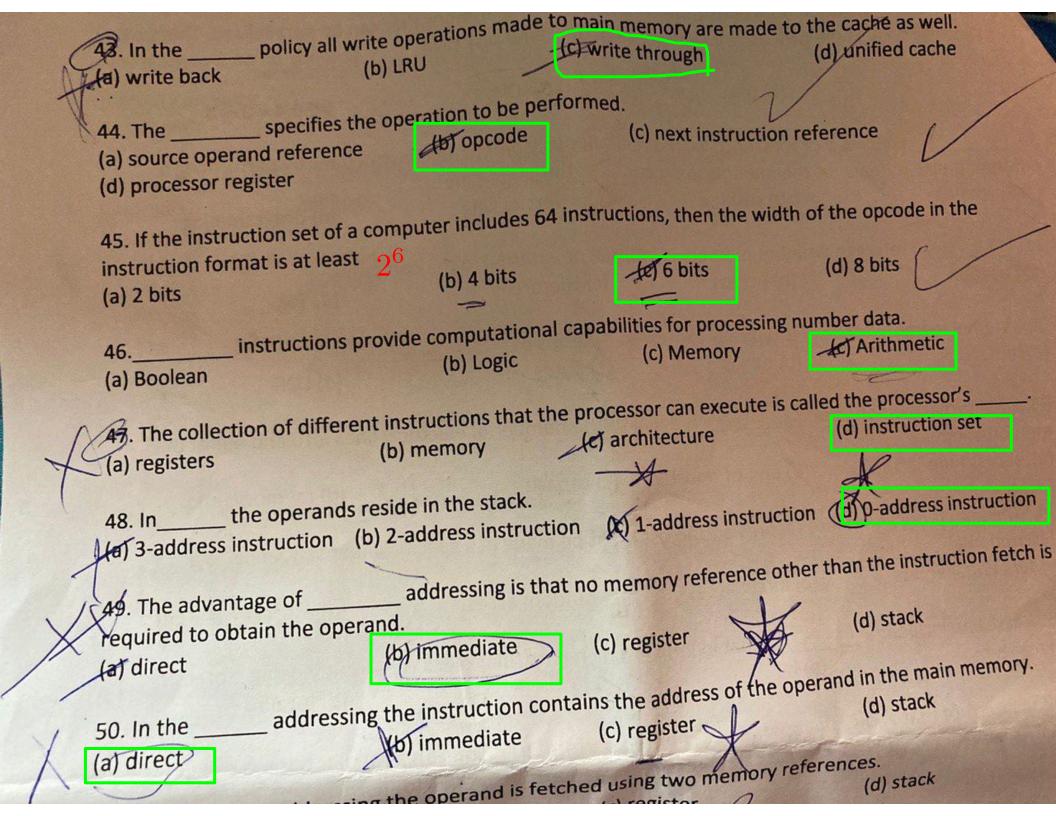
	Final Exam -	-2021-2022 - Model2	
1. The sto	ores data.		
(a) system bus	(b) I/O	(g) main memory	
2. Then (a) data transport	noves data between the co	mputer and its externa (c) register	(d) CPU interconnection
3 provid (a) Control units	e storage internal to the CP	PU.	Ad) Registers
			- OK
A. The F	performs the computer's da (b) CPU interconnection	(c) ALU	ns. (at) system bus
5. A is a r	mechanism that provides fo nection (b) CPU int	er communication amo terconnection (c)	ong CPU, main memory, and I/O. peripheral (d) processor
6. Computer technology (a) slow	ology is changing at a (b) slow to medium	pace.	(d) non-existent
7. It is a(n)	design issue whether a c	computer will have a mi	ultiply instruction.
(a) architectural	(b) memory	(c) elementary	(b) organizational
or by a mechanism	n that makes repeated use of	the add dille of the sys	mplemented by a special multiply stem.
or by a mechanism (a) architectural 9 attri	(b) memory butes include hardware deta	(c) mechanical	organizational
or by a mechanism (a) architectural 9 attri (a) Interface	(b) memory (b) contact that makes repeated use of the co	(c) mechanical ails transparent to the (c) Memory	programmer. (d) Architectural
or by a mechanism (a) architectural 9 attri (a) Interface 20. When data are as	(b) memory butes include hardware deta (b) Organizational moved over longer distance	(c) mechanical ails transparent to the (c) Memory	programmer.
or by a mechanism (a) architectural 9 attri (a) Interface 20. When data are as (a) data commun	(b) memory butes include hardware deta (b) Organizational moved over longer distance ications (b) registering	(c) mechanical ails transparent to the (c) Memory es, to or from a remote (c)structuring	programmer. (d) Architectural e device, the process is known (d) data transport
or by a mechanism (a) architectural 9 attri (a) Interface 20. When data are as (a) data commun 11. The logic that accesses	(b) memory butes include hardware deta (b) Organizational moved over longer distance ications (b) registering	(c) mechanical ails transparent to the (c) Memory es, to or from a remote (c)structuring	programmer. (d) Architectural e device, the process is known (d) data transport ween a larger, slower memory and
or by a mechanism (a) architectural 9 attri (a) Interface 20. When data are as (a) data commun 11. The logic that accesses (a) peripheral	that makes repeated use of (b) memory butes include hardware deta (b) Organizational e moved over longer distance ications (b) registering is a relatively small fast not see the larger memory. (b) cache	(c) mechanical ails transparent to the (c) Memory es, to or from a remote (c)structuring nemory interposed beta (c) processor	programmer. (d) Architectural e device, the process is known (d) data transport ween a larger, slower memory and (d) arithmetic and logic unit
or by a mechanism (a) architectural 9 attri (a) Interface 20. When data are as (a) data commun 11. The logic that accesses (a) peripheral	that makes repeated use of (b) memory butes include hardware deta (b) Organizational e moved over longer distance ications (b) registering is a relatively small fast ness the larger memory.	(c) mechanical ails transparent to the (c) Memory es, to or from a remote (c)structuring nemory interposed beta (c) processor	programmer. (d) Architectural e device, the process is known (d) data transport ween a larger, slower memory and (d) arithmetic and logic unit
or by a mechanism (a) architectural 9 attri (a) Interface 20. When data are as (a) data commun 11. The logic that accesse (a) peripheral 12. An increase in (a) the same	that makes repeated use of (b) memory butes include hardware deta (b) Organizational e moved over longer distance ications (b) registering is a relatively small fast notes the larger memory. (b) cache n clock rate means that indiv (b) slower	(c) mechanical ails transparent to the (c) Memory es, to or from a remote (c)structuring nemory interposed beta (c) processor idual operations are ex (c) with very little	programmer. (d) Architectural e device, the process is known (d) data transport ween a larger, slower memory and (d) arithmetic and logic unit ecuted e change (d) faster
or by a mechanism (a) architectural 9 attri (a) Interface 20. When data are as (a) data commun 11. The logic that accesses (a) peripheral 12. An increase in (a) the same 13. A (a) MIC	that makes repeated use of (b) memory butes include hardware deta (b) Organizational e moved over longer distance ications (b) registering is a relatively small fast notes the larger memory. (b) cache n clock rate means that indiv (b) slower is a core designed to perfo (b) ALU	(c) mechanical ails transparent to the (c) Memory es, to or from a remote (c)structuring nemory interposed beta (c) processor idual operations are ex (c) with very little orm parallel operations of GPU	programmer. (d) Architectural e device, the process is known (d) data transport ween a larger, slower memory and (d) arithmetic and logic unit ecuted e change (d) faster on graphics data. (d) PGD
or by a mechanism (a) architectural 9 attri (a) Interface 20. When data are as (a) data commun 11. The logic that accesses (a) peripheral 12. An increase in (a) the same 13. A (a) MIC	that makes repeated use of (b) memory butes include hardware deta (b) Organizational e moved over longer distance ications (b) registering is a relatively small fast notes the larger memory. (b) cache n clock rate means that indiv (b) slower is a core designed to perfo (b) ALU	(c) mechanical ails transparent to the (c) Memory es, to or from a remote (c)structuring nemory interposed beta (c) processor idual operations are ex (c) with very little orm parallel operations of GPU	programmer. (d) Architectural e device, the process is known (d) data transport ween a larger, slower memory and (d) arithmetic and logic unit ecuted e change (d) faster on graphics data. (d) PGD
or by a mechanism (a) architectural 9 attri (a) Interface 20. When data are as (a) data commun 11. The logic that accesse (a) peripheral 12. An increase in (a) the same 13. A (a) MIC	that makes repeated use of (b) memory butes include hardware deta (b) Organizational e moved over longer distance ications (b) registering is a relatively small fast notes the larger memory. (b) cache n clock rate means that indiv (b) slower is a core designed to perfo (b) ALU	(c) mechanical ails transparent to the (c) Memory es, to or from a remote (c)structuring nemory interposed beta (c) processor idual operations are ex (c) with very little orm parallel operations of GPU	programmer. (d) Architectural e device, the process is known (d) data transport ween a larger, slower memory and (d) arithmetic and logic unit ecuted e change (d) faster

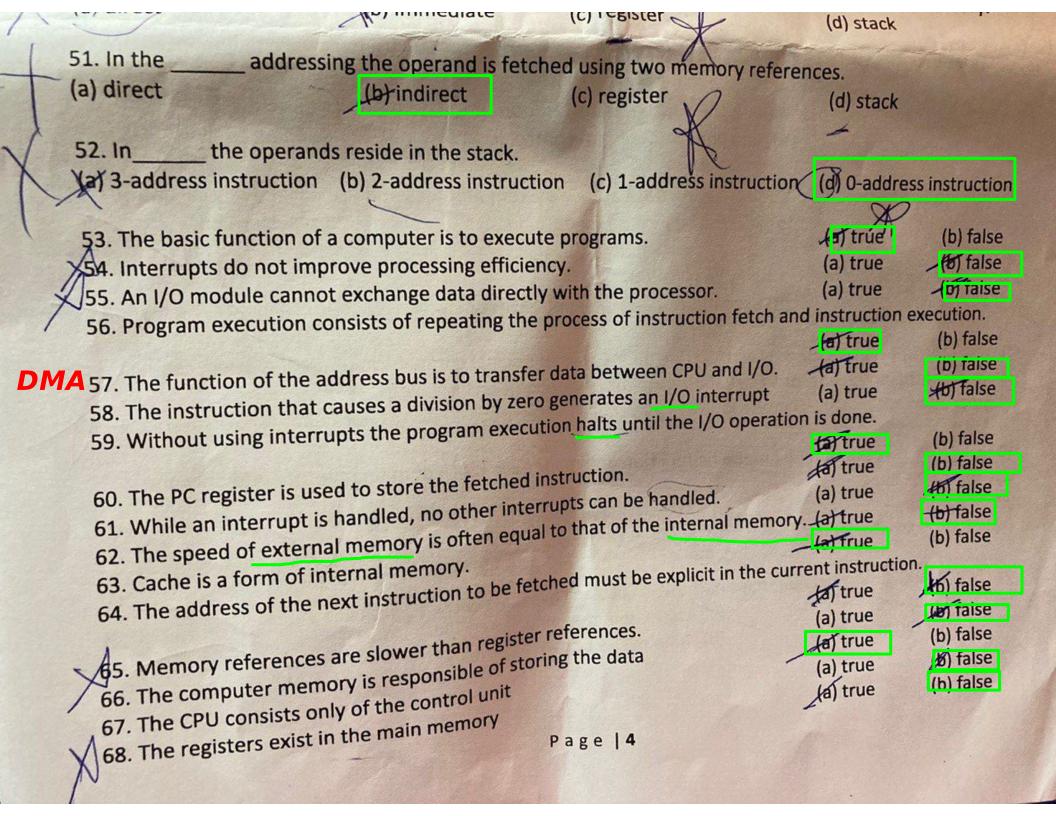
15 law deals with the potential speedup of a program using	multiple processors compared to
a single processor. (a) Moore's (c) Little's	(d) Murphy's
16. The register is used to hold the word received from the memor	ν.
(c) IR	(d) IBR
17. The register specifies the address in the memory of the word to	o be read or written.
17. The register specifies the address in the memory of the word to (a) MBR (c) IR	(d) IBR
18. The register contains the address of the next instruction to be	fetched 1
(a) IR (b) IBR (E) PC	(d) AC
19. The register is used to temporarily hold operands and results of	of the ALU
(a) TR (b) AC (c) IBR	(d) MBR `
20. The desktop application(s) that require the great power of today's i	microprocessor-based systems
include (a) image processing (b) speech recognition (c) videoconfere	encing (a) all of the above
21. The von Neumann general-purpose architecture IAS is based on wh	hich concept?
(a) data and instructions are stored in a single read-write memory	
(b) the contents of this memory are addressable by location	
(c) execution occurs in a sequential fashion	
(d) all of the above	

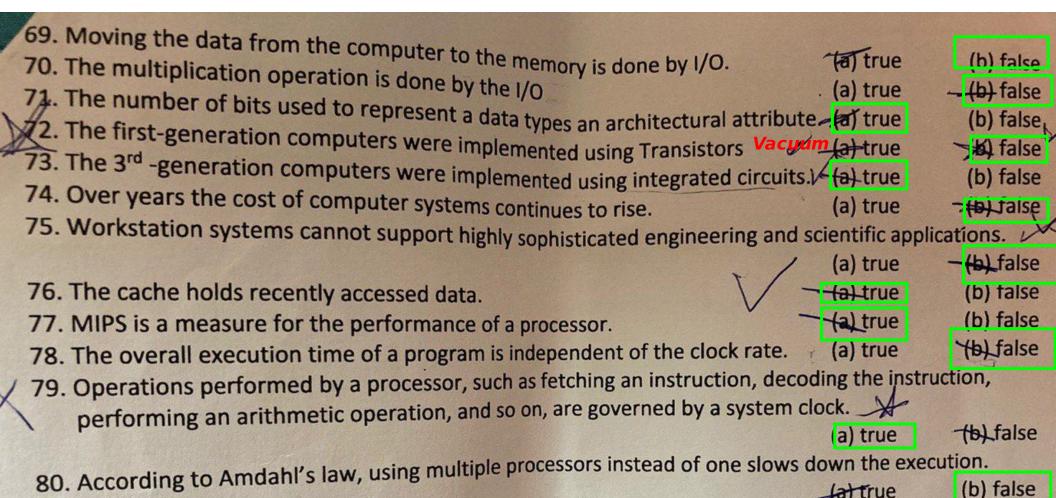
22. A sequence of	codes or instructions is c		
(a) a program	memory	(c) an interconnect	(d) a register
23. The processing (a) execute	required for a single ins	truction is called the (c) storing Instruct	cycle. uio(t) packet
(a) timer interrup	_ is generated by a failur t _ /b) I/O interrupt	e such as power failure or r (c) program interrupt	nemory pa rity error. hardware failure interry
(a) timer interrup	is generated by some of (b) I/O interrupt	ondition that occurs as a res	sult of an instruction execution. (d) hardware failure interrup
(a) clock cycle		(c) clock speed	(et) cycle time
(a) clock cycle	(B) Clock 1212	is known as clock spe (c) performance	(d) cycle time
28. The use of motential to incr	ease performance without (b) GPU	ame chip is referred to as increasing the clock rate. (c) data channels	and provides the (d) MPC



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/	37. The are used to designate the source or destination of the data on the data bus. (a) system lines (b) data lines (c) control lines (d) address lines
/	38. The data lines provide a path for moving data among system modules and are collectively called the (a) control bus (b) address bus (c) data bus
	39. The first part of the instruction cycle is called (b) execution cycle (c) optimization cycle (d) cashing cycle
+	40. The interrupt is generated by an I/O controller to signal normal completion of an operation, request service from the processor, or to signal a variety of error conditions is called. (a) timer interrupt (b) I/O interrupt (c) excedute 7 (d) hardware failure interrupt (a) timer interrupt is the simplest mapping function and maps each block of main memory into only one
	possible cache line. (b) Associative mapping (d) None of the above
	(c) Set associative mapping (a) Direct mapping (b) Associative mapping (c) Set associative mapping (d) None of the above (e) Set associative mapping







Best wishes!

(a) true