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EECE 2060C Laboratory – 002
Lab 4: Project Design Report
Report Due: October 2, 2017

Signed 2's Complement Five Bit Adder Design

Requirements:

- **Summary –** Design an adder of a computer and gain understanding of designing a computing circuit through usage of a 74181 IC and logic gate.

- **Inputs –** First Number (A_0, A_1, A_2, A_3, A_4), Second Number (B_0, B_1, B_2, B_3, B_4)

- **Outputs –** Output Number (F_0, F_1, F_2, F_3, F_4), Overflow Indicator (V), Carry-out (C5)

- First task must be to test understand the usage of the 74181 IC. The second will be to implement the 5-bit adder design utilizing the 74181

- Since there are 10 inputs, V_{cc} and Gnd can be utilized for the remaining two inputs after the switches are used.

- LEDs will display output results

Task 1:

- **Design:**
    1. Properly wire 74181 for first test (S_0 – Gnd (0), S_1 – Gnd (0), S_2 – Gnd (0), S_3 – V_{dd} (1), M – Gnd (0), C_n – V_{dd} (1))

    2. Utilize Table 1 below in order to wire switches for first and second number

    3. Execute each test, recording the binary output and carry-out value

    4. Rewire 74181 for second test (S_0 – V_{dd} (1), S_1 – Gnd (0), S_2 – Gnd (0), S_3 – V_{dd} (1), M – Gnd (0), C_n – V_{dd} (1)) and repeat steps 2 and 3

    5. Evaluate results to see if expected results were achieved.
    Note: If the binary output is wrong altogether, recheck wiring and check if C_n must be different. If the number is right but carry-out value is wrong, see pattern of carry-out values in results. It is possible that carry-out 1 is represented as logic zero.

Pattern no.	1st number A3-A0	2nd number B3-B0	Expected Results C(n+4), F3-F0	Actual Results $S_3S_2S_1S_{0=}$ 0001 C(n+4), F3-F0	Actual Results $S_3S_2S_1S_{0=}$ 1001 C(n+4), F3-F0	Purpose
1	0110	0001	(0)0111			Pos+pos C(n+4) = 0
2	1110	1110	(1)1100			Neg+neg C(n+4) = 1
3	0110	1110	(1)0100			Pos+neg C(n+4)=1
4	1110	0110	(1)0100			Neg+pos C(n+4)=1

Table 1. Test Patterns for Task 1

Task 2:

- **Design:**
  - **Last Stage Circuit:**

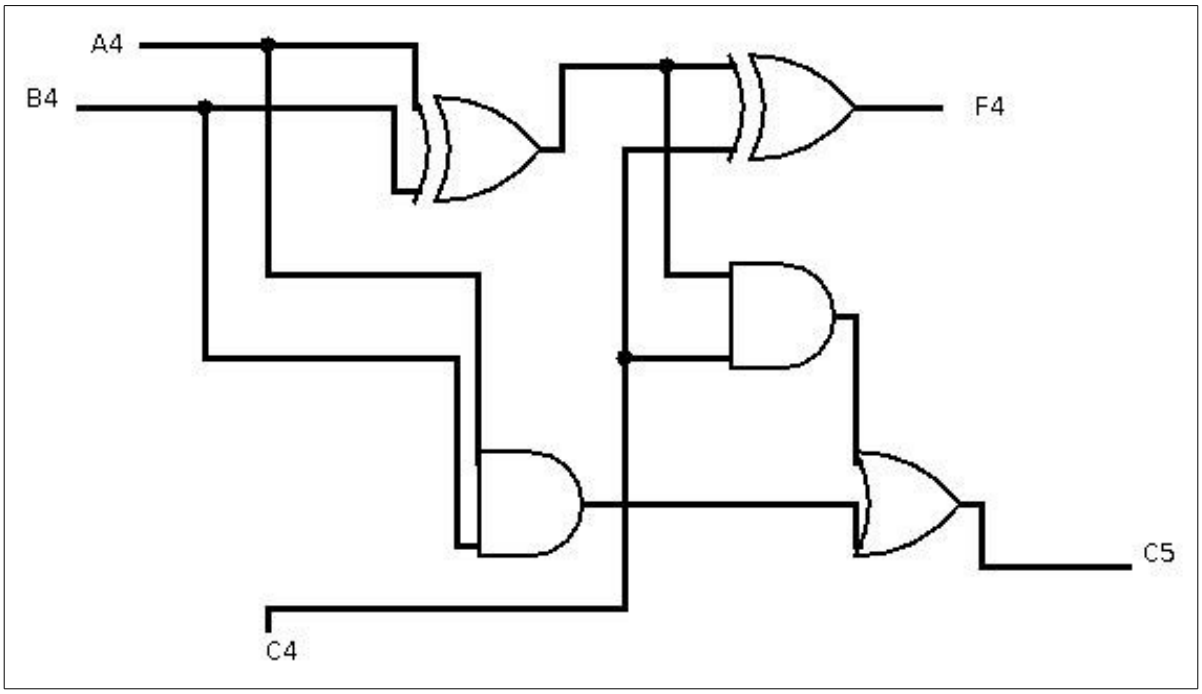

Figure 1. Last Stage Circuit for MSB

- **Full Circuit Design:**

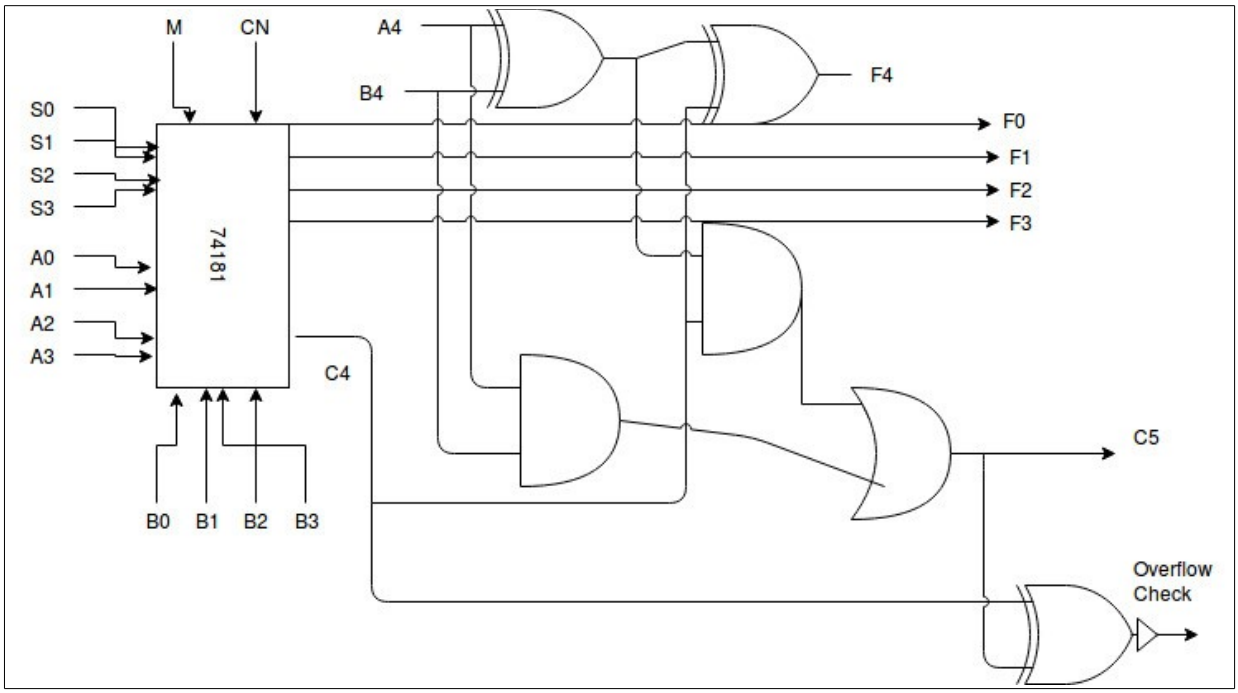

Figure 2. Full Circuit Design with Last Stage and Overflow Checker

- S_0, S_1, S_2, and S_3 will be used in order to properly utilize the addition functionality of the 74181 and properly define the C(n+4) as logic 1 in the event of a carry-out
- The C(n+4) will be used to aid in the final bit addition by providing the carry-out for the single bit adder.

Test Procedure:

Pattern no.	1st number A4-A0	2nd number B4-B0	Expected Results V, C5, F4-F0	Actual Results V, C5, F4-F0	Purpose
1	00000	00000	0, 0, 00000		Test no input
2	00010	00001	0, 0, 00011		Test small pos+pos
3	01111	01001	1, 0, 11000		Test pos+pos overflow
4	00001	11110	0. 0, 11111		Test pos+neg small
5	00100	11110	0, 1, 00010		Test pos+neg with sign change and carry-out
6	11000	00010	0, 0, 11010		Test neg+pos small
7	10110	01110	0, 1, 00100		Test neg+pos with carry-out and sign change
8	10100	11111	0, 1, 11101		Test small neg+neg
9	10000	10001	1, 1, 00001		Test neg+neg overflow
10	11111	11111	0, 1, 11110		Test all active

Table 2. Full Circuit Test Patterns

Design Time: 4 hours