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Release 14.7 - xst P.20131013 (lin64)
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-->
Parameter TMPDIR set to xst/projnav.tmp


Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.03 secs

-->
Parameter xsthdpdir set to xst


Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.03 secs

-->
Reading design: Test.prj

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=========================================================================
*                      Synthesis Options Summary                        *
=========================================================================
---- Source Parameters
Input File Name                    : "Test.prj"
Input Format                       : mixed
Ignore Synthesis Constraint File   : NO

---- Target Parameters
Output File Name                   : "Test"
Output Format                      : NGC
Target Device                      : xc3s100e-4-cp132

---- Source Options
Top Module Name                    : Test
Automatic FSM Extraction           : YES
FSM Encoding Algorithm             : Auto
Safe Implementation                : No
FSM Style                          : LUT
RAM Extraction                     : Yes
RAM Style                          : Auto
ROM Extraction                     : Yes
Mux Style                          : Auto
Decoder Extraction                 : YES
Priority Encoder Extraction        : Yes
```

```
Shift Register Extraction          : YES
Logical Shifter Extraction         : YES
XOR Collapsing                     : YES
ROM Style                          : Auto
Mux Extraction                     : Yes
Resource Sharing                   : YES
Asynchronous To Synchronous        : NO
Multiplier Style                   : Auto
Automatic Register Balancing       : No

---- Target Options
Add IO Buffers                     : YES
Global Maximum Fanout              : 500
Add Generic Clock Buffer(BUFG)     : 24
Register Duplication               : YES
Slice Packing                      : YES
Optimize Instantiated Primitives   : NO
Use Clock Enable                   : Yes
Use Synchronous Set                : Yes
Use Synchronous Reset              : Yes
Pack IO Registers into IOBs        : Auto
Equivalent register Removal        : YES

---- General Options
Optimization Goal                  : Speed
Optimization Effort                : 1
Keep Hierarchy                     : No
Netlist Hierarchy                  : As_Optimized
RTL Output                         : Yes
Global Optimization                : AllClockNets
Read Cores                         : YES
Write Timing Constraints           : NO
Cross Clock Analysis               : NO
Hierarchy Separator                : /
Bus Delimiter                      : <>
Case Specifier                     : Maintain
Slice Utilization Ratio            : 100
BRAM Utilization Ratio             : 100
Verilog 2001                       : YES
Auto BRAM Packing                  : NO
Slice Utilization Ratio Delta      : 5

=========================================================================


=========================================================================
*                           HDL Compilation                             *
=========================================================================
Compiling verilog file "Test.v" in library work
Module <Test> compiled
No errors in compilation
Analysis of file <"Test.prj"> succeeded.


=========================================================================
*                       Design Hierarchy Analysis                       *
=========================================================================
Analyzing hierarchy for module <Test> in library <work>.


=========================================================================
```

```
*                            HDL Analysis                                     *
=========================================================================
Analyzing top module <Test>.
Module <Test> is correct for synthesis.


=========================================================================
*                            HDL Synthesis                                    *
=========================================================================

Performing bidirectional port resolution...

Synthesizing Unit <Test>.
    Related source file is "Test.v".
Unit <Test> synthesized.


=========================================================================
HDL Synthesis Report

Found no macro
=========================================================================

=========================================================================
*                       Advanced HDL Synthesis                            *
=========================================================================


=========================================================================
Advanced HDL Synthesis Report

Found no macro
=========================================================================

=========================================================================
*                         Low Level Synthesis                             *
=========================================================================

Optimizing unit <Test> ...

Mapping all equations...
Building and optimizing final netlist ...
Found area constraint ratio of 100 (+ 5) on block Test, actual ratio is 0.

Final Macro Processing ...

=========================================================================
Final Register Report

Found no macro
=========================================================================

=========================================================================
*                            Partition Report                             *
=========================================================================

Partition Implementation Status
-------------------------------

  No Partitions were found in this design.
```

```
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=========================================================================
*                            Final Report                               *
=========================================================================
Final Results
RTL Top Level Output File Name     : Test.ngr
Top Level Output File Name         : Test
Output Format                      : NGC
Optimization Goal                  : Speed
Keep Hierarchy                     : No

Design Statistics
# IOs                              : 5

Cell Usage :
# BELS                             : 2
#      INV                         : 1
#      LUT3                        : 1
# IO Buffers                       : 5
#      IBUF                        : 3
#      OBUF                        : 2
=========================================================================

Device utilization summary:
---------------------------

Selected Device : 3s100ecp132-4

 Number of Slices:                        1  out of    960     0%
 Number of 4 input LUTs:                  2  out of   1920     0%
 Number of IOs:                           5
 Number of bonded IOBs:                   5  out of     83     6%

---------------------------
Partition Resource Summary:
---------------------------

  No Partitions were found in this design.

---------------------------


=========================================================================
TIMING REPORT

NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.
      FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT
      GENERATED AFTER PLACE-and-ROUTE.

Clock Information:
------------------
No clock signals found in this design

Asynchronous Control Signals Information:
----------------------------------------
No asynchronous control signals found in this design

Timing Summary:
---------------
Speed Grade: -4
```

```
   Minimum period: No path found
   Minimum input arrival time before clock: No path found
   Maximum output required time after clock: No path found
   Maximum combinational path delay: 6.236ns

Timing Detail:
--------------
All values displayed in nanoseconds (ns)

=========================================================================
Timing constraint: Default path analysis
  Total number of paths / destination ports: 4 / 2
-------------------------------------------------------------------------
Delay:               6.236ns (Levels of Logic = 3)
  Source:            C (PAD)
  Destination:       D (PAD)

  Data Path: C to D
                                Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     IBUF:I->O             2   1.218   0.622  C_IBUF (C_IBUF)
     LUT3:I0->O            1   0.704   0.420  D1 (D_OBUF)
     OBUF:I->O                 3.272          D_OBUF (D)
    ----------------------------------------
    Total                      6.236ns (5.194ns logic, 1.042ns route)
                                       (83.3% logic, 16.7% route)

=========================================================================


Total REAL time to Xst completion: 4.00 secs
Total CPU time to Xst completion: 3.57 secs

-->


Total memory usage is 509760 kilobytes

Number of errors   :    0 (   0 filtered)
Number of warnings :    0 (   0 filtered)
Number of infos    :    0 (   0 filtered)
```