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EECE 2060
Lab 1: Gate Logic and Alarm Circut
September 15, 2017

Implementation:

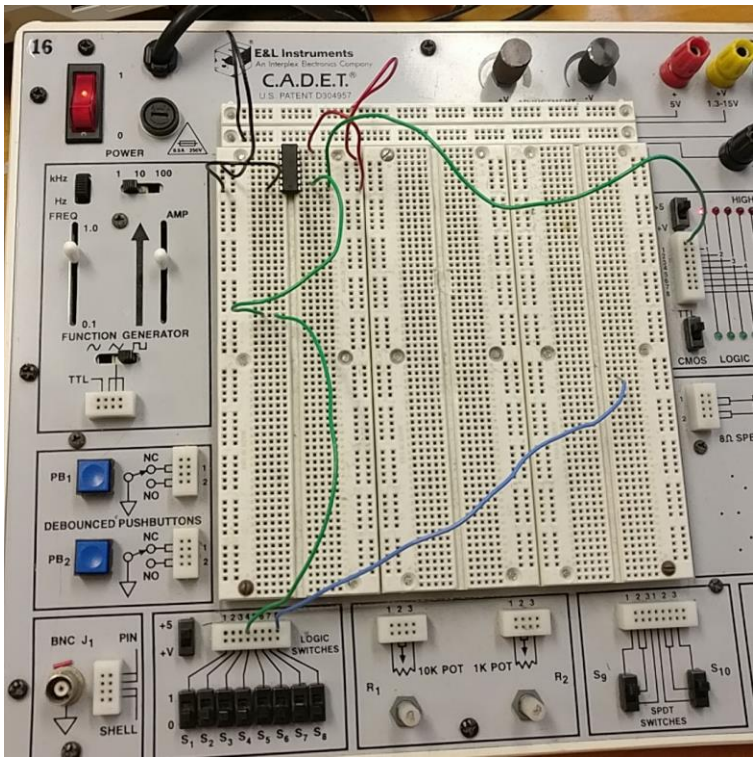

Figure 1. Inverter Gate logic test, similar setups were used for both NAND and NOR gates

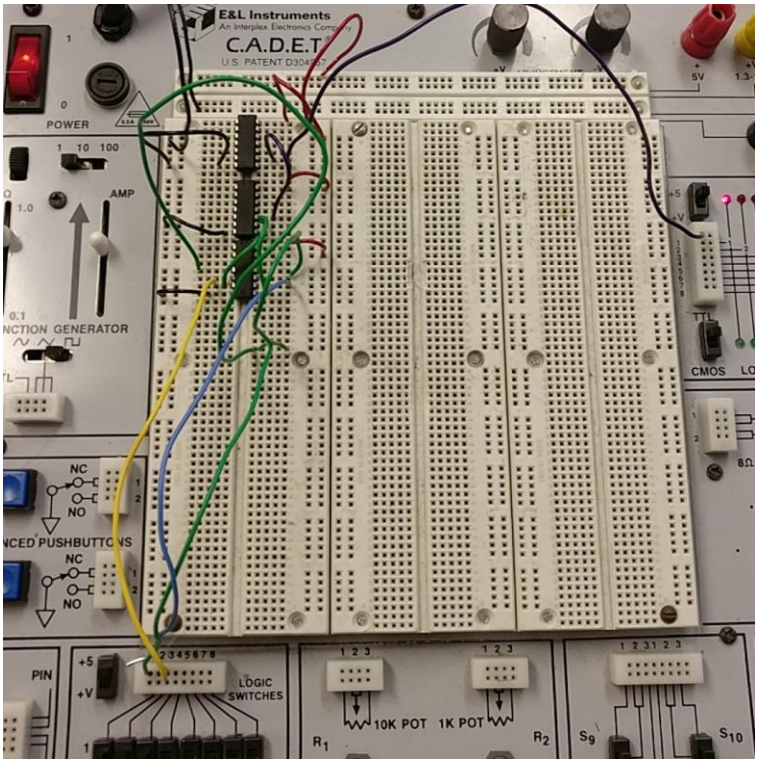

Figure 2. Alarm Gate final design

Common Questions:

1. What is the utilization of your components (i.e., total number of used gates divided by the number of IC components? Can you think of any way(s) you could improve the component utilization?

   The component utilization is 4/3. The NOR gate followed by the inverter gate could have been changed to an OR gate. The inverter IC would have been removed and the component utilization would have been 3/2.

2. How many test vectors were required to *assure* correctness of the circuit?

   Because there were three binary inputs, there was a total of eight test vectors as 2^3=8.

3. Define in detail the contribution of each team member to the accomplishment of the project for each phase (i.e., Pre-lab, In-Lab, and Post-Lab). The idea is that over the quarter all team members share equally in all aspects of the laboratory activity (requirements, design, simulation, test, implementation, and report writing).

   Pre-Lab: Not applicable

   In-Lab: Partner did not attend, so work was done mostly by self with some interaction with another lab members who's partner was absent.

   Post-Lab: Was done wholly by myself as there was no set up means of communication with absent partner