Lecture #	Slide	Topic	Tutorials (Playlist)	
1	Lecture 0 [Introduction]	Basic Introduction to the course, self-introduction, ice breaking session		
2	Lecture 1 [Number System Basics & Calculations]	i. Positional Notations, ii. Different Number systems, iii. Base-R to Decimal iv. Decimal to Base-R v. Base-R to Base-R vi. Binary to Oct/Hex vii. Base-R addition viii. Base-R sub ix. Base-R mul x. Base-R div	Any Base to Decimal Conversion | Digital Logic Design	
3	Lecture 2 [Signed & Unsigned Numbers - 1's & 2's Complement]	i. Decimal to BCD/ Excess-3 ii. Negative Number Representation iii. Sign and Magnitude iv. 1s Complement v. 2s Complement vi. Overflow vii. 2s complement Add/Sub ix. 1s complement Add/Sub	Unsigned & Signed Number (Basic Intro) | Digital Logic Design	
4	Lecture 3 [Boolean Algebra and Logic gates]	i. Logic gates ii. Boolean Algebra iii. Simplification iv. Duality v. Complement	Boolean Simplification (Different Examples) | Digital Logic Design	
5	Lecture 3 [Boolean Algebra and Logic gates]	Universal Gates	NOT Gate using NAND Gate | Universal Gate | NAND Realization | Digital Logic Design	Quiz - 1

	6	Lecture 4 [SOP & POS]	i. Minterm, ii. Maxterm, iii. How to convert a given equation to canonical SOP? iv. How to convert a given equation to canonical POS?	Min Terms & Max Terms | Digital Logic Design	
	7	Lecture 5 [K-Map]	i. Basics of K-Map ii. 2 Var K-Map, iii. 3 Var K-Map, iv. 4 Var K-Map	Introduction to Karnaugh Map (K-Map) || How to build K-Maps	
	8	Lecture 5 [K-Map]	i. K-Map with Don't care. ii. Scenario based K-Map	Scenario Based K-Map (Sample Problem - 1) | Karnaugh Maps | K-Map | Digital Logic Design	
	9	Lecture 5 [K-Map]	More Examples	Scenario Based K-Map (Sample Problem - 1) | Karnaugh Maps | K-Map | Digital Logic Design	Quiz - 2
	10	Lecture 6 [Adder-Subtractor with Applications]	i. Combinational Circuit Basics, ii. Half Adder Design, iii. Full Adder Design, iv. 4-bit parallel Adder, v. 4-bit parallel Adder/Subtractor, vi. Code Converter	Half Adder | Combinational Circuit | Digital Logic Design	
	11	Lecture 6 [Adder-Subtractor with Applications]	i. Voting System, ii. Other applications	Half Adder | Combinational Circuit | Digital Logic Design	
	Midterm				

	12	Lecture 7 [Encoder-Decoder-Mux-Demux]	i. Intro to Decoder, ii. Full Adder using Decoder, iii. Intro to Demux, iv. Building a large decoder using small decoders, v. Function implementation using decoders, vi. Intro to Multiplexer	Introduction to Decoder | Digital Logic Design	
	13	Lecture 7 [Encoder-Decoder-Mux-Demux]	i. Building a large MUX using smaller MUX(s), ii. Intro to Encoder, iii. Octal-Binary Encoder, iv. Priority Encoder, v. Function Implementation using MUX. (a single MUX/ multiple MUX(s)), vi. Combining MSI circuits - Full adder, Code Converter using Encoder-Decoder. vii. Full adder using MUX	How to Implement a 8:1 MUX using 4:1 and 2:1 MUX (Method 1) | Digital Logic Design	
	14	Lecture 8 [Sequential Circuits-Flipflops].pptx	i) Basics of Latch ii) Clock and Triggering Mechanism iii) Basics of FF (SR, D, JK, T)	SR Latch | Truth Table | Build SR Latch using NAND Gate #sequentialcircuits #flipflops #srlatch	
	15	Lecture 8 [Sequential Circuits-Flipflops].pptx	Timing Diagram	SR Latch | Truth Table | Build SR Latch using NAND Gate #sequentialcircuits #flipflops #srlatch	
	16	Lecture 9 [Sequential Circuit Analysis].pptx	i. Circuit to State Diagram, ii. State to Circuit Diagram,	Circuit Diagram to State Diagram | Sequential Circuit Analysis #sequentialcircuits #flipflops	
	17	Lecture 9 [Sequential Circuit Analysis].pptx	Counter Design	Design 2 bit Synchronous UP Counter 2 bit and 3 bit Counter Design	

	18	Lecture 10 [Memory]	What is memory Memory Architecture Memory related Calculations	Memory Unit Basic Theory | Block Diagram of Memory Unit #digitalelectronics #memoryunit	
	19	Lecture 10 [Memory]	Difference between Static and Dynamic RAM Desigining a RAM	Memory Unit Basic Theory | Block Diagram of Memory Unit #digitalelectronics #memoryunit	
	20	Review / Practice			
	21				
	22				
	Final				