Application Report
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Understanding and Interpreting Standard-Logic Data Sheets

Stephen M.Nolan, Jose M. Soltero, Shreyas Rao

ABSTRACT

Texas Instruments (TI) standard-logic product data sheets include descriptions of functionality and electrical specifications for the devices. Each specification includes acronyms, numerical limits, and test conditions that may be foreign to the user. The proper understanding and interpretation of the direct, and sometimes implied, meanings of these specifications are essential to correct product selection and associated circuit design. This application report explains each data sheet parameter in detail, how it affects the device, and how it impacts the application. This will enable component and system-design engineers to derive the maximum benefit from TI logic devices.

Contents

1 Application Note Outline

This application report is organized into five main sections:

1. *Introduction*
2. *Top-Level Look at the TI Logic Data Sheet*. Overall layout and component parts of a data sheet are explained.
3. *Dissecting the TI Logic Data Sheet*. JEDEC definition, the TI definition, an explanation, and, where possible, helpful hints are presented for each specification term commonly found in TI logic data sheets.
4. *Logic Compatibility*. Information in TI logic data sheets for determining the interface compatibility between different logic families is explained.
5. End matter, including the *Conclusion*, *Acknowledgments*, and *References* sections.

2 Introduction

This application report is a synopsis of the information available from a typical TI data sheet with the purpose of assisting component and system-design engineers in selecting Texas Instruments (TI) standard-logic products. Information includes a brief description of terms, definitions, and testing procedures currently used for commercial, automotive and military specifications. Symbols, terms, and definitions generally are in accordance with those currently agreed upon by the JEDEC Solid State Technology Association for use in the USA and by the International Electrotechnical Commission (IEC) for international use.

3 Top-Level Look at the TI Logic Data Sheet

The TI logic data sheet presents pertinent technical information for a particular device and is organized for quick access. This application report dissects a typical TI logic data sheet and describes the organization of all data sheets.

Typically, there are ten sections in TI-logic data sheets:

1. Front Page
   (a) Features
   (b) Applications
   (c) Description
   (d) Device Information Table
   (e) Front-Page Graphic(s)
2. Table of Contents
3. Revision History
4. Pin Configuration and Functions
5. Specifications
   (a) Absolute Maximum Ratings
   (b) ESD Ratings
   (c) Recommended Operating Conditions
   (d) Thermal Information
   (e) Electrical Characteristics
   (f) Timing Requirements
   (g) Switching Characteristics
   (h) Typical Characteristics
6. Parameter Measurement Information
7. Detailed Description
   (a) Overview
   (b) Functional Block Diagram
   (c) Feature Description
   (d) Device Functional Modes
8. Application and Implementation
   (a) Application Information
   (b) Typical Application
   (c) Design Requirements
   (d) Detailed Design Procedure
   (e) Application Curves
9. Power Supply Recommendations
10. Layout
    (a) Layout Guidelines
    (b) Layout Example
11. Device and Documentation Support
12. Mechanical, Packaging, and Ordering Information

3.1 Device Summary

The first page of a data sheet contains all of the general information about a device (see Figure 1). This information includes:

1. Title, literature number, and dates of origination and revision, as applicable. Also, the top navigation contains hyperlinks leading directly to Product Folder, Sample & Buy, Technical Documents (related to the device), Tools & Software, and Support & Community.

Figure 1. Example of Device Summary

2. The *Features* section identifies the main features and benefits of the device. This section includes features in a bulleted form. Figure 2 shows an example of the bulleted features.

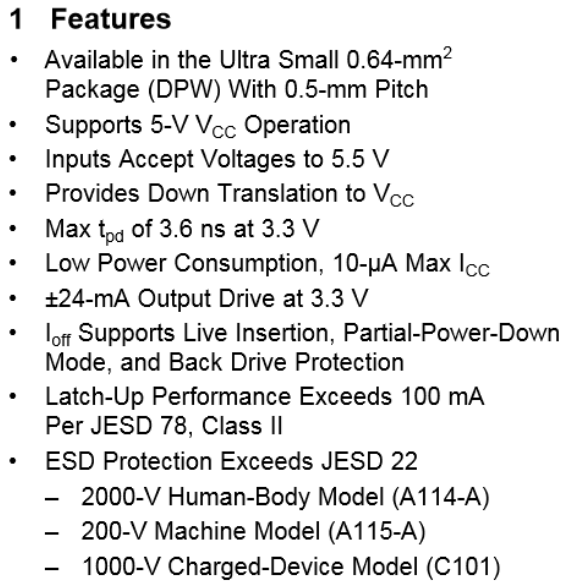


Figure 2. Feature Bullets

3. The *Applications* section for the device identifies the application scenarios for the device. Figure 3 shows an example of typical applications.

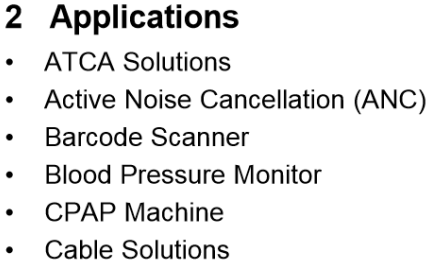


Figure 3. Typical Applications

4. The *Description* section provides a brief description of the device and its functionality

3 Description

This single 2-input positive-AND gate is designed for 1.65-V to 5.5-V V_{CC} operation.

The SN74LVC1G08 device performs the Boolean function or $Y = A \bullet B$ or $Y = \overline{\overline{A} + \overline{B}}$ in positive logic.

Figure 4. Brief Description of Device

5. Figure 5 shows a logic diagram. The device information defines the nominal size of the device in each of the available packages.

Device Information(1)

DEVICE NAME	PACKAGE	BODY SIZE
SN74LVC1G08	SOT-23 (5)	2.9mm × 1.6mm
	SC70 (5)	2.0mm × 1.25mm
	X2SON (4)	0.8mm × 0.8mm
	SON (6)	1.45mm × 1.0mm
	SON (6)	1.0mm × 1.0mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Figure 5. Device Information

6. Product-development stage note at the bottom of the data sheet
7. Table of contents to list the contents and the link to the page numbers alongside it.
8. Revision history for the device mentioning the changes to the data sheet with the dates.

4 Revision History

Changes from Revision X (March 2014 to Revision Y

Figure 6. Revision History

3.2 Pin Configuration and Functions

Figure 7 shows all the package options for the device. Figure 8 shows the functions of each pin sorted by the package list and their corresponding pin locations.

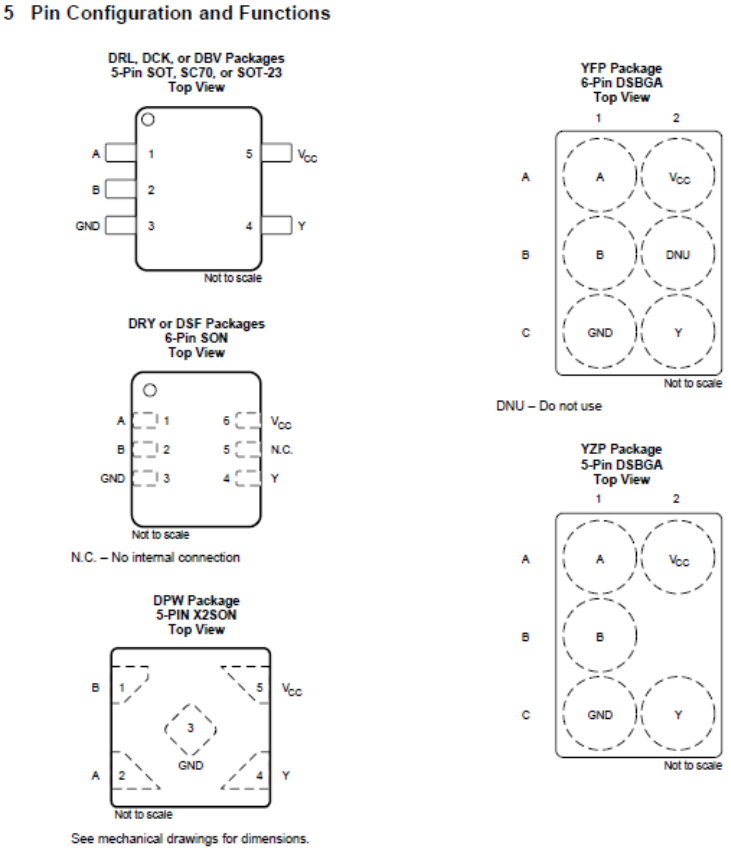


Figure 7. Pin Configuration and Functions

Pin Functions

PIN						I/O	DESCRIPTION
NAME	DRL, DCK, DBV	DPW	DRY, DSF	YZP	YFP		
A	1	2	1	A1	A1	I	Input A
B	2	1	2	B1	B1	I	Input B
DNU	–	–	–	–	B2	–	Do not use
GND	3	3	3	C1	C1	–	Ground
N.C.	–	–	5	–	–	–	No internal connection
V_{CC}	5	5	6	A2	A2	–	Power Pin
Y	4	4	4	C2	C2	O	Output Y

Figure 8. Pin Functions Table

3.3 Absolute Maximum Ratings

The *Absolute Maximum Ratings* section (Figure 9) specifies the stress levels that, if exceeded, may cause permanent damage to the device. However, these are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Also, exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

As Figure 9 indicates, there are two absolute maximums that may be exceeded under certain conditions. The input and output voltage ratings, V_I and V_O, may be exceeded if the input and output maximum clamp-current ratings, I_{IK} and I_{OK}, are observed.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		–0.5	6.5	V
V_I	Input voltage range(2)		–0.5	6.5	V
V_O	Voltage range applied to any output in the high-impedance or power-off state(2)		–0.5	6.5	V
V_O	Voltage range applied to any output in the high or low state(2)(3)		–0.5	V_{CC} + 0.5	V
I_{IK}	Input clamp current	V_I < 0		–50	mA
I_{OK}	Output clamp current	V_O < 0		–50	mA
I_O	Continuous output current			±50	mA
	Continuous current through V_{CC} or GND			±100	mA
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input negative-voltage and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
(3) The value of V_{CC} is provided in the *Recommended Operating Conditions* table.

Figure 9. Example of Absolute Maximum Ratings Section

Helpful Hint:

All currents are defined with respect to conventional current flow into the respective terminal of the integrated circuit. This means that any current that flows out of the respective terminal is considered to be a negative quantity.

All limits are given according to the absolute-magnitude convention, with a few exceptions. In this convention, maximum refers to the greater magnitude limit of a range of like-signed values; if the range includes both positive and negative values, both limit values are maximums. Minimum refers to the smaller magnitude limit of a range of like-signed values; if the range includes both positive and negative values, then the minimum is implicitly zero. The most common exceptions to the absolute magnitude convention are temperature and logic levels. In these levels, zero does not represent the least-possible quantity, so the algebraic convention is commonly accepted. In this case, maximum refers to the most-positive value.

3.4 ESD Ratings

The ESD Ratings section of the data sheet specifies the Electrostatic Discharge ratings for the device tested as per JEDEC (Joint Electron Device Engineering Council) standards.

Usually, HBM (Human Body Model) and CDM (Charged Device Model) spec is tabulated as per the qualification process. Machine Model (MM) is discontinued.

ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101 (2)	1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

Figure 10. Example of ESD Ratings Section

3.5 Recommended Operating Conditions

The *Recommended Operating Conditions* section of the data sheet sets the conditions for which Texas Instruments specifies device operation (see Figure 11). These are the conditions that the application circuit should provide to the device in order for it to function as intended. The limits for items that appear in this section are used as test conditions for the limits that appear in the *Electrical Characteristics*, *Timing Requirements*, *Switching Characteristics*, and *Operating Conditions* sections.

Recommended Operating Conditions (see Note 4)

			SN54LVTH16646		SN74LVTH16646		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		2.7	3.6	2.7	3.6	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage			5.5		5.5	V
I_{OH}	High-level output current			-24		-32	mA
I_{OL}	Low-level output current			48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
$\Delta t/\Delta V_{CC}$	Power-up ramp rate		200		200		µs/V
T_A	Operating free-air temperature		-55	125	-40	85	°C

NOTE: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

Figure 11. Example Recommended Operating Conditions Section

3.6 Electrical Characteristics

The *Electrical Characteristics (over recommended free-air temperature range)* table, also known in the industry as the DC table, provides the specified electrical characteristic limits of the device when tested under the conditions in the *Recommended Operating Conditions* table, as given specifically for each parameter (see Figure 12).

Helpful Hint:

Although some parameters, such as C_i and C_{io}, can be tested with an ac signal, sometimes the electrical characteristics table is called the DC section.

Electrical Characteristics (Over Recommended Operating Free-air Temperature Range (unless otherwise noted))

PARAMETER		TEST CONDITIONS		SN54LVTH16646			SN74LVTH16646			UNIT
				MIN	TYP (4)	MAX	MIN	TYP (4)	MAX	
V_{IK}		V_{CC} = 2.7 V,	I_I = -18 mA			–1.2			–1.2	V
V_{OH}		V_{CC} = 2.7 V to 3.6 V,	I_{OH} = -100 µA	V_{CC}-0.2			V_{CC}-0.2			V
		V_{CC} = 2.7 V,	I_{OH} = -8 mA	2.4			2.4			
		V_{CC} = 3 V	I_{OH} = -24 mA	2						
			I_{OH} = -32 mA				2			
V_{OL}		V_{CC} = 2.7 V	I_{OL} = 100 µA			0.2			0.2	V
			I_{OL} = 24 mA			0.5			0.5	
		V_{CC} = 3 V	I_{OL} = 16 mA			0.4			0.4	
			I_{OL} = 32 mA			0.5			0.5	
			I_{OL} = 48 mA			0.55				
			I_{OL} = 64 mA						0.55	
I_I	Control inputs	V_{CC} = 3.6 V,	V_I = V_{CC} or GND			±1			±1	µA
		V_{CC} = 0 or 3.6 V,	V_I = 5.5 V			10			10	
	A or B ports (5)	V_{CC} = 3.6 V	V_I = 5.5 V			20			20	
			V_I = V_{CC}			1			1	
			V_I = 0			–5			–5	
I_{off}		V_{CC} = 0 V,	V_I or V_O = 0 to 4.5 V						±100	µA
$I_{I(hold)}$	A or B ports	V_{CC} = 3 V	V_I = 0.8 V	75			75			µA
			V_I = 2 V	–75			–75			
		V_{CC} = 3.6 V (6),	V_I = 0 to 3.6 V						±500	
I_{OZPU}		V_{CC} = 0 to 1.5 V, V_O = 0.5 V to 3 V, $\overline{OE}$ = don't care				±100 *			±100	µA
I_{OZPD}		V_{CC} = 1.5 V to 0, V_O = 0.5 V to 3 V, $\overline{OE}$ = don't care				±100 *			±100	µA
I_{CC}		V_{CC} = 3.6 V, I_O = 0, V_I = V_{CC} or GND	Outputs high			0.19			0.19	mA
			Outputs low			5			5	
			Outputs disabled			0.19			0.19	
ΔI_{CC} (7)		V_{CC} = 3 V to 3.6 V, One input at V_{CC} - 0.6 V, Other inputs at V_{CC} or GND				0.2			0.2	mA
C_i		V_I = 3 V or 0			4			4		pF
C_{io}		V_O = 3 V or 0			10			10		pF

(3) On products compliant to MIL-PRF-38535, this parameter is not production tested.

(4) All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

(5) Unused pins at V_{CC} or GND

(6) This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.

(7) This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V_{CC} or GND.

Figure 12. Example Electrical-Characteristics Section

3.7 Live-Insertion Specifications

The *Live-Insertion* section of the data sheet provides information about the parameters needed for true live insertion. These parameters include I_{off}, I_{OZPU}, I_{OZPD}, and BIAS V_{CC} for precharging purposes. An example of a typical live-insertion section is shown in Figure 13.

Live-insertion Specifications for B port Over Recommended Operating Free-air Temperature Range

PARAMETER	TEST CONDITIONS			MIN	MAX	UNIT
I_{off}	V_{CC} = 0,	BIAS V_{CC} = 0,	V_I or V_O = 0 to 1.5 V		10	µA
I_{OZPU}	V_{CC} = 0 to 1.5 V,	BIAS V_{CC} = 0,	V_O = 0.5 V to 1.5 V, $\overline{OE}$ = 0		±30	µA
I_{OZPD}	V_{CC} = 1.5 V to 0,	BIAS V_{CC} = 0,	V_O = 0.5 V to 1.5 V, $\overline{OE}$ = 0		±30	µA
I_{CC} (BIAS V_{CC})	V_{CC} = 0 to 3.15 V	BIAS V_{CC} = 3.15 V to 3.45 V,	V_O (B port) = 0 to 1.5 V		5	mA
	V_{CC} = 3.15 V to 3.45 V				10	µA
V_O	V_{CC} = 0,	BIAS V_{CC} = 3.3 V,	I_O = 0	0.95	1.05	V
I_O	V_{CC} = 0,	BIAS V_{CC} = 3.15 V to 3.45 V,	V_O (B port) = 0.6 V	-1		µA

Figure 13. Example Live-Insertion Section

3.8 Timing Requirements

The*Timing Requirements* section of the data sheet is similar to the *Recommended Operating Conditions* section (see Figure 14). These are timings that the application circuit should provide to the device for it to function as intended. This section addresses the timing relationships between transitions of one or more input signals that are necessary to ensure device functionality and applies only to sequential-logic devices (for example, flip-flops, latches, and registers).

Timing Requirements (Over Recommended Operating Free-air Temperature Range (unless otherwise noted)) (see Figure 2)

			SN54LVTH16646				SN74LVTH16646				UNIT
			V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency			150		150		150		150	MHz
t_w	Pulse duration, CLK high or low		3.3		3.3		3.3		3.3		ns
t_{su}	Setup time, A or B before CLKAB↑ or CLKBA↑	Data high	1.2		1.5		1.2		1.5		ns
		Data low	2		2.8		2		2.8		
t_h	Hold time, A or B after CLKAB↑ or CLKBA↑	Data high	0.5		0		0.5		0		ns
		Data low	0.5		0.5		0.5		0.5		

Figure 14. Example Timing-Requirements Section

3.9 Switching Characteristics

The *Switching Characteristics* section of the data sheet, also known in the industry as the AC table, includes the parameters that specify how fast the outputs will respond to signal changes at the inputs under specified conditions of supply voltage, temperature, and load (see Figure 15).

Helpful Hint:

The *Switching Characteristics* table is sometimes called the AC section, and should not be confused with the AC small-signal performance because switching characteristics describe the large-signal transient response of the circuit.

Switching Characteristics (Over recommended Operating Free-air Temperature Range, C_L = 50 pF (unless otherwise noted)) (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVTH16646				SN74LVTH16646				UNIT
			V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		V_{CC} = 3.3 V ± 0.3 V			V_{CC} = 2.7 V	
			MIN	MAX	MIN	MAX	MIN	TYP (8)	MAX	MIN MAX	
f_{max}			150		150		150			150	MHz
t_{PLH}	CLKBA or CLKAB	A or B	1.3	4.5		5	1.3	2.8	4.2	4.7	ns
t_{PHL}			1.3	4.5		5	1.3	2.8	4.2	4.7	
t_{PLH}	A or B	B or A	1	3.6		4.1	1	2.4	3.4	3.9	ns
t_{PHL}			1	3.6		4.1	1	2.1	3.4	3.9	
t_{PLH}	SBA or SAB (9)	A or B	1	4.7		5.6	1	2.8	4.5	5.4	ns
t_{PHL}			1	4.7		5.6	1	3	4.5	5.4	
t_{PZH}	$\overline{OE}$	A or B	1	4.5		5.4	1	2.5	4.3	5.2	ns
t_{PZL}			1	4.5		5.4	1	2.6	4.3	5.2	
t_{PHZ}	$\overline{OE}$	A or B	2	5.8		6.3	2	4	5.6	6.1	ns
t_{PLZ}			2	5.6		6.3	2	3.6	5.4	6.1	
t_{PZH}	DIR	A or B	1	4.6		5.5	1	3	4.4	5.3	ns
t_{PZL}			1	4.6		5.5	1	3	4.4	5.3	
t_{PHZ}	DIR	A or B	1.5	6		7.1	1.5	3.9	5.7	6.8	ns
t_{PLZ}			1.5	5.5		6	1.5	3.6	5.2	5.7	

(8) All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

(9) These parameters are measured with the internal output state of the storage register opposite that of the bus input.

Figure 15. Example of Switching Characteristics Section

3.10 Noise Characteristics

This section indicates a device's noise performance due to power-rail and ground-rail bounce associated with the high peak currents during dynamic switching (see Figure 16).

Noise Characteristics, V_{CC} = 5 V, C_L = 50 pF, T_A = 25°C (see Note 4)

PARAMETER		SN74AHCT16541			UNIT
		MIN	TYP	MAX	
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}		0.6		V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}		-0.3		V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}		4.6		V
$V_{IH(D)}$	High-level dynamic input voltage	2			V
$V_{IL(D)}$	Low-level dynamic input voltage			0.8	V

(10) Characteristics are for surface-mount packages only.

Figure 16. Example Noise-Characteristics Section

3.11 Operating Characteristics

The *Operating Characteristics* section of the data sheet includes the parameter that specifies the power-dissipation capacitance (C_{pd}) in a CMOS device (see Figure 17). For additional information on how C_{pd} is measured and used to calculate total CMOS-device power consumption in the application, refer to the TI application report, *CMOS Power Consumption and C_{pd} Calculation*, literature number SCAA035.

Operating Characteristics, T_A = 25°C

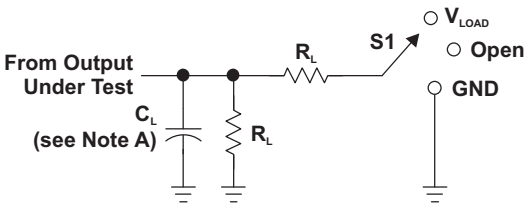
PARAMETER		TEST CONDITIONS		V_{CC} = 1.8 V	V_{CC} = 2.5 V	V_{CC} = 3.3 V	UNIT
				TYP	TYP	TYP	
C_{pd}	Power dissipation capacitance per gate	C_L = 0,	f = 10 MHz	20	21	23	pF

Figure 17. Example of Operating-Characteristics Section

3.12 Parameter Measurement Information

The *Parameter Measurement Information* section of the data sheet illustrates the test loads and waveforms that are used when testing the device (see Figure 18).

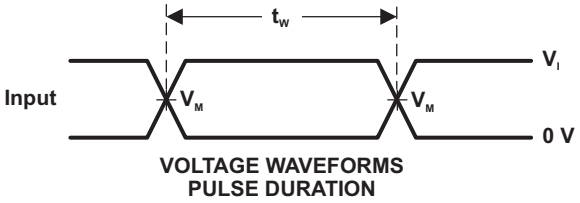
8 Parameter Measurement Information



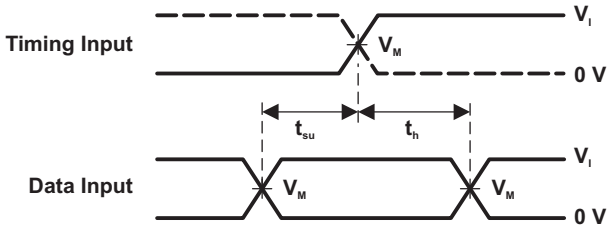
LOAD CIRCUIT

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

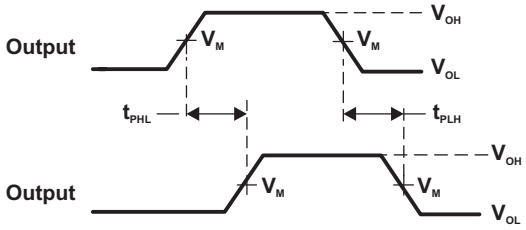
V_{CC}	INPUTS		V_M	V_{LOAD}	C_L	R_L	V_Δ
	V_I	t_r/t_f					
1.8 V ±0.15 V	V_{CC}	≤2 ns	$V_{CC}/2$	2 × V_{CC}	30 pF	1 kΩ	0.15 V
2.5 V ± 0.2 V	V_{CC}	≤2 ns	$V_{CC}/2$	2 × V_{CC}	30 pF	500Ω	0.15 V
2.7 V	2.7 V	≤2.5 ns	1.5 V	6 V	50 pF	500Ω	0.3 V
3.3 V ± 0.3 V	2.7 V	≤2.5 ns	1.5 V	6 V	50 pF	500Ω	0.3 V



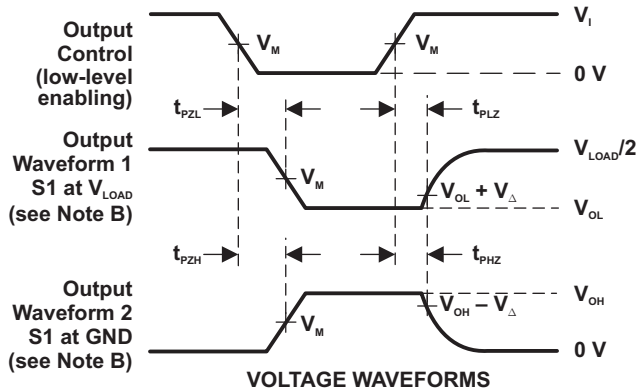
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤10 MHz, Z_O = 50 Ω.
D. The outputs are measured one at a time, with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.
H. All parameters and waveforms are not applicable to all devices.

Figure 18. Example Parameter Measurement Information Section

4 Dissecting the TI Logic Data Sheet

In the following paragraphs, the TI logic data sheet is dissected, and every section and specification is explained in detail.

4.1 Summary Device Description

4.1.1 Title, Literature Number, and Dates of Origination and Revision

The device number and title appear at the top of every page. The device number is the number of the parent device. The fully qualified part number for a specific device can be found in the *Orderable Part Number* table. Figure 19 is a chart to help decode information in the TI logic-device part number.

The literature number is a unique identifier used by TI to identify, store and retrieve a data sheet in internal files.

The month and year of origination is the first date of publication of the data sheet. If a data sheet is modified, the revision date (month and year) is added. If there are multiple revisions, only the latest revision date appears.

Example:

SN	74	LVC		1G		66		DBV	R
1	2	3	4	5	6	7	8	9	10

1 Standard Prefix

Examples: SN – Standard Prefix
SNJ – Conforms to MIL-PRF-38535 (QML)

2 Temperature Range

Examples: ~~54~~ Military
74 – Commercial

3 Family

Examples: Blank = Transistor-Transistor Logic (TTL)
ABT – Advanced BiCMOS Technology
ABTE/ETL – Advanced BiCMOS Technology/ Enhanced Transceiver Logic
AC/ACT – Advanced CMOS Logic
AHC/AHCT – Advanced High-Speed CMOS Logic
ALB – Advanced Low-Voltage BiCMOS
ALS – Advanced Low-Power Schottky Logic
ALVC – Advanced Low-Voltage CMOS Technology
ALVT – Advanced Low-Voltage BiCMOS Technology
AS – Advanced Schottky Logic
AUC – Advanced Ultra Low-Voltage CMOS Logic
AVC – Advanced Very Low-Voltage CMOS Logic
BCT – BiCMOS Bus-Interface Technology
CBT – Crossbar Technology
CBTLV – Low-Voltage Crossbar Technology
CD4000 – CMOS B-Series Integrated Circuits
F – F Logic
FB – Backplane Transceiver Logic/Futurebus+
FCT – Fast CMOS TTL Logic
GTL – Gunning Transceiver Logic
GTLP – Gunning Transceiver Logic Plus
HC/HCT – High-Speed CMOS Logic
HSTL – High-Speed Transceiver Logic
LS – Low-Power Schottky Logic
LV – Low-Voltage CMOS Technology
LVC – Low-Voltage CMOS Technology
LVT – Low-Voltage BiCMOS Technology
PCA/PCF – I^2C Inter-Integrated Circuit Applications
S – Schottky Logic
SSTL/SSTV – Stub Series-Terminated Logic
TVC – Translation Voltage Clamp Logic
VME – VERSAmodule Eurocard Bus Technology

4 Special Features

Examples: Blank = No Special Features
C – Configurable V_{CC} (LVCC)
D – Level-Shifting Diode (CBTD)
H – Bus Hold (ALVCH)
K – Undershoot-Protection Circuitry (CBTK)
R – Damping Resistor on Inputs/Outputs (LVCR)
S – Schottky Clamping Diode (CBTS)
Z – Power-Up 3-State (LVCZ)

5 Bit Width

Examples: Blank = Gates, MSI, and Octals
1G – Single Gate
2G – Dual Gate
3G – Triple Gate
8 – Octal IEEE 1149.1 (JTAG)
16 – Widebus (16, 18, and 20 bit)
18 – Widebus IEEE 1149.1 (JTAG)
32 – Widebus+ (32 and 36 bit)

6 Options

Examples: Blank = No Options
2 – Series Damping Resistor on Outputs
4 – Level Shifter
25 – 25-Ω Line Driver

7 Function

Examples: ~~244~~ Noninverting Buffer/Driver
374 – D-Type Flip-Flop
573 – D-Type Transparent Latch
640 – Inverting Transceiver

8 Device Revision

Examples: Blank = No Revision
Letter Designator A–Z

9 Packages

Commercial: D, DW – Small-Outline Integrated Circuit (SOIC)
DB, DBQ, DCT, DL – Shrink Small-Outline Package (SSOP)
DBB, DGV – Thin Very Small-Outline Package (TVSOP)
DBQ – Quarter-Size Small-Outline Package (QSOP)
DBV, DCK, DCY, PK – Small-Outline Transistor (SOT)
DCU – Very Thin Shrink Small-Outline Package (VSSOP)
DGG, PW – Thin Shrink Small-Outline Package (TSSOP)
FN – Plastic Leaded Chip Carrier (PLCC)
GGM, GKE, GKF, ZKE, ZKF – MicroStar BGA Low-Profile Fine-Pitch Ball Grid Array (LFBGA)
GQL, GQN, ZQL, ZQN – MicroStar Jr. Very-Thin-Profile Fine-Pitch Ball Grid Array (VFBGA)
N, NT, P – Plastic Dual-In-Line Package (PDIP)
NS, PS – Small-Outline Package (SOP)
PAG, PAH, PCA, PCB, PM, PN, PZ – Thin Quad Flatpack (TQFP)
PH, PQ, RC – Quad Flatpack (QFP)
PZA – Low-Profile Quad Flatpack (LQFP)
RGY – Quad Flatpack No Lead (QFN)
YEA, YZA – NanoStar and NanoFree Die-Size Ball Grid Array (DSBGA†)
Military: – FK Leadless Ceramic Chip Carrier (LCCC)
GB – Ceramic Pin Grid Array (CPGA)
HFP, HS, HT, HV – Ceramic Quad Flatpack (CQFP)
J, JT – Ceramic Dual-In-Line Package (CDIP)
W, WA, WD – Ceramic Flatpack (CFP)

10 Tape and Reel

Devices in the DB and PW package types include the R designation for reeled product. Existing product inventory designated LE may remain, but all products are being converted to the R designation.

Examples: Old Nomenclature – SN74LVTxxxDBLE
New Nomenclature – SN74LVTxxxADBR
LE – Left Embossed (valid for DB and PW packages only)
R – Standard (valid for all surface-mount packages)

There is no functional difference between LE and R designated products, with respect to the carrier tape, cover tape, or reels used.

† DSBGA is the JEDEC reference for wafer chip scale package (WCSP).

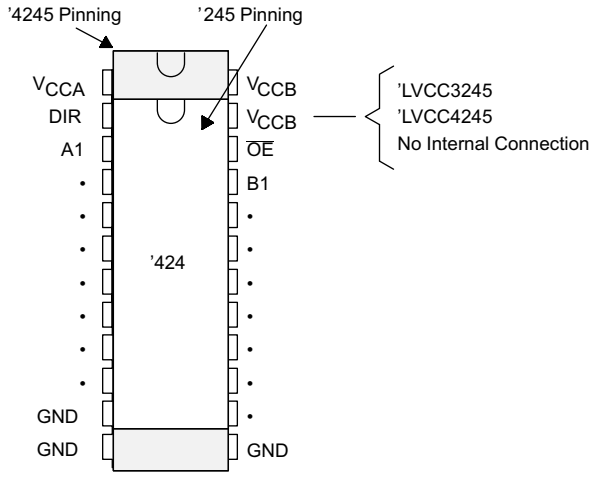
Figure 19. Device Number and Package Designators for TI Devices

Special features of TI standard logic devices are designated in the device number by abbreviations, as shown in the following list and defined in the following paragraphs.

- Blank - No special features
- C - Configurable V_{CC}
- D - Level-shifting diode
- H - Bus hold
- K - Undershoot-protection circuitry
- R - Damping resistor on inputs/outputs
- S - Schottky clamping diode
- Z - Power-up 3-state

4.1.1.1 Configurable V_{CC} (C)

Configurable V_{CC} is a feature of devices that are designed as dual-supply level shifters, for example, SN74LVCC3245A and SN74LVCC4245A. Using these devices allows selection of the voltage to be applied to V_{CC} on the B-port side (V_{CCB}) or A-port side (V_{CCA}) (see Figure 20).



	V_{CCA} A Port	V_{CCB} B PORT	TRANSLATION (BIDIRECTIONAL FLOW)
SN74LVCC3245A	2.3 V-3.6 V	3 V-5.5 V	2.5 V to 3.3 V or 3.3 V to 5 V
SN74LVCC4245A	5 V	3 V-5 V	5 V to 3.3 V

Figure 20. Example of Configurable V_{CC} Devices

Designers can use these devices in existing single-voltage systems. When systems become mixed-voltage systems, these devices do not need to be replaced, allowing for quicker time to market.

4.1.1.2 Level-Shifting Diode (D)

Devices with D as part of the device number have an integrated diode in the V_{CC} line. Examples are crossbar switches SN74CBTD3306 (with the integrated diode) and SN74CBT3306 (without the integrated diode). These devices allow 5-V to 3.3-V translation if no drive is required. Bidirectional data transmission is allowed between 5-V TTL and 3.3-V LVTTL, whereas only unidirectional level translation is allowed from 5-V CMOS to 3.3-V LVTTL (see Figure 21). The integrated diode saves designers both board space and component cost.

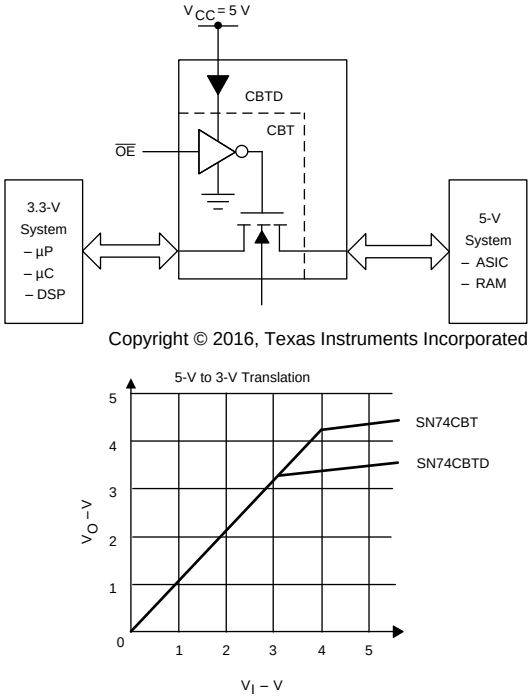


Figure 21. CBT vs CBTD With Internal Diode

4.1.1.3 Bus-Hold (H)

A bus-hold circuit is implemented in selected logic families to help solve the floating-input problem inherent in all CMOS inputs (refer to the application report, *Implications of Slow or Floating CMOS Inputs,* literature number SCBA004). The bus-hold circuit maintains the last known input state into the device and, as an additional benefit, pullup or pulldown resistors no longer are needed (see Figure 22). The advantages of devices with this circuit are board-space savings and reduced component costs.

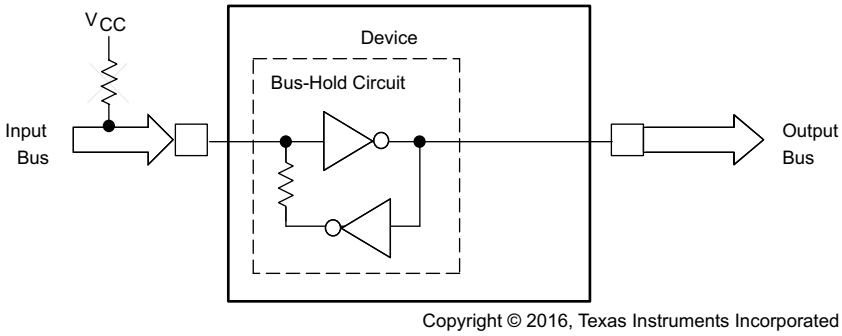


Figure 22. Benefit of Using Bus-Hold Devices

4.1.1.4 Damping Resistor on Inputs/Outputs (R)

Series damping resistors (SDR), denoted by R in the device number, are included at all input/output and output ports of designated devices (see Figure 23). The SDRs limit the current, thereby reducing signal undershoot and overshoot noise. Additionally, SDRs make line termination easier, which improves signal quality by reducing ringing and line reflections.

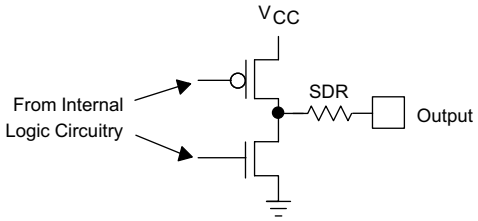


Figure 23. Series-Damping-Resistor Option

4.1.1.5 Schottky Clamping Diode (S)

Schottky diodes are incorporated in inputs and outputs to clamp undershoot (see Figure 24). The Schottky diodes prevent undershoot signals from dropping below a specified level, reducing the possibility of damage to connected devices by large undershoots that can occur without the Schottky diodes.

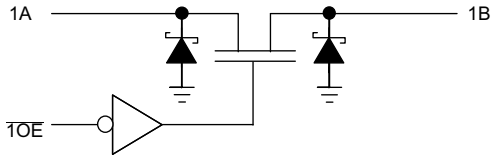
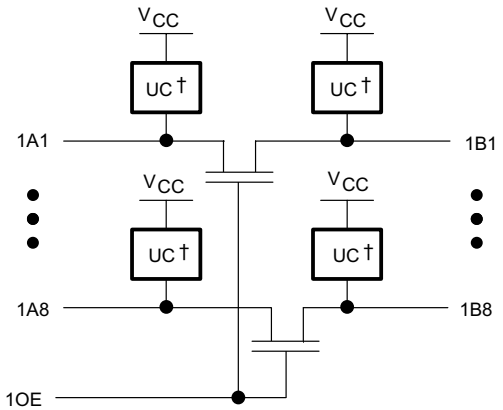


Figure 24. Schottky Clamping-Diode Device Schematic

4.1.1.6 Undershoot-Protection Circuitry (K)

TI undershoot-protection circuitry (UPC) functions similarly to Schottky clamping diodes, with one major difference. UPC is an active clamping structure. UPC can greatly reduce undershoot voltage, increasing protection from corrupted data (see Figure 25).



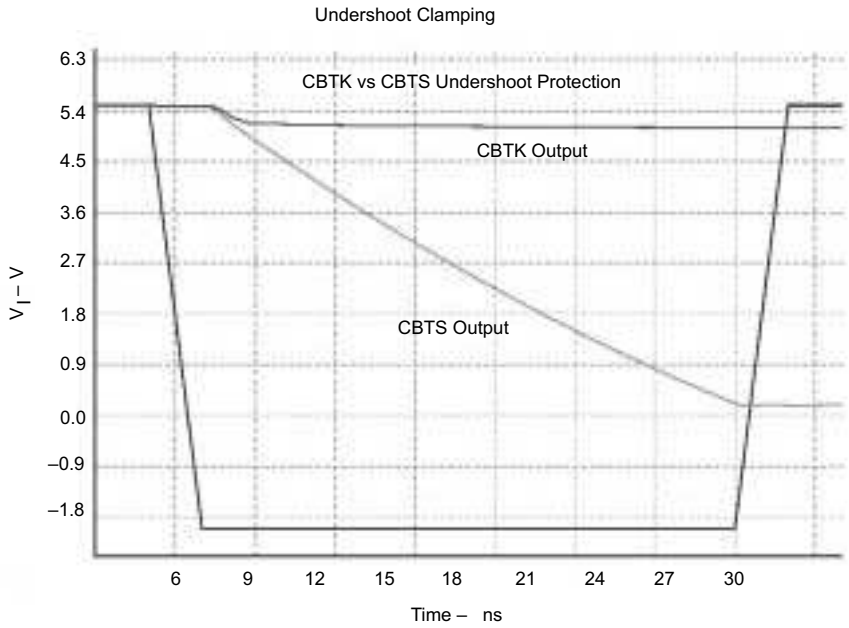


Figure 25. Undershoot-Proctection Circuity in K-Option Devices

4.1.1.7 Power-Up 3-State (Z)

The power-up 3-state (PU3S) feature ensures valid output levels during power up and ensures the valid high-impedance state during power down. The output enable pin ($\overline{OE}$) must be tied high (to V_{CC}) through an external pullup resistor (see Figure 26). For more information, see I_{OZPD} and I_{OZPU} specifications in the *Electrical Characteristics* section.

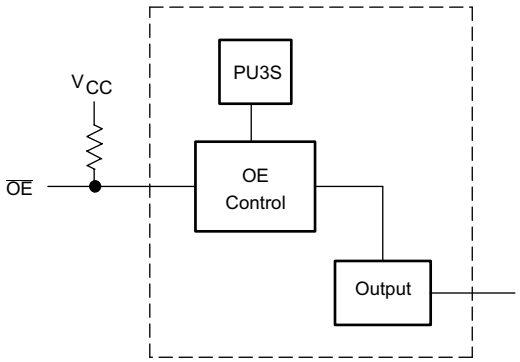


Figure 26. PU3S Circuit Implementation

4.1.2 Features Bullets

The *Features* section highlights information about the salient functions, features, and benefits of the device. Some features bullets provide an indication of functionality and application of the device, such as "Eight D-type Flip-Flops in a Single Package", "3-State Outputs", "Carry Output for N-bit Cascading" (for a binary counter), "Performs Parallel-to-Serial Conversion", or "Bidirectional Interface Between GTLP Signal Levels and LVTTL Logic Levels". Some data sheets contain electrostatic discharge (ESD) or latch-up test results and the associated JEDEC test conditions. The following are explanations of some common features bullets.

- Flow-Through Architecture Optimizes PCB Layout
- The data inputs and corresponding outputs are on opposite sides of the package. This feature makes printed circuit board trace routing easier.
- Bus-Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Active bus-hold circuitry holds unused or non-driven inputs at a valid logic state. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended. For more information on bus hold refer to the TI application report, *Bus-Hold Circuit*, literature number SCLA015.
- I_{off} Supports Partial-Power-Down Mode Operation
- This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.
- I_{off} and Power-Up 3-State Support Hot Insertion
- This device is fully specified for hot-insertion applications using I_{off} and power-up 3-state. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down. The power-up 3-state circuitry places the outputs in the high-impedance state during power up and power down, which prevents driver conflict.
- I_{off}, Power-up 3-State, and BIAS V_{CC} Support Live Insertion
- This device is fully specified for live-insertion applications using I_{off}, power-up 3-state, and BIAS V_{CC}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down. The power-up 3-state circuitry places the outputs in the high-impedance state during power up and power down, which prevents driver conflict. The BIAS V_{CC} circuitry precharges and preconditions the input/output connections on a device port, preventing disturbance of active data on the bus during card insertion or removal and permits true live-insertion capability.

4.1.3 Package Options and Pinouts

This section contains a top-view illustration of the leaded-package pinout(s) and a bottom view of certain nonleaded packages. Package dimensions and other package information is available in the *Mechanical Data* section of the *Semiconductor Group Packaging Outlines Reference Guide*, or *Analog and Logic packaging* literature number SSZB138A.

4.1.4 Applications

The *Applications* section contains a list of the typical system applications the device can used in.

4.1.5 Description

The *Description* section contains a written detailed explanation of the functionality and features of the device.

4.1.6 BGA Packaging Top-View Illustrations and Pin-Assignments Table

This section contains the top-view illustrations and pin assignments for applicable BGA package types.

4.1.7 Device Information

A table is provided that gives the fully qualified orderable part number and topside symbolization for every package option of the device.

TI has converted to an advanced order-entry system that provides significant improvements to all facets of TI business, from production, to order entry, to logistics. One requirement is a limitation of TI part numbers to no more than 18 characters. Based on customer inputs, TI determined that the least-disruptive implementations would be as outlined below:

1. Package alias

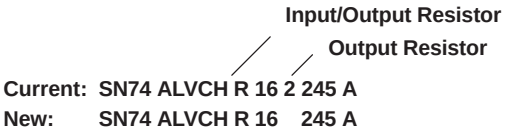
   TI uses an alias to denote specific packages for device numbers that exceed 18 characters. Table 1 shows a mapping of package codes to an alias representation.

Table 1. Package Alias

Current Package Code	Alias
DL	L
DGG/DBB	G
DGV	V
GKE/GKF/GQL	K
DLR	LR - tape/reel packing
DGGR/DBBR	GR - tape/reel packing
DGVR	VR - tape/reel packing
GKER/GKFR/GQLR	KR - tape/reel packing

2. Resistor-option nomenclature

   For device numbers of more than 18 characters and with input and output resistors, TI has adopted a simplified nomenclature to designate the resistor option. This eliminates the redundant "2" (designating output resistors) when the part number also contains an "R" (designating input/output resistors).



There is no change to the device or data sheet electrical parameters. The packages involved and the changes in nomenclature are given in Table 1.

The approximate body size in millimeters are given for each of the package .

4.1.8 Function Table

The function table illustrates the expected logic values on the outputs, when the inputs have the given stimuli applied.

The following symbols are used in function tables in TI data sheets:

H	=	high level (steady state)
L	=	low level (steady state)
↑	=	transition from low to high level
↓	=	transition from high to low level
→	=	value/level or resulting value/level is routed to indicated destination
↶	=	value/level is re-entered
X	=	irrelevant (any input, including transitions)
Z	=	off (high-impedance) state of a 3-state output
a . . . h	=	the level of steady-state inputs A through H, respectively
Q_0	=	level of Q before the indicated steady-state input conditions were established
$\overline{Q}_0$	=	complement of Q_0 or level of $\overline{Q}$ before the indicated steady-state input conditions were established
Q_n	=	level of Q before the most-recent active transition indicated by ↓ or ↑
⎍	=	one high-level pulse
⎎	=	one low-level pulse
Toggle	=	each output changes to the complement of its previous level on each active transition indicated by ↓ or ↑

In the input columns, if a row contains only the symbols H, L, or X, the indicated output is valid when the input configuration is achieved, regardless of the sequence in which it is achieved. The output persists as long as the input configuration is maintained.

In the input columns, if a row contains H, L, and/or X, together with ↑ and/or ↓, the output is valid when the input configuration is achieved, but the transition(s) must occur after steady-state levels are attained. If the output is shown as a level (H, L, Q_0, or $\overline{Q}_0$), it persists as long as the steady-state input levels and the levels that terminate indicated transitions are maintained. Unless otherwise indicated, input transitions in the opposite direction to those shown have no effect at the output. If the output is shown as a pulse, "-" , or "- -", the pulse follows the indicated input transition and persists for an interval that is dependent on the circuit.

Among the most complex function tables are those of the shift registers. These embody most of the symbols used in any of the function tables, and more. Table 2 is the function table of a 4-bit bidirectional universal shift register.

Table 2. Function Table

INPUTS										OUTPUTS			
CLEAR	MODE		CLOCK	SERIAL		PARALLEL				Q_A	Q_B	Q_C	Q_D
	S1	S0		LEFT	RIGHT	A	B	C	D				
L	X	X	X	X	X	X	X	X	X	L	L	L	L
H	X	X	L	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
H	H	H	↑	X	X	a	b	c	d	a	b	c	d
H	L	H	↑	X	H	H	H	H	H	H	Q_{An}	Q_{Bn}	Q_{Cn}
H	L	H	↑	X	L	L	L	L	L	L	Q_{An}	Q_{Bn}	Q_{Cn}
H	H	L	↑	H	X	X	X	X	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	H
H	H	L	↑	L	X	X	X	X	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	L
H	L	L	X	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}

The first row of the table represents a synchronous clearing of the register and states that, if clear is low, all four outputs will be reset low, regardless of the other inputs, which are denoted by X. In the following rows, clear is inactive (high); therefore, it has no effect.

The second row shows that, as long as the clock input remains low (while clear is high), no other input has any effect, and the outputs maintain the levels they assumed before the steady-state combination of clear high and clock low was established. Because, on other rows of the table only the rising transition of the clock is shown to be active, the second row implicitly shows that no further change in the outputs occurs while the clock remains high or on the high-to-low transition of the clock.

The third row of the table represents synchronous parallel loading of the register and states that if S1 and S0 are both high, then, without regard to the serial input, the data entered at A is at output Q_A, data entered at B is at Q_B, and so forth, following a low-to-high clock transition.

The fourth and fifth rows represent the loading of high- and low-level data, respectively, from the shift-right serial input and the shifting of previously entered data one bit; data previously at Q_A is now at Q_B, the previous levels of Q_B and Q_C are now at Q_C and Q_D, respectively, and the data previously at Q_D no longer is in the register. This entry of serial data and shift takes place on the low-to-high transition of the clock when S1 is low and S0 is high, and the levels at inputs A through D have no effect.

The sixth and seventh rows represent the loading of high- and low-level data, respectively, from the shift-left serial input and the shifting of previously entered data one bit; data previously at Q_B is now at Q_A, the previous levels of Q_C and Q_D now are at Q_B and Q_C, respectively, and the data previously at Q_A no longer is in the register. This entry of serial data and shift takes place on the low-to-high transition of the clock when S1 is high and S0 is low, and the levels at inputs A through D have no effect.

The last row shows that, as long as both inputs are low, no other input has any effect and, as in the second row, the outputs maintain the levels they assumed before the steady-state combination of clear high and both mode inputs low was established.

The function table functional tests do not reflect all possible combinations or sequential modes.

4.1.9 Logic Diagram

The logic diagram is a positive-logic illustration of the Boolean functionality of the device. Furthermore, in some logic-device data sheets that have wide identical configurations, such as a 16-bit or a 32-bit device, the logic diagram often is shown in partial format that includes the unique circuitry and only one of the data paths.

For D-type flip-flops and latches, it is TI convention to name the outputs and other inputs of a D-type flip-flop or latch and to draw its logic symbol, based on the assumption of true data (D) inputs. Outputs that produce data in phase with the data inputs are called Q, and those producing complementary data are called $\overline{Q}$. An input that causes a Q output to go high or a $\overline{Q}$ output to go low is called preset (PRE). An input that causes a $\overline{Q}$ output to go high or a Q output to go low is called clear (CLR). Bars are placed over these pin names ($\overline{PRE}$ and $\overline{CLR}$) if they are active low.

The devices on several data sheets are second-source designs, and the pin-name conventions used by the original manufacturers have been retained. That makes it necessary to designate the inputs and outputs of the inverting circuits, $\overline{D}$ and Q.

In some applications, it may be advantageous to re-designate the data input from D to $\overline{D}$, or vice versa. In that case, all the other inputs and outputs should be renamed, as shown Figure 27. Also shown, are corresponding changes in the graphical symbols. Arbitrary pin numbers are shown.

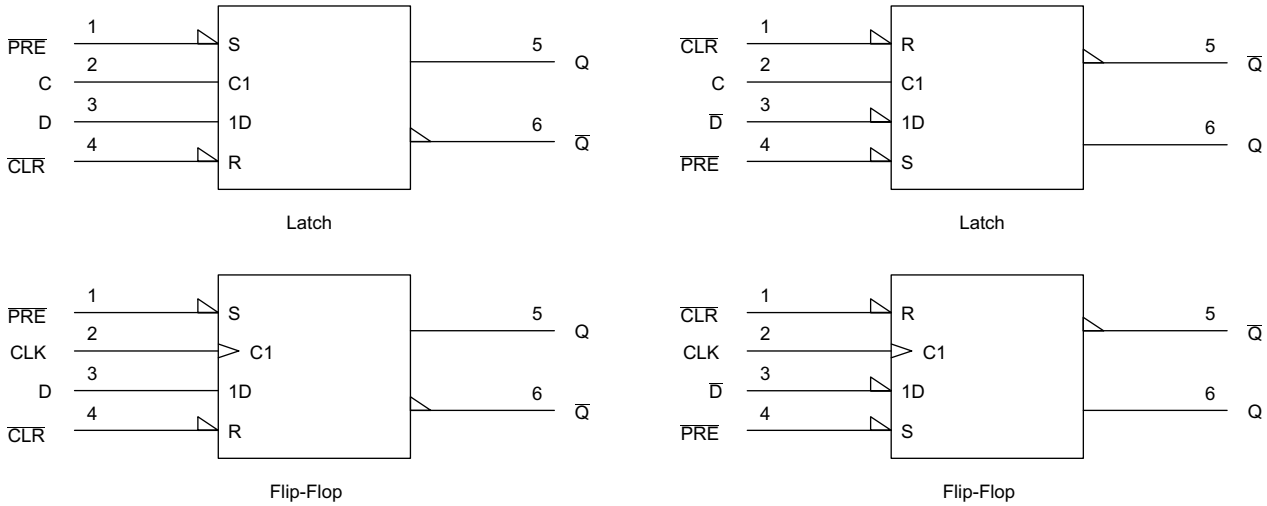


Figure 27. Example Logic Diagram

The figures show that when Q and $\overline{Q}$ exchange names, the preset and clear pins also exchange names. The polarity indicators (⊾) on $\overline{PRE}$ and $\overline{CLR}$ remain, as these inputs still are active low, but the presence or absence of the polarity indicator changes at D (or $\overline{D}$), Q, and $\overline{Q}$. Pin 5 (Q or $\overline{Q}$) is still in phase with the data input (D or $\overline{D}$); their active levels change together.

4.1.10 Product Development Stage Note

The product development stage note is a standard disclaimer placed at the lower left corner of the first page of data sheets, and the words **ADVANCED INFORMATION** or **PRODUCT PREVIEW**, as applicable, appear in the left and right margins of all pages of the data sheet. There is only the product development stage note on the first page for production-data devices. For additional information, see the EIA/JEDEC engineering publication, *Suggested Product-Documentation Classifications and Disclaimers*, JEP103A.

4.1.11 Table Of Contents

The *Table of Contents* section provides the outline for the data sheet with each section and a hyperlink which when clicked to take directly to the specified page.

4.2 Revision History

The changes for the data sheet compared to previous revision is mentioned in a tabular format along with the pages affected in the *Revision History*.

4.3 Pin Configuration And Functions

Each of the packages top view or the bottom view (whenever applicable) is shown along with a tabular representation of the name of each pin , the pin position in each of the packages and the description of each pin. Each pin being input , output , Input /Output , power or ground pin is also mentioned in the same table.

4.4 Absolute Maximum Ratings

4.4.1 Supply Voltage, V_{CC}

This is the maximum voltage that can be applied safely to the V_{CC} terminal, with respect to the ground of the device. However, no data sheet parameters are ensured when a device is operated at the absolute maximum V_{CC} level.

4.4.2 Input Voltage, V_I

This is the maximum voltage that can be applied safely to an input terminal, with respect to the ground of the device. This maximum V_I specification may be exceeded if the output clamp rating, I_{IK}, is observed.

Helpful Hint:

If there are clamp diodes between the device inputs and the V_{CC} supply (see Figure 28) for ESD protection or overshoot clamping, the positive absolute-maximum rating for the input voltage is specified as V_{CC} + 0.5 V. Keeping the applied input voltage less than 0.5 V above V_{CC} ensures that there will not be enough voltage across the clamp diode to forward-bias it and cause current to flow through it. The TI logic families with clamp diodes in the inputs are: AC, ACT, AHC, AHCT, ALB, ALS, ALVC, AS, F, (CD)FCT, HC, HCT, HSTL, LS, PCA, PCF, S, SSTL, and TTL.

If there are no clamp diodes between the device inputs and the V_{CC} supply, the positive absolute maximum rating is a limitation of the process technology and is specified as an absolute voltage (for example, 5.5 V). The TI logic families without clamp diodes in the inputs are: ABT, ABTE, ALS, ALVT, AUC, AVC, BCT, FB, GTLP, GTL, LS, LV, LVC, LVCZ, LVT, (CY)FCT, SSTV, and VME.

You may exceed the negative input-voltage rating if you ensure that you are not putting too much current through the ground-clamp diode. The I_{IK} absolute maximum rating specifies the maximum current that may be put through the ground-clamp diode.

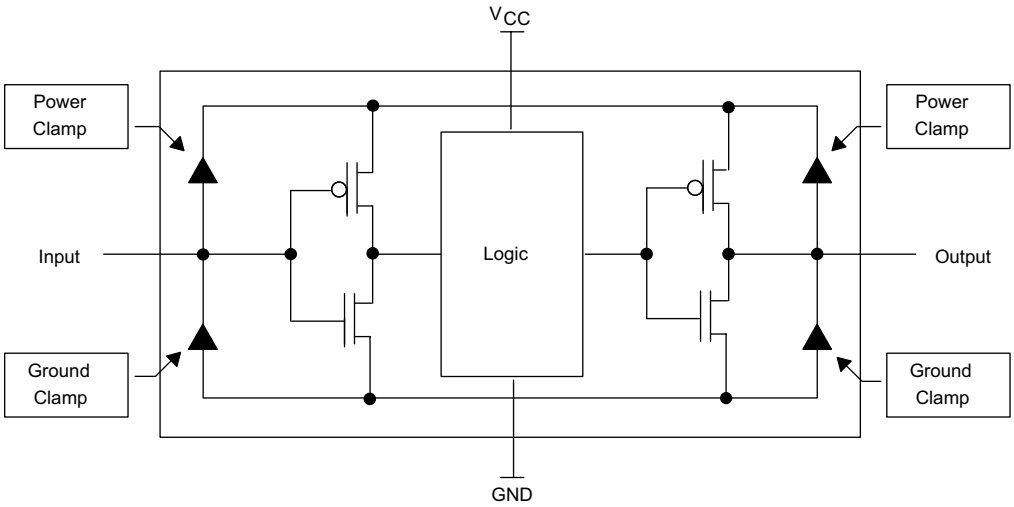


Figure 28. Representation of Typical Logic I/O Clamping Circuits

4.4.3 Output Voltage, V_O

This is the maximum voltage that can be applied safely to an output terminal, with respect to the ground of the device.

Helpful Hint:

If there are clamp diodes between the device outputs and the V_{CC} supply (see Figure 28) for ESD protection or parasitic current paths in the output p-channel pullup transistor, the positive absolute maximum rating for the output voltage is specified as V_{CC} + 0.5 V. This ensures that there will not be enough voltage applied between the output and V_{CC} to forward bias the clamp diode and cause current to flow. You may exceed the negative rating if you ensure that you are not putting too much current through the ground-clamp diode. The maximum current that you may put through the ground-clamp diode is specified in the I_{OK} absolute maximum rating.

If there are no clamp diodes or parasitic current paths in the output P-channel pullup transistor between the device outputs and the V_{CC} supply, the positive absolute maximum rating is a limitation of the process technology and is specified as an absolute voltage.

4.4.4 Voltage Range Applied to Any Output in the High-Impedance or Power-Off State, V_O

This specification is similar to the *Output Voltage, V_O* specification and is used with the *Voltage Range Applied to Any Output in the High State, V_O* specification. On devices with the I_{off} feature, there are no clamp diodes or parasitic current paths in the output P-channel pullup transistor between the device outputs and the V_{CC} supply; the positive absolute-maximum rating is a limitation of the process technology and is specified as an absolute voltage. You may exceed the negative rating if you ensure that you are not putting too much current through the ground-clamp diode. The maximum current that you may put through the ground-clamp diode is specified in the I_{OK} absolute-maximum rating.

Helpful Hint:

This specification is necessary only for devices with the I_{off} feature.

4.4.5 Voltage Range Applied to Any Output in the High State, V_O

This specification is similar to the *Output Voltage, V_O* specification and is used with the *Voltage Range Applied to Any Output in the High-Impedance or Power-Off State, V_O* specification. When the output is enabled and is in the output high state, there is a current path between the output and V_{CC} through the output P-channel pullup transistor. Applying a voltage to the output that is greater than the V_{CC} voltage causes damaging current to flow back from the output into the V_{CC} supply. You may exceed the negative rating if you ensure that you are not putting too much current through the power-clamp diode. The I_{OK} absolute-maximum rating specifies the maximum current that you may put through the ground-clamp diode.

Helpful Hint:

This specification is necessary only for devices with the I_{off} feature.

4.4.6 Input Clamp Current, I_{IK}

This is the maximum current that can flow safely into an input terminal of the device at voltages above or below the normal operating range.

Helpful Hint:

If there are clamp diodes between the device inputs and the V_{CC} supply (see Figure 28), for ESD protection or overshoot clamping, there will be both a positive and negative absolute maximum rating for the input clamp current. If there is only a negative absolute maximum rating, that implies that there is only a ground-clamp diode at the input, not a power-clamp diode.

4.4.7 Output Clamp Current, I_{OK}

This is the maximum current that can flow safely into an output terminal of the device at voltages above or below the normal operating range.

Helpful Hint:

If there are clamp diodes between the device outputs and the V_{CC} supply (see Figure 28), for ESD protection or parasitic current paths in the output P-channel pullup transistor, there will be both a positive and a negative absolute-maximum rating for the output clamp current. If there is only a negative absolute-maximum rating, that implies that there is only a ground-clamp diode at the output, not a power-clamp diode or a parasitic current path in the output P-channel pullup transistor.

4.4.8 Continuous Output Current, I_O

This is the maximum output source or sink current that can flow safely into an output terminal of the device at voltages within the normal operating range.

4.4.9 Continuous Current Through V_{CC} or GND Terminals

This is the maximum current that can flow safely into the V_{CC} or GND terminals of the integrated circuit.

4.4.10 Package Thermal Impedance, Junction-to-Ambient, Θ_{JA}

This is the thermal resistance from the operating portion of a semiconductor device to a natural convection (still air) environment surrounding the device. Tested per JEDEC Standard JESD51-3. For additional information, refer to the TI Application Report; *Thermal Characteristics of Standard Linear and Logic (SLL) Packages and Devices*, literature number SCZA005.

4.4.11 Storage Temperature Range, T_{stg}

This is the range of temperatures over which a device can be stored without causing excessive degradation of its performance characteristics. Typically, the junction temperature T_J is the same as storage temperature.

4.5 Recommended Operating Conditions

4.5.1 V_{CC} Supply Voltage

JEDEC - The supply voltage applied to a circuit connected to the reference terminal.

TI - The range of supply voltages for which operation of the logic element is specified.

The example in Figure 11 lists 2.7 V as the minimum V_{CC}. No electrical or switching characteristic is specified for V_{CC} less than 2.7 V. Operation outside of the minimum and maximum values is not recommended, and a previously established logic state might not be maintained under such conditions.

Helpful Hint:

Frequently, TI receives requests from customers wanting assurance that TI logic devices will operate properly outside of specified conditions. The logic device may, indeed, perform flawlessly in the application posed by the customer, but TI does not represent that the device will provide the same level of reliability and performance when operated outside of specified conditions.

4.5.2 BIAS V_{CC} Bias Supply Voltage

JEDEC - *no definition offered*

TI - A supply voltage used in generating a precharge voltage that is applied to an I/O for live-insertion purposes.

Power sequencing is critical in live-insertion applications. Therefore, care must be taken with the timing of application of BIAS V_{CC}, V_{CC}, ground, and data input voltages during an insertion or extraction of a daughter card implementing a device with this capability (see the application report, *Logic in Live-Insertion Applications With a Focus on GTLP,* literature number SCEA026).

Helpful Hint:

Texas Instruments offers only three technologies with true live-insertion capabilities: FB, GTLP, and VME.

4.5.3 V_{TT} Termination Voltage

JEDEC - *no definition offered*

TI - A supply voltage used to terminate a bus (most commonly used in open-drain devices) and in generating a reference voltage for differential inputs.

Because open-drain devices such as GTLP and FB cannot raise the output voltage to a high state by their own accord, external resistors, which are tied to an external termination voltage, are used.

Helpful Hint:

V_{TT} determines the high-level voltage value and, since most open-drain technologies can tolerate a wide range of voltage levels, open-drain devices are used quite often in voltage-translation applications.

4.5.4 V_{ref} Reference Voltage

JEDEC - A power supply that acts as a reference for determining internal threshold voltages, but does not supply any substantial power to the device.

TI - A reference bias voltage used to set the switching threshold of differential input devices.

4.5.5 V_{IH} High-Level Input Voltage

JEDEC - V_{IH} min is the least positive (most negative) value of high-level input voltage for which operation of the logic element within specification limits is to be expected. V_{IH} max is the most positive (least negative) value of high-level input voltage for which operation of the logic element within specification limits is to be expected.

TI - An input voltage within the more positive (the less negative) of the two ranges of values used to represent the binary variables.

NOTE: A minimum is specified that is the least positive value of high-level input voltage for which operation of the logic element within specification limits is to be expected.

A voltage within this range corresponds to the logic-1 state in positive logic. During device testing, V_{IH} min is specified for all inputs. Since V_{IH} min is used to set up V_{OH}, V_{OL}, I_{OZH}, and I_{OZL} tests, all possible combinations of input thresholds may not be verified. The non-data inputs (for example, direction, clear, enable, and preset) may be considered unused inputs and may not be at threshold conditions. These inputs control functions that can cause all the outputs to switch simultaneously. The noise that can be generated by switching a majority of the outputs at one time can cause significant tester ground and V_{CC} movement. This can result in false test measurements.

Helpful Hint:

Some bipolar-input devices sink a certain amount of current into the input pin, as specified on the data sheet. The higher the V_{IH} voltage is, the more current that will be drawn into the input pin. CMOS-input devices behave in a different manner because, in most cases, the input pin essentially is tied directly to the high-impedance gate of an input inverter. In a static dc state, a CMOS input sinks or sources only a minute amount of leakage current (a few µA). However, it is imperative that for any logic device, but especially for a CMOS input, the input high logic level always be above the recommended V_{IH} min. Failure to do this causes a surge of current to flow through the input inverter from the V_{CC} supply to ground and, subsequently, may destroy the device.

Helpful Hint:

TI data sheets do not specify a V_{IH} max that typically is found in competitor data sheets. Instead, see V_I max for the same value.

Helpful Hint:

Failure to supply a voltage to the input of a CMOS device that meets the V_{IH} or V_{IL} recommended operating conditions can cause: (1) propagation of incorrect logic states, (2) high I_{CC} currents, (3) high input noise gain and oscillations, (4) power- and ground-rail surge currents and noise, and (5) catastrophic device and circuit failure.

Helpful Hint:

A device with an input V_{IH} = 2 V and a V_{IL} = 0.8 V has a TTL-compatible input. A device with the input levels scaled with respect to V_{CC} (for example, $V_{IH} = 0.7 \times V_{CC}$, $V_{IL} = 0.3 \times V_{CC}$) has CMOS inputs.

4.5.6 V_{IL} Low-level Input Voltage

JEDEC - V_{IL} min is the least-positive (most negative) value of low-level input voltage for which operation of the logic element within specification limits is to be expected. V_{IL} max is the most positive (least negative) value of low-level input voltage for which operation of the logic element within specification limits is to be expected.

TI - An input voltage within the less positive (more negative) of the two ranges of values used to represent the binary variables.

NOTE: A maximum is specified that is the most-positive value of low-level input voltage for which operation of the logic element within specification limits is to be expected.

A voltage within this range corresponds to the logic-0 state in positive logic. During device testing, V_{IL} max is specified for all inputs. Because V_{IL} max is used to set up V_{OH}, V_{OL}, I_{OZH}, and I_{OZL} tests, all possible combinations of input thresholds may not be verified. The non-data inputs (for example, direction, clear, enable, and preset) may be considered unused inputs and may not be at threshold conditions. These inputs control functions that can cause all the outputs to switch simultaneously. The noise that can be generated by switching a majority of the outputs at one time can cause significant tester ground and V_{CC} changes. This can result in false test measurements.

Helpful Hint:

Most bipolar-input devices source a certain amount of current out of the input pin, as specified on the data sheet. The lower the V_{IL} voltage is, the more current that will be drawn out of the input pin. CMOS-input devices behave in a different manner because, in most cases, the input pin essentially is tied directly to the gate of an input inverter. In a static dc state, a CMOS input sinks or sources only a minute amount of leakage current (a few µA). However, it is imperative that for any logic device, but especially for a CMOS input, the input low logic level always be below the recommended V_{IL} max.

CAUTION

Failure to do this will cause a surge of current to flow through the input inverter from the V_{CC} supply to ground and, subsequently, may destroy the device.

Helpful Hint:

TI data sheets do not specify a V_{IL} min that typically is found in competitor data sheets. Instead, see V_I min for the same value.

Helpful Hint:

Failure to supply a voltage to the input of a CMOS device that meets the V_{IH} or V_{IL} recommended operating conditions can cause: (1) propagation of incorrect logic states, (2) high I_{CC} currents, (3) high input noise gain and oscillations, (4) power- and ground-rail surge currents and noise, and (5) catastrophic device and circuit failure.

Helpful Hint:

A device with an input V_{IH} = 2 V and a V_{IL} = 0.8 V has a TTL-compatible input. A device with the input levels scaled with respect to V_{CC} (for example, $V_{IH} = 0.7 \times V_{CC}$, $V_{IL} = 0.3 \times V_{CC}$) has CMOS inputs.

4.5.7 I_{OH} High-Level Output Current

JEDEC - The current into the output terminal with input conditions applied that, according to the product specification, establishes a high level at the output.

TI - The current into an output with input conditions applied that, according to the product specification, establishes a high level at the output.

TI data sheets specify currents flowing out of a device as a negative value. I_{OH} max is used as a test condition for V_{OH}. See V_{OH} testing for further details.

Logic output drivers have a maximum current drive capability that they can source and still be able to sustain a valid logic-high level. In a static dc state, where current is drawn continuously from the output, because CMOS drivers operate in the linear region, their behavior is somewhat like a low-impedance resistor and increases in voltage potential (that is, decreases the V_{OH} level) as the increasing current is sourced out of the output pin during a V_{OH} test. Consequently, a TI logic device operates with a high-level output current that is above the recommended operating range (but below the absolute maximum rating), but TI does *NOT* represent that the device can sustain the specified V_{OH} level or that the device will operate without any reliability concerns.

4.5.8 I_{OHS} Static High-Level Output Current

JEDEC - *no definition offered*

TI - The static and testable current into a Dynamic Output Control (DOC™ circuitry) output with input conditions applied that, according to the product specifications, establishes a static high level at the output. The dynamic drive current is not specified for devices with DOC circuitry outputs because of its transient nature; however, it is similar to the dynamic drive current that is available from a high-drive (nondamping resistor) standard-output device.

TI data sheets specify currents flowing out of a device as a negative value.

DOC circuitry is designed to drive CMOS input devices, which are capacitive in nature, in point-to-point applications (one receiver input per driver output). For this reason, a large static high-level output current is not required. In this case, what matters most is the high transient-drive capability of the output.

For additional information about DOC circuitry, refer to the TI application report, *Dynamic Output Control (DOC™) Circuitry Technology and Applications*, literature number SCEA009.

4.5.9 I_{OL} Low-Level Output Current

JEDEC - The current into the output terminal with input conditions applied that, according to the product specification, will establish a low level at the output.

TI - The current into an output with input conditions applied that, according to the product specification, establishes a low level at the output.

TI data sheets specify currents flowing out of a device as a negative value. I_{OL} maximum is used as a test condition for V_{OL}. See V_{OL} testing for details.

Logic output drivers have a maximum current-drive capability that they can sink and still be able to sustain a valid logic-low level. In a static dc state where current is continuously drawn into the output, because CMOS drivers operate in the linear region, their behavior will be somewhat like a low-impedance resistor and will increase in voltage potential (that is, increase the V_{OL} level) as the increasing current is sunk into the output pin during a V_{OL} test. Consequently, a TI logic device will operate with a low-level output current that is above the recommended operating range (but below the absolute maximum rating), but TI does *NOT* represent that the device can sustain the specified V_{OL} level or that the device will operate without any reliability concerns.

4.5.10 I_{OLS} Static Low-Level Output Current

JEDEC - *no definition offered*

TI - The static and testable current into a Dynamic Output Control (DOC circuitry) output with input conditions applied that, according to the product specifications, establishes a static low level at the output. The dynamic drive current is not specified for devices with DOC circuitry outputs because of its transient nature; however, it is similar to the dynamic drive current that is available from a high-drive (nondamping resistor) standard-output device.

TI data sheets specify currents flowing out of a device as a negative value.

DOC circuitry is designed to drive CMOS input devices, which are capacitive in nature, in point-to-point applications (one receiver input per driver output). For this reason, a large static low-level output current is not required. What matters most in this case is the high-transient-drive capability of the output.

For additional information about DOC circuitry, refer to the TI application report, *Dynamic Output Control (DOC™) Circuitry Technology and Applications*, literature number SCEA009.

4.5.11 V_I Input Voltage

JEDEC - The voltage at the input terminals.

TI - The range of input voltage levels over which the logic element is specified to operate.

V_I min and V_I max values are used as test conditions for the I_I, I_{CC}, ΔI_{CC}, C_i, and C_{io} test. See those specifications for details.

Helpful Hint:

If there are clamp diodes between the device inputs and the V_{CC} supply (see Figure 28) for ESD protection or overshoot clamping, the positive absolute maximum rating for the input voltage will be specified as V_{CC} + 0.5 V. Keeping the applied input voltage less than 0.5 V above V_{CC} ensures that there will not be enough voltage across the clamp diode to forward bias it and cause current to flow through it.

You may exceed the negative rating if you ensure that you are not putting too much current through the ground-clamp diode. The maximum current that you may put through the ground-clamp diode is specified in the I_{IK} absolute-maximum rating.

Helpful Hint:

This parameter provides a means to determine if the device is tolerant of a higher voltage than the supply voltage. If the input is overvoltage tolerant, the positive maximum rating for the input voltage will be an absolute voltage rating (for example, 5.5 V) and will be limited by the capabilities of the wafer-fab process. For example, the LVC technology is specified to operate at a voltage supply no higher than 3.6 V. However, the input voltage is recommended to be 5.5 V maximum. This indirectly states that the device is a 5-V tolerant device. The same can be said about AUC devices because the maximum supply voltage is 2.7 V, whereas the maximum input voltage is 3.6 V, making this technology 3.3-V tolerant.

Helpful Hint:

This parameter explicitly states the recommended minimum and maximum input voltage levels for any input. While the V_I specification typically spans the range from below ground to above V_{CC}, failure to supply a voltage to the input of a CMOS device that meets the V_{IH} or V_{IL} recommended operating conditions can cause: (1) propagation of incorrect logic states, (2) high I_{CC} currents, (3) high input noise gain and oscillations, (4) power- and ground-rail surge currents and noise, and (5) catastrophic device and circuit failure.

4.5.12 V_O Output Voltage

JEDEC - The voltage at the output terminals.

TI - The range of output voltage levels over which the logic element is specified.

V_O minimum and maximum values are used as test conditions for I_{OZH} and I_{OZL}. See these tests for details.

Helpful Hint:

The load at the output strictly determines the output voltage. As discussed in the V_{OH} and V_{OL} descriptions, a constant dc current decreases and increases, respectively, the output voltage. For this reason, TI does not recommend to drive bipolar inputs with CMOS outputs unless the sum of all bipolar input current is less than the rated I_{OH} and I_{OL} of the CMOS output. Highly capacitive loads, such as any CMOS type input, will not incur any static dc current, so a CMOS output voltage should be close to the rail when asserted high or low. Capacitive loads, not the ultimate static dc voltage level, determine the time it takes for the output to arrive at the logic high or low state.

4.5.13 $\Delta t/\Delta v$ Input Transition Rise or Fall Rate

JEDEC - *no definition offered*

TI - The rate of change of the input voltage waveform during a logic transition (low-to-high or high-to-low).

To avoid output-waveform abnormalities, input voltage transitions should be within the range set forth in the recommended operating conditions.

Customers often place external capacitors on a trace to ensure the driver does not switch rapidly from one logic state to another. This is sometimes done to prevent unwanted overshoot and undershoot voltage conditions that could cause ringing and degrade signal integrity, or in switch debounce circuits. However, this could cause problems at the input; therefore, TI provides input transition rise or fall rates. The problem may not arise due to external capacitive loading, however, but may be the result of choosing a device with a weak driver. In either case, the end result is a voltage waveform that is too slow for the device.

Slow transition rates wreak havoc on CMOS inputs because a slowly changing input voltage will induce a large amount of current from the power supply to ground. This phenomenon is known as *through current*. Through currents are normal ac transient currents, but when they are sustained indefinitely-as are those caused by slow input transition rates-the device will not perform as expected, and its output voltage may oscillate or, even worse, damage the device. This surge of current, if large enough, will disturb the ground reference because of the inductive nature of the package [V = L × (di/dt)] and produce a positive-going glitch on the ground reference. The glitch may, in turn, reduce the relative magnitude, causing the output node of the input inverter to switch states. Ultimately, this erroneous data propagates to the output of the device, thereby causing oscillations. The more inputs that are being switched in the same manner, the worse this condition becomes, as more current is being forced into ground during a short time. TI data sheets specify the slowest input transition rate to avoid this problem. For additional information, refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

Helpful Hint:

If you must supply a slowly changing voltage to the input of a logic device, select a device that has Schmitt-trigger inputs. These inputs have been specifically designed to tolerate slow edges. An example of such a device in the LVC family is the SN74LVC14A.

4.5.14 $\Delta t/\Delta V_{CC}$ Power-up Ramp Rate

JEDEC - *no definition offered*

TI - The rate of change of the supply voltage waveform during power up.

4.5.15 T_A Operating Free-Air Temperature

JEDEC - *no definition offered*

TI - The range of operating temperatures over which the logic element is specified.

In digital-system design, consideration must be given to thermal management of components. The small size of packages makes this more critical. Figure 36 shows the high-effect (high-K) thermal resistance for the 5-, 14-, 16-, 20-, 24-, 48-, 56-, 64-, and 80-pin packages for various rates of airflow calculated in accordance with JESD51-7.

The thermal resistance in Figure 36 can be used to approximate typical and maximum virtual junction temperatures. In general, the junction temperature for any device can be calculated using the following equation:

$$T_J = R_{\Theta JA} \times P_T + T_A \quad (1)$$

where

- T_J = virtual junction temperature (°C)
- $R_{\Theta JA}$ = thermal resistance junction to free air (°C/W)
- P_T = total power dissipation of the device (W)
- T_A = free-air temperature (°C)

More additional information on all the thermal metrics used for integrated circuit refer to the TI application report , *Semiconductor and IC package Thermal Metrics* ,SPRA953.

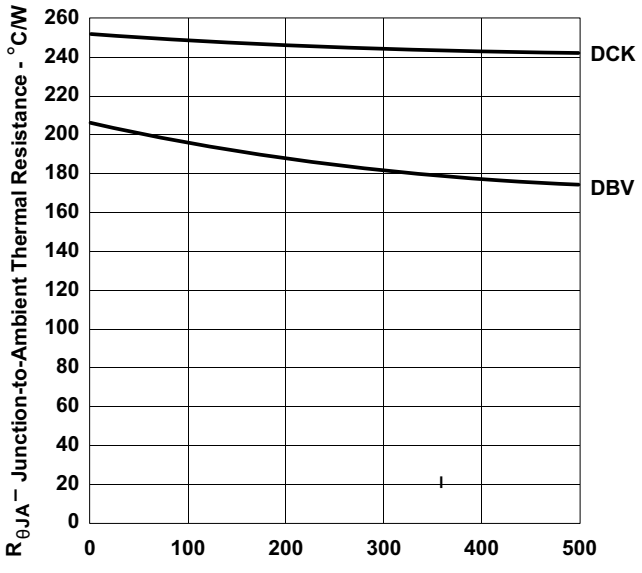


Figure 29. JUNCTION-TO-AMBIENT THERMAL RESISTANCE vs Air Velocity

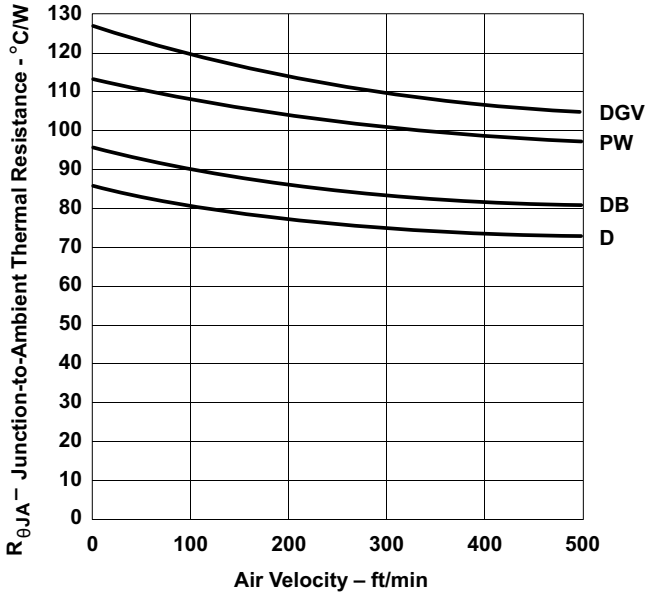


Figure 30. JUNCTION-TO-AMBIENT THERMAL RESISTANCE vs Air Velocity

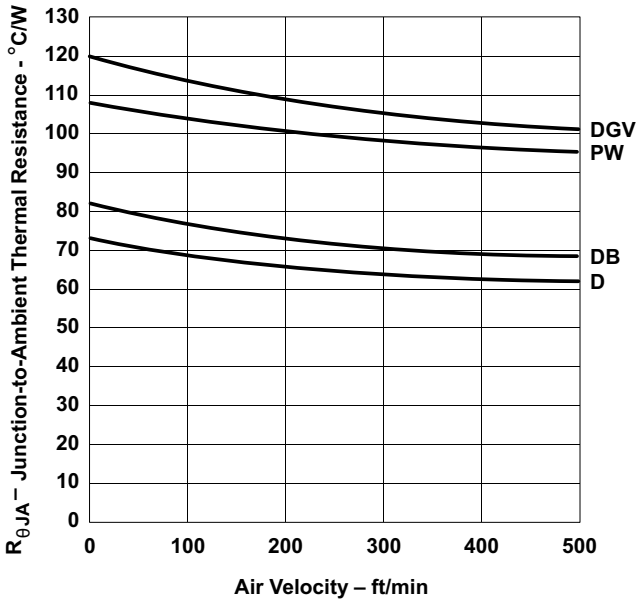


Figure 31. JUNCTION-TO-AMBIENT THERMAL RESISTANCE vs Air Velocity

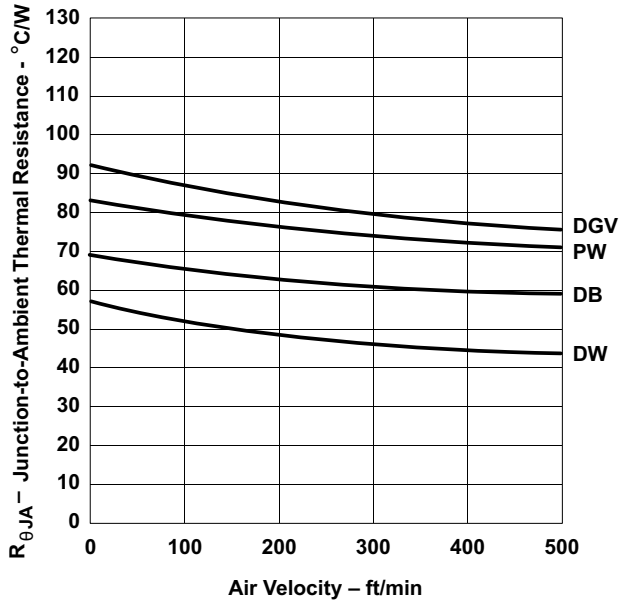


Figure 32. JUNCTION-TO-AMBIENT THERMAL RESISTANCE vs Air Velocity

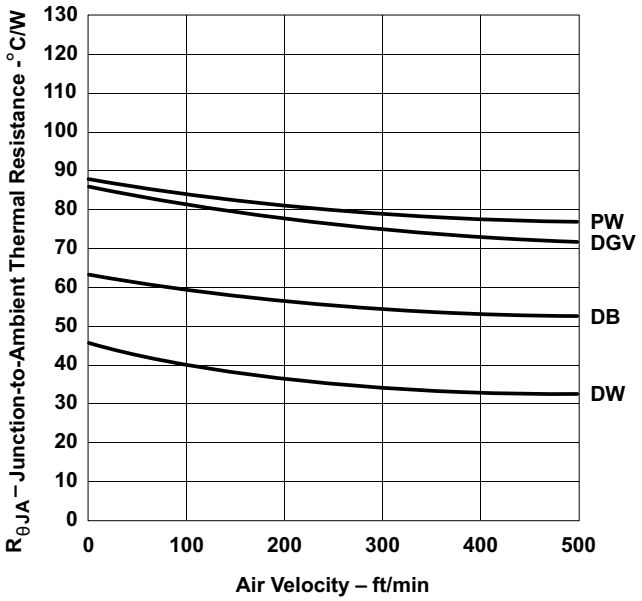


Figure 33. JUNCTION-TO-AMBIENT THERMAL RESISTANCE vs Air Velocity

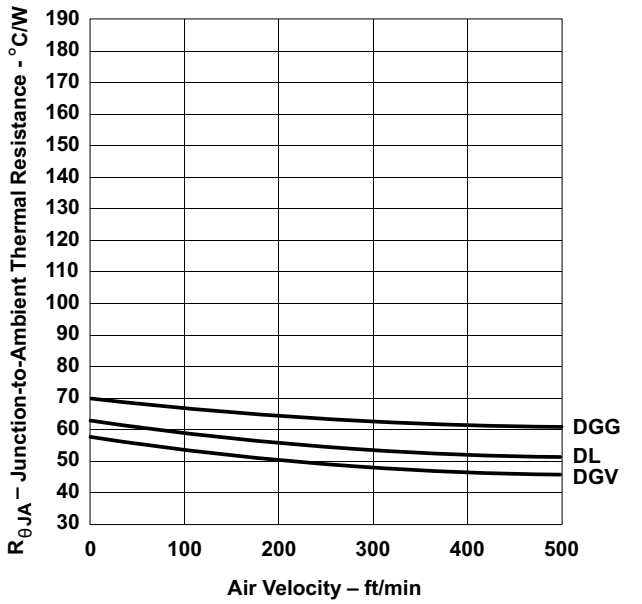


Figure 34. JUNCTION-TO-AMBIENT THERMAL RESISTANCE vs Air Velocity

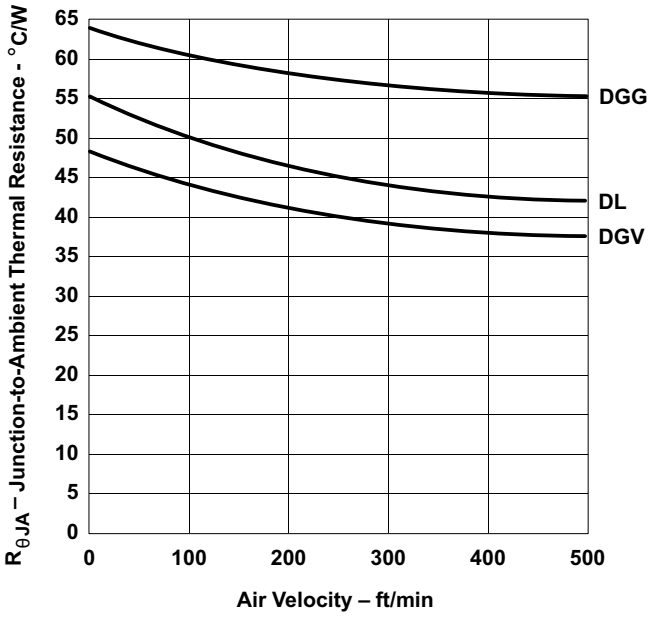


Figure 35. JUNCTION-TO-AMBIENT THERMAL RESISTANCE vs Air Velocity

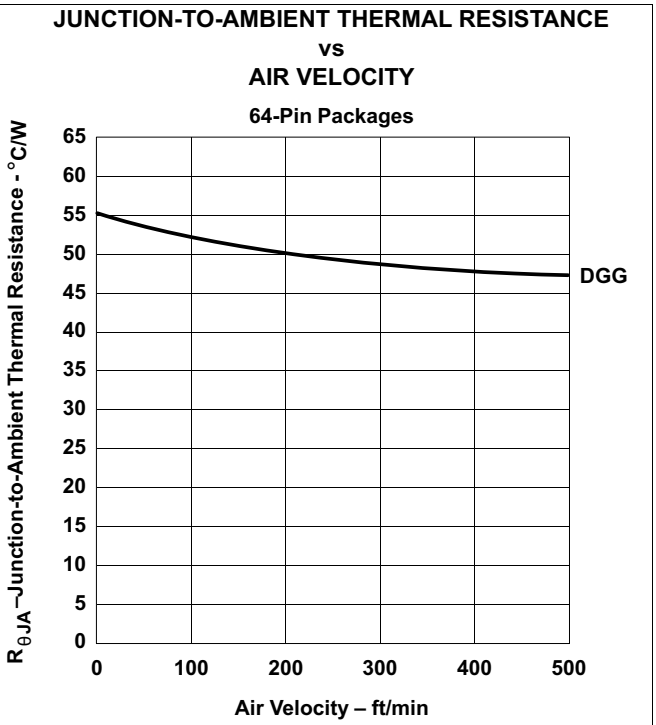


Figure 36. High-K Thermal-Resistance Images for 5-, 14-, 16-, 20-, 24-, 48-, 56-, 64-, and 80-Pin Packages

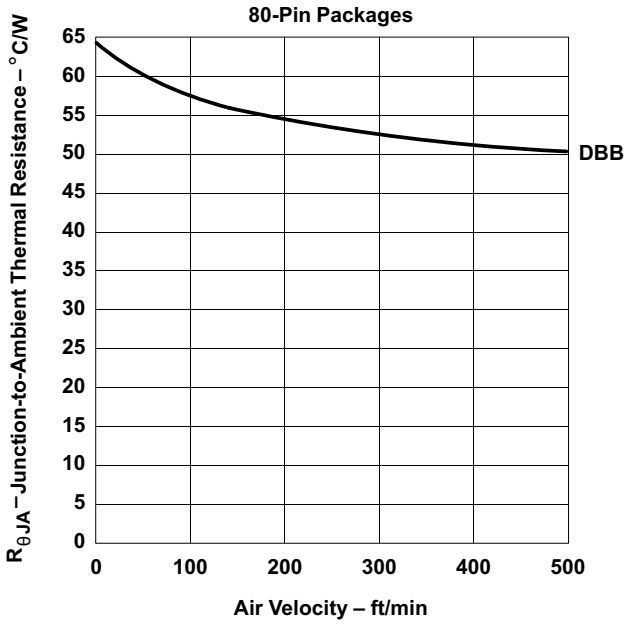


Figure 37. High-K Thermal-Resistance Images for 5-, 14-, 16-, 20-, 24-, 48-, 56-, 64-, and 80-Pin Packages (Continued)

4.6 Electrical Characteristics

4.6.1 V_{T+} Positive-Going Input Threshold Level

JEDEC - The input threshold voltage when the input voltage is rising.

TI - The voltage level at a transition-operated input that causes operation of the logic element, according to specification, as the input voltage rises from a level below the negative-going threshold voltage, V_{T-}.

See Section 4.6.3, *ΔVT Hysteresis (VT+ - VT-)*, for further information.

4.6.2 V_{T-} Negative-Going Input Threshold Level

JEDEC - The input threshold voltage when the input voltage is falling.

TI - The voltage level at a transition-operated input that causes operation of the logic element according to specification, as the input voltage falls from a level above the positive-going threshold voltage, V_{T+}.

See Section 4.6.3, *ΔVT Hysteresis (VT+ - VT-)*, for further information.

4.6.3 ΔV_T Hysteresis (V_{T+} - V_{T-})

JEDEC - The difference between the positive-going and negative-going input threshold voltages.

TI - Refer to the JEDEC definition above.

Hysteresis has been incorporated into logic devices for many years and exists in bipolar as well as CMOS circuitry. Although the circuitry is different, the implementation is the same: the input voltage threshold actually changes internally from one level to another, as the input logic level itself switches. Figure 38 is the most common voltage plot for the input and output, as the input transitions from one logic state to the other. Figure 39, however, shows V_{IT+} and V_{IT-} in a voltage versus time waveform.

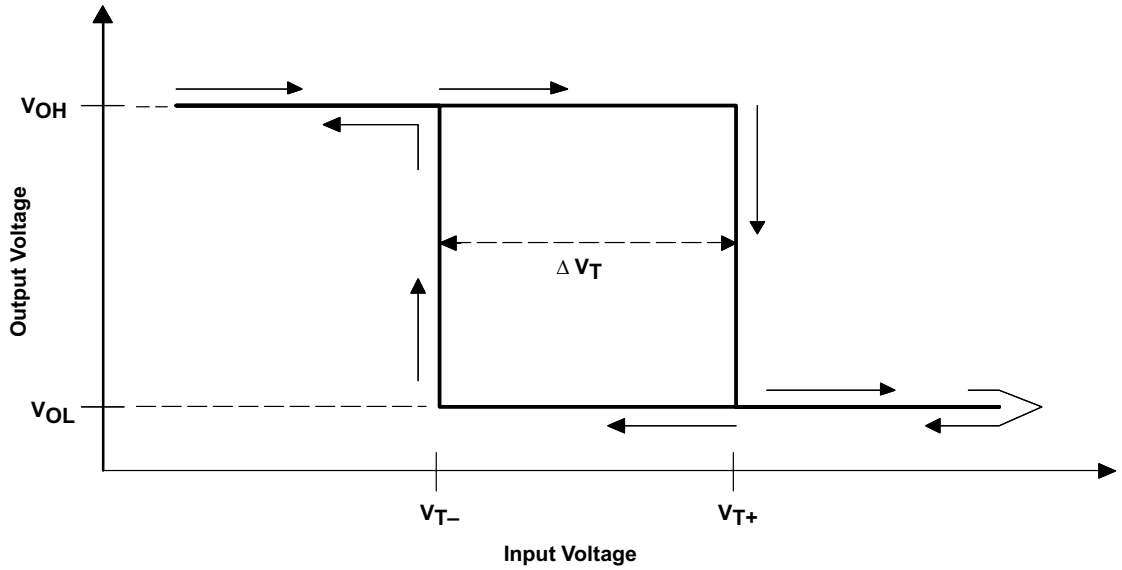


Figure 38. Hysteresis: V_I vs V_O

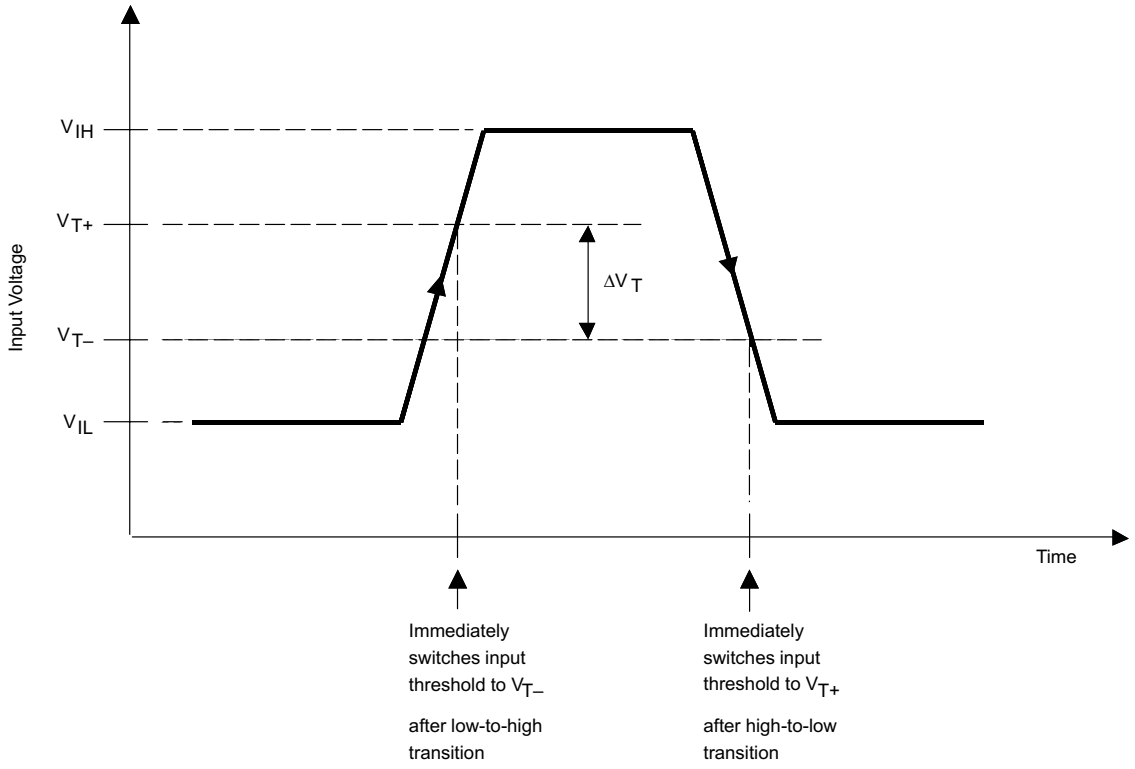


Figure 39. Hysteresis: Input Voltage vs Time

The benefit of a device that has built-in dc hysteresis is that, depending on the amount of hysteresis and the amount of noise present, the input is immune to such noise. This digital form of filtering out unwanted noise can be beneficial in a system where noise caused by electromagnetic interference (EMI) or crosstalk cannot be reduced. Figure 40 and Figure 41 conceptually depict the functionality of hysteresis.

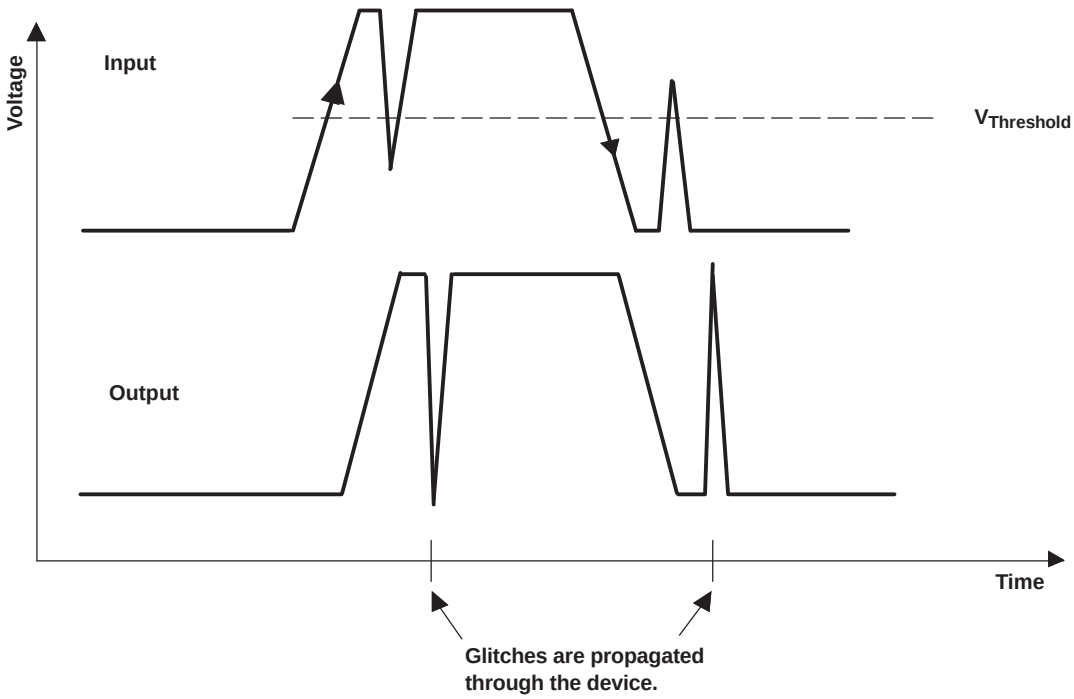


Figure 40. Possible Output-Voltage Outcome for Devices Without Hysteresis

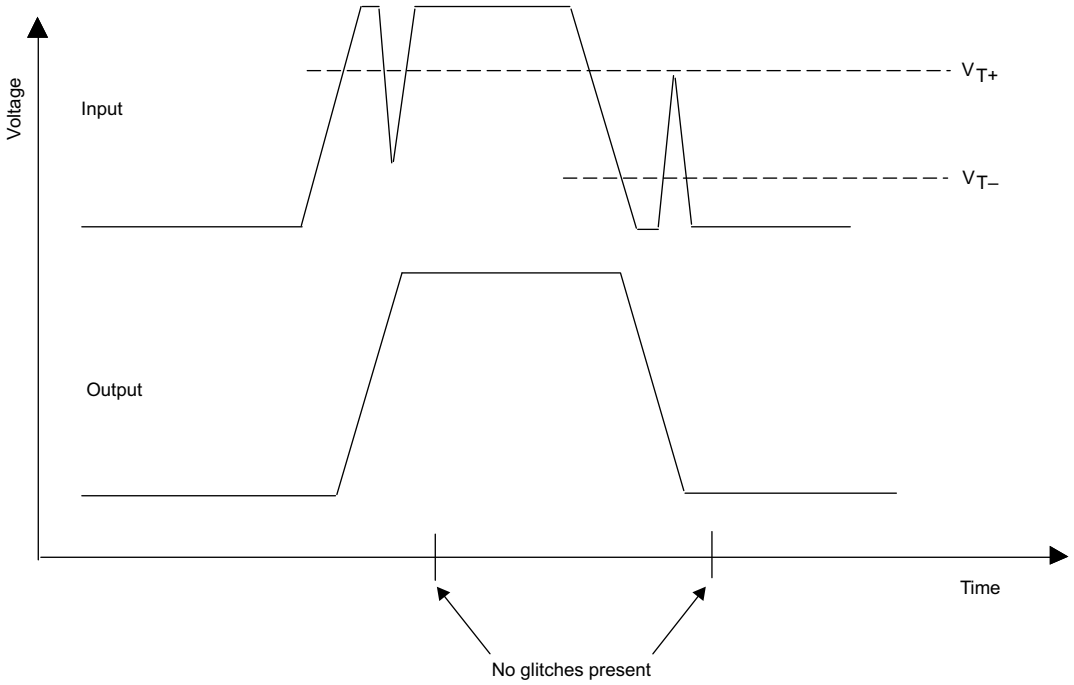


Figure 41. Glitch-Rejection Capabilities of Devices With Hysteresis

4.6.4 V_{IK} Input Clamp Voltage

JEDEC - An input voltage in a region of relatively low differential resistance that serves to limit the voltage swing.

TI - The maximum voltage developed across an input diode with test current applied.

Helpful Hint:

The presence of a V_{IK} specification indicates that there is a ground-clamp diode on the input and the V-I characteristics of that diode in its forward-biased region are given.

4.6.5 V_{OH} High-Level Output Voltage

JEDEC - The voltage level at an output terminal with input conditions applied that, according to the product specification, will establish a high level at the output.

TI - The voltage level at an output terminal with input conditions applied that, according to the product specification, establishes a high level at the output.

V_{OH} is tested with input conditions that should cause the output under test to be at a high-level voltage. The output then is forced to source the required current, as defined in the data sheet, and the output voltage is measured. The test is passed if the voltage is greater than V_{OH} min. The input voltage levels used to precondition the device are V_{IL} max and V_{IH} min, as defined in the *Recommended Operating Conditions*. See Section 4.5.7, *I_{OH} High-Level Output Current*, for further information.

Helpful Hint:

Inclusion of a V_{OH} specification with a test condition of I_{OH} = –100 µA is done primarily to indicate that the device has CMOS outputs instead of bipolar (npn or pnp) drivers. Bipolar output transistors typically are not able to swing the output voltages all the way to the power-supply rail or ground rail, even under no-load or lightly loaded conditions. If a device has bipolar outputs, this test condition would not apply and is not included in the data sheet. If you see this specification, you can safely assume the outputs to be of CMOS construction.

4.6.6 V_{OHS} Static High-Level Output Voltage

JEDEC - *no definition offered*

TI - The static and testable voltage at a Dynamic Output Control (DOC circuitry) output with input conditions applied that, according to the product specifications, establishes a static high level at the output. The dynamic drive voltage is not specified for devices with DOC circuitry outputs because of its transient nature.

See Section 4.5.8, *I_{OHS} Static High-Level Output Current*, for further information.

For additional information about DOC circuitry, refer to the TI application report, *Dynamic Output Control (DOC™) Circuitry Technology and Applications*, literature number SCEA009.

4.6.7 V_{OL} Low-Level Output Voltage

JEDEC - The voltage level at an output terminal with input conditions applied that, according to the product specification, will establish a low level at the output.

TI - The voltage level at an output terminal with input conditions applied that, according to the product specification, establishes a low level at the output.

V_{OL} is tested with input conditions that should cause the output under test to be at a low level. The output then is forced to sink the required current, as defined in the data sheet, and the output voltage is measured. The test is passed if the voltage is less than V_{OL} max. The input voltage levels used to precondition the device are V_{IL} max and V_{IH} min, as defined in the recommended operating conditions. See Section 4.5.9, *I_{OL} Low-Level Output Current*, for further information.

Helpful Hint:

Inclusion of a V_{OL} specification with a test condition of I_{OL} = 100 µA is done primarily to indicate that the device has CMOS outputs instead of bipolar (npn or pnp) drivers. Bipolar output transistors typically are not able to swing the output voltages all the way to the power-supply rail or ground rail, even under no-load or lightly loaded conditions. If the outputs were bipolar, this test condition would not apply and is not included in the data sheet. If you see this specification, you can safely assume the outputs to be of CMOS construction.

4.6.8 V_{OLS} Static Low-Level Output Voltage

JEDEC - *no definition offered*

TI - The static and testable voltage at a Dynamic Output Control (DOC circuitry) output with input conditions applied that, according to the product specifications, establishes a static low level at the output. The dynamic drive voltage is not specified for devices with DOC circuitry outputs because of its transient nature.

See Section 4.5.10, I_{OLS} *Static Low-level Output Current*, for further information.

For additional information about DOC circuitry, refer to the TI application report, *Dynamic Output Control (DOC™) Circuitry Technology and Applications*, literature number SCEA009.

4.6.9 r_{on} On-State Resistance

JEDEC - The resistance between specified terminals with input conditions applied that, according to the product specification, will establish minimum resistance (the on-state) between those terminals.

TI - The resistance measured across the channel drain and source (or input and output) of a bus-switch device.

4.6.10 Peak On-State Resistance

TI - The highest resistance measured across the drain and source channels of switch across the valid input range of operation.

4.6.11 Delta On-State Resistance

TI -The difference between the on-state resistance between any 2 channels of the switch.

4.6.12 I_I Input Current

JEDEC - The current at the input terminals.

TI - The current into an input (current into a terminal is given as a positive value).

Helpful Hint:

CMOS inputs sink or source only minute amounts of current (commonly called leakage current) because of the behavior of standard CMOS technology, which is voltage controlled instead of current controlled. As a result, this parameter always should have a maximum specification no greater than a few tens of micro amperes. For most bipolar inputs, which are current controlled instead of voltage controlled, a large amount of current is normal (a few milliamperes). In fact, a good method to determine if a device has a CMOS input is to examine its maximum input current specification: if this current is approximately the value of leakage current, typically, this means that it is a CMOS input.

Helpful Hint:

For the data signals of a device without bus-hold, the I_I specification includes both input and output leakage currents at the I/O pin. For devices that have bus-hold on the data signals, the I_I specification should apply only to the control inputs because the bus-hold output supplies enough current to overcome any internal input leakage.

An exception to this is an I_I specification for an overvoltage-tolerant bus-hold input with a test condition of $V_I >> V_{CC}$. This is used to indicate that the overvoltage-tolerant bus-hold output has a Schottky blocking diode in series with the output p-channel pullup transistor to $V_{CC,}$ which prevents current from flowing from the output back into the V_{CC} supply. See $I_{I(hold)}$ and I_{off} for more information.

4.6.13 I_{IH} High-Level Input Current

JEDEC - The current into an input terminal when a specified high-level voltage is applied to that input.

TI - The current into an input when a high-level voltage is applied to that input.

Helpful Hint:

I_{IH} and I_{IL} typically are found only on devices with bipolar inputs that usually require a significantly different amount of pulldown current on the input to provide a logic low, rather than pullup current to provide a logic high. CMOS inputs usually have only leakage currents at the inputs and use the I_I parameter, but are measured at both low- and high-bias conditions.

4.6.14 I_{IL} Low-Level Input Current

JEDEC - The current into an input terminal when a specified low-level voltage is applied to that input.

TI - The current out of an input when a low-level voltage is applied to that input.

Helpful Hint:

I_{IH} and I_{IL} typically are found only on devices with bipolar inputs that usually require a significantly different amount of pulldown current on the input to provide a logic low, rather than pullup current to provide a logic high. CMOS inputs usually have only leakage currents at the inputs and use the I_I parameter.

4.6.15 $I_{I(hold)}$ Input Hold Current

JEDEC - *no definition offered*

TI - The input current that holds the input at the previous state when the driving device goes to the high-impedance state.

For additional information about the bus-hold feature, refer to the TI application report, *Bus-Hold Circuit*, literature number SCLA015.

Older technologies, such as ABT, LVT, LVC and ALVC (on devices that have the H option), specify this parameter. This parameter is measured with the minimum V_{CC} and an input bias voltage that is at V_{IH} min and V_{IL} max of the particular input threshold. For example, the ALVC family has a specified V_{IL} max of 0.7 V for a V_{CC} ranging from 2.3 V to 2.7 V, whereas its V_{IH} min is 1.7 V for the same supply voltage. Within a V_{CC} range of 2.7 V to 3.6 V, the input threshold for the ALVC family is V_{IH} min = 2 V and V_{IL} max = 0.8 V. Therefore, with V_{CC} = 2.3 V, $I_{I(hold)}$ is measured with the input voltage set to 0.7 V and 1.7 V. With a V_{CC} = 2.7 V (minimum V_{CC} of 2.3 V to 2.7 V), $I_{I(hold)}$ is measured with the input voltage set to 0.8 V and 2 V. This specification explicitly states the minimum amount of current the input structure sources or sinks, with input voltages set to the minimum threshold requirements of the device.

Another parameter that may be included with this $I_{I(hold)}$ specification is the maximum current the device can sink or source as the input transitions from one logic state to another. This maximum current is the minimum amount of drive capability that must be provided by the driver that is connected to this bus-hold input to switch the input stage to the other logic state. In newer technologies such as AVC, the parameters I_{BHH}, I_{BHL}, I_{BHHO}, and I_{BHLO} have been defined with their own separate specifications, but are identical in nature to those that are lumped with the $I_{I(hold)}$ parameter. Figure 42 is a representation of these bus-hold current measurements.

Helpful Hint:

The $I_{I(hold)}$ specification is not used in recent data sheets; instead, I_{BHH}, I_{BHL}, I_{BHHO}, and I_{BHLO} are used.

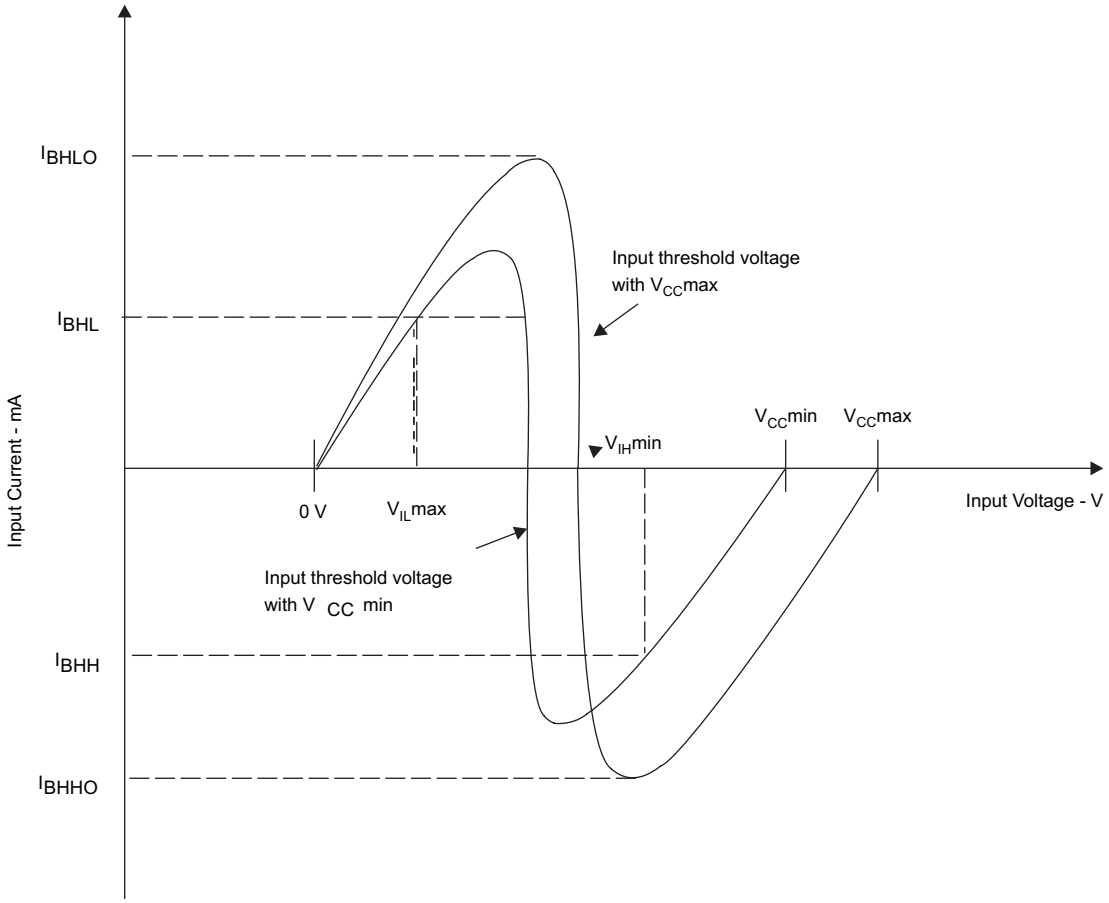


Figure 42. Bus-Hold Currents

4.6.16 I_{BHH} Bus-Hold High Sustaining Current

JEDEC - *no definition offered*

TI - The bus-hold circuit can source at least the minimum high sustaining current at V_{IH} min. I_{BHH} should be measured after raising the input voltage to $V_{CC,}$ then lowering it to V_{IH} min.

For additional information about the bus-hold feature, refer to the TI application report, *Bus-Hold Circuit*, literature number SCLA015. Also, see Section 4.6.15, $I_{I(hold)}$ *Input Hold Current*, for further information.

4.6.17 I_{BHL} Bus-Hold Low Sustaining Current

JEDEC - *no definition offered*

TI - The bus-hold circuit can sink at least the minimum low sustaining current at V_{IL} max. I_{BHL} should be measured after lowering the input voltage to GND and raising it to V_{IL} max.

For additional information about the bus-hold feature, refer to the TI application report, *Bus-Hold Circuit*, literature number SCLA015. Also, see Section 4.6.15, $I_{I(hold)}$ *Input Hold Current*, for further information.

4.6.18 I_{BHHO} Bus-Hold High Overdrive Current

JEDEC - *no definition offered*

TI - The current that an external driver must sink to switch this node from high to low.

For additional information about the bus-hold feature, refer to the TI application report, *Bus-Hold Circuit*, literature number SCLA015. Also, see Section 4.6.15, $I_{I(hold)}$ *Input Hold Current*, for further information.

4.6.19 I_{BHLO} Bus-Hold Low Overdrive Current

JEDEC - *no definition offered*

TI - The current that an external driver must source to switch this node from low to high.

For additional information about the bus-hold feature, refer to the TI application report, *Bus-Hold Circuit*, literature number SCLA015. Also, Section 4.6.15 for further information.

4.6.20 I_{off} Input/Output Power-Off Leakage Current

JEDEC - The current into a circuit node when the device or a portion of the device affecting that circuit node is in the off state.

TI - The maximum leakage current into an input or output terminal of the device, with the specified voltage applied to the terminal and V_{CC} = 0 V.

The I_{off} protection circuitry ensures that no excessive current is drawn from or to an input, output, or combined I/O that is biased to a specified voltage while the device is powered down, and is said to support partial-power-down mode of system operation. This condition can occur when subsections of a system are powered down (partial power down) to reduce power consumption. The TI logic families with the I_{off} feature that support partial power down are: AVC, LV, LVC, (CY)FCT, GTL, LS, ALS, and AUC.

All TI standard logic devices with I_{off} allow a maximum of approximately 100 µA to flow under these conditions. Any current in excess of this amount (a pn junction, for example, being forward biased) is not considered normal leakage current. Inherent in all CMOS designs are the parasitic diodes in all N-channel and P-channel FETs, which must be properly biased to prevent unwanted current paths. The output structure of a typical CMOS output is shown in Figure 43.

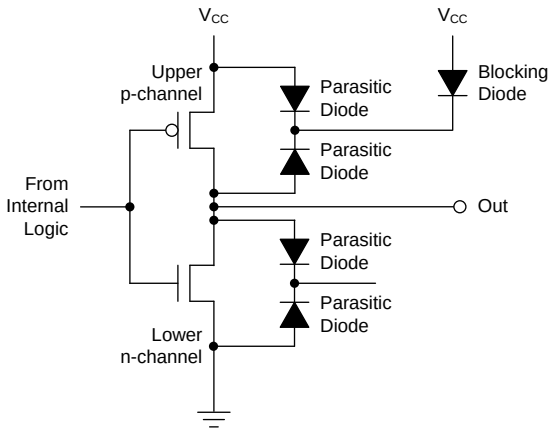


Figure 43. Typical CMOS Totem-Pole Output With I_{off}

The common cathode connection for the parasitic diodes on the p-channel MOS transistor is called the back gate and, typically, is tied to the highest potential on the device (V_{CC}, in the case of TI logic devices). For P-channel transistors, which are directly connected to external pins, the back gate is blocked with a diode to prevent excess currents flowing from the external pin to the supply-voltage V_{CC} when the output voltage is greater than V_{CC} by at least 0.7 V. This blocking diode is a subcircuit of the complete I_{off} circuitry found in several logic families, such as ABT and LVC. The other portion of the I_{off} circuit is not shown, but is, essentially, added FET circuitry that prevents the upper output P-channel from turning on during a partial-power-down event. The output N-channel, however, does not pose a problem because the parasitic diode already blocks current when the device is powered down and the output is biased high.

Figure 44 shows a typical CMOS input structure with bus-hold circuitry, which is essentially a weak latch that holds the previous state of the input inverter. The blocking diode is, again, required in the upper p-channel transistor that is connected to the external input pin. A non-bus-hold device does not require a blocking diode, as there is no p-channel source or drain connected to an external pin.

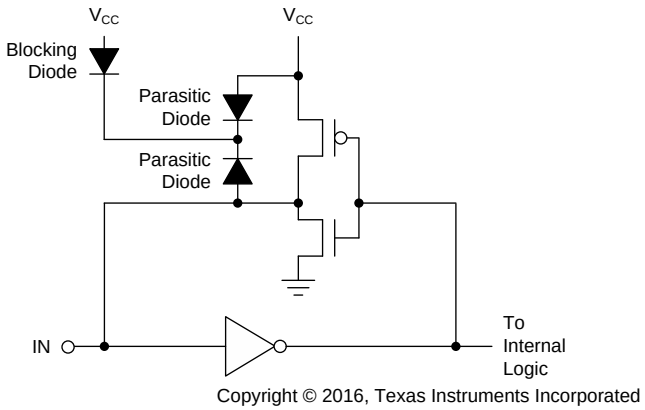


Figure 44. Typical CMOS Input With Bus-Hold and I_{off}

4.6.21 I_{OZ} Off-State (High-Impedance State) Output Current (of a 3-State Output)

JEDEC - *no definition offered*

TI - The current flowing into an output with the input conditions applied that, according to the product specification, establishes the high-impedance state at the output

TI data sheets specify currents flowing out of a device as a negative value.

The electrical characteristic, I_{OZ}, is verified utilizing the I_{OZH} and I_{OZL} tests. Two tests are required to verify the integrity of both the P- and N-channel transistors.

Helpful Hint:

For bidirectional (transceiver) devices that have bus hold on the data input/output pins, there should not be an I_{OZ} specification because the bus-hold output supplies enough current to overcome any internal output leakage.

An exception to this is an I_{OZH} specification for an overvoltage-tolerant bus-hold output with a test condition of $V_O >> V_{CC}$. This is used to indicate that the overvoltage-tolerant bus-hold output has a Schottky blocking diode in series with the output p-channel pullup transistor to V_{CC} and I_{off} circuitry, preventing the upper P-channel from turning on, which prevents current from flowing from the output back into the V_{CC} supply. See $I_{I(hold)}$ and I_{off} for more information.

4.6.22 I_{OZH} Off-State Output Current With High-Level Voltage Applied

JEDEC - *no definition offered*

TI - The current flowing into a 3-state output with input conditions established that, according to the product specification, will establish the high-impedance state at the output with a high-level voltage applied to the output.

This parameter is measured with other input conditions established that would cause the output to be at a low level if it were enabled. I_{OZH} is tested by applying the specified voltage to the output and measuring the current into the device with the output in the high-impedance state. Input conditions that would establish a low level on the output if it were enabled areV_{IL} = V_{IL} max and V_{IH} = V_{IH} min. Each output is tested individually. For example, the unused inputs are at V_{IL} = 0 or V_{IH} = V_{CC} for AC devices and V_{IL} = 0 or V_{IH} = 3 V for ACT devices, depending on the desired state of the outputs not being tested.

Helpful Hint:

An I_{OZH} specification on bidirectional (transceiver) devices with bus hold on the data input/output pins, with a test condition of $V_O >> V_{CC}$, indicates that the overvoltage-tolerant bus-hold output has a Schottky blocking diode in series with the output P-channel pullup transistor to V_{CC}. This diode prevents current flowing from the output back into the V_{CC} supply. See $I_{I(hold)}$ and I_{off} for more information.

4.6.23 I_{OZL} Off-State Output Current With Low-Level Voltage Applied

JEDEC - *no definition offered*

TI - The current flowing into a 3-state output with input conditions established that, according to the product specification, will establish the high-impedance state at the output, with a low-level voltage applied to the output.

This parameter is measured with other input conditions established that would cause the output to be at a high level if it were enabled. I_{OZL} is tested by applying the specified voltage to the output and measuring the current into the device with the output in the high-impedance state. Input conditions that would establish a high level on the output if it were enabled areV_{IL} = V_{IL} max and V_{IH} = V_{IH} min. Each output is tested individually.

4.6.24 I_{OZPD} Power-Down Off-State (High-Impedance State) Output Current (of a 3-State Output)

JEDEC - *no definition offered*

TI - The current flowing into an output that is switched to or held in the high-impedance state as the device is being powered down to V_{CC} = 0 V.

TI data sheets specify currents flowing out of a device as a negative value.

Power-up 3-state (PU3S) circuitry is characterized by the parameters I_{OZPD} and I_{OZPU}. For hot-insertion support, I_{off}, and the addition of I_{OZPD} and I_{OZPU} are necessary. The TI logic families with the I_{off} and PU3S features that support hot insertion are: ABT (some), ALVT, BCT, LVT, and LVCZ.

While I_{off} is tested in a steady-state dc environment, PU3S is checked dynamically by ramping the power supply from 0 V to its maximum recommended value, then back to 0 V. The power-up and power-down ramp rates also affect the internal circuitry, but a ramp rate faster than 20 µs/V is not recommended for GTLP devices, for example, and slower than that (~200 µs/V) for older logic technologies. This ramp rate sometimes is specified as $\Delta t/\Delta V_{CC}$ in the *Recommended Operating Conditions* section of the data sheet. Because typical power supplies power up within a few milliseconds (due, in part, to the enormous capacitance distributed throughout a PCB), the PU3S circuit should function properly in all applications.

PU3S circuitry disables the logic device outputs at a V_{CC} range of 0 V to a specified power-supply voltage trip point, regardless of the state of the output enable pin. At a certain guard-banded voltage above this supply voltage, the device will assert a voltage at the output, as indicated by its respective bit input-voltage logic level. This is true only if the voltage at the input of the output-enable pin enables the outputs during normal operation of the device. If the output is required to be in the high-impedance state while the device is being powered up or powered down throughout the entire range, the output-enable pin must be set to disable the output.

The voltage-versus-time plot shown in Figure 45 demonstrates how PU3S functions. As the device is being powered up, until it reaches the minimum V_{CC} supply voltage (labeled *Supply Trip Point* in Figure 45), the device output remains in the high-impedance state and remains at the pullup voltage, as defined by the load at the output. Once the internal PU3S circuitry determines that the supply voltage is slightly above this trip point, the device resumes normal functionality and enables the output. In this case, the input pin is such that the output goes low when enabled. The falling edge of the power-supply voltage shows similar results: just before V_{CC} reaches this trip point, the output is disabled.

For further information on power-up 3-state, refer to the TI application report, *Power-Up 3-State (PU3S) Circuits in TI Standard Logic Devices*, literature number SZZA033.

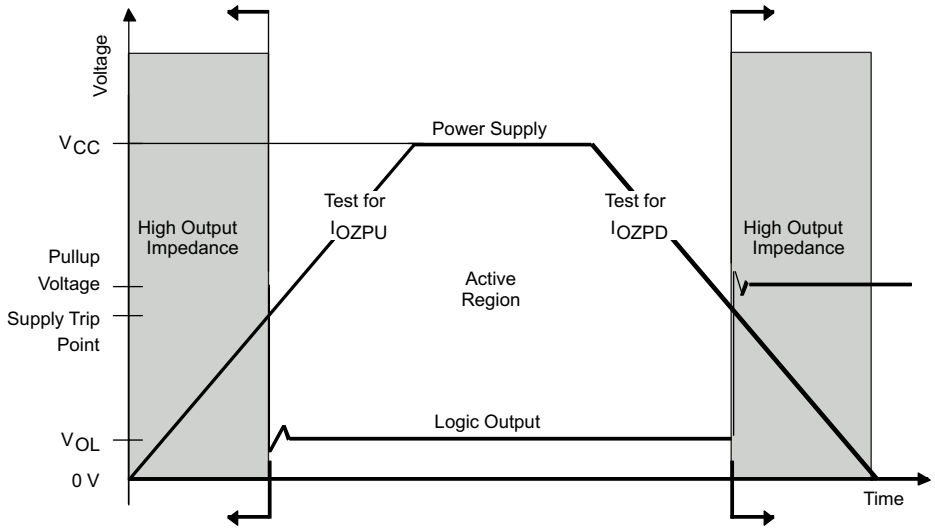


Figure 45. TI Logic Device I/O Text for I_{OZPU} and I_{OZPD}

4.6.25 I_{OZPU} Power-Up Off-State (High-Impedance State) Output Current (of a 3-State Output)

JEDEC - *no definition offered*

TI - The current flowing into an output that is switched to or held in the high-impedance state as the device is being powered up from V_{CC} = 0 V.

See I_{OZPD} power-down off-state output current for further information.

TI data sheets specify currents flowing out of a device as a negative value.

4.6.26 I_{CEX} Output High Leakage Current

JEDEC - *no definition offered*

TI - The maximum leakage current into an output that is in the high state and $V_O = V_{CC}$.

4.6.27 I_{CC} Supply Current

JEDEC - I_{CCH} is the current into a supply terminal of an integrated circuit when the output is (all outputs are) at a high-level voltage. I_{CCL} is the current into a supply terminal of an integrated circuit when the output is (all outputs are) at a low-level voltage.

TI - The current into the V_{CC} supply terminal of an integrated circuit.

This parameter is the current into the V_{CC} supply terminal of an integrated circuit under static no-load conditions. I_{CC} is tested by applying the specified V_{CC} level and measuring the current into the device.

The outputs of the device are left open, while all inputs—control and data—are biased to either V_{CC} or GND. For CMOS technologies, this is done to eliminate any current that may be caused by any input conditions or output loads.

4.6.28 ΔI_{CC} Supply-Current Change

JEDEC - *no definition offered*

TI - The increase in supply current for each input that is at one of the specified TTL voltage levels, rather than 0 V or V_{CC}.

If n inputs are at voltages other than 0 V or V_{CC}, the increase in supply current will be n × I_{CC}. The change in supply current (I_{CC}) is tested by applying the specified V_{CC} level, setting one input lower than V_{CC} (for example, V_{CC} - 0.6 V for LVC and ALVC devices) and all other inputs the same as the I_{CC} test, at 0 V or V_{CC}, then measuring the current into the device (see Figure 46). The outputs of the device are open, as well. The ΔI_{CC} specification typically is useful only on CMOS products that are designed to be operated at 5 V or 3.3 V because its purpose is to provide information about the supply-current performance of the CMOS device when driven by 5-V TTL signal levels.

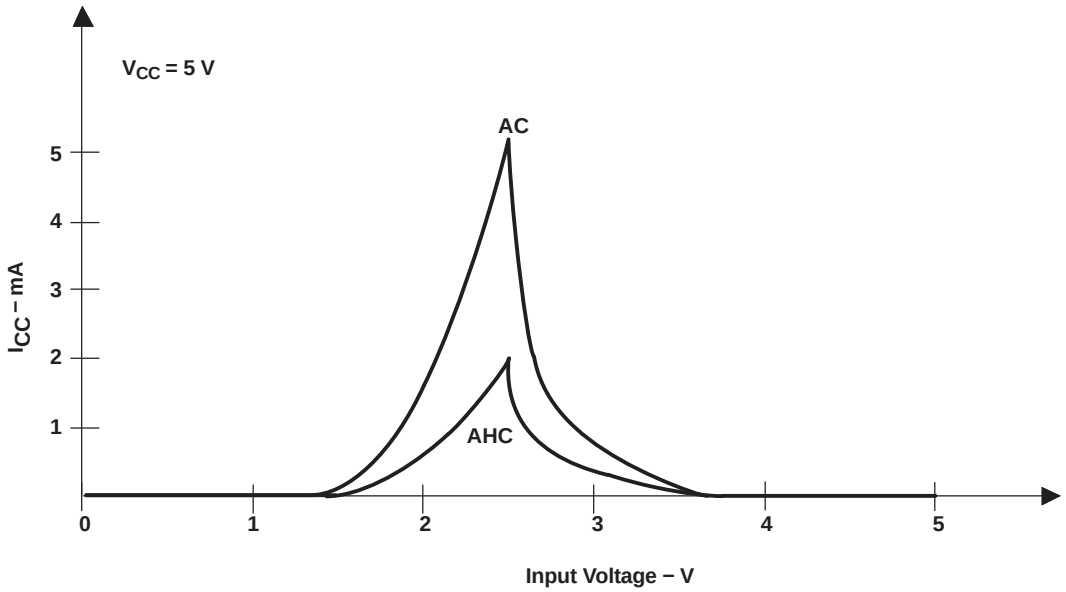


Figure 46. Example Typical AC and AHC I_{CC} vs Input Voltage

Helpful Hint:

Use the ΔI_{CC} specification as a reference when driving a CMOS device input with a TTL output driver.

Helpful Hint:

The ΔI_{CC} specification also demonstrates the high currents that can occur if V_{IH} and V_{IL} recommended operating conditions are not observed.

4.6.29 C_i Input Capacitance

JEDEC - *no definition offered*

TI - The capacitance of an input terminal of the device.

This parameter is the internal capacitance encountered at an input of the device. The values that are given are not production-tested values. Normally, they are typical values given for the benefit of the designer. These values are established by the design, process, and package of the device.

4.6.30 C_{io} Input/Output Capacitance

JEDEC - *no definition offered*

TI - The capacitance of an input/output (I/O) terminal of the device with the input conditions applied that, according to the product specification, establishes the high-impedance state at the output.

This parameter is the internal capacitance encountered at an input/output (I/O) of the device. The values that are given are not production-tested values. Normally, they are typical values given for the benefit of the designer. These values are established by the design, process, and package of the device.

4.6.31 C_o Output Capacitance

JEDEC - *no definition offered*

TI - The capacitance of an output terminal of the device with the input conditions applied that, according to the product specification, establishes the high-impedance state at the output.

This parameter is the internal capacitance encountered at an output of the device. The values that are given are not production-tested values. Normally, they are typical values given for the benefit of the designer. These values are defined by the design, process, and package of the device.

4.7 Live-Insertion Specifications

In addition to the following parameters, I_{off}, I_{OZPU}, and I_{OZPD} are specified in the live-insertion table because these parameters are necessary for live-insertion applications and typically are not stated in the *electrical characteristics section* of the data sheet, if already mentioned in this section.

4.7.1 I_{CC} (BIAS V_{CC}) BIAS V_{CC} Current

JEDEC - *no definition offered*

TI - This specification defines the maximum current at the BIAS V_{CC} pin during the ramp up or ramp down of the V_{CC} voltage.

4.7.2 V_O Output Bias Voltage

JEDEC - *no definition offered*

TI - This specification defines the range of voltages that will be applied to the output pin when the device is powered down.

4.7.3 I_O Output Bias Current

JEDEC - *no definition offered*

TI - This specification defines the minimum current measured at the output pin when the device is powered down.

4.8 Timing Requirements

4.8.1 f_{clock} Clock Frequency

JEDEC - *no definition offered*

TI - This specification defines the range of clock frequencies over which a bistable device can be operated while maintaining stable transitions between logic levels at the outputs.

The f_{clock} parameter is tested by driving the clock input with a predetermined number of pulses. The output then is checked for the correct number of output transitions corresponding to the number of input pulses applied. The output is loaded as defined in the data sheet specifications. Each output is individually tested and not checked simultaneously with other recommended operating conditions or propagation delays. For counters, shift registers, or any other devices for which the state of the final output is dependent on the correct operation of the previous outputs, f_{clock} will be tested only on the final output, unless specified independently in the data sheet. Full functionality testing is not performed during f_{clock} testing or f_{max} testing.

Helpful Hint:

The f_{max} and f_{clock} parameters are two sides of the same coin. The f_{clock} parameter tells you, the user, how fast you can reliably switch the input to the device. The f_{max} parameter informs TI when to reject a device that fails to function below a minimum speed. If you are a device user, you should simply disregard the f_{max} specification and use the f_{clock} specification.

Helpful Hint:

For products that are not clocked (for example, buffers and transceivers) for which you would like to know the maximum operating frequency, an estimate is the f_{clock} value from a comparable clocked part. For example, an SN74LVC16245A maximum data frequency is conservatively similar to the SN74LVC16374 maximum clock frequency. However, this is highly dependent upon load, and is a rule-of-thumb only.

4.8.2 t_w Pulse Duration (Width)

JEDEC - The time interval between the specified reference points on the two transitions of the pulse waveform.

TI - The time interval between specified reference points on the leading and trailing edges of the pulse waveform.

A minimum value is specified that is the shortest interval for which correct operation of the digital circuit is specified (see Figure 47). Pulse duration is tested by applying a pulse to the specified input for a time period equal to the minimum specified in the data sheet. The device passes if the outputs switch to their expected logic levels and fails if they do not. Pulse-duration times are not checked simultaneously with other inputs or other recommended operating conditions.

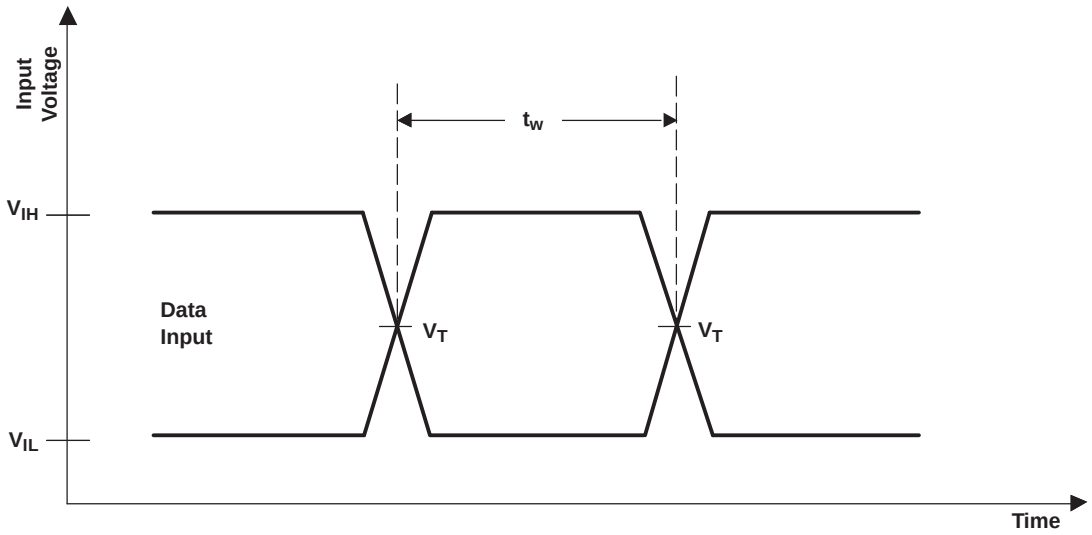


Figure 47. Pulse Duration

4.8.3 t_{su} Setup Time

JEDEC - The time interval between the application of a signal at a specified input terminal and a subsequent active transition at another specified input terminal.

TI - The time interval between the application of a signal that is maintained at a specified input terminal and a consecutive active transition at another specified input terminal.

NOTE: 1. The setup time is the time interval between two signal events and is determined by the system in which the digital circuit operates. A minimum value is specified that is the shortest interval for which correct operation of the digital circuit is specified.

NOTE: 2. The setup time may have a negative value, in which case the minimum limit defines the longest interval (between the active transition and the application of the other signal) for which correct operation of the digital circuit is specified.

Setup time is tested by switching an input to a fixed logic level at a specified time before the transition of the other input (see Figure 48). The device passes if the outputs switch to their expected logic levels and fails if they do not. Setup times are not checked simultaneously with other inputs or other recommended operating conditions. For additional information about setup time, refer to the TI application report, *Metastable Response in 5-V Logic Circuits*, literature number SDYA006.

4.8.4 t_h Hold Time

JEDEC - The time interval during which a signal is retained at a specified input terminal after an active transition occurs at another specified input terminal.

TI - The time interval during which a signal is retained at a specified input after an active transition occurs at another specified input.

NOTE: 1. The hold time is the actual time interval between two signal events and is determined by the system in which the digital signal operates. A minimum value is specified that is the shortest interval for which correct operation of the digital circuit is to be expected.

NOTE: 2. The hold time may have a negative value, in which case, the minimum limit defines the longest interval (between the release of the signal and the active transition) for which correct operation of the digital circuit is to be expected.

Hold time is tested by holding an input at a fixed logic level for the specified time after the transition of the other input (see Figure 48). The device passes if the outputs switch to their expected logic levels and fails if they do not. Hold times are not checked simultaneously with other inputs or other recommended operating conditions. For additional information about hold time, refer to the TI application report; *Metastable Response in 5-V Logic Circuits*, literature number SDYA006.

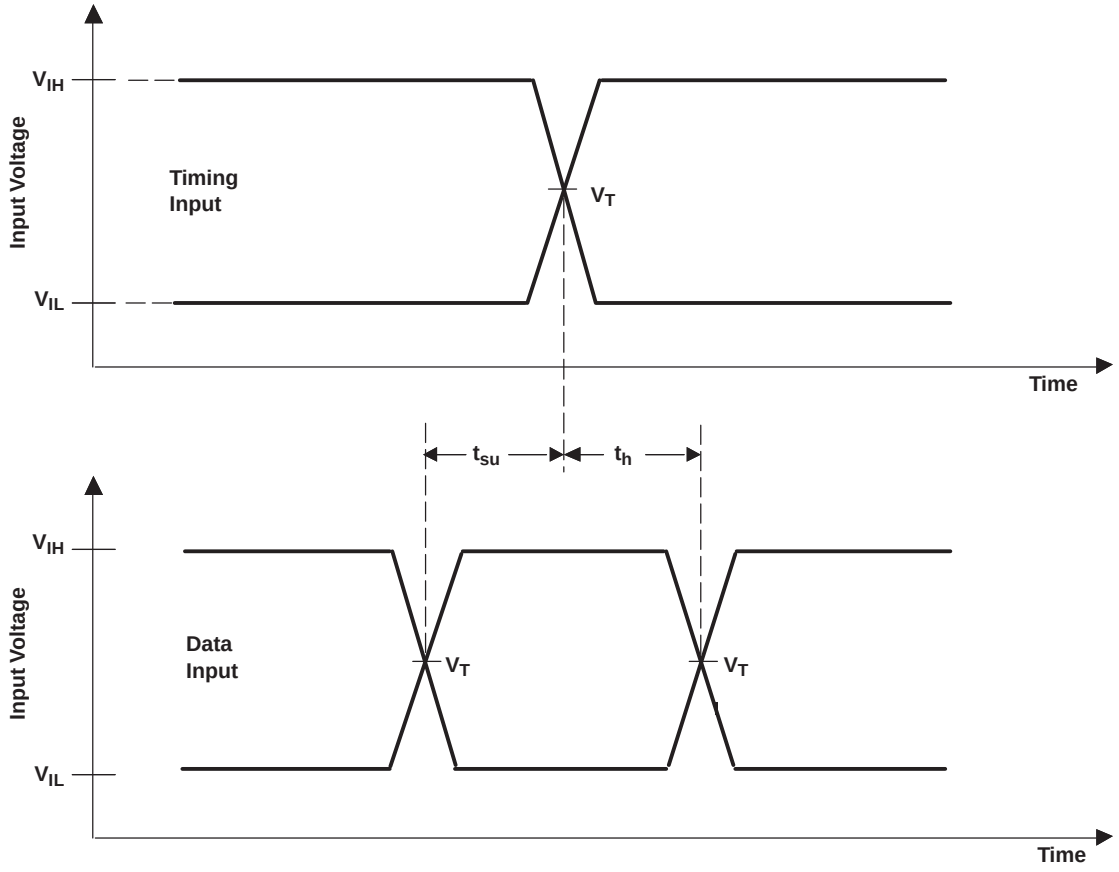


Figure 48. Setup and Hold Times

4.9 Switching Characteristics

4.9.1 f_{max} Maximum Clock Frequency

JEDEC - The highest frequency at which a clock input of an integrated circuit can be driven, while maintaining proper operation.

TI - The highest rate at which the clock input of a bistable circuit can be driven through its required sequence, while maintaining stable transitions of logic level at the output with input conditions established that should cause changes of output logic level in accordance with the specification.

The f_{max} value is the value of the upper limit of the f_{clock} specification, and is specified in the data sheet as a minimum limit. The circuit is specified to operate up to the minimum frequency value. See f_{clock} for additional f_{max} testing information. Due to test-machine capability limitations, it may be necessary to test f_{max} or minimum recommended operating conditions (that is, pulse duration, setup time, hold time) in accordance with the following paragraph.

The f_{max} parameter may be tested in either of two ways. One method is to test simultaneously the responses to the symmetrical clock-high and clock-low pulse durations that correspond to the period of the specified minimum value of f_{max}. The second method is to test individually the responses to the minimum clock-high and clock-low pulse durations under specified load conditions. A pulse generator is used to propagate a signal through the device to verify device operation with the minimum pulse duration. When clock-high and clock-low pulse durations are equal to or less than the corresponding f_{max} pulse duration, f_{max} testing suffices for testing clock-high and clock-low pulse durations.

Helpful Hint:

The f_{max} and f_{clock} parameters are two sides of the same coin. The f_{clock} parameter tells you, the user, how fast you can reliably switch the input to the device. The f_{max} parameter informs TI when to reject a device that fails to function below a minimum speed. If you are a device user, you should simply disregard the f_{max} specification and use the f_{clock} specification.

Helpful Hint:

For products that are not clocked (for example, buffers and transceivers) for which you would like to know the maximum operating frequency, an estimate is the f_{clock} value from a comparable clocked part. For example, an SN74LVC162451A maximum data frequency is conservatively similar to the SN74LVC16374 maximum clock frequency. However, this is highly dependent upon load and is a rule-of-thumb only.

4.9.2 t_{pd} Propagation Delay Time

JEDEC - The time interval between specified reference points on the input and output voltage waveforms with the output changing from one defined level (high or low) to the other defined level.

TI - The time between the specified reference points on the input and output voltage waveforms, with the output changing from one defined level (high or low) to the other defined level ($t_{pd} = t_{PHL}$ or t_{PLH}).

A common misconception about logic devices is that the maximum data-signaling rate (or maximum frequency, as it is commonly misnamed) is equal to the inverse of the propagation delay. The maximum data rate on buffers is dependent on several factors, such as propagation delay matching, input sensitivity, and output edge rates. A device can have a high maximum signaling rate if the propagation delays from low-to-high and high-to-low are matched, the input is fast enough to respond to the fast data rate, and the output edge rate does not interfere with the low and high-level steady states. Clocked devices behave in the same manner, but now the set-up and hold times must be taken into account.

Helpful Hint:

The maximum value of t_{PD} simply is the worst case of t_{PHL} or t_{PLH}.

Helpful Hint:

Bus switch devices such as CBT and CBTLV typically are specified with a maximum limit of 0.25 ns. This limit is not a measured value, but is derived from the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

4.9.3 t_{PHL} Propagation Delay Time, High-Level to Low-Level Output

JEDEC - The time interval between specified reference points on the input and output voltage waveforms with the output changing from the defined high level to the defined low level.

TI - The time between the specified reference points on the input and output voltage waveforms, with the output changing from the defined high level to the defined low level.

Propagation delay time, t_{PHL}, is tested by causing a transition on the specified input that causes the designated output to switch from a high logic level to a low logic level. For example, the transition applied is 0 V to V_{CC} or V_{CC} to 0 V for AC devices and 0 V to 3 V or 3 V to 0 for ACT devices. Trip points used for the timing measurements and output loads used during testing are defined in the individual data sheets in the *Parameter Measurement Information* section, typically found after the *Switching Characteristics* (over recommended ranges of supply and operating free-air temperature) table. Propagation delay time, t_{PHL}, is not checked simultaneously with other outputs or with other recommended operating conditions. The time between the specified reference point on the input voltage waveform and the specified reference point on the output voltage waveform is measured.

4.9.4 t_{PLH} Propagation Delay Time, Low-Level to High-Level Output

JEDEC - The time interval between specified reference points on the input and output voltage waveforms with the specified output changing from the defined low level to the defined high level.

TI - The time between the specified reference points on the input and output voltage waveforms, with the output changing from the defined low level to the defined high level.

Propagation delay time, t_{PLH}, is tested by causing a transition on the specified input that causes the designated output to switch from a low logic level to a high logic level. For example, the transition applied is 0 V to V_{CC} or V_{CC} to 0 V for AC devices and 0 V to 3 V or 3 V to 0 for ACT devices. Trip points used for the timing measurements and output loads used during testing are defined in the individual data sheets in the *Parameter Measurement Information* section, typically found after the *Switching Characteristics* (over recommended ranges of supply and operating free-air temperature) table. Propagation delay time, t_{PLH}, is not checked simultaneously with other outputs or with other recommended operating conditions. The time between the specified reference point on the input voltage waveform and the specified reference point on the output voltage waveform is measured.

4.9.5 t_{en} Enable Time (of a 3-State or Open-Collector Output)

JEDEC - The propagation time between specified reference points on the input and output voltage waveforms with the output changing from a high-impedance (off) state to either of the defined active levels (high or low).

TI - The propagation time between the specified reference points on the input and output voltage waveforms, with the output changing from the high-impedance (off) state to either of the defined active levels (high or low).

NOTE: Open-collector outputs change only if they are responding to data that would cause the output to go low, so $t_{en} = t_{PHL}$.

4.9.6 t_{PZH} Enable Time (of a 3-State Output) to High Level

JEDEC - The propagation time between specified reference points on the input and output voltage waveforms with the output changing from a high-impedance (off) state to the defined high level.

TI - The time interval between the specified reference points on the input and output voltage waveforms, with the 3-state output changing from the high-impedance (off) state to the defined high level.

This parameter is the propagation delay time between the specified reference point on the input voltage waveform and the specified reference point on the output voltage waveform, with the 3-state output changing from the high-impedance (off) state to the defined high level. Output enable time, t_{PZH}, is tested by generating a transition on the specified input that will cause the designated output to switch from the high-impedance state to a high logic level. Trip points used for the timing measurements and output loads used during testing are defined in the individual data sheets in the *Parameter Measurement Information*

section, typically found after the *Switching Characteristics* (over recommended ranges of supply and operating free-air temperature) table. Output enable time, t_{PZH}, is not checked simultaneously with other outputs or with other recommended operating conditions. Outputs not being tested should be set to a condition that minimizes switching currents. The tested output load includes a pulldown resistor to obtain a valid logic-low level when the output is in the high-impedance state.

4.9.7 t_{PZL} Enable Time (of a 3-State Output) to Low Level

JEDEC - The propagation time between specified reference points on the input and output voltage waveforms with the output changing from a high-impedance (off) state to the defined low level.

TI - The time interval between the specified reference points on the input and output voltage waveforms, with the 3-state output changing from the high-impedance (off) state to the defined low level.

This parameter is the propagation delay time between the specified reference point on the input voltage waveform and the specified reference point on the output voltage waveform, with the 3-state output changing from the high-impedance (off) state to the defined low level. Output enable time, t_{PZL}, is tested by generating a transition on the specified input that will cause the designated output to switch from the high-impedance state to a low logic level. Trip points used for the timing measurements and output loads used during testing are defined in the individual data sheets in the *Parameter Measurement Information* section, typically found after the *Switching Characteristics* (over recommended ranges of supply and operating free-air temperature) table. Output enable time, t_{PZL}, is not checked simultaneously with other outputs or with other recommended operating conditions. Outputs not being tested should be set to a condition that minimizes switching currents. The tested output load includes a pullup resistor to obtain a valid logic-high level when the output is in the high-impedance state.

4.9.8 t_{dis} Disable Time (of a 3-State or Open-Collector Output)

JEDEC - *no definition offered*

TI - The propagation time between the specified reference points on the input and output voltage waveforms, with the output changing from either of the defined active levels (high or low) to the high-impedance (off) state.

NOTE: For 3-state outputs, $t_{dis} = t_{PHZ}$ or t_{PLZ}. Open-collector outputs change only if they are low at the time of disabling, so $t_{dis} = t_{PLH}$.

4.9.9 t_{PHZ} Disable Time (of a 3-State Output) From High Level

JEDEC - The propagation time between specified reference points on the input and output voltage waveforms with the output changing from the defined high level to a high-impedance (off) state.

TI - The time interval between the specified reference points on the input and the output voltage waveforms, with the 3-state output changing from the defined high level to the high-impedance (off) state.

4.9.10 t_{PLZ} Disable Time (of a 3-State Output) From Low Level

JEDEC - The propagation time between specified reference points on the input and output voltage waveforms with the output changing from the defined low level to a high-impedance (off) state.

TI - The time interval between the specified reference points on the input and the output voltage waveforms, with the 3-state output changing from the defined low level to the high-impedance (off) state.

4.9.11 t_f Fall Time

JEDEC - The time interval between one reference point on a waveform and a second reference point of smaller magnitude on the same waveform.

TI - The time interval between two reference points (90% and 10%, unless otherwise specified) on a waveform that is changing from the defined high level to the defined low level.

4.9.12 t_r Rise Time

JEDEC - The time interval between one reference point on a waveform and a second reference point of greater magnitude on the same waveform.

TI - The time interval between two reference points (10% and 90%, unless otherwise specified) on a waveform that is changing from the defined low level to the defined high level.

4.9.13 Slew Rate

JEDEC - *no definition offered*

TI - The voltage rate of change of an output ($\Delta V/\Delta t$).

4.9.14 $t_{sk(i)}$ Input Skew

JEDEC - The magnitude of the difference in propagation delay times between two inputs and a single output of an integrated circuit at identical operating conditions.

TI - The difference between any two propagation delay times that originate at different inputs and terminate at a single output. Input skew describes the ability of a device to manipulate (stretch, shrink, or chop) a clock signal. Typically, this is accomplished with a multiple-input gate wherein one of the inputs acts as a controlling signal to pass the clock through. $t_{sk(i)}$ describes the ability of the gate to shape the pulse to the same duration, regardless of the input used as the controlling input.

4.9.15 $t_{sk(l)}$ Limit Skew

JEDEC - The difference between (1) the greater of the maximum specified values of propagation delay times t_{PLH} and t_{PHL}, and (2) the lesser of the minimum specified values of propagation delay times t_{PLH} and t_{PHL}.

TI - The difference between: the greater of the maximum specified values of t_{PLH} and t_{PHL} and the lesser of the minimum specified values of t_{PLH} and t_{PHL}. Limit skew is not directly observed on a device and is calculated from the data sheet limits for t_{PLH} and t_{PHL}. $t_{sk(l)}$ quantifies for the designer how much variation in propagation delay time is induced by operation over the entire ranges of supply voltage, temperature, output load, and other specified operating conditions. Specified as such, $t_{sk(l)}$ also accounts for process variation. In fact, all other skew specifications ($t_{sk(o)}$, $t_{sk(i)}$, $t_{sk(p)}$, and $t_{sk(pr)}$) are subsets of $t_{sk(l)}$; they never are greater than $t_{sk(l)}$.

4.9.16 $t_{sk(o)}$ Output Skew

JEDEC - The skew time between two outputs of a single integrated circuit with all driving inputs switching simultaneously and the outputs switching in the same direction while driving identical loads.

TI - The skew between specified outputs of a single logic device, with all driving inputs connected together and the outputs switching in the same direction while driving identical specified loads.

4.9.17 $t_{sk(p)}$ Pulse Skew

JEDEC - The magnitude of the difference between the propagation delay times t_{PHL} and t_{PLH} when a single switching input causes one or more outputs to switch.

TI - The magnitude of the time difference between the propagation delay times, t_{PHL} and t_{PLH}, when a single switching input causes one or more outputs to switch.

4.9.18 $t_{sk(pr)}$ Process Skew

JEDEC - The part-to-part skew time between corresponding terminals of two samples of an integrated circuit from a single manufacturer.

TI -The magnitude of the difference in propagation delay times between corresponding terminals of two logic devices when both logic devices operate with the same supply voltages, operate at the same temperature, have identical package styles, have identical specified loads, have identical internal logic functions, and have the same manufacturer.

Helpful Hint:

Process variation is the only factor that affects process skew.

4.10 Noise Characteristics

4.10.1 $V_{OL(P)}$ Quiet Output, Maximum Dynamic V_{OL}

JEDEC - *no definition offered*

TI - The maximum positive voltage level at an output terminal with input conditions applied that, according to the product specification, establishes a low level at the specified output and a high-to-low transition at all other outputs.

Commonly called ringback, this parameter is the peak voltage of an output in the quiescent low condition, while all other outputs are switched from high to low (see Figure 49). Sometimes called a one-quiet-low test, this is a simultaneous switching measurement and indicates a device's noise performance due to power-rail and ground-rail bounce caused by the high peak currents during dynamic switching. $V_{OL(P)}$ also can apply to a switching output just after a high-to-low transition.

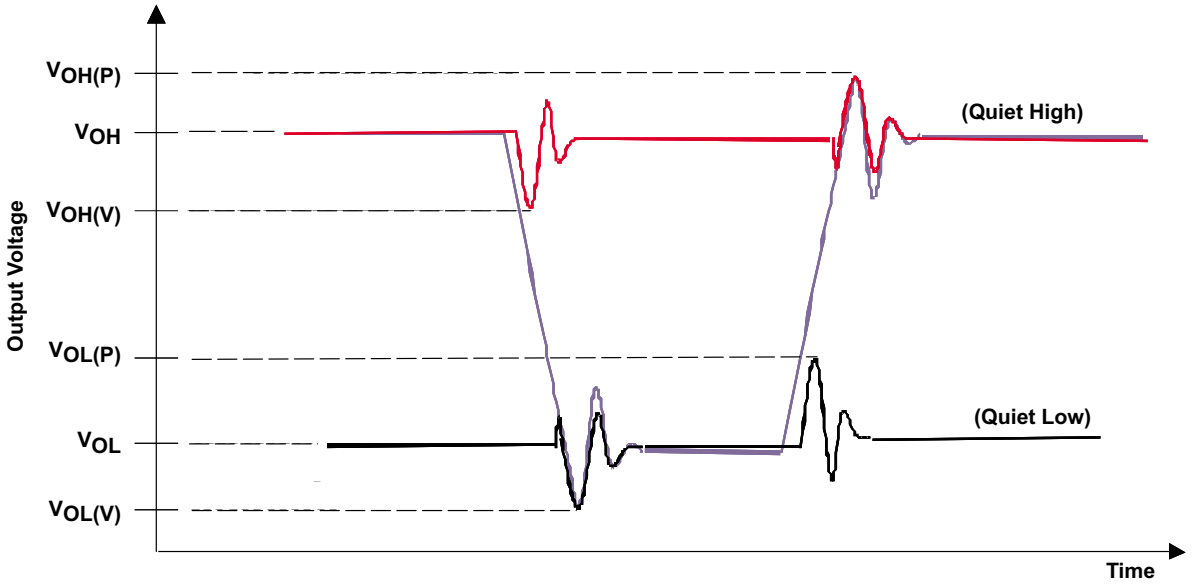


Figure 49. Output Noise Characteristics

4.10.2 $V_{OL(V)}$ Quiet Output, Minimum Dynamic V_{OL}

JEDEC - *no definition offered*

TI - The maximum negative voltage level at an output terminal with input conditions applied that, according to the product specification, establishes a low level at the specified output and a high-to-low transition at all other outputs.

Commonly called undershoot, this parameter is the valley voltage of an output in the quiescent low condition, while all other outputs are switched from high to low (see Figure 49). Sometimes called a one-quiet-low test, this is a simultaneous-switching measurement and indicates a device's noise performance due to power-rail and ground-rail bounce caused by the high peak currents during dynamic switching. $V_{OL(V)}$ also can apply to a switching output during a high-to-low transition.

4.10.3 $V_{OH(P)}$ Quiet Output, Maximum Dynamic V_{OH}

JEDEC - *no definition offered*

TI - The maximum positive voltage level at an output terminal with input conditions applied that, according to the product specification, establish a high level at the specified output and a low-to-high transition at all other outputs.

Commonly called overshoot, this parameter is the peak voltage of an output in the quiescent high condition, while all other outputs are switched from low to high (see Figure 49). Sometimes called a one-quiet-high test, this is a simultaneous-switching measurement and indicates a device's noise performance due to power-rail and ground-rail bounce caused by the high peak currents during dynamic switching. $V_{OH(P)}$ also can apply to a switching output during a low-to-high transition.

4.10.4 $V_{OH(V)}$ Quiet Output, Minimum Dynamic V_{OH}

JEDEC - *no definition offered*

TI - The minimum positive voltage level at an output terminal with input conditions applied that, according to the product specification, establishes a high level at the specified output and a low-to-high transition at all other outputs.

Commonly called ringback, this parameter is the valley voltage of an output in the quiescent high condition, while all other outputs are switched from low to high (see Figure 49). Sometimes called a one-quiet-high test, this is a simultaneous-switching measurement and indicates a device's noise performance due to power-rail and ground-rail bounce caused by the high peak currents during dynamic switching. $V_{OH(V)}$ also can apply to a switching output just after a low-to-high transition.

4.10.5 $V_{IH(D)}$ High-Level Dynamic Input Voltage

JEDEC - *no definition offered*

TI - An input voltage during dynamic switching conditions within the more positive (less negative) of the two ranges of values used to represent the binary variables.

NOTE: A minimum is specified that is the least positive value of high-level input voltage for which operation of the logic element within specification limits is to be expected.

High-level dynamic input voltage is a measurement of the shift of the input threshold due to noise generated while under the multiple-outputs-switching condition, with outputs operating in phase. This test is package and test-environment sensitive.

4.10.6 $V_{IL(D)}$ Low-Level Dynamic Input Voltage

JEDEC - *no definition offered*

TI - An input voltage during dynamic switching conditions within the less positive (more negative) of the two ranges of values used to represent the binary variables.

NOTE: A maximum is specified that is the most positive value of low-level input voltage for which operation of the logic element within specification limits is to be expected.

Low-level dynamic input voltage is a measurement of the shift of the input threshold due to noise generated while under the multiple-outputs-switching condition, with outputs operating in phase. This test is package and test-environment sensitive.

4.11 Operating Characteristics

4.11.1 C_{pd} Power-Dissipation Capacitance

JEDEC - *no definition offered*

TI - This parameter is the equivalent capacitance used to determine the no-load dynamic power dissipation per logic function for CMOS devices. $P_D = C_{pd} V_{CC}^2 f + I_{CC} V_{CC}$

The C_{pd} test is a measure of the dynamic power a device requires with a specific load. The values given on the data sheet are typical values that are not production tested. These values are defined by the design and process of the device. For more information on C_{pd}, refer to the TI application report, *CMOS Power Consumption and C_{pd} Calculation*, literature number SCAA035.

4.12 Parameter Measurement Information

The *Parameter Measurement Information* (PMI) section of a data sheet is a graphical illustration of the test conditions used to characterize a logic device. Usually this includes a load schematic, example waveforms with measurement points, and related notes. The PMI that is attached to each data sheet is typically a generic PMI for the entire logic family and may include additional information that is not used for that specific device. For example, the *voltage waveforms for enable and disable times* (which are used on devices with 3-state outputs) may be included in the data sheet of a device without 3-state outputs. This is superfluous information for the specific device and can be disregarded. The PMI may include the test information for multiple V_{CC}s in one page, with a table of test-load circuit and measurement point information, or the test information for each separate V_{CC} range at which the device operates may be in separate PMI pages, in which case the V_{CC} range will be stated at the top of the PMI illustration. Relevant load and test setup information also is included in the *footnotes* at the bottom of the PMI illustration.

5 Logic Compatibility

Logic compatibility has become more prevalent since the first 3.3-V logic devices were introduced into the market, creating an evolutionary trend in logic ICs. The trend demands that lower power-supply-voltage devices have the capability to communicate with older 5-V devices. In time, power-supply nodes have decreased even further, mainly due to power-consumption reduction. This reduction in supply nodes, coupled with the fact that 5-V systems are not only still in use, but thriving, has forced logic manufacturers to provide logic devices that are compatible with technologies from several different output-voltage levels (see Table 3).

Table 3. Key Parameters per Technology for Logic Compatibility

TECHNOLOGY	PORT(S)	V_{CC} MIN (V)	I/O VOLTAGE TOLERANCE (V)	V_{IH} MIN (V)	V_{IL} MAX (V)	V_{OH} MIN AT GIVEN CURRENT (V)	V_{OL} MAX AT GIVEN CURRENT (V)
ABT	A and B	4.5	5	2	0.8	2.5 (at -3 mA)	Not specified
						2 (at -32 mA)	Not specified
						Not specified	0.55 (at 64 mA)
AHC	A and B	2	V_{CC} + 0.5	1.5	0.5	Not specified	
		3	V_{CC} + 0.5	2.1	0.9	2.48 (at -4 mA)	0.44 (at 4 mA)
		4.5	V_{CC} + 0.5	Not Specified		3.8 (at -8 mA)	0.44 (at 8 mA)
		5.5	V_{CC} + 0.5	3.85	1.65	Not specified	

NOTE: These values are general technology performance characteristics. Because these values are derived from standard '245 or '16245 functions, carefully read the data sheet for each device for exact performance values.

Suppose you have created Table 3, which details the most important parameters discussed in the previous section that affect the compatibility of one device to another. Using the table to determine if a port from one technology is compatible to another, simply compare the V_{OH} min and V_{OL} max levels to the input threshold (V_{IH} min and V_{IL} max). If the output dc steady-state logic-high and logic-low voltage levels (V_{OH} and V_{OL}) are outside of the minimum V_{IH} and maximum V_{OL} range of an input port, then, in general, one can consider these two ports compatible (see Figure 50).

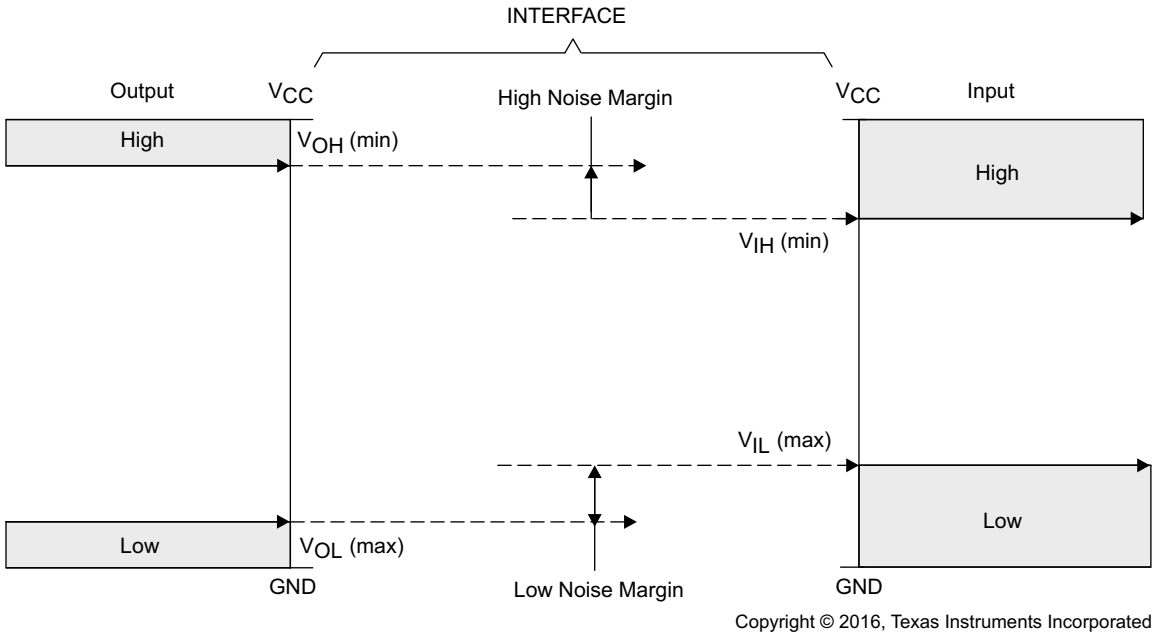


Figure 50. Logic Compatibility Between I/Os

For example, is the A-port output of an ABT device compatible with a B-port input of the same technology? Because the input of an ABT device is CMOS technology (I_I input current was discussed for determination of CMOS or bipolar input type), if it is connected in a point-to-point topology with an ABT output, the static dc current will be very low-leakage current range-and the V_{OH} level will not be lower than 2.5 V and the V_{OL} level will be no greater than 0.55 V. The input threshold to any ABT input port is set at the standard TTL/LVTTL threshold of 0.8 V - 2 V. Because the V_{OH} level of 2.5 V is greater than the minimum V_{IH} level of 2 V, and the V_{OL} level of 0.55 V is less than the maximum V_{IL} level of 0.8 V, these two ports are considered compatible.

Care must be taken when driving bipolar inputs because of the excessive currents at the input. If sufficiently large, the V_{OH} level could drop (or, conversely, the V_{OL} level could increase) to a level that violates the input threshold of the receiver.

Another major consideration is the voltage tolerance of the I/O structure. Simply because the previous conditions were satisfied, that does not mean I/Os are compatible. Take, for example, the same ABT output, which, if driving a CMOS input, will provide a V_{OH} level that will not be lower than 2.5 V and a V_{OL} level that will be no greater than 0.55 V, to drive an AHC input (which is CMOS) powered with a 3-V supply. The input threshold is met (that is, 2.5 V > 2.1 V and 0.55 V < 0.9 V), but the I/O voltage tolerance is only 3.5 V (3 V + 0.5 V). An ABT output is very capable of producing voltage logic-high levels greater than 3.5 V, therefore, an ABT (5-V V_{CC}) output is not compatible to an AHC input powered with a 3-V supply.

6 Detailed Description

The detailed description of the device including the functional block diagram of the device, functional modes which defines the truth table, feature description explaining in detail about the unique features of the device described in the initial page of the data sheet, belongs in this section.

7 Application and Implementation

This section details the device's typical application which it could be used for. The design requirements goes into detailing the design criteria and the calculation involved. Usually the recommended operating conditions and the absolute maximum conditions are highlighted to reinforce the device's capabilities and restrictions. The typical characteristics curve helps to describe the application's expected output.

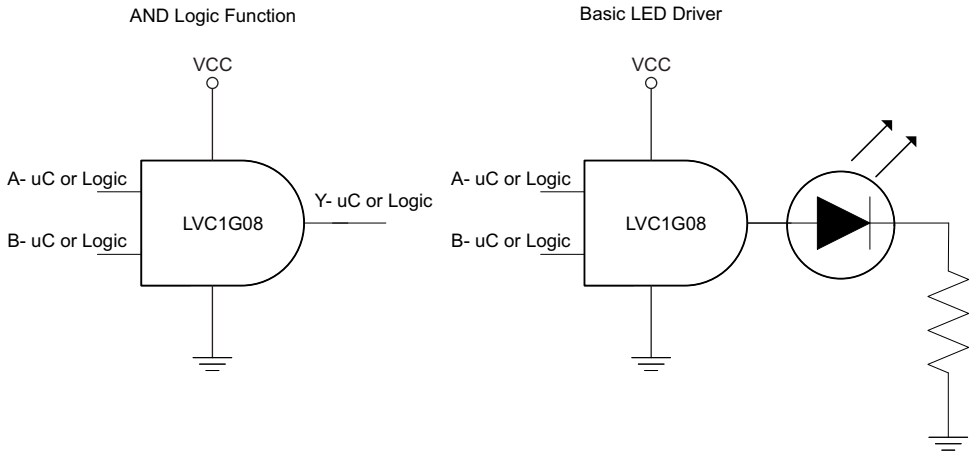


Figure 51. Typical Application for SN74LVC1G08

8 Power Supply Recommendations

Power supply guidelines are the best practice while using the device in the application described in this section. The operating voltage range of the device apart from the bypass caps which are best suited are discussed.

9 Layout

General layout guidelines for optimum performance of the device is discussed in this section. Basic rules of biasing the floating inputs which, otherwise, could cause instability in the application are among the topics discussed in this section.

10 Conclusion

The information in this application report is provided so that the designer can derive the maximum amount of information about standard-logic devices from the device data sheets. Texas Instruments provides this information to ease the task of the designer in incorporating standard-logic products into new system designs and upgrading legacy systems.

11 Acknowledgments

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12 References

1. *JESD88 - JEDEC Dictionary of Terms for Solid State Technology, First Edition*, JEDEC Solid State Technology Association, Arlington, VA, September 2001.
2. *Semiconductor Group Packaging-Outlines Reference Guide*, SSYU001, Texas Instruments.
3. *JEP103A - Suggested Product-Documentation Classifications and Disclaimers*, Electronic Industries Association, Arlington, VA, July 1996.
4. *CMOS Power Consumption and C_{pd} Calculation*, SCAA035, Texas Instruments.
5. *Bus-Hold Circuit*, SCLA015, Texas Instruments.
6. *JESD51-3 - Low Effective Thermal Conductivity Test Board For Leaded Surface Mount Packages*, JEDEC Solid State Technology Association, Arlington, VA, August 1996.
7. *Thermal Characteristics of Standard Linear and Logic (SLL) Packages and Devices*, SCZA005, Texas Instruments.
8. *Logic in Live-Insertion Applications With a Focus on GTLP*, SCEA026, Texas Instruments.

9. *Dynamic Output Control (DOC™) Circuitry Technology and Applications*, SCEA009, Texas Instruments.
10. *Implications of Slow or Floating CMOS Inputs*, SCBA004, Texas Instruments.
11. *JESD51-7 - High Effective Thermal Conductivity Test Board For Leaded Surface Mount Packages*, JEDEC Solid State Technology Association, Arlington, VA, February 1999.
12. *Power-Up 3-State (PU3S) Circuits in TI Standard Logic Devices*, SZZA033

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