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74 189  $\rightarrow$  Cam Ant.

Cam based multi capture  
module

mult module inputs

segments:  $16A + 16B + 1D = 33$

mult module outputs

segments: 1b

data in/out  
[0,3]

Cam Ant.

## Possible Places to Start Ram-access

- hard disk → i.e. floppy Q:
- Turbo Use static ram
- ↳ Possible time anomaly.

### Door Sequence:

1. Computer starts on wait instruction,  
assuming wait instruction does not involve  
data-demandant commands.
2. Computer auto loads into screen number/  
hard drive program and begins programming data  
demands into.

↓  
16 ready to use I/O pins for  
extra programming + extra signals.

26 I/O pins, 10 extra, 16 I/O.

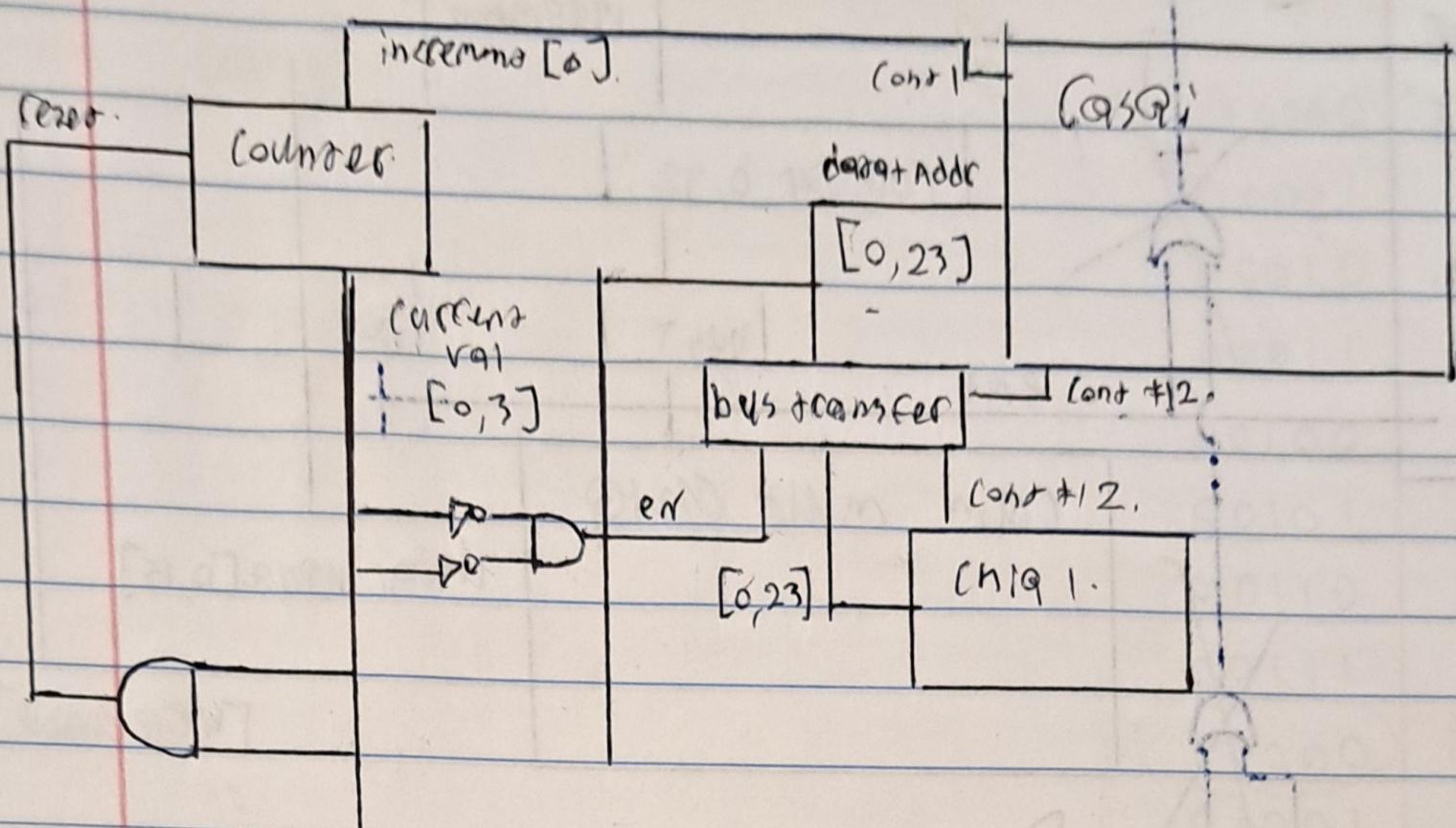
↓

2 bits for selected chip + 4 possible  
chips

b0 = write pulse

b1 = next chip advance pulse.

(ANSI Programming hardware:  
(Assuming 3 dd areas)



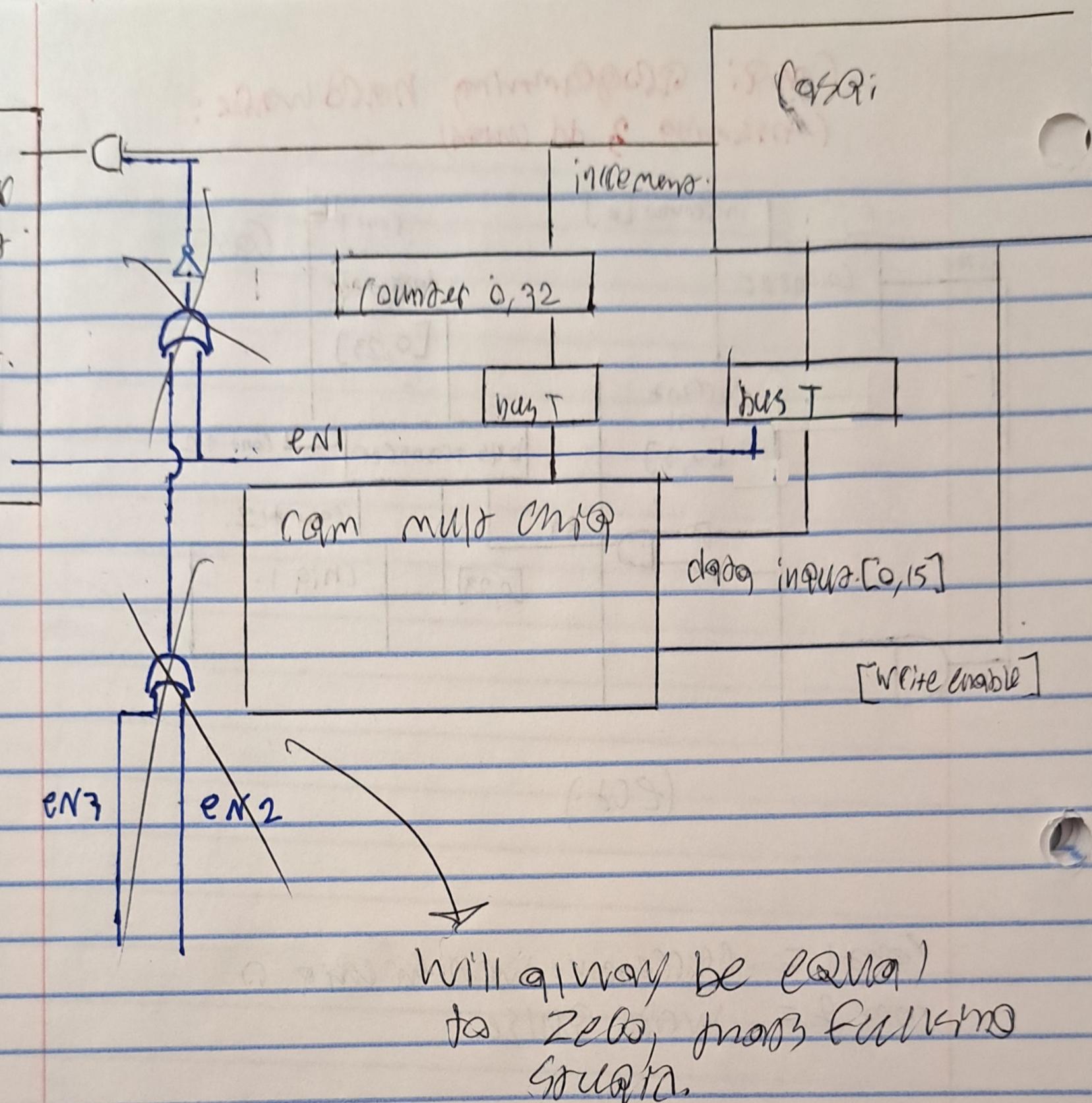
(ECS.)

Contra = Advance current on IP.

comp 2 = wave QHSE.

36.

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$$\frac{C_1}{00} \frac{C_2}{00}$$

It could be the caffeine in it

991

people with 12 could be for drug addicts

0010

recently being programmed on the chip.

0011

This would work ~~pretty~~ well if all the

0.150

dentists were roughly the same size in

0101

terms of what had to be programmed.

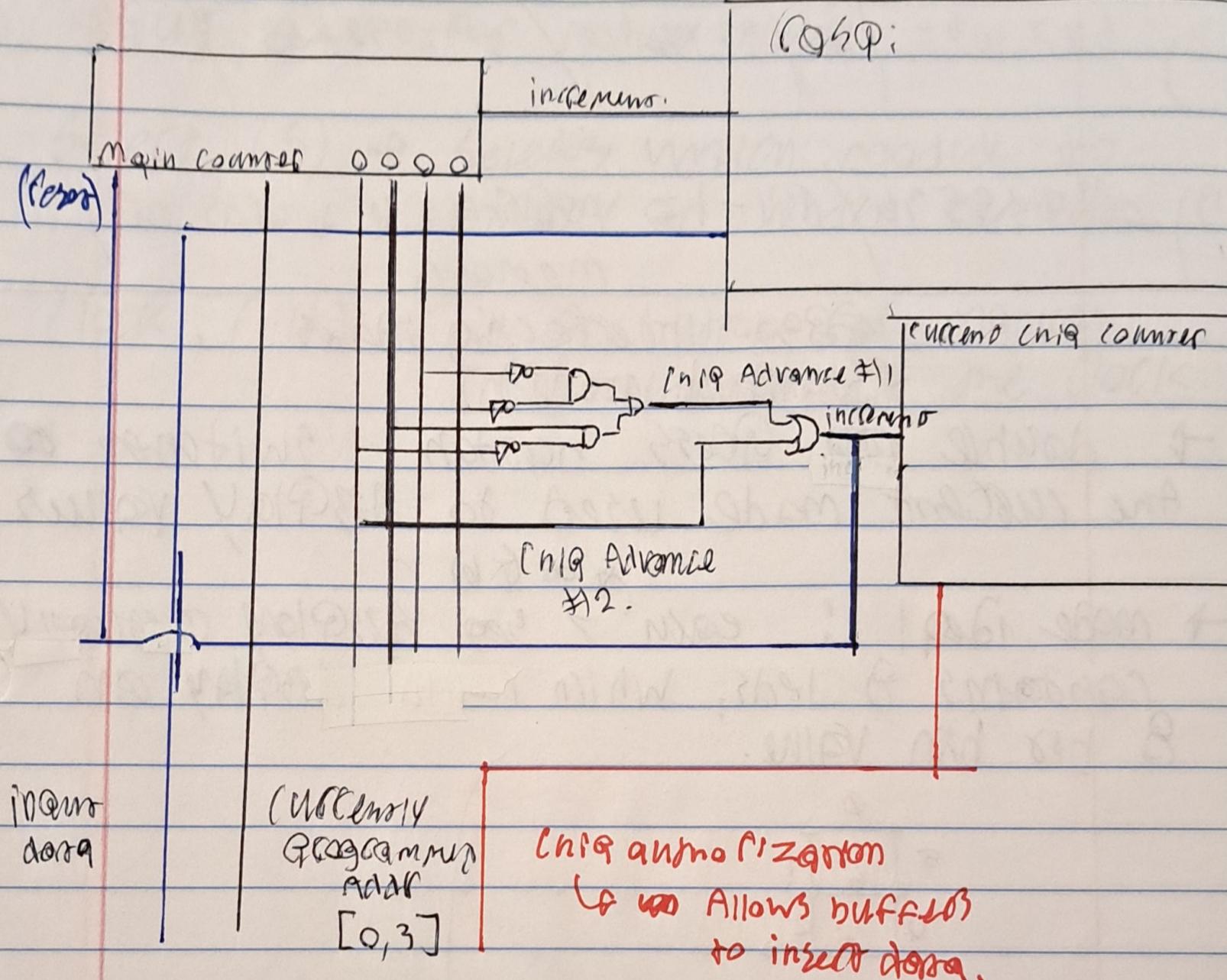
0110

100

0 111

1000

Assuming max sizes of 4 and 8 slots. Add  
Conts are programmed in order of smallest  
Capacity to largest capacity. 39



There is also another logic mechanism that checks  
for when last position is not, and makes  
sure the chq programming circuit is responsive  
to future inputs.

! Also, you need 50 latches when doing  
the smallest capacity programmed upon the first  
layer.

Sw

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0 0000

0 0001

0 0010

0 0011

0 0100 4

0 0101

0 0110

0 0111

0 1000 8

0 1001

0 1010

0 1011

0 1100

0 1101

0 1110

0 1111

1 0000

1 0001

1 0010

1 0011

1 0100

1 0101

1 0110

1 0111

1 1000

1 1001

1 1010

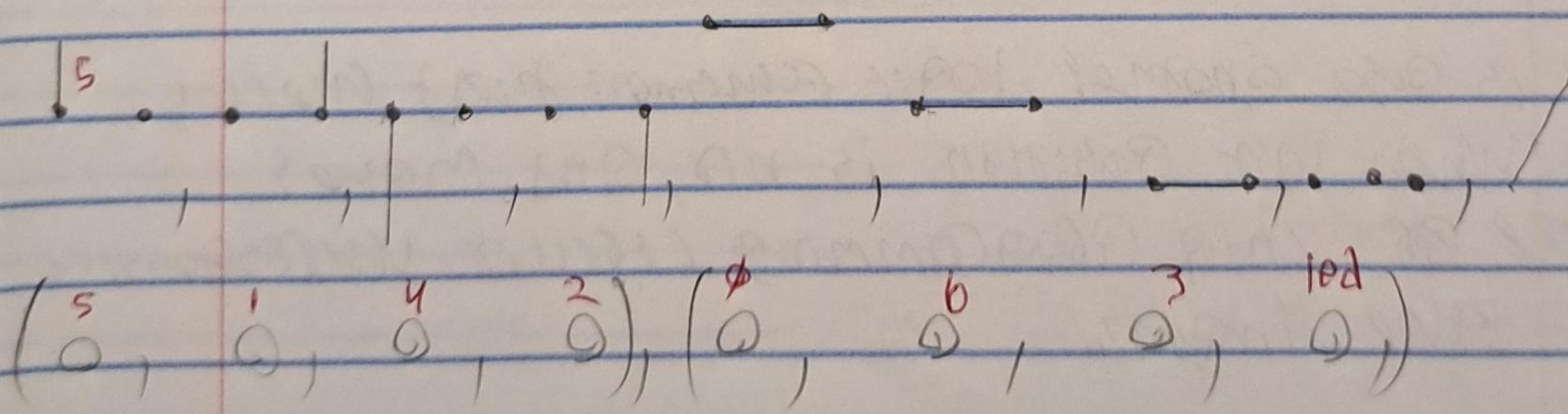
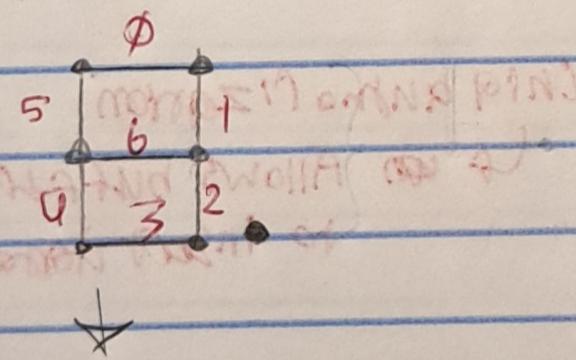
## FPGA Shopping Notes

$$A) 64 \times 10^6 = (2)(32 \times 10^6) / 2^15 = 32768 \cdot /$$

$$B) 2^{16} = 65536 / 131 - 1 = \text{Addressable words of memory}$$

FPGA interfacing ideas:  
(Standard mode)

- double ~~8~~ 7-seg board: switches ~~8~~ to the current mode used to display values
- mode idea: each ~~7~~ seg display ~~8~~ buttons, which could display an 8 bit bin value.



- Also has 10 LEDs, so max values: (4) + 2 extra

Q13 configurations:

00 input, I → fat module input.

01 Select, (S) → selects which module to display on which outputs.

01 CLOCK, (CLK) → is a button for manual implementation of the clock.

## Possible modes of interfacing

### 1. HEX VALUE MODE (8) (Signed) (lower)

In this mode two displays are implemented within utilizing 3 7-segment hex indicators each. The decimal value is shown for the currently selected module being either the upper or lower 8 bits. ~~This~~ You can also select whether this value is signed or not, if a signed value is negative, the decimal place on each indicator is off the display lights up.

### 2. HEX VALUE MODE (16) (Signed).

A 16 bit value requires 5 indicators for the max value, so, this takes the whole set of indicators. Maybe the remaining indicators could be used to display a front minus sign. :-)

(Standard mode)

Contains 10 slice switches, 4 buttons. 41

