Kmap

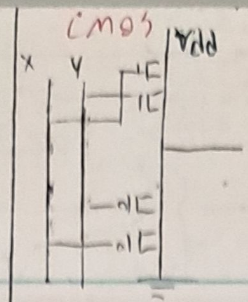
C ($C_1 C_0 A B$)

C_1C_0 \ AB	00	01	11	10
00	1			
01			1	
11		1	1	1
10	1		1	

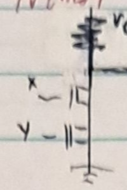
simplified logic

A) $\bar{C_0}\bar{A}\bar{B} + C_1C_0B + C_0AB + C_1C_0A + C_1AB = f$

CMOS (x•y)



NMOS $\overline{x \cdot y}$



SOP reduction

$\bar{x_1}\bar{x_2}x_3 + \bar{x_1}\bar{x_2}\bar{x_3} = \bar{x_1}\bar{x_2}$

POS reduction

$(\bar{x_1}+x_2+x_3)(\bar{x_1}+x_2+\bar{x_3}) = (\bar{x_1}+x_2)$

SOP problem solving

A) $m_0+m_1+m_2 = m_0+m_0+m_1+m_2 = \sum m(0,1,2)$

POS problem solving

A) $(M_0)(M_1)(M_2) = (M_0)(M_0)(M_1)(M_2) = \prod M(0,1,2)$

POS source

A) $f(x_1,x_2,x_3) = m_0+m_2+m_3+m_7$

$\bar{\bar{F}} = F = m_0+m_2+m_3+m_7$

$= (\bar{m_0})(\bar{m_2})(\bar{m_3})(\bar{m_7}) = (M_0)(M_2)(M_3)(M_7)$

SOP KMAP

A) missing logic $= \prod M(4,5,6) = (\bar{x_1}+x_2+x_3)(\bar{x_1}+x_2+\bar{x_3})(\bar{x_1}+\bar{x_2}+x_3) = \bar{F()}$

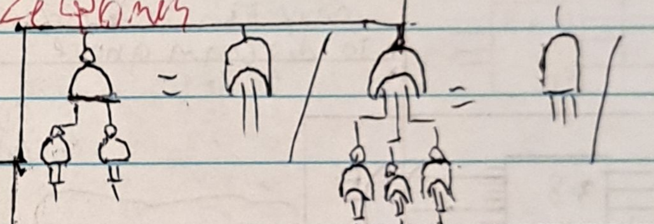
B) $= (0\,0\,0)(0\,1\,0\,1)(0\,1\,1\,0)$ / M_4 = location of zero / $(\ , x_1, x_2, x_3)$

When $F=0$, $\bar{F}=1$

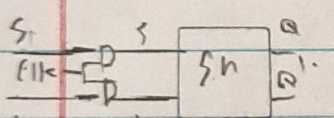
Nand primes

x_3 \ x_1x_2	00	01	11	10
0	1	1	0	0
1	1	1	1	0

3 inverters, 2 primes



C) simplified logic $= f = (\bar{x_1}+x_2)(\bar{x_1}+x_3)$



= Gated SR latch

XOR boolean algebra

$X \oplus 0 = X$ $\quad A \oplus AB = A\bar{B}$

$X \oplus 1 = \bar{X}$ $\quad A \oplus A\bar{B} = AB$

$X \oplus X = 0$ $\quad A \oplus \bar{A}B = A+B$

$X \oplus \bar{X} = 1$ $\quad (A\oplus B)(A\oplus C) = \bar{A}BC + A\bar{B}\bar{C}$

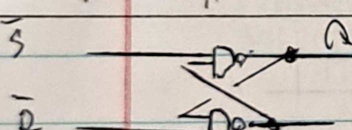
$\bar{X} \oplus \bar{X} = 0$

$X \oplus \bar{X} = \overline{X \oplus X}$

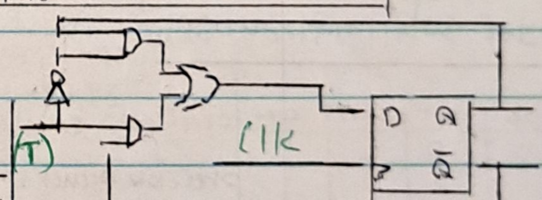
Flip flop = edge triggered

latch = whenever 1 0

(TFF)

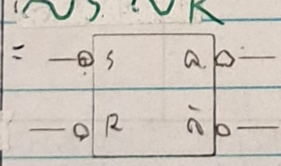


= ~S ~R latch

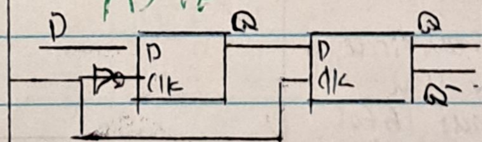


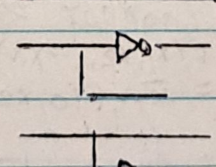
S̄	R̄	Q
0	0	1
0	1	1
1	0	0
1	1	0/1

~S~R latch same =



MS FF





= Positive edge

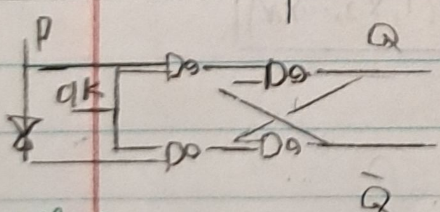
= Neg edge

MS FF Negation

(T)

T	Q(T)
0	Q(T−1)
1	$\overline{Q(T-1)}$

a one on T switches the current value of Q, to Q̄, when the positive edge of clock occurs.

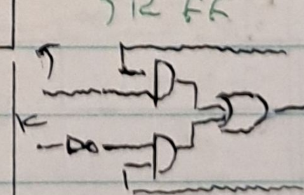


Gated D latch

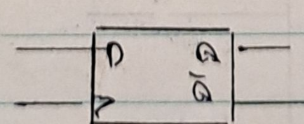
Clk	D	Q(T)
0	X	Q(T−1)
1	0	0
1	1	1

= Gated S latch table.

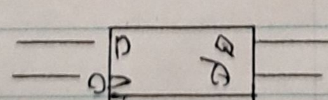
JK FF



everything about T flip flop the same except T is broken into J and K inputs.



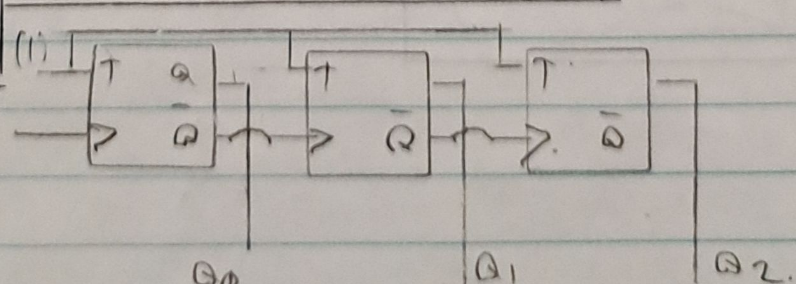
} Positive edge.

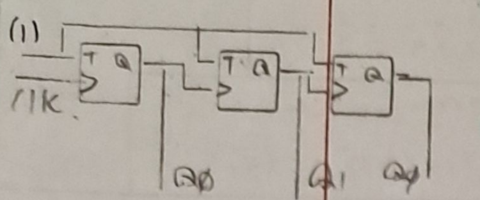


} Negative edge

- counts clock cycles passed.
- on rising edge = increments value

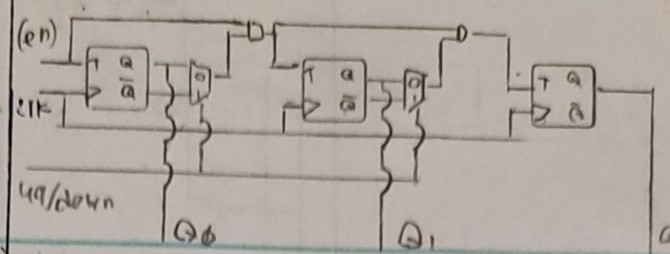
up counter with TFF



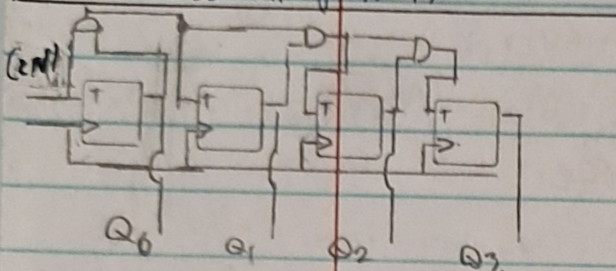


TFF down counter (Asynchronous)

On rising edge, de-increment current value of clk that is

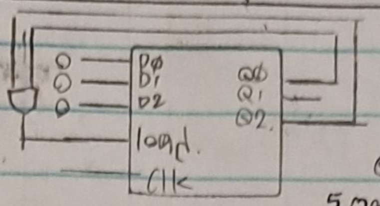


Synchronous up/down counter with en function



Synchronous up counter with TFF

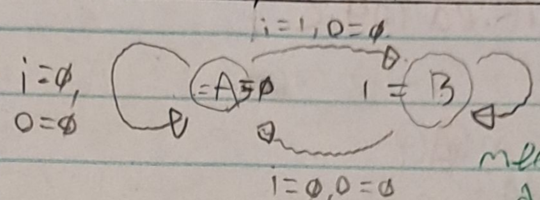
Shared clk signal = synchronous. While en = 1 will count upwards. Every and in the circuit has en as an input, and as a result, if en = 0 no toggling will occur.



Modulo-6 up counter synchronous reset

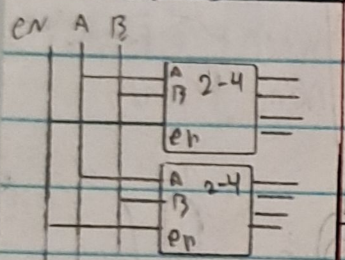
When $Q_2 - Q_0 = 5$, load pin goes high and resets
5 mod 2 = 1, 5 mod 3 = 2

Counts from 0 to 5, never reaches six



Mealy state diagram

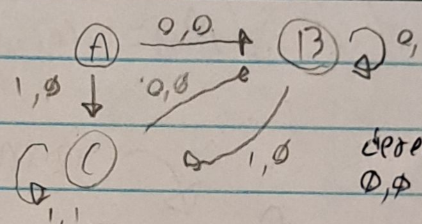
W = input
Z = output
FSM bit notation



3-8 decoder w 2-4 decoders

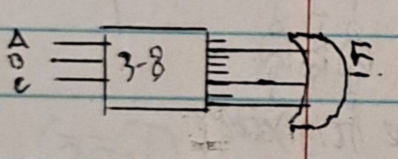
w	s	s+1	z
0	0	0	0
0	1	0	0
1	0	1	0
1	1	1	1

Mealy FSM TT → corresponds to diagram above



Sequence detector FSM

detects pattern of 0,0 or 1,1



$F = \bar{A}BC + \bar{A}B\bar{C} + ABC + A\bar{B}C$

decoder SOP implementation

C_i	X_i	Y_i	S_i	C_{i+1}
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Full Adder

$S_i = C_i \oplus X_i \oplus Y_i$

$C_{i+1} = XY + XC + YC$

$overflow = (C_{n-1}) \oplus C_n$

Overflow occurs in red circle, and the overflow you really care about is for the sign bit, the full adder handling the sign bits is the one only one that matters.

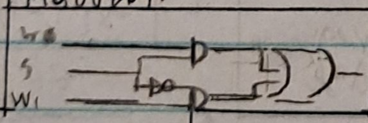
Present state	Next state		Output z	
	W=0	W=1	W=0	W=1
A	B	C	0	0
B	B	C	1	0
C	B	C	0	1

w	s_2	s_1	s_{2+1}	s_{1+1}	z
0	0	0	0	1	0
0	0	1	0	1	1
0	1	0	0	1	0
0	1	1	X	X	X
1	0	0	0	1	0
1	0	1	0	1	0
1	1	0	0	1	1
1	1	1	X	X	X

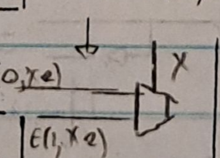
Sequence detector FSM truth table + pseudo TT

i	s_1	s_0	s_{1+1}	s_{0+1}	out
0	0	0	0	0	0
0	0	1	0	0	0
0	1	0	0	0	1
0	1	1	x	x	x
1	0	0	0	1	0
1	0	1	1	0	0
1	1	0	1	0	1
1	1	1	x	x	x

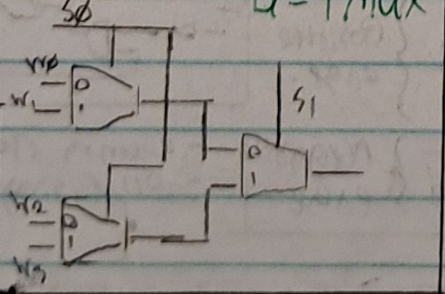
Shannon expansion theorem
$F(x_1, x_2, \dots x_n)$ can be written as
$= \bar{x}_1 \cdot F(0, x_2 \dots x_n) + x_1 \cdot F(1, x_2, \dots x_n)$



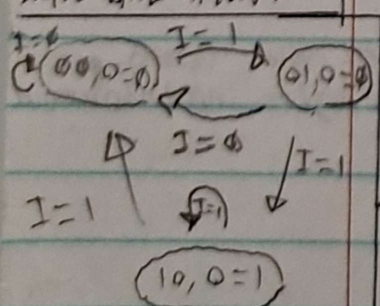
2-1 mux



Moore FSM, output depends only on current state, each state bit in next iteration depends on cur state and input.



4-1 mux



Moore FSM diagram corresponds to TT above.