

Hardware computation of conductance-based neuron models

L. Alvado¹, J. Tomas¹, S. Saïghi¹, S. Renaud¹, T. Bal², A. Destexhe², G. Le Masson³

¹*Laboratoire IXL, CNRS UMR 5818, ENSEIRB-Université Bordeaux 1, 351 cours de la Libération, 33405 Talence, France.*

²*Unité de Neurosciences Intégratives et Computationnelles, CNRS UPR 2191, Institut de Neurobiologie Alfred Fessard, 1 av. de la Terrasse, 91198 Gif-sur-Yvette, France*

³*Laboratoire de Physiopathologie des Réseaux Neuronaux Médullaires, EPI INSERM 9914, Institut François Magendie, Univ. Bordeaux 2, 1 rue C. St Saëns, 33077 Bordeaux, France.*

Understanding how neurons and networks can process information through their electrical activity is one of the major issue of computational neuroscience. Theoretical approaches have made successful use of neural simulation software packages dedicated to biologically realistic simulations. However, there are still difficult compromises to be done between the precision of the models and the computing speed that limits the model's complexity, at the single neuron level as well as at the network level. We propose an alternative technical approach for temporal simulation, based on hardware real-time computation of conductance-based neuron models.

- We start by reviewing analog circuit implementations of Hodgkin-Huxley type models. We designed specific analog integrated circuits (ASICs) which exploit the intrinsic voltage-current of individual transistors (bipolar and MOSFET) to simulate the membrane equation of neurons including voltage-dependent conductances [1]. Synaptic conductances can also be modeled using a similar representation. The model variables (state variables, conductances, ionic currents, membrane voltage) are identified to electrical variables in the circuit (currents, voltages). The circuit computes them continuously and in real-time. The model's parameters can be tuned via dedicated circuit inputs. We illustrate a configurable single-neuron analog ASIC circuit including 6 programmable conductances, which can be used to simulate the salient dynamical properties of most central neurons (such as the adapting neurons of cerebral cortex, thalamic bursting, etc).

- We next illustrate an original approach to address computational neuroscience issues based on these circuits. Artificial neurons act as a dedicated processor, which computes in real time the activity of the simulated neuron. Electronics boards support these circuits, and are connected to a standard computer. The computer runs a user interface, to control the hardware models and treat the simulation results. Direct analog outputs of the chips are available for external connections. They replicate the neuron membrane voltages and the synaptic currents; they also allow the construction of hybrid neural networks, in which hardware artificial neurons are connected to living neurons, via artificial synapses and intracellular micro-electrodes.

- We illustrate the use of analog neurons in the study of the thalamus filtering properties. The thalamus is major relay structure of the brain where major sensory pathways (visual, somatosensory, auditory...) are relayed to cerebral cortex. This position allows the thalamus to filter or faithfully transmit this sensory information depending on the state of arousal (sleep, awake). To study how this sensory gating is performed, we have investigated the interaction between two cell types, the thalamocortical neurons (TC) that relay sensory inputs from the sensory organs (retina, cutaneous receptor, ears, ..), and local inhibitory interneurons (nRt). These two cells populations are reciprocally connected by an excitatory (TC to nRt) and inhibitory (nRt to TC) loop. This network was modeled in real time using analog circuits and was used to study the role of oscillations on information transfer by the visual thalamus. It appeared in the simulation that changes in the synaptic gains did affect the temporal

correlation between nRt spikes and TC spikes, thus offering a mechanism for spike transfer control. The validity of that hypothesis was recently proven by hybrid experiments on the TC-nRt network [2].

- We next present a new tool which is presently developed to address neural computation at the network level. We designed a mixed analog-digital architecture in which all membrane equations including synaptic integration are solved by analog ASIC circuits, while the connectivity is managed by a digital interface. Analog neurons are similar to the ASIC circuits described above, except that the model parameters are limited to a few configurations (excitatory and inhibitory neurons based on Hodgkin-Huxley type kinetics). Synaptic interactions are modeled using simple "monoexponential" kinetic synapses [3] where the synaptic conductance increases instantaneously of a given "quantal conductance" when a presynaptic spike occurs, then relaxes exponentially to zero. The neural activity and the presynaptic information are digitally coded; the digital interface reads the neuron's activity (spikes), and dispatch them as inputs to other neurons according to the connection matrix, which is digitally controlled. The main advantage is flexibility: different types of connectivity can be tested, as well as different types of plasticity rules (also managed by the digital interface). The system can also be used to implement probabilistic release and short-term plasticity.

- We terminate by showing results from a prototype analog/digital network of a few excitatory and inhibitory neurons connected via glutamatergic (AMPA) and GABAergic synapses. We compare the activity of the network to numerical simulations for simple configurations of connectivity. In principle this type of architecture can be scaled up to simulate hundreds or even thousands of neurons in real time, depending on the speed of the digital interface. We give estimates of the maximal size realizable using presently available processors for different types of network architectures.

In conclusion, we show here that ASIC circuits can provide useful tools for computational neuroscience, both at the single-cell and network levels, such as the confinement of models of spiking neurons and synaptic plasticity, with mechanisms such as simple weight updates, or more complex algorithms such as spike-timing dependent synaptic plasticity (STDP, weight updates dependent on the temporal relation of activity). The most fascinating application is probably the possibility of interfacing single neurons - or networks of neurons - to intracellularly-recorded neurons in slices or even in vivo. Such applications necessarily require models simulated in real time, in which case the present approach can be extremely useful.

References

- [1] Le Masson, S., Laflaquière, A., Dupeyron, D., Bal, T., Le Masson, G., Analog circuits for modeling biological neural networks: design and applications, *IEEE Transactions on Biomedical Engineering*, **46-6**, 638-645 (1999).
- [2] Le Masson, G., Renaud-le Masson, S., Debay, D., Bal, T., Feedback inhibition controls spike transfer in hybrid thalamic circuits, *Nature*, **417**, 854-858 (2002).
- [3] Destexhe, A., Mainen, Z., Sejnowski, T., Synthesis of models for excitable membranes, synaptic transmission and neuromodulation using a common kinetic formalism, *J. Computational Neurosci.*, **1**, 195-230 (1994).
- [4] Bi G., Poo M., Synaptic modification by correlated activity: Hebb's postulate revisited, *Annu. Rev. Neurosci.*, **24**: 139-166 (2001).