A Selective Attention Chip for implementing multi–chip sensory systems

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Abstract

Selective attention is a process widely used by biological sensory systems to overcome the problem of limited parallel processing capacity: salient subregions of the input stimuli are serially processed, while non–salient regions are suppressed. We present an analog Very Large Scale Integration implementation of a building block for a multi–chip neuromorphic hardware model of selective attention. We describe the chip's architecture underlining the similarity between the circuits and biological neurons and synapses. We plan to present experimental results that explore the dynamics of the system varying its bias settings corresponding to physiological properties of neurons and synapses.

Key words: Selective Attention, AVLSI, Multi–Chip Systems

1 Introduction

Selective attention is one of the most powerful strategies used by biological systems, from which robotics and in general all artificial computation can take advantage. In a biological sensory system, selective attention acts as a dynamical filter that selects the most salient regions of the input, sequentially allocating computational resources, for analyzing the target. This strategy limits the computational demand respect to parallel processing.

Many of the models proposed on the literature, both software [13,3,18,1] and hardware [4,7,16,8] are based on the concept of *saliency map* proposed by Koch and Ullman [14]. These types of models account for many psychophysical and neurophysiological observations [12]. Hardware implementations of selective attention systems have the advantage of real time computation and compactness: they can be used for building artificial systems that interact with real world stimuli in real time, with immediate, measurable reactions to the stimuli. From this point of view hardware implementations can be a powerful tool for studying computational properties of different types of selective attention models.

Here we present a module, the Selective Attention Chip (SAC), that is a building block for hardware multi–chip sensory systems based on selective attention models. The SAC was designed using a standard $0.35\mu m$ CMOS process and occupies an area of $2.5 \times 2.5mm^2$; it was realized with neuromorphic Very Large Scale of Integration (VLSI) technology that allows us to directly map biophysical neuronal

properties onto silicon.

The SAC contains an array of 32×32 cells, laid out on a square grid. Each cell in the bidimensional array comprises an input circuit that models the dynamics of a biological excitatory synapse, generating Excitatory Post–Synaptic Currents (EPSCs), a hysteretic Winner–Take–All (WTA) competitive element [9], an output leaky, adaptive, low–power Integrate and Fire (I&F) neuron [17] and a feedback inhibitory synapse.

Input and output signals are interfaced to an external bus with Address Event Representation (AER) circuits. The AER is inspired by cortical communication: it is based on asynchronous standard events (spikes) that encode the address of the sending neuron and carry the information in their temporal structure (for an introduction see chapter 3, ”The Silicon Optic Nerve” in ”An analog VLSI System for Stereoscopic Vision” [15]). This protocol allows the chip to communicate using spikes, just like the cortex, and can be used in multi–chip systems, with multiple senders and multiple receivers [5,6]. Using this representation the SAC can exchange data, while processing signals in parallel, in real time [10].

Input spikes arriving for example from a silicon retina [10] or from a software based vision system [8] are integrated by the excitatory synapses of the array into excitatory analog currents (see I_{ex} of Fig.1); each synaptic circuit implements a local gain control mechanism to model short time depression [2], observed in physiological recordings.

The resulting excitatory current goes to the correspondent WTA cell that competes with the other cells by means of lateral excitatory and inhibitory connections. The spatial extent of the competition can be set by the strength of these lateral connections; in particular we can set global competition, allowing only one cell to win, or we can have local competition, with multiple spatially distant winners.

As soon as a cell wins the competition it sources a fixed amount of current I_{inj} (see Fig.1) in the membrane capacitance of an adaptive, leaky, low power I&F neuron [11]. As soon as the membrane voltage crosses a threshold, the neuron spikes, with a frequency that depends on the current amplitude. Thanks to its spike–frequency adaptation mechanism, the firing rate of the winning cell decreases with time.

The output spikes go to an arbitration circuit that sends the address of the winning pixel to the AER bus and, in parallel, to the corresponding inhibitory synapse that is responsible for generating the inhibitory current I_{ior} (see Fig.1); this current is subtracted from the input excitatory current I_{ex}, therefore the net input current to the winning cell decreases until a different cell is eventually selected as winner. This negative feedback mechanism is known as Inhibition of Return (IOR), it allows the network to deselect the winning cell and switch between inputs with different salience.

The SAC has been designed with tunable parameters that allow to modify the strength of synaptic contributions, the dynamics of synaptic short term depression and of neuronal adaptation, as well as the spatial extent of competition and the dy-

namics of IOR. All these parameters enrich the dynamics of the network that can be exploited to model the complex mammal selective attention scan path.

Our goal is to use the WTA chip as building block for multi–chip models of selective attention: its analog, continuous–time response characteristics, its ability to interact with the real world in real time, the adjustable properties of many of its circuits, and the spike–based communication infrastructure adopted, allows us to investigate different architectural and computational hypotheses of selective attention models and possibly to validate current theories of selective attention mechanisms. We plan to present experimental results of a test system composed of the SAC interfaced to a 32×32 silicon retina. We will explore the dynamics of the system varying its bias settings corresponding to physiological properties of neurons and synapses such as adaptation rates and short term depression time constants.

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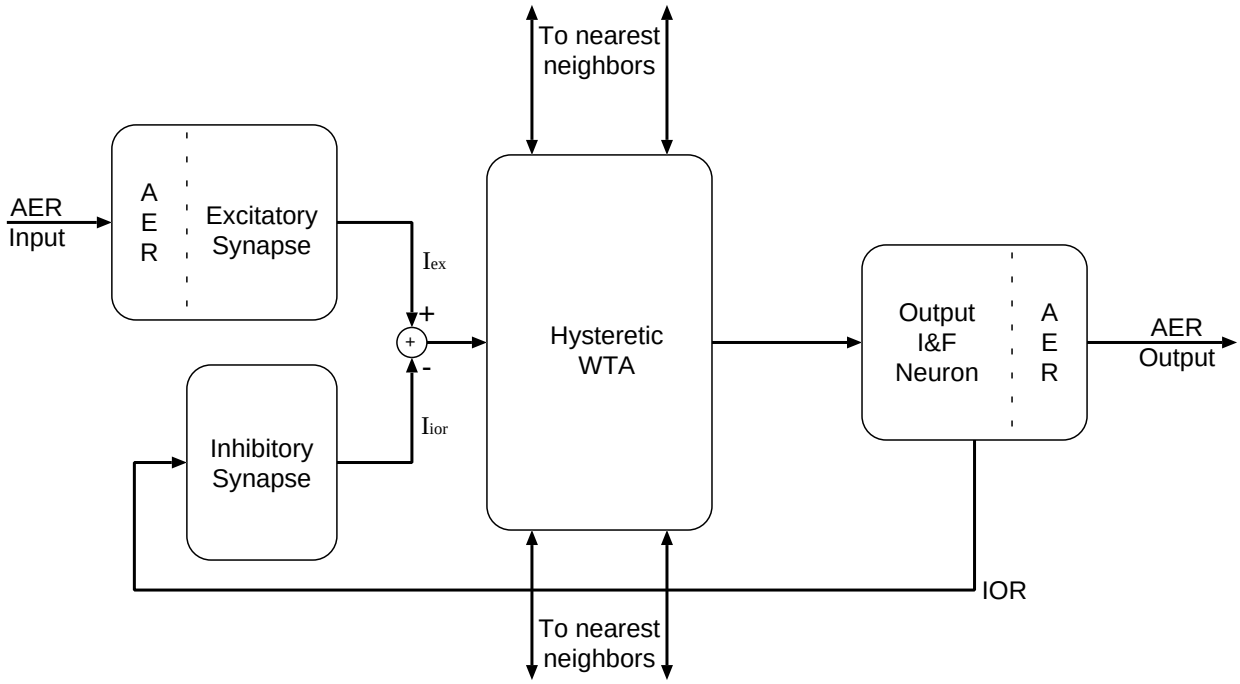

Fig. 1. Block diagram of the SAC elementary cell.

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