Digital Assignment1 – Dr. Waweru.

Using LTSPICE design a DTL NAND gate and simulate for 5 clock cycles

1. Remove Diode D_A and D_B and repeat.
2. Return D_A and repeat with additive noise of 0.7 or higher.
3. Return D_B and repeat with additive noise of 0.7 or higher.
4. Report you findings using three power point slides.