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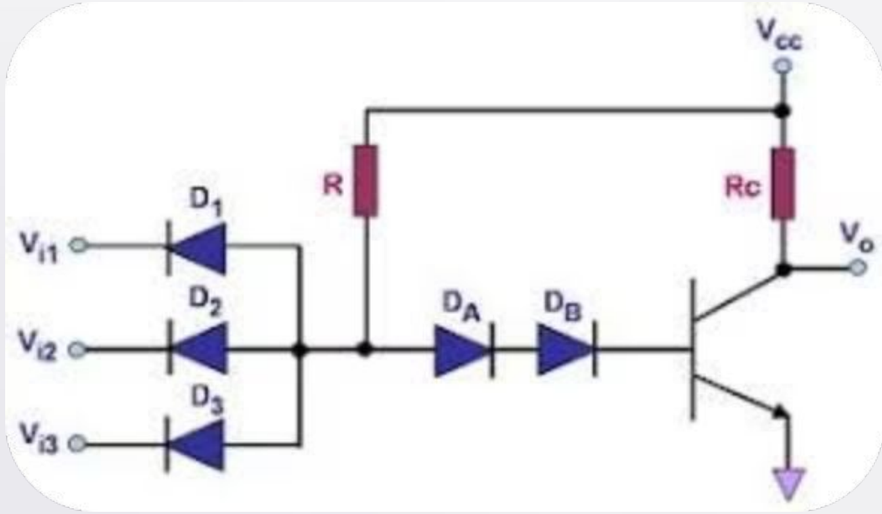
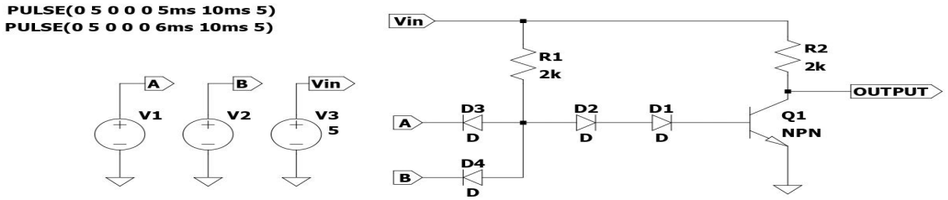
Simulation of DTL NAND Gate: Diode Effects and Noise Analysis

Exploring the impact of component modifications in a basic DTL NAND gate



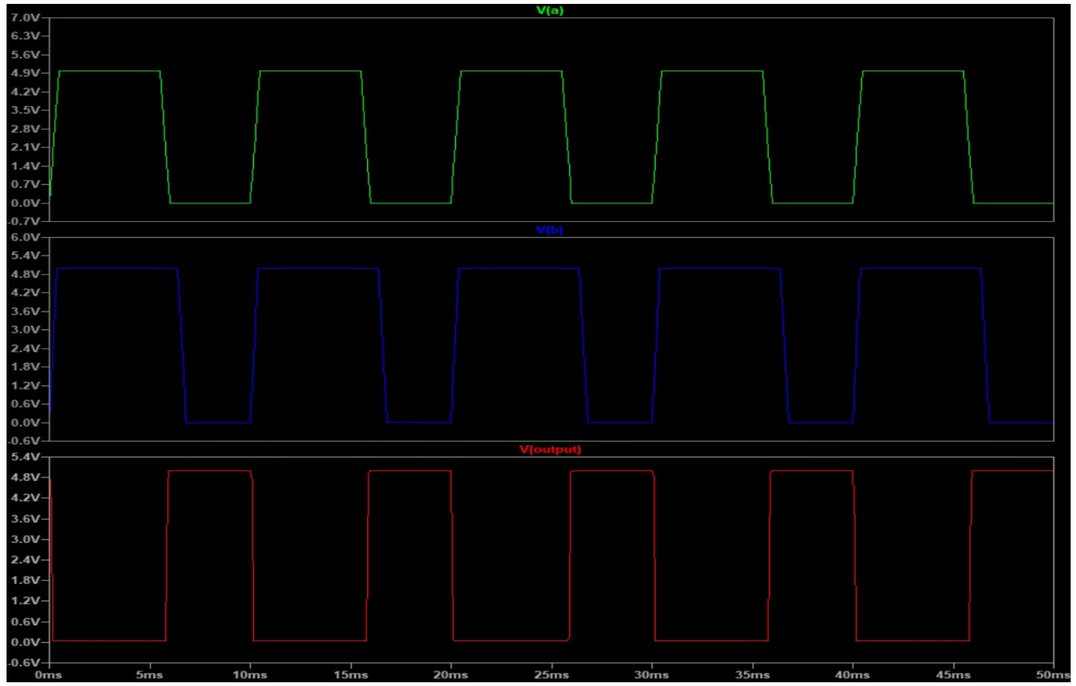
DTL NAND GATE ANALYSIS

schematic Diagram



Output LOW only if **both inputs are HIGH**

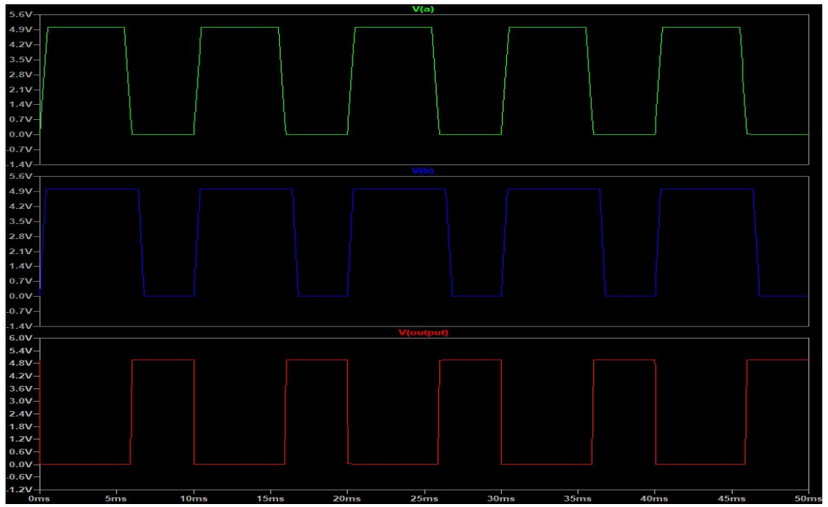
simulation Results

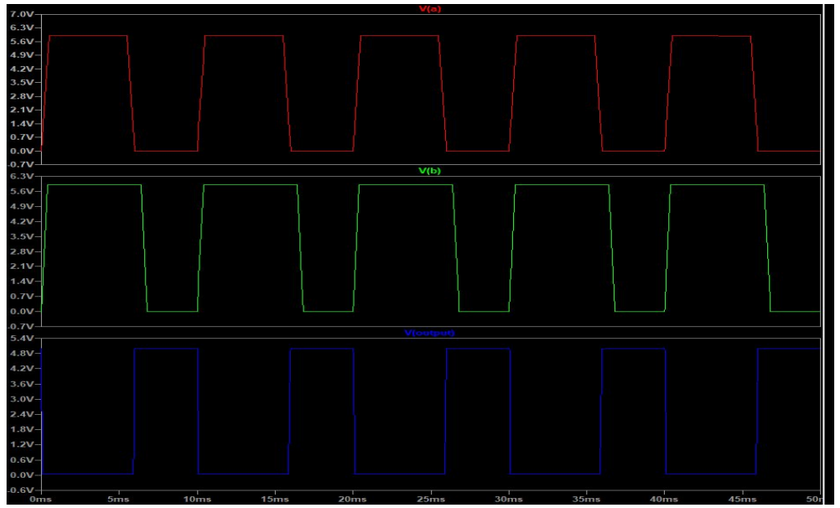


Truth Table

A	B	F
0	0	1
0	1	1
1	0	1
1	1	0

Effect of Removing Diodes & Noise





Remove middle 2 diodes

Output logic fails (always **HIGH** or **unstable**).

Inserting D3 and additive noise of 0.9v

The output is partially stable.

Inserting D4 and D3 and additive noise of 0.9v

The output of the DTL NAND gate is stable.