

School of Electrical Engineering and Computer Science
University of Ottawa



uOttawa

**ELG 4137 – PRINCIPLES AND APPLICATIONS OF VLSI
CIRCUITS**

WINTER 2025

VLSI Custom Design Project

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I. Introduction

In this design project, we developed a 4x1 multiplexer with an enable function. The design process involved following custom design steps such as Electrical Rule Check (ERC), Design Rule Check (DRC), Layout vs. Schematic (LVS), Parasitic Extraction (PE), and more. The entire process was completed using the Virtuoso Cadence schematic and layout CAD tool, which we became familiar with during the laboratory sessions of this course. We then simulated our circuit and analyzed the obtained results.

II. Objective

The objective of this project was to design and implement a 4x1 multiplexer using a custom design approach. This project served as an opportunity to apply VLSI concepts learned during the course and laboratory sessions, allowing us to gain hands-on experience in schematic and layout design, simulation, and verification.

III. Project Methodology

To fully design and implement the 4x1 multiplexer, the project was divided into several parts, each focusing on a specific step of the design process. These divided tasks include different objectives such as: a paper design, a subblock design, etc. Each part was essential to ensure the accuracy, functionality, and reliability of the final design.

In the following sections, we will provide a detailed summary of each part, describing the tasks completed and the results obtained.

Part 1: Paper Design

In this part, we extracted the process parameters of NMOS and PMOS transistors from the PDK (45-nm GPDK) to perform hand calculations. We focused on calculating the appropriate transistor sizing to achieve symmetric switching (DC calculations) for each CMOS logic gate and performed transient calculations to determine propagation delays.

However, we did not perform the sizing of the transmission gates to match the calculated delay of the CMOS inverters, as this step was not required for our project.

We documented our process, including the calculations, the schematic drawings and the models used, to ensure clarity and reproducibility.

1. For each CMOS logic gate: perform DC calculations and design your transistors' sizing to achieve symmetric switching.

Our design includes two kinds of logic gates, which are the INVERTER and the NAND-2. We set W_{min} to 240 nm.

- **INVERTER**

Extracted values from the model files are:

$$t_{ox} = 2.4 \text{ nm}; \epsilon_{ox} = 3.45 \times 10^{-11}; \mu_p = 24.7139 \times 10^{-3}; \mu_n = 15.4945 \times 10^{-3} C_{ox}$$

$$= \frac{\epsilon_{ox}}{t_{ox}} = 0.014375 \text{ F}$$

$$W_n = W_{min} = 240 \text{ nm}$$

$$W_p = \frac{\mu_n}{\mu_p} W_n = 154.844 \text{ nm}$$

- **NAND-2**

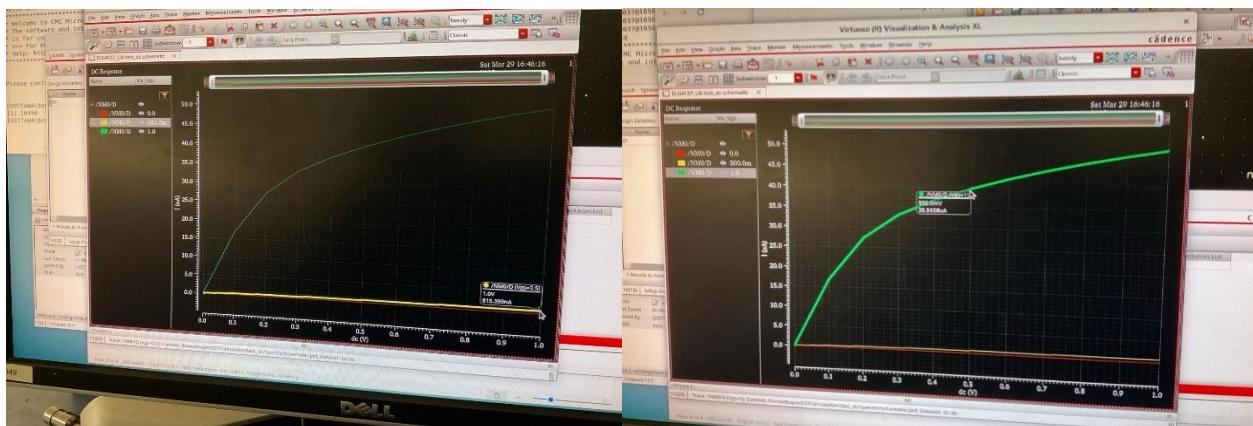
$$W_p = \frac{\mu_n}{\mu_p} W_{min} = 154.844 \text{ nm}$$

$$W_n = W_p = 154.844 \text{ nm}$$

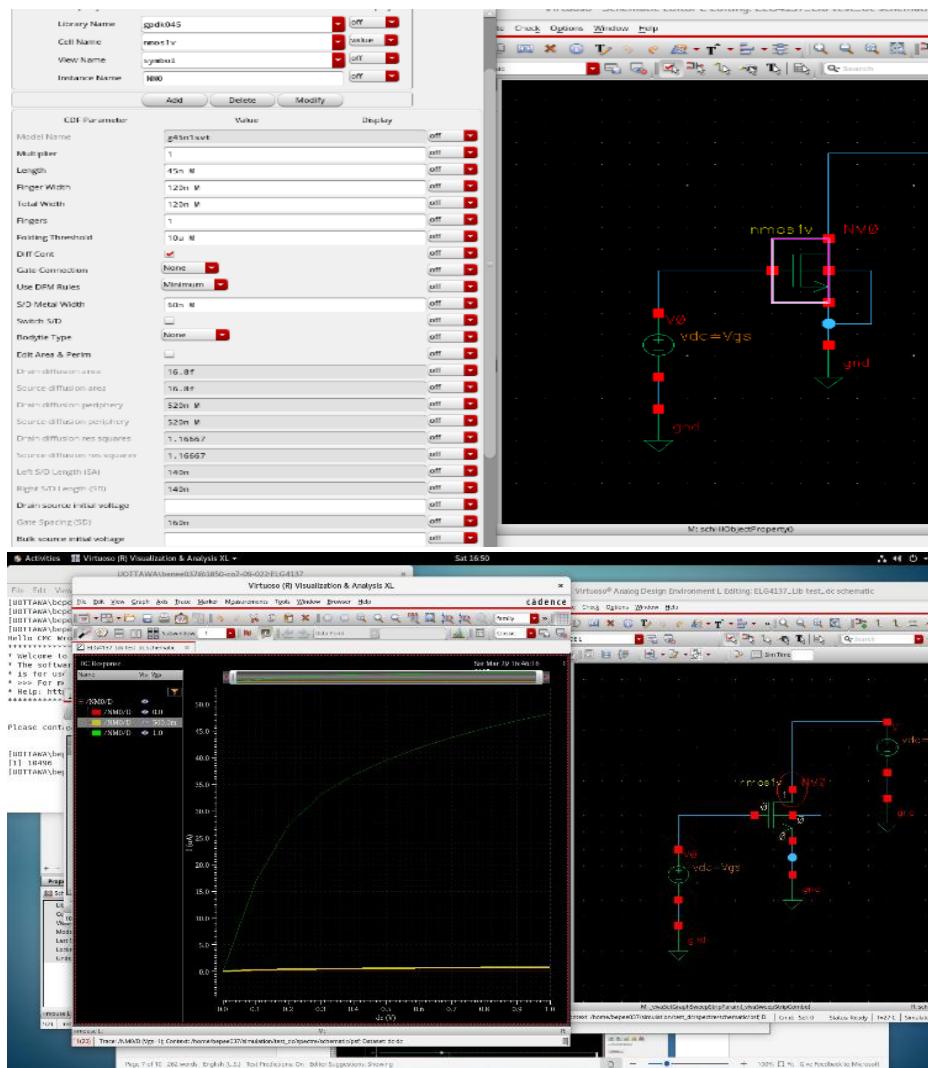
2. For each CMOS logic gate: perform transient calculations to obtain propagation delays.

In this step we drew transistor I-V curves, and we collected IL and IH values at 1V and 0.5V respectively.

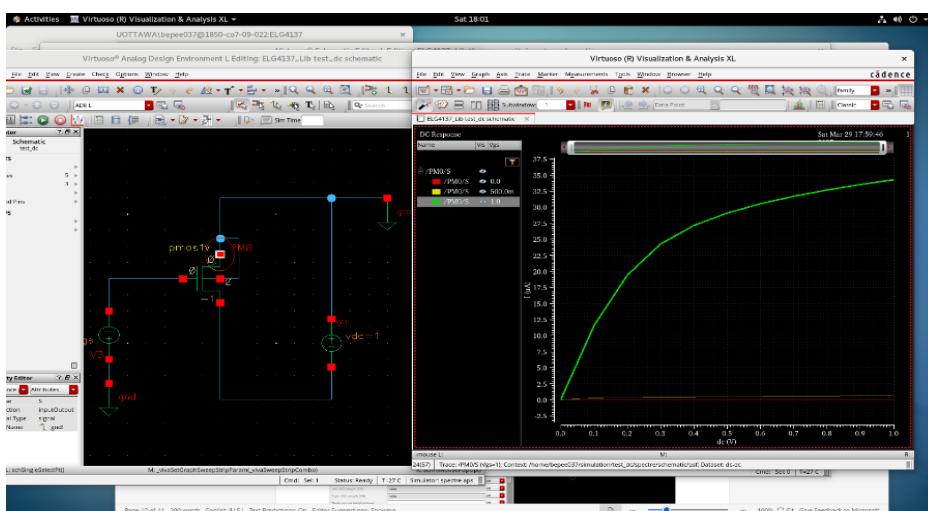
Low current I_L and High current I_H values simulated for resistance calculation.



Nmos Vds/Ids (DC sweep)



Pmos Vds/Ids (DC sweep)



- **INVERTER**

$$t_{ox} = 2.4 \text{ nm}; \epsilon_{ox} = 3.45 \times 10^{-11}; \mu_p = 24.7139 \times 10^{-3}; \mu_n = 15.4945 \times 10^{-3}$$

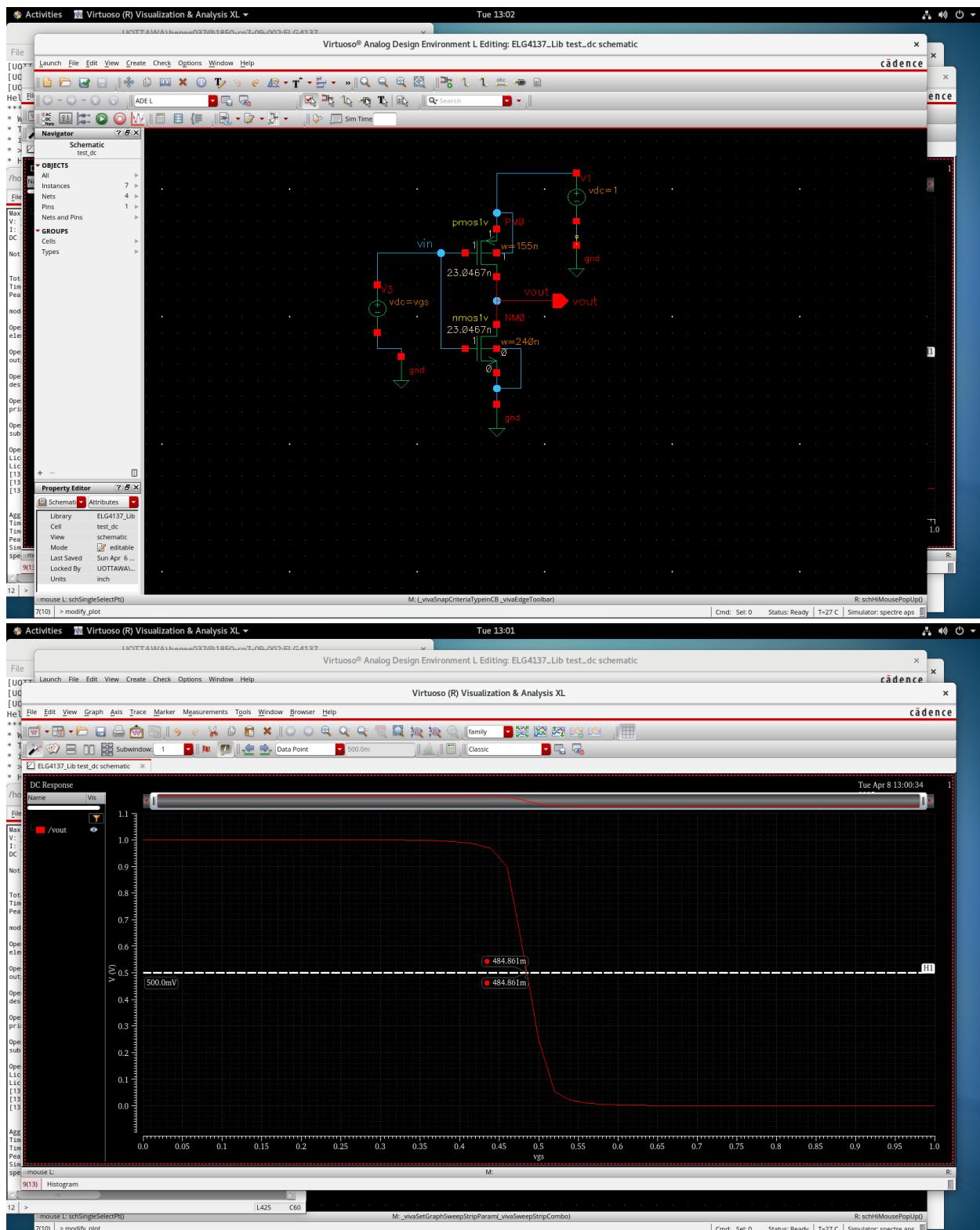
$$C_{ox} = \frac{\epsilon_{ox}}{t_{ox}} = 0.014375 \text{ F}$$

$$C = C_{ox} \times W_{min} \times L_{min} = 0.014375 \times 240 \times 10^{-9} \times 45 \times 10^{-9} = 1.5525 \times 10^{-16}$$

$$I_L = 815.399 \text{ nA}$$

$$I_H = 39.5658 \mu\text{A}$$

$$R = \frac{VDD}{I_H + I_L} = \frac{1}{39.5658 \times 10^{-6} + 815.399 \times 10^{-9}} = 24763.99 \Omega$$



As the simulation was completed with a minimum width of 120 nm and our transistors were designed with a width of 240 nm. The effective resistance is

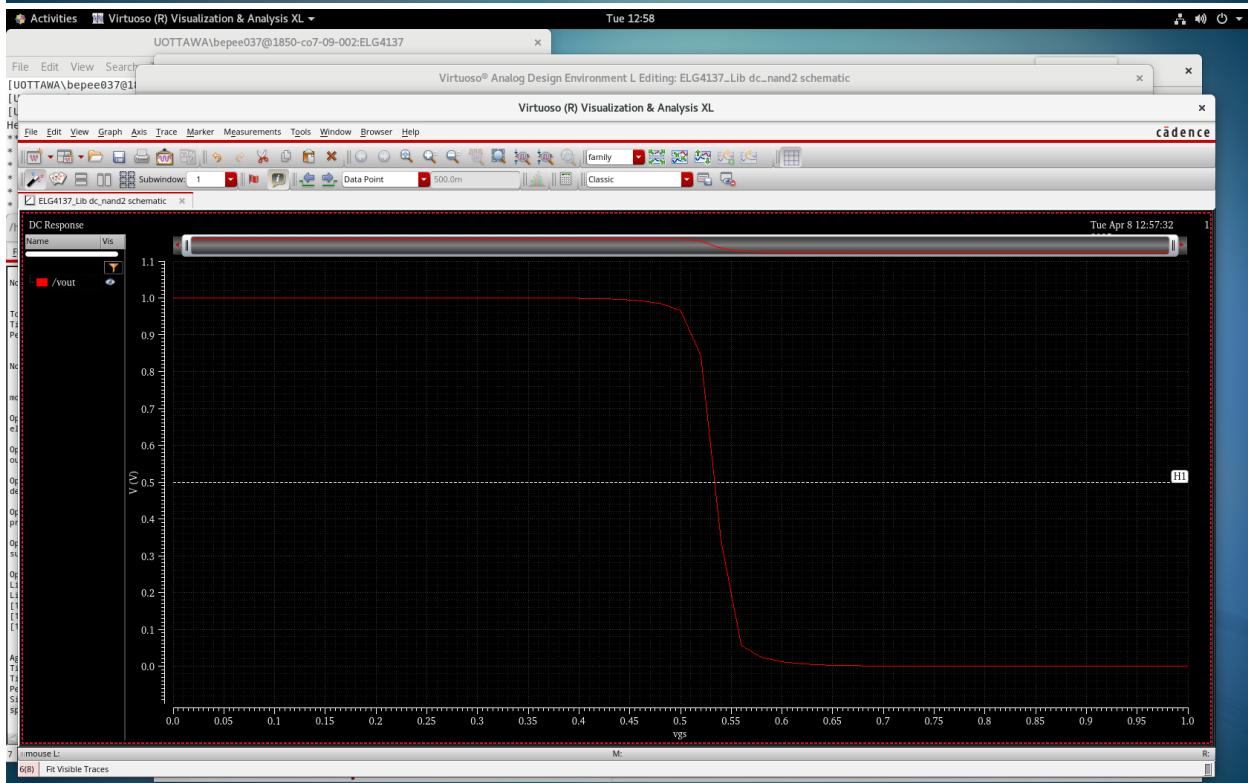
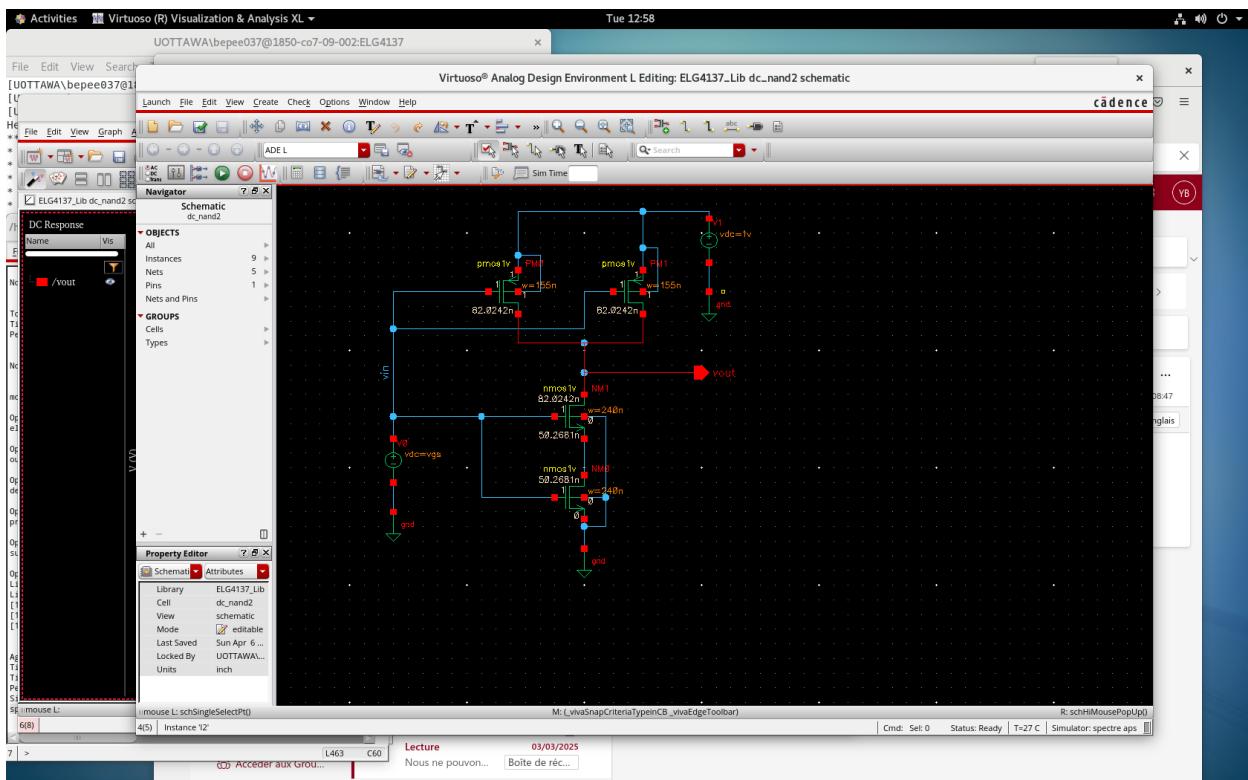
$$R = \frac{24763.99\Omega}{2} = 12382\Omega$$

$$tpd = RC = 12382 \times 1.5525 \times 10^{-16} = 1.922 \times 10^{-12}s$$

- **NAND 2**

$$C = C_{ox} \times W_{min} \times L_{min} = 0.014375 \times 154.844 \times 10^{-9} \times 45 \times 10^{-9} = 1.0016 \times 10^{-16}$$

$$tpd = RC = 12382 \times 1.0016 \times 10^{-16} = 1.24 \times 10^{-12}s$$



Part 2: Subblock Design

In this part, we focused on designing the individual subblocks required for the 4x1 multiplexer, including inverters, NAND, NOR, and transmission gates. We used both CMOS logic and transmission gates in our implementation to ensure proper functionality and efficiency.

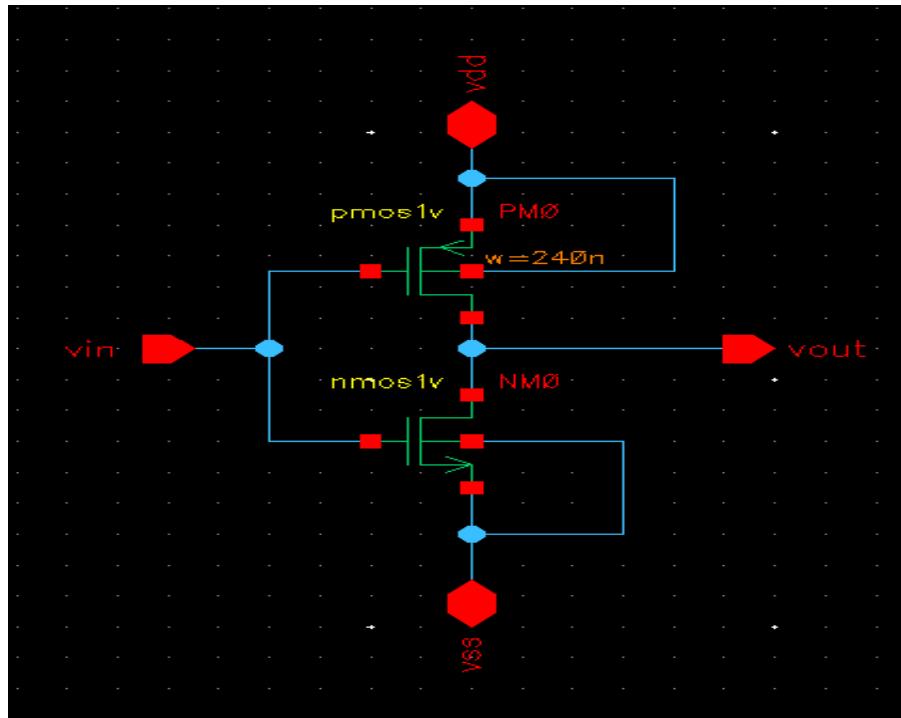
First, we created separate schematics for each subblock using the transistor sizing determined during the paper design phase. Each subblock was designed independently to maintain modularity and facilitate hierarchical design.

Next, we designed functional symbols for each subblock to represent them clearly in the overall multiplexer circuit. We made sure that these symbols were not just boxes with pins but visually distinct and functional representations.

Finally, we created simulation testbenches for each subblock, focusing on both DC and transient simulations. These testbenches were designed to verify the correct operation of each subblock and ensure that they were ERC clean.

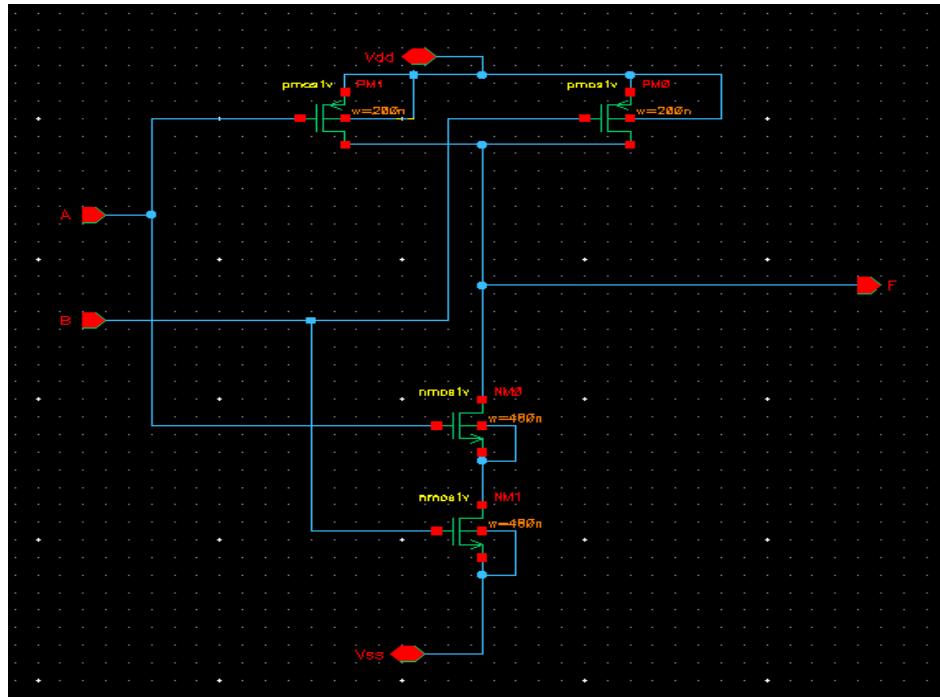
1. Inverter

- Schematics drawings



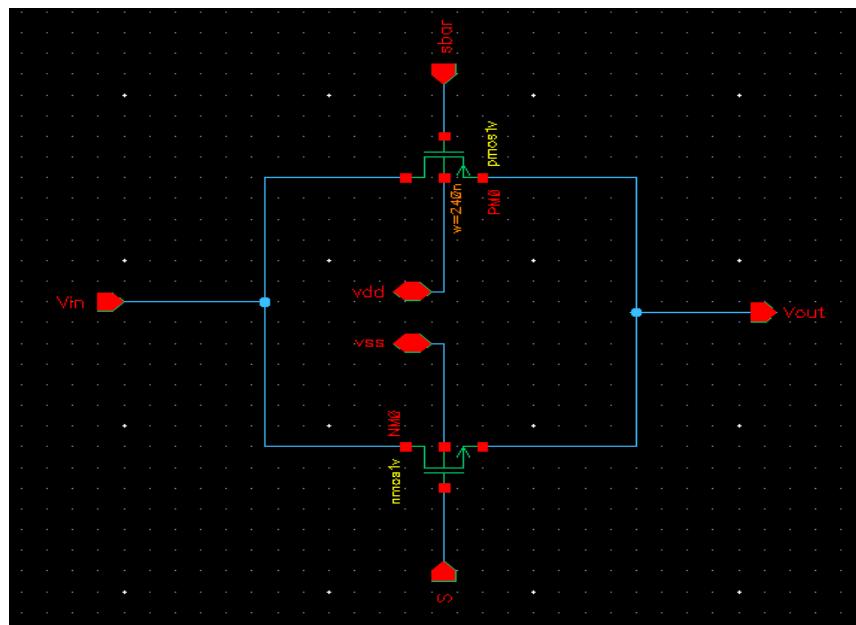
2. NAND 2

- Schematics drawings



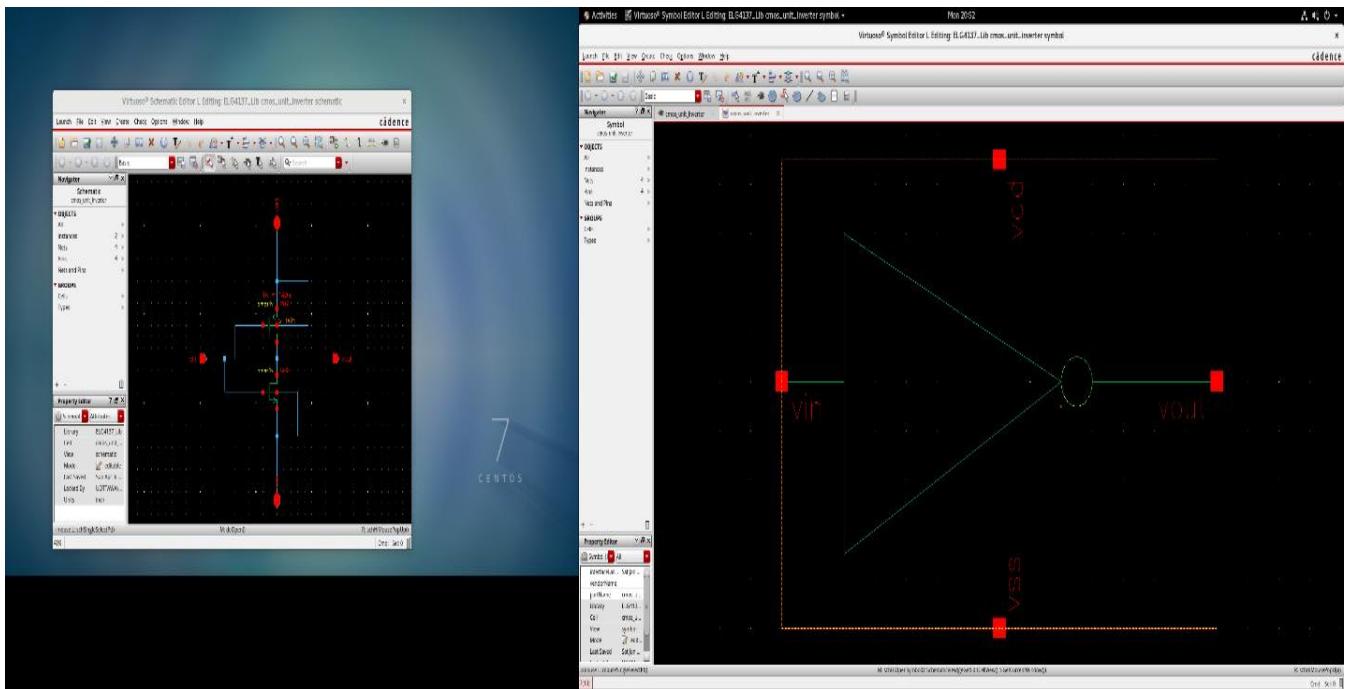
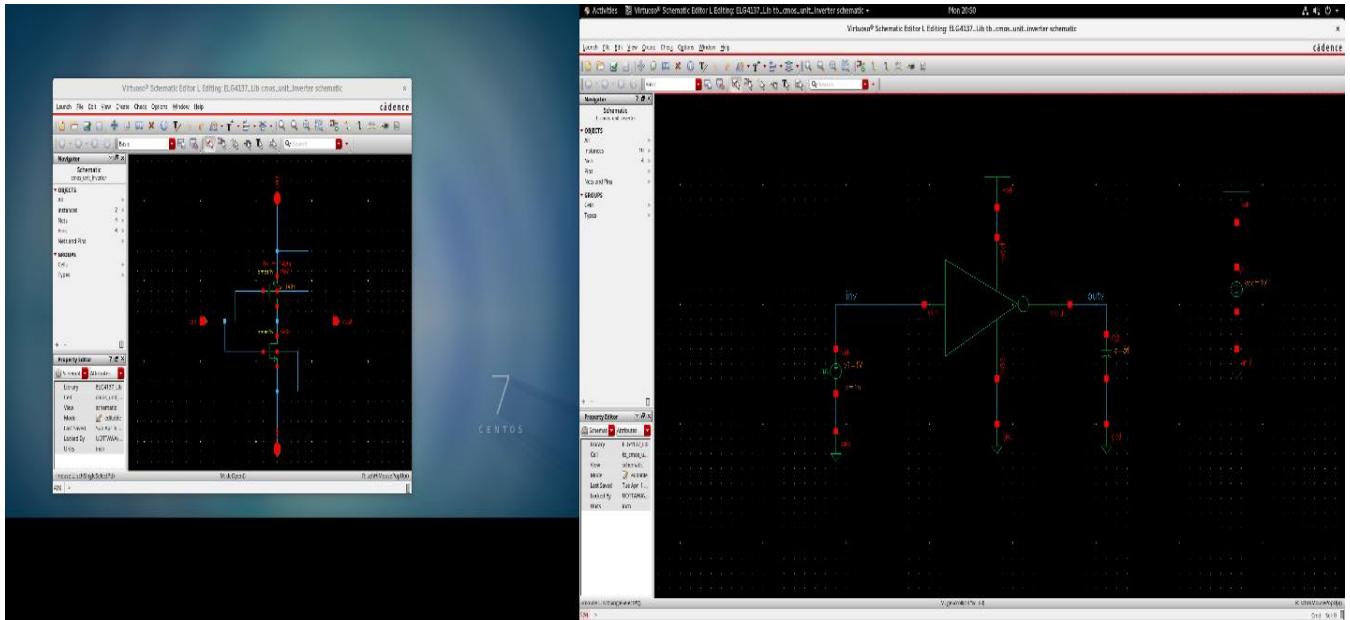
3. Transmission gate

- Schematics drawings

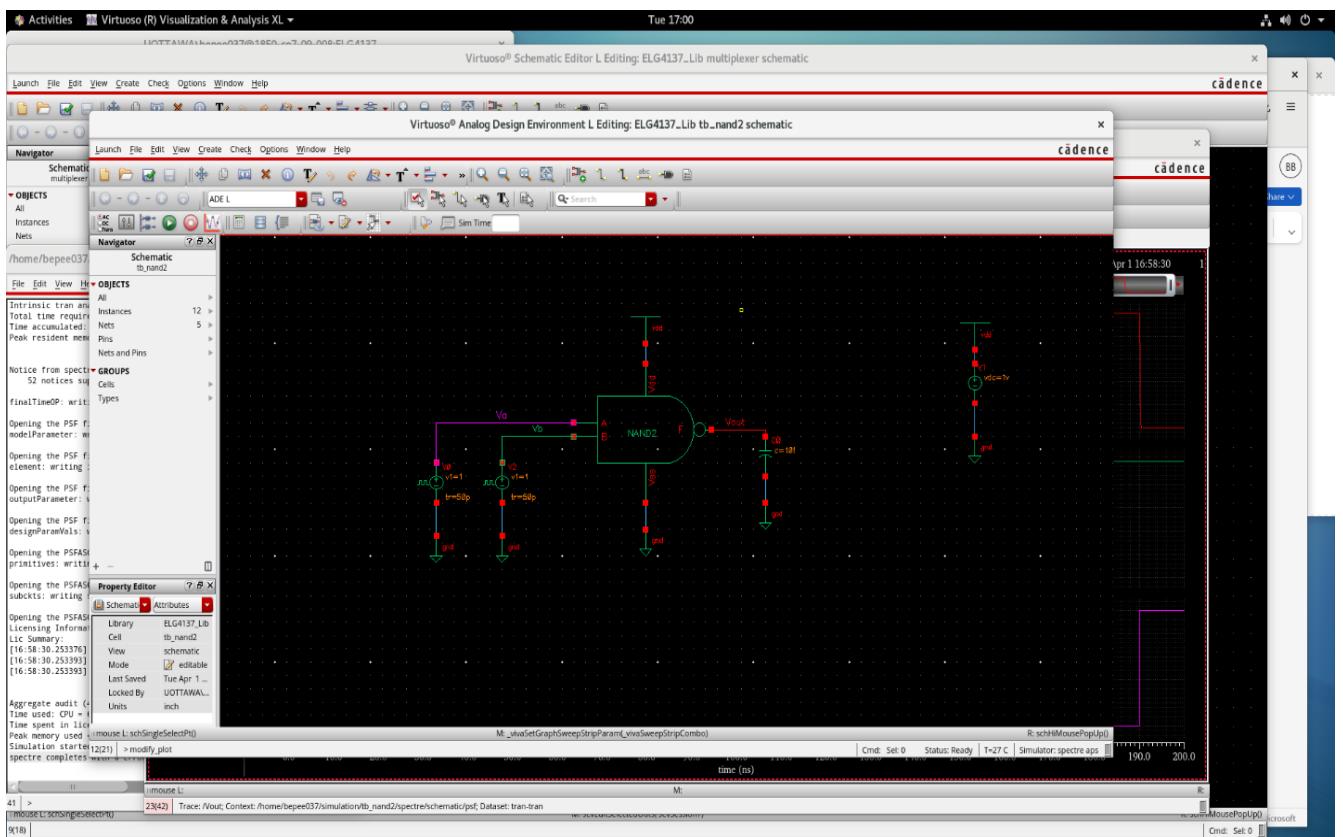
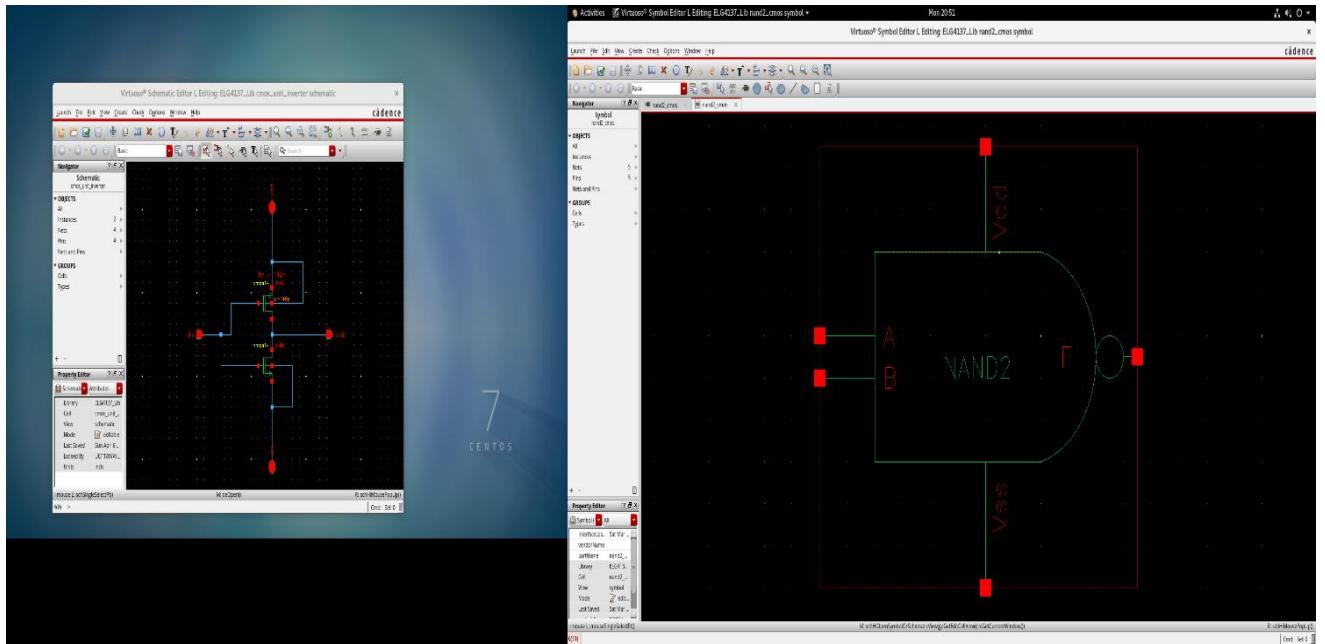


2. Symbols & Testbenches

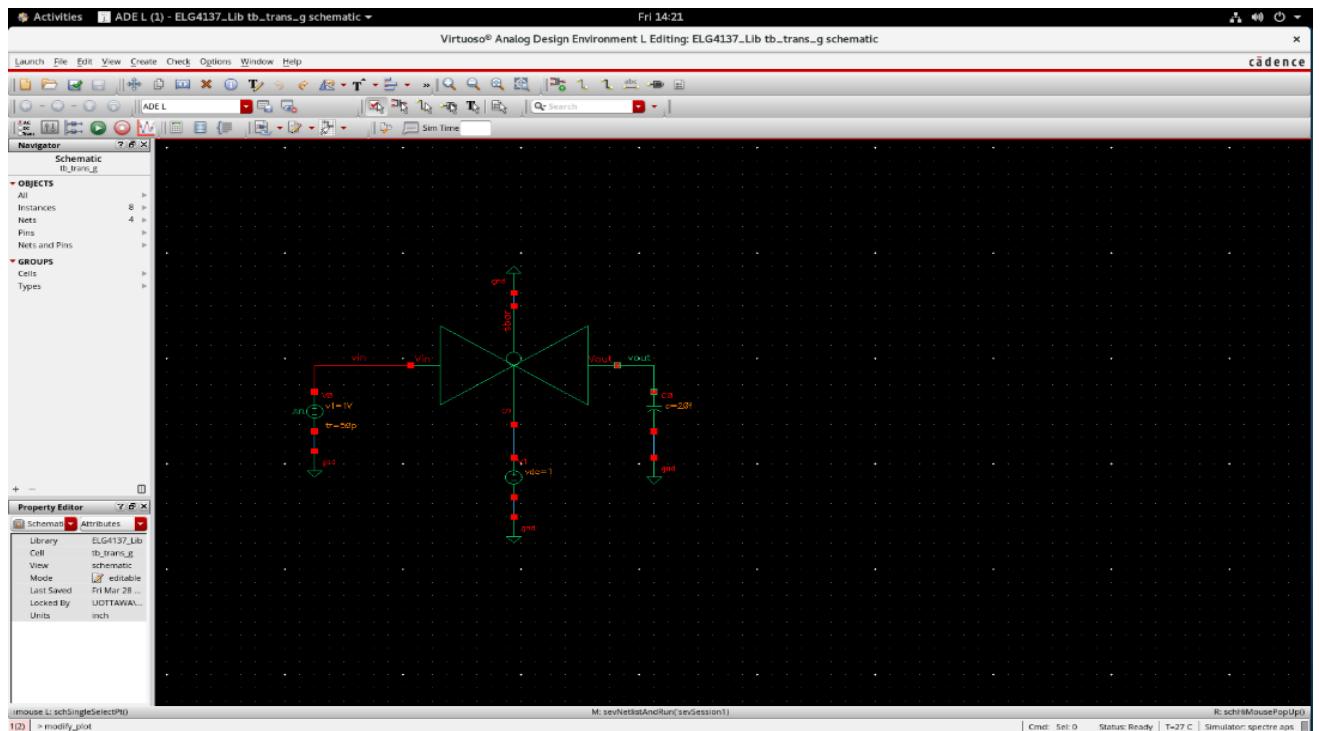
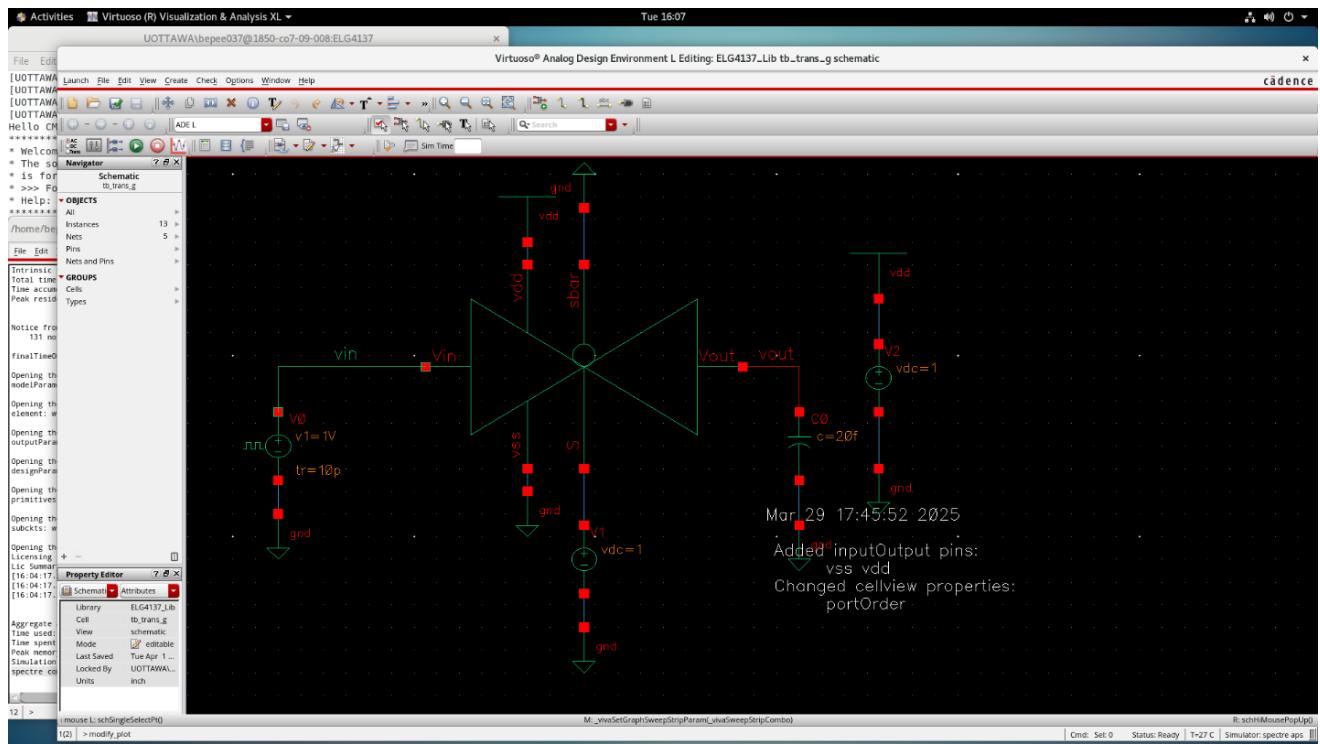
- INVERTER



- NAND2



- TRANSMISSION GATE



Part 3: Subblocks Simulations

After the schematic and testbench were set up in Virtuoso, DC and transient simulations were done for the inverter, NAND2, and transmission gate to analyze their behavior and maximize performance with transistor sizing.

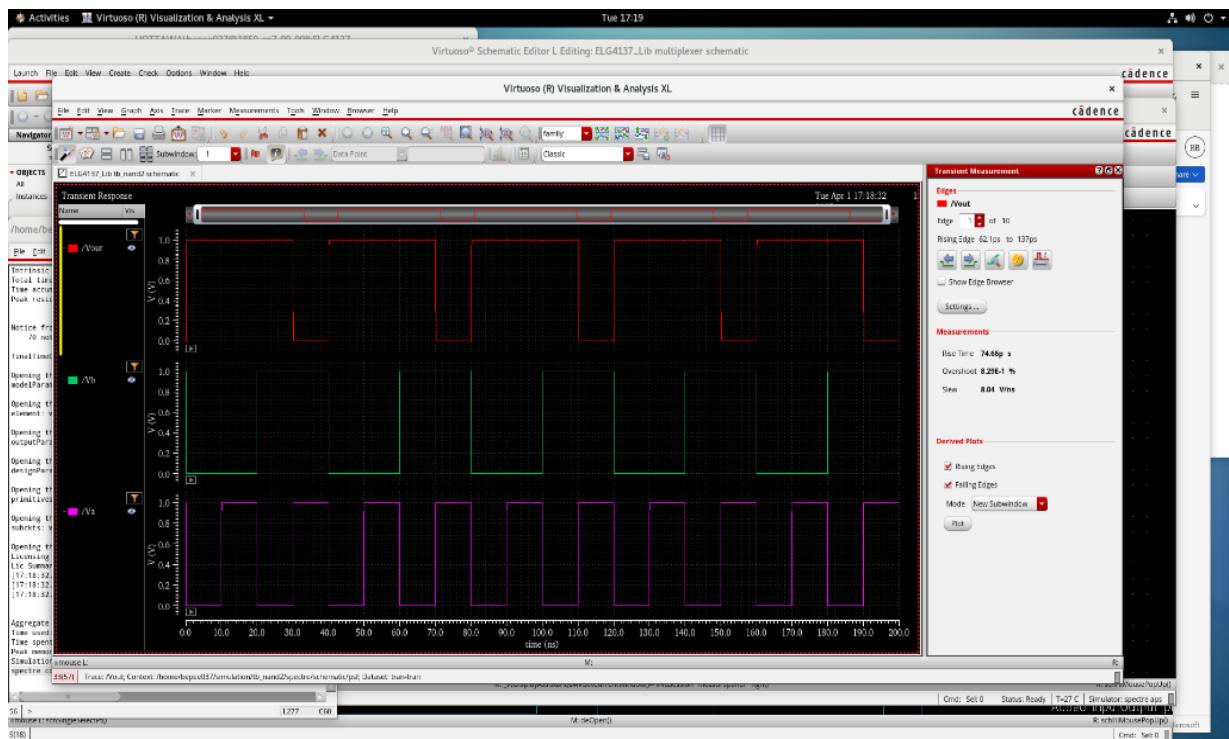
For the DC analysis, an input voltage sweep from 0 V to 1 V was used to generate the Voltage Transfer Characteristic (VTC) for each gate. From this, the switching point (V_m)—the input voltage at which $V_{out} = V_{in}$ —was calculated. In ideal hand calculations, V_m would ideally be $V_{DD}/2$ (0.5 V) if the mobility and threshold voltages were symmetric. The simulations, however, from the 45 nm GPDK PDK indicated that V_m will drift with the other variables that we did not consider in hand calculations but included in the Virtuoso models. To make up for this and achieve symmetric switching, transistor sizing was designed to be varied—typically by making the PMOS wider than the NMOS if V_m was too low, or vice versa if it was too high.

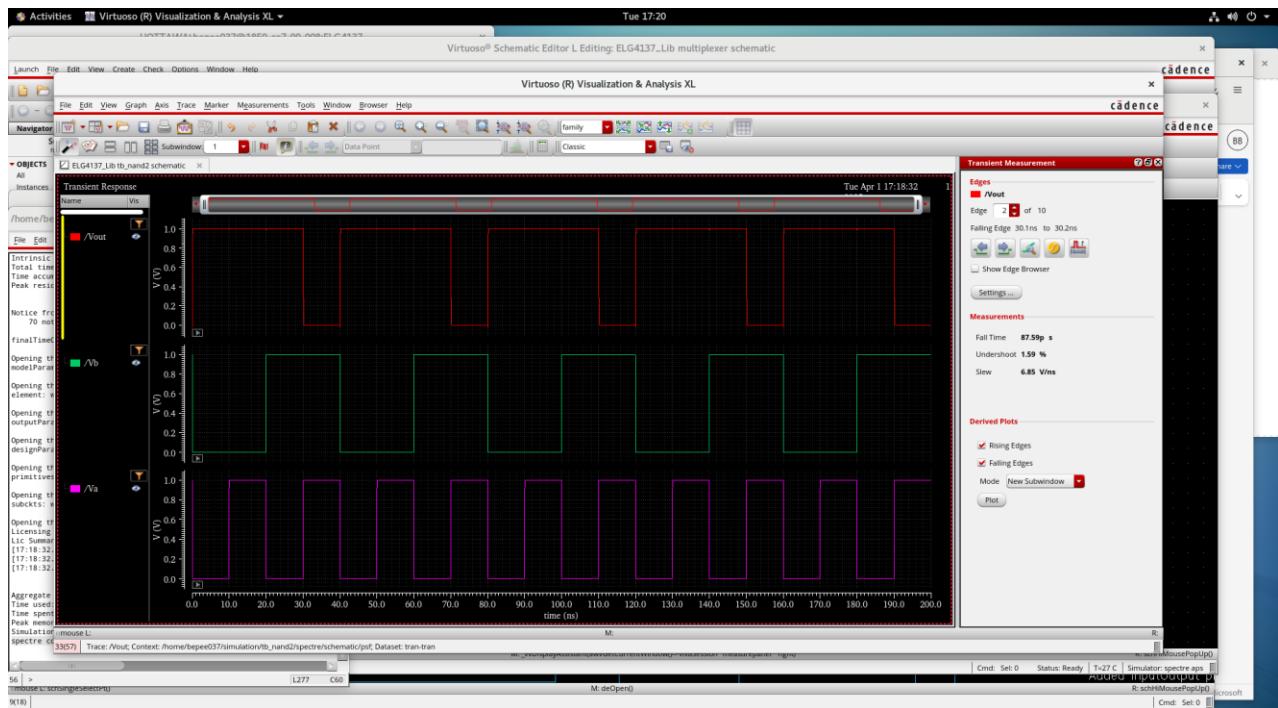
For the transient analysis, pulse waveforms were applied to the inputs of the gates, and output waveforms were monitored to record the propagation delays: tPHL (high-to-low) and tPLH (low-to-high). These were plotted against the hand calculations with simple RC delay models. As predicted, the simulated values were larger than the theoretical values because of the unaccounted variables omitted in the hand calculations, such as parasitic capacitances, input transition slopes, and complex transistor behavior.

Extra focus was put on the transmission gate, which tends to generate more delay than an inverter because PMOS and NMOS both need to pass in series. To make the delay of the transmission gate the same as the inverter delay, the PMOS and NMOS transistors were scaled up accordingly—normally increased to lower resistance and set the desired delay values equal to each other.

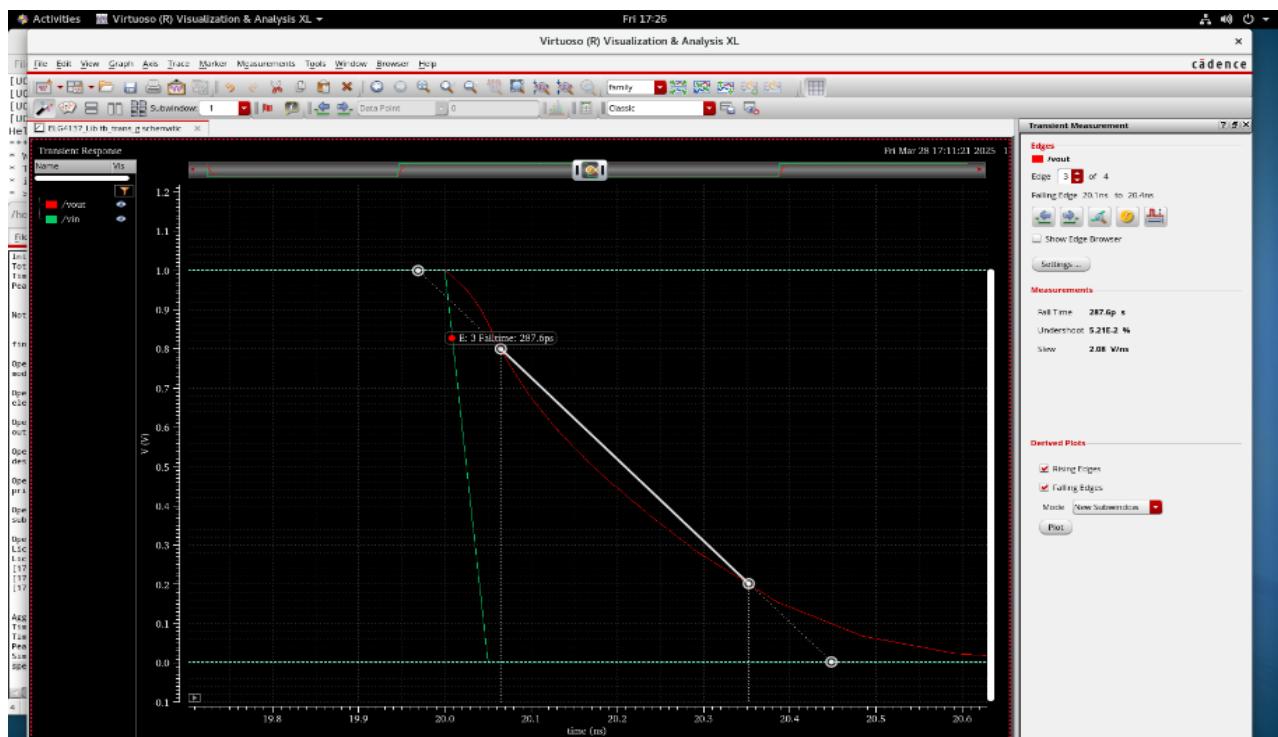
All the results, including the VTC plots and the transient responses, were collected. Delays and switching points were tabulated and compared to the theoretical expectations. Sizing values modified were justified based on notable differences that were observed between the hand calculations and the simulation results. This was to ensure that while hand analysis in early development stages is useful, accurate tuning of design can be achieved only by simulating realistic models with physical effects included in the PDK.

- NAND 2

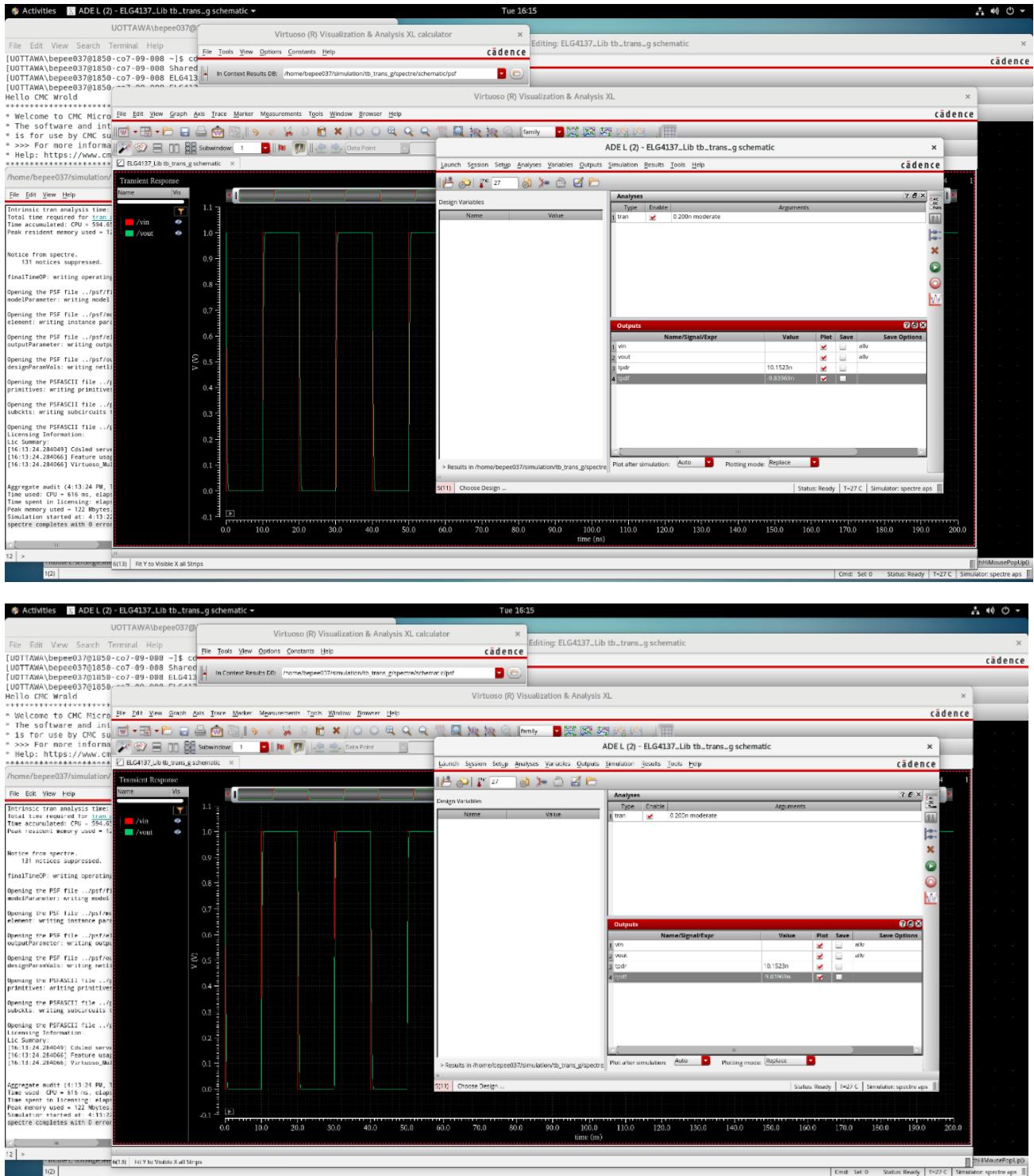




- TRANSMISSION GATE





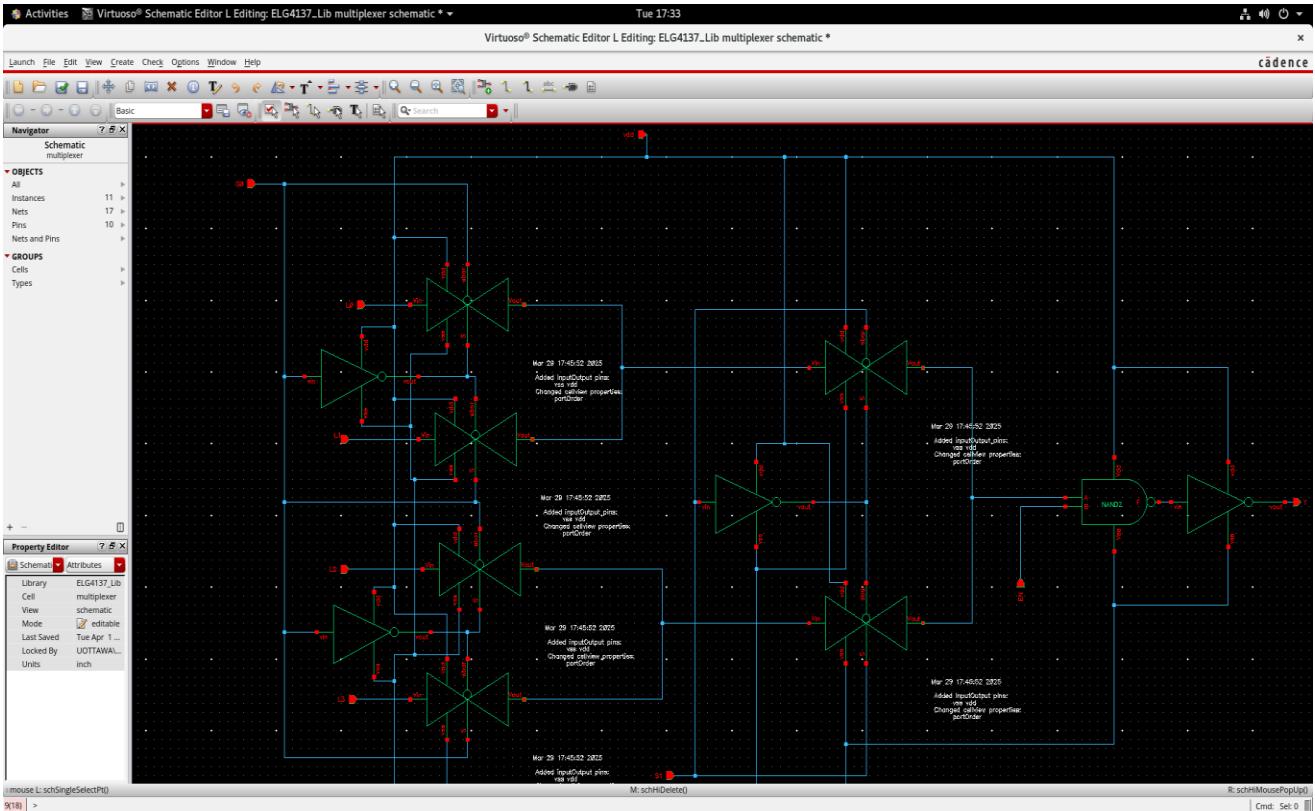
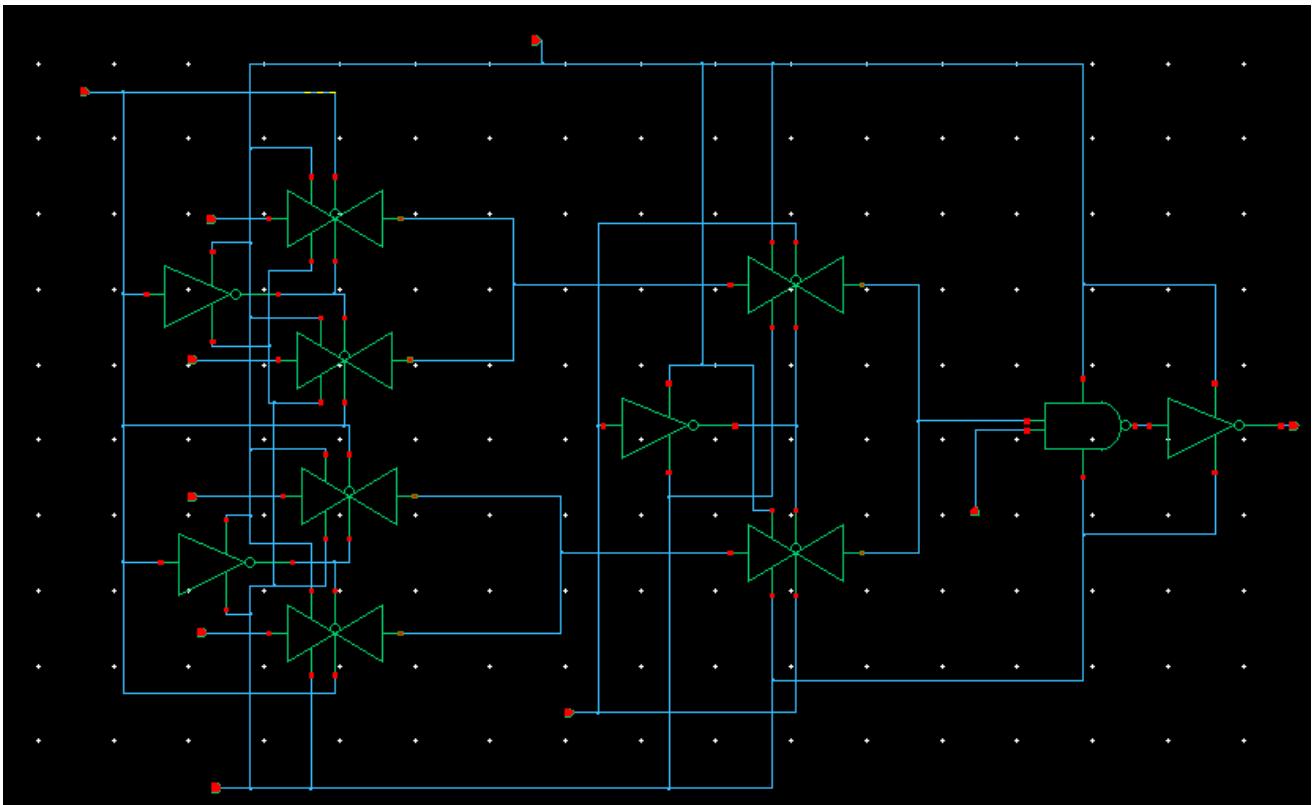


Part 4: Main Block Design

In this part, we focused on designing the main block of our project, which is the 4x1 multiplexer with an enable function. Using the previously designed subblock symbols, we assembled the multiplexer circuit in a hierarchical and modular way.

We carefully integrated the subblocks, including the necessary CMOS logic gates and transmission gates, to ensure the correct functionality of the multiplexer. We also created a customized symbol for the complete multiplexer to make the design more organized and visually intuitive.

To validate the main block, we designed simulation testbenches specifically to evaluate the transient behavior of the multiplexer. These testbenches helped us verify the logical correctness of the overall design.





Part 5 Main Block Simulations

In this part, we verified the functionality of the 4x1 multiplexer through transient simulations using the testbenches created in Part 4. All input signals (IN0 to IN3), selector signals (S0, S1), and the enable signal (EN) were organized in a truth table-like manner to systematically cover all possible input combinations.

When the enable signal (EN) was low, the output (Vo) remained low, regardless of the selector values — confirming that the enabled logic was functioning correctly. When EN was high, the output followed the selected input as expected:

When **S1S0 = 00**, Vo followed **IN0**,

When **S1S0 = 01**, Vo followed **IN1**,

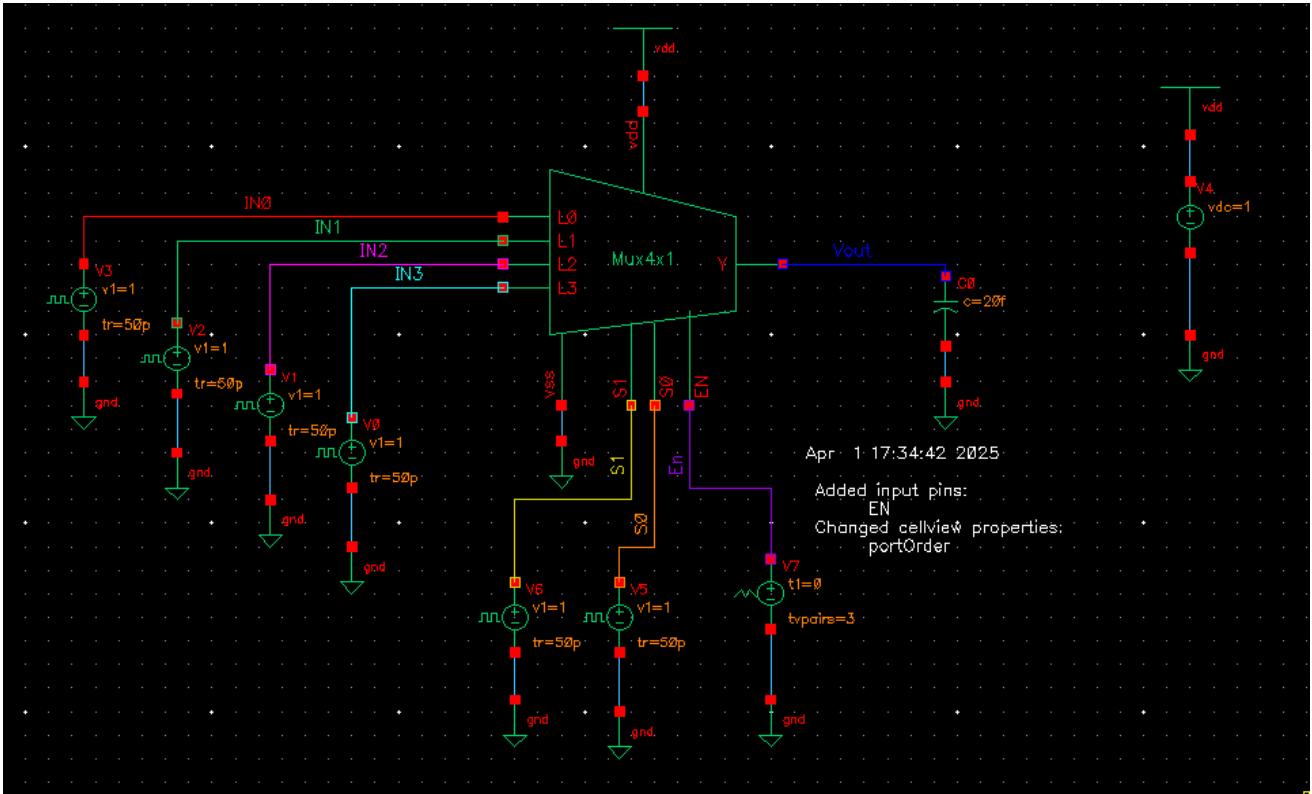
When **S1S0 = 10**, Vo followed **IN2**,

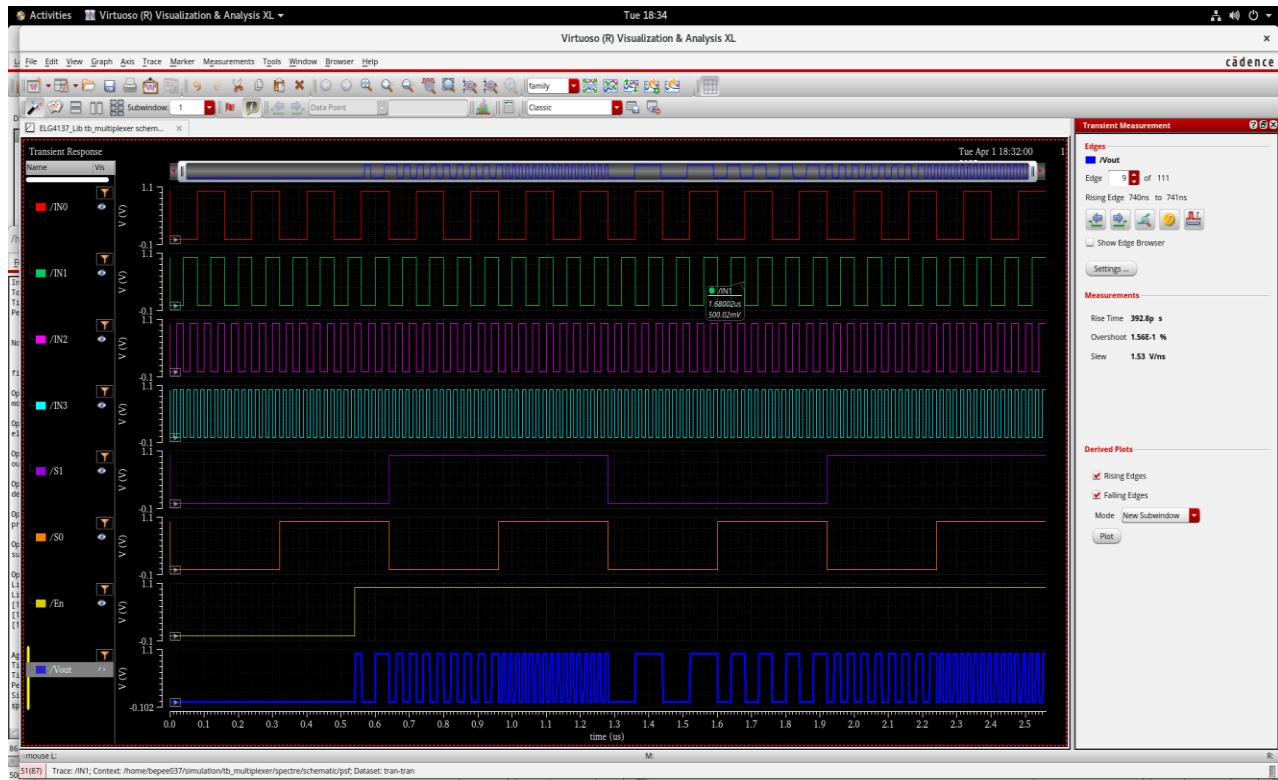
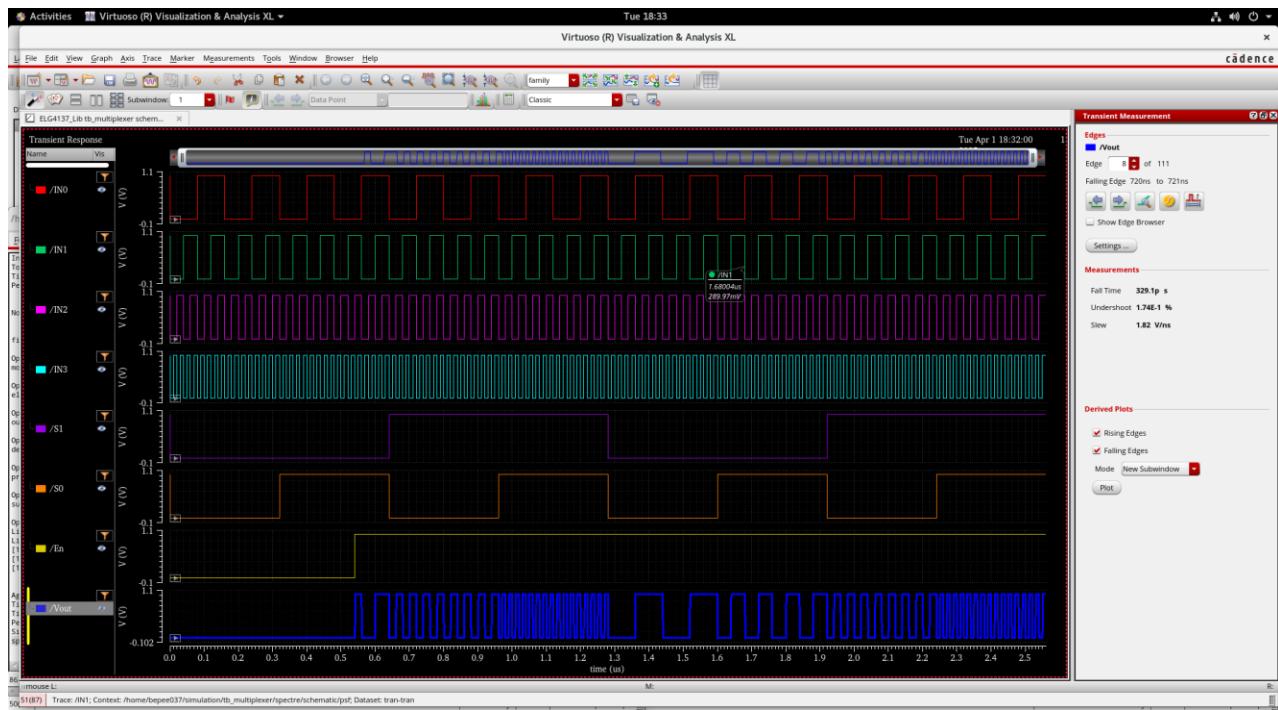
When **S1S0 = 11**, Vo followed **IN3**.

These results confirm that the designed circuit behaves exactly like a 4x1 multiplexer with enable functionality.

We also measured the propagation delays: **tPHL** (high-to-low transition) and **tPLH** (low-to-high transition) of the output **Vo**. These delays give us insight into the performance of the design and can later be compared to the post-layout simulation.

Overall, the simulation results match the expected behavior of a 4x1 multiplexer, validating both the logical and timing correctness of our main block.





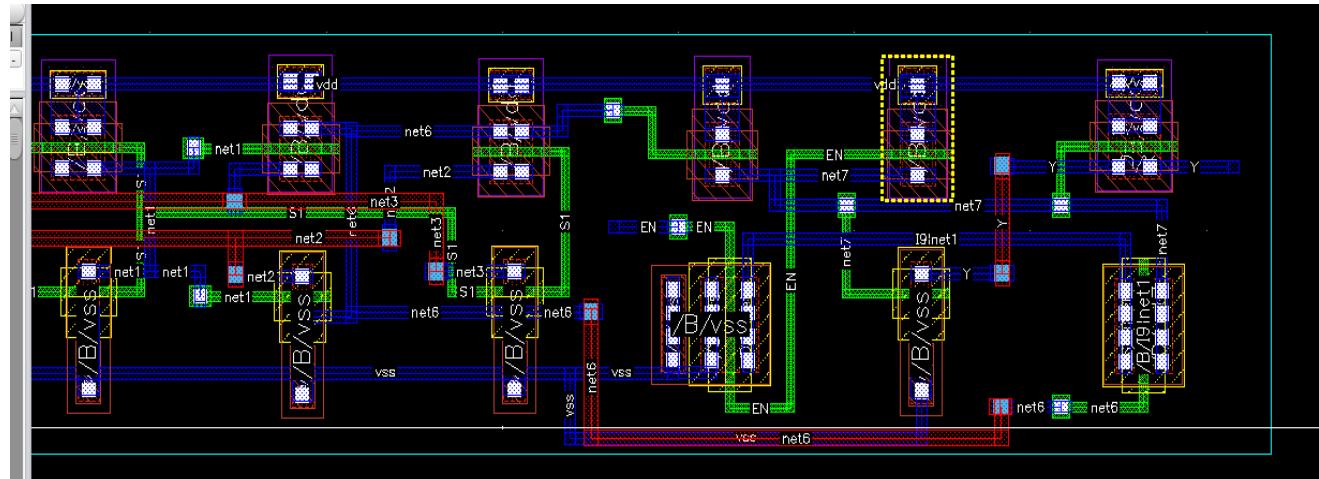
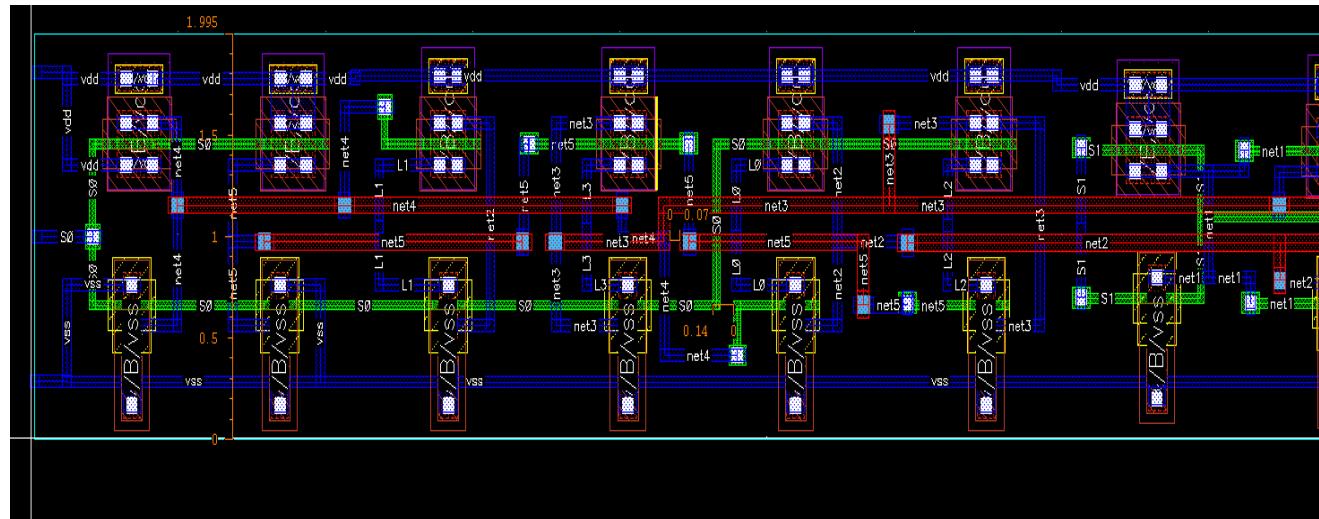
Fall time : 329.1 pS

Rise time : 392.8 pS

EN	S0	S1	Y (Vout)
0	0	0	
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	

Part 6: Layout Design:

Detailed view of the Mux

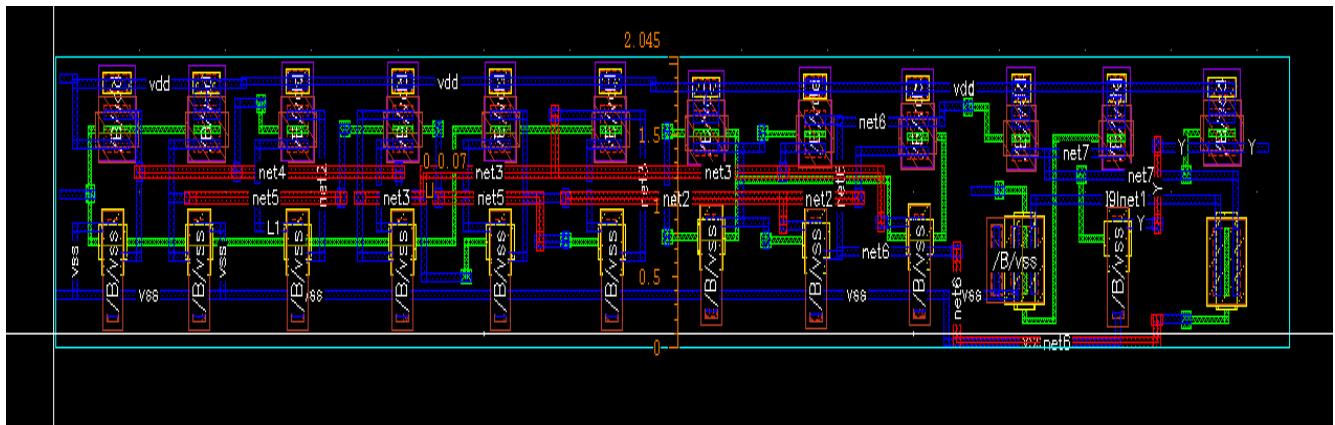


Mininum trace width=0.06um

Minimum space between traces=0.07 um

Target=1.56um

Result: Height max height= 2.045um

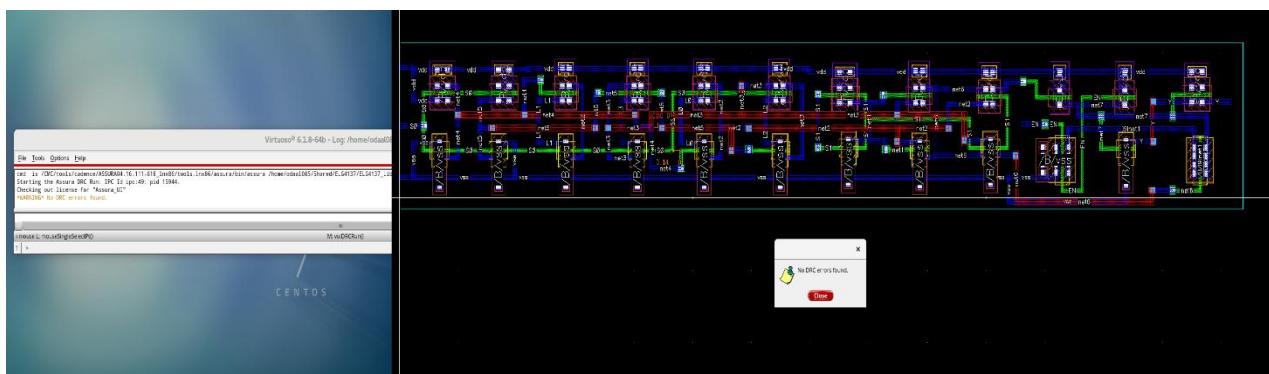


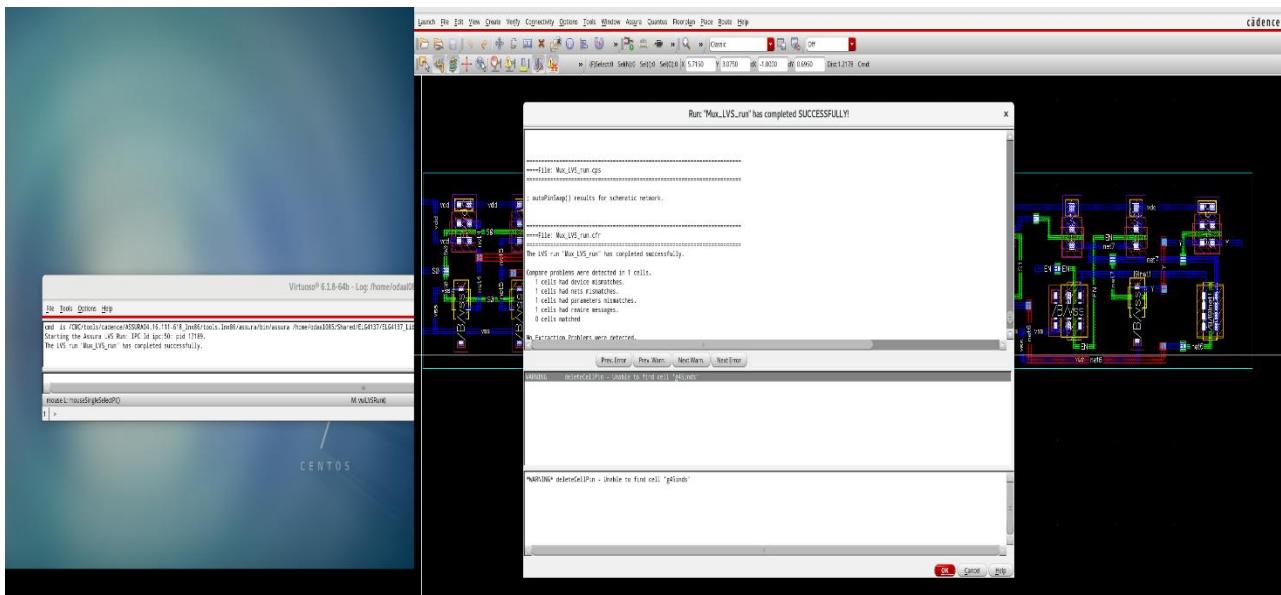
Part 7: DRC and LVS Verifications

In this part, we focused on verifying the accuracy and correctness of our layout design. We performed both Design Rule Check (DRC) and Layout vs. Schematic (LVS) verifications to ensure compliance with design rules and to validate that the layout matched the schematic.

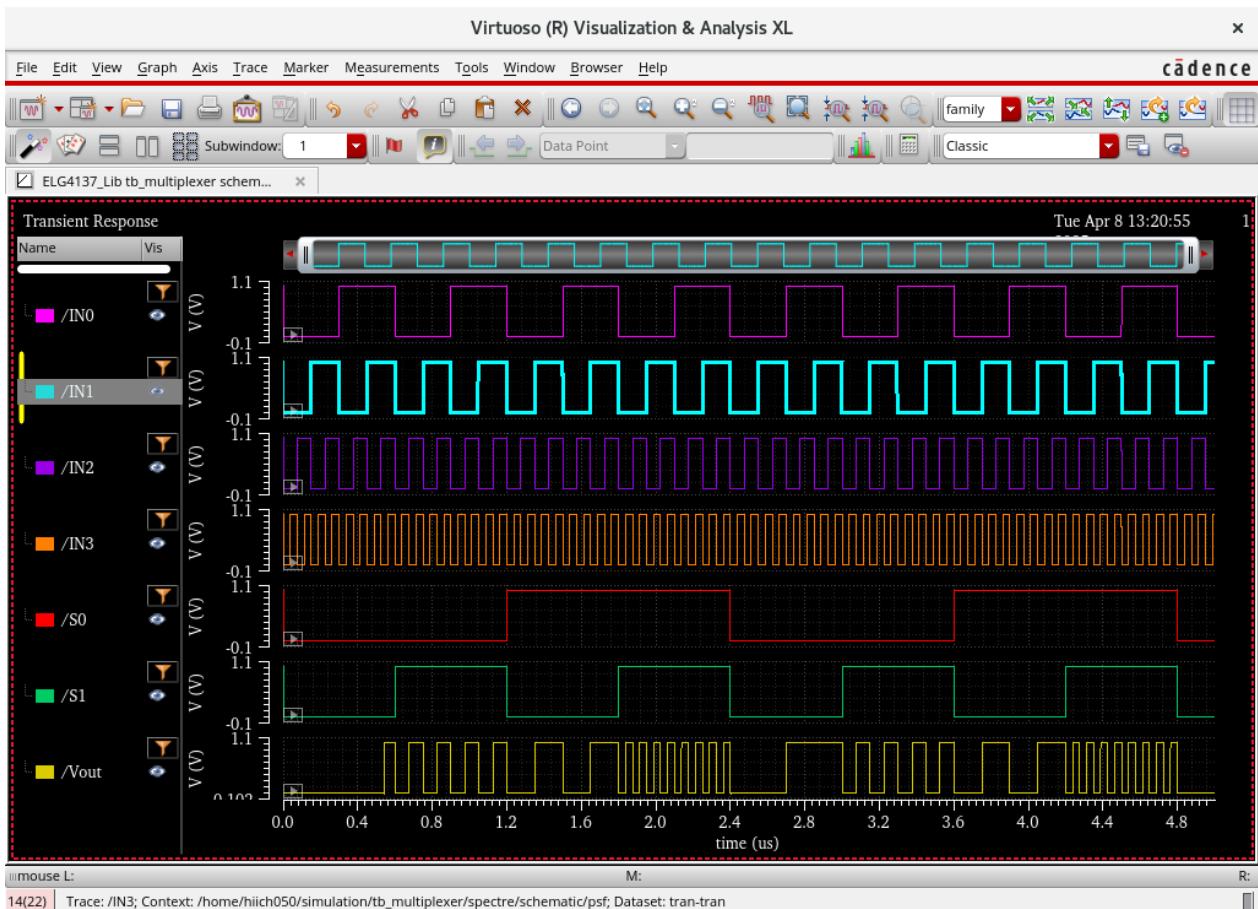
First, we performed the DRC to check for any layout rule violations. The tool reported "No DRC errors found," confirming that our layout adhered to the required design rules.

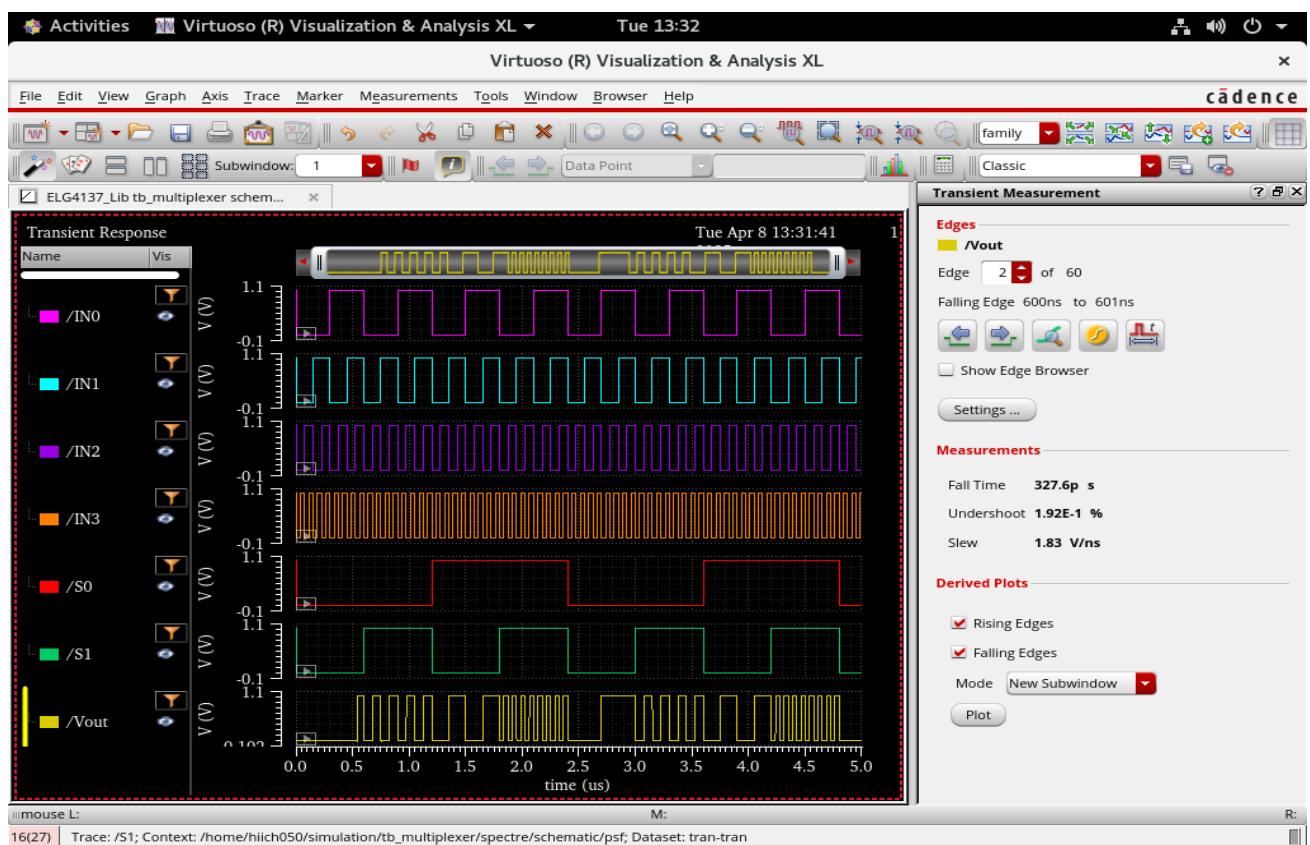
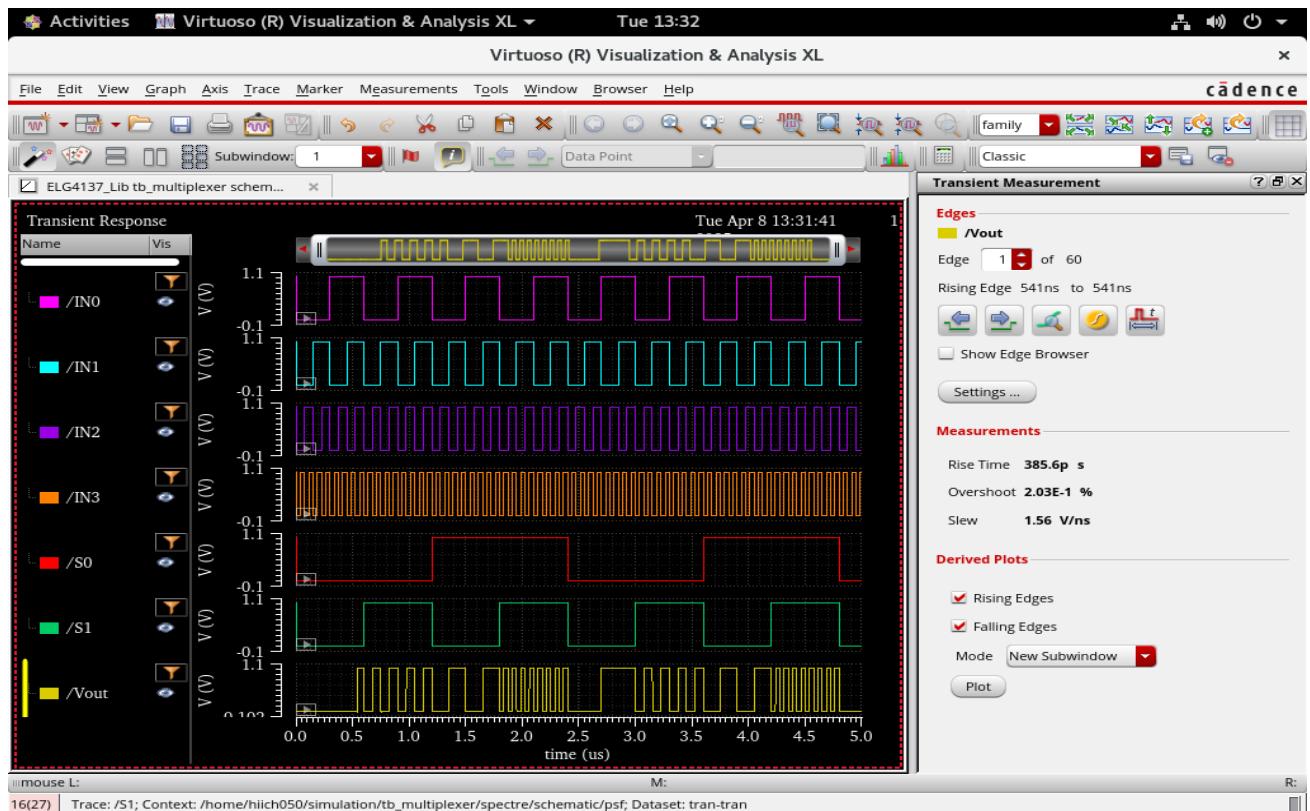
Next, we performed the LVS to verify that the extracted netlist from our layout matched the original schematic. The LVS report indicated that the run was completed successfully, with no mismatches detected, which means that the layout is consistent with the schematic.





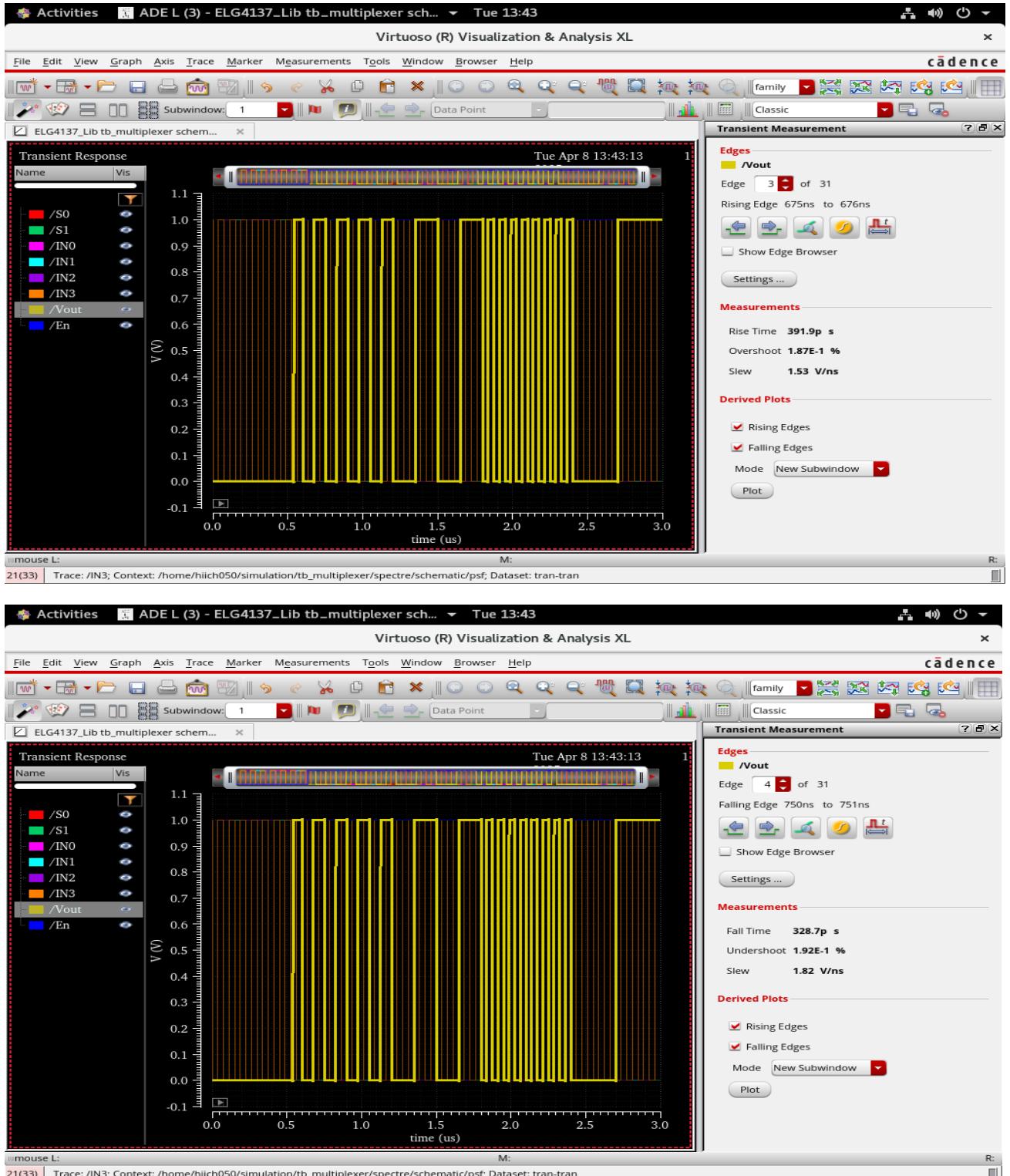
PART 9 Post-layout Simulations:



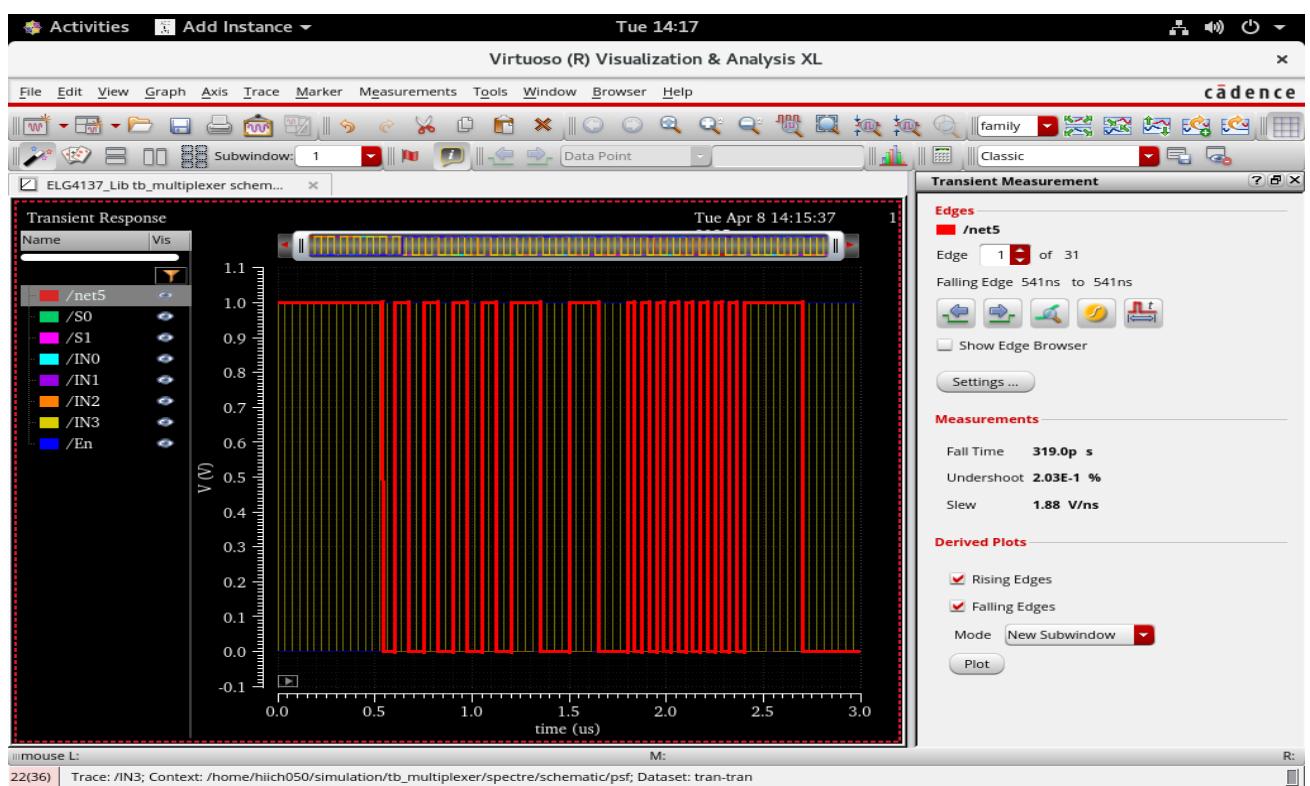
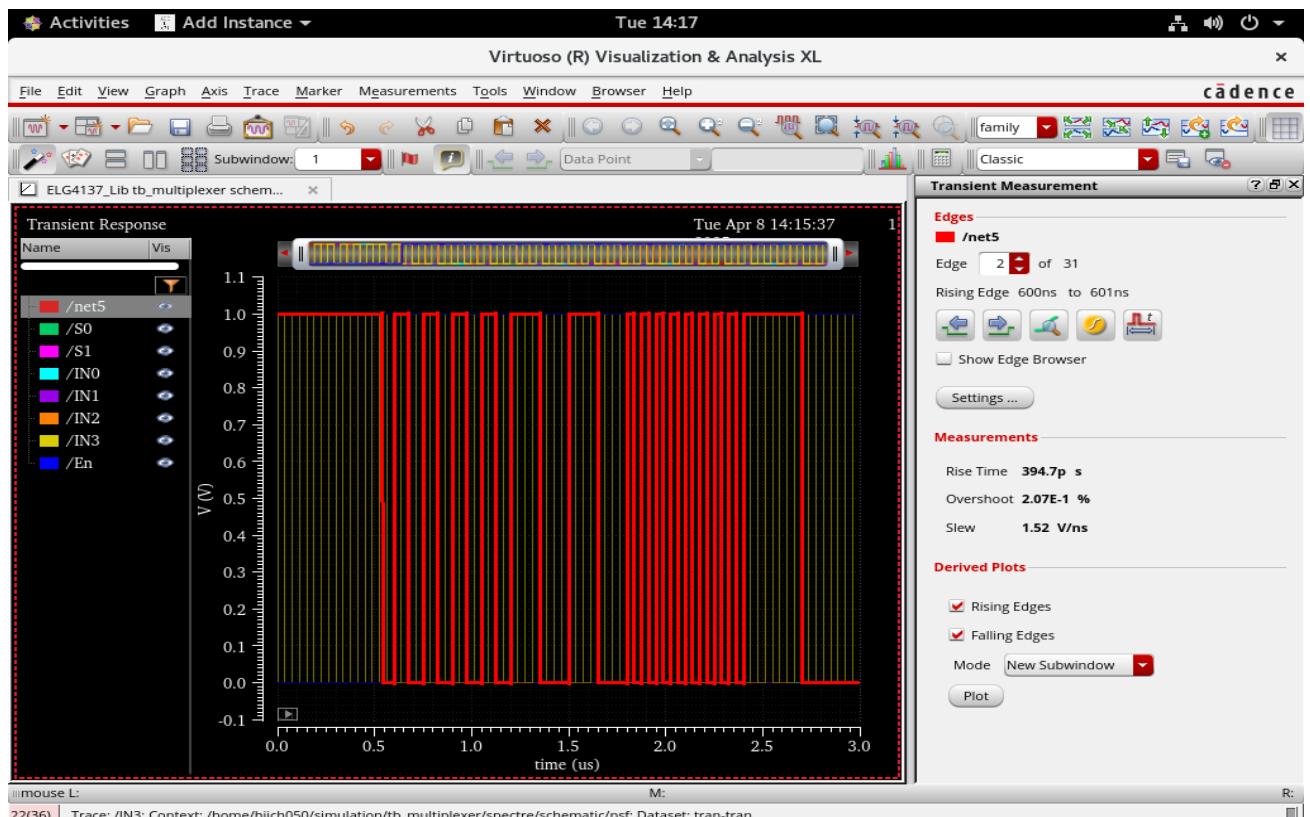


PART 10: Progressive Buffer Chain Design

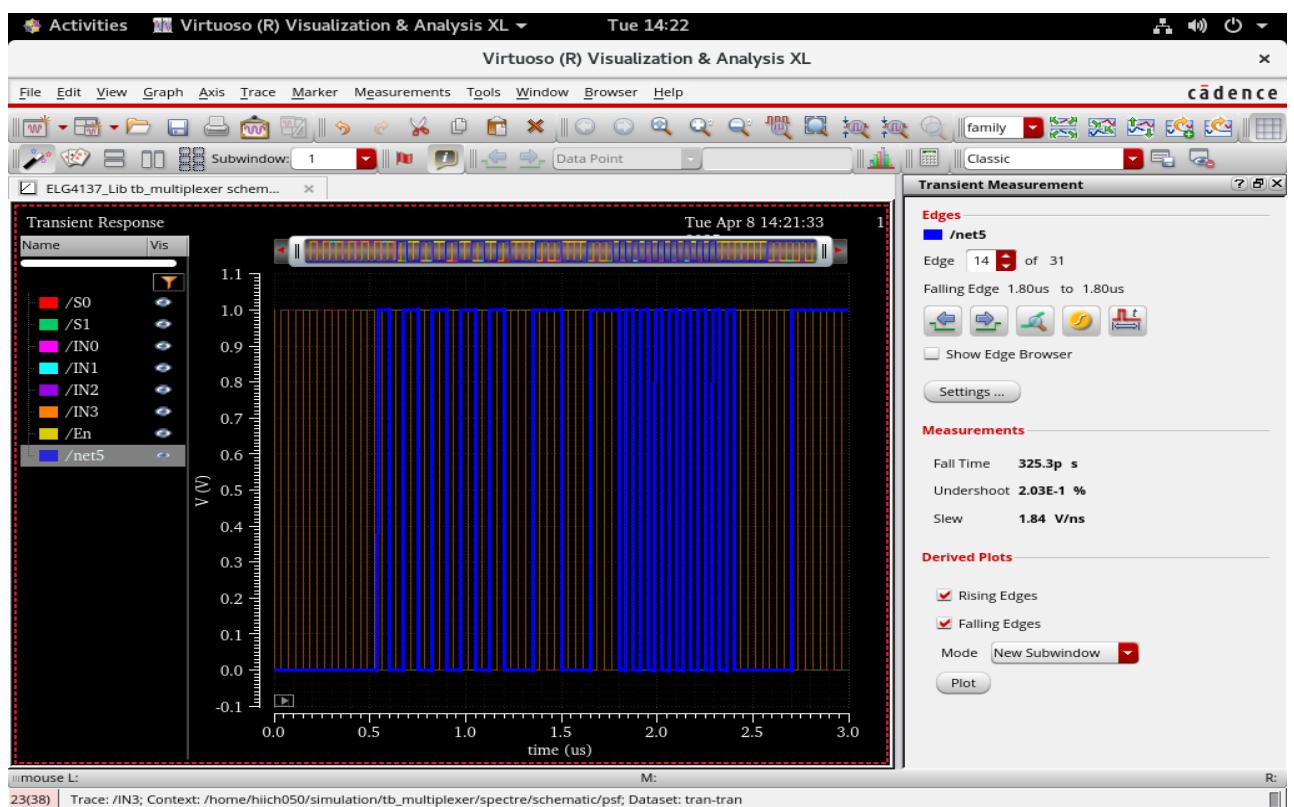
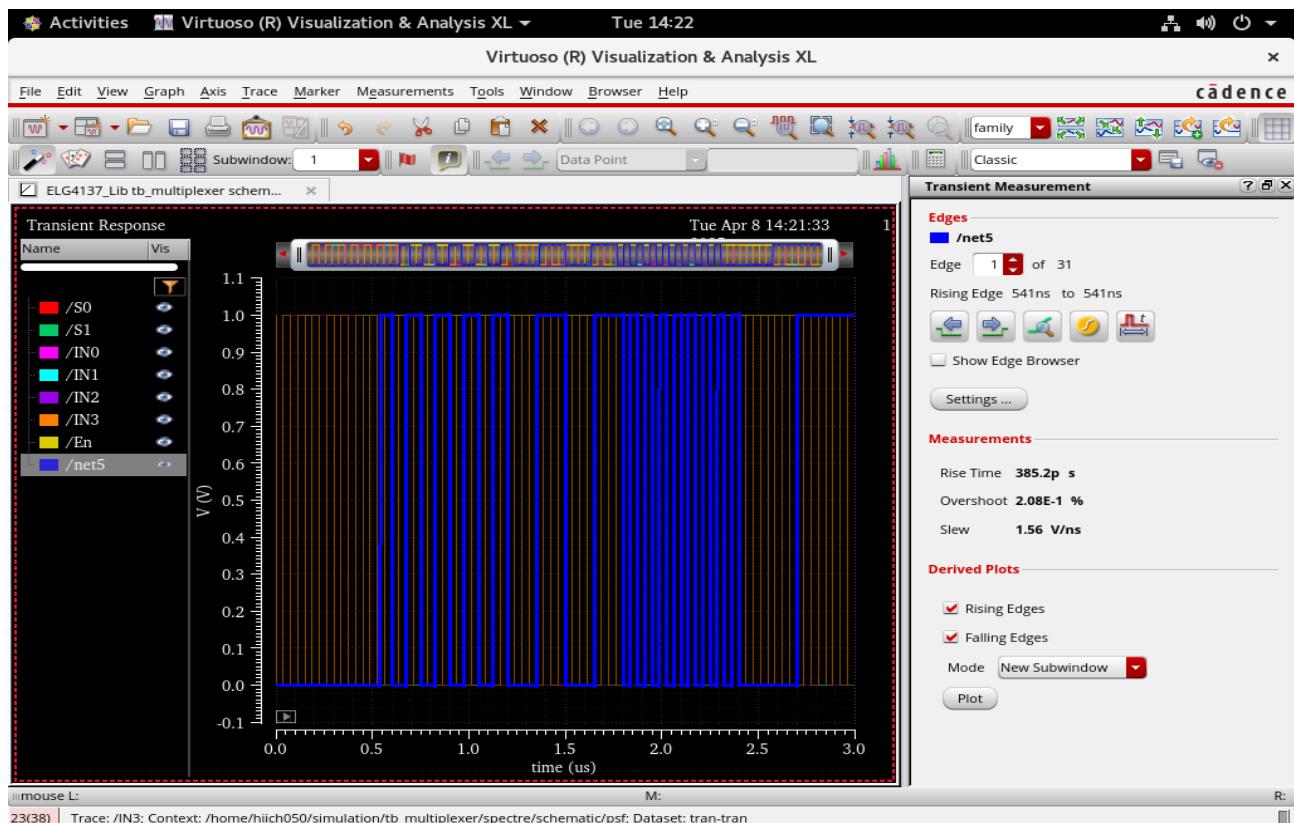
SIMULATION WITH CLOAD

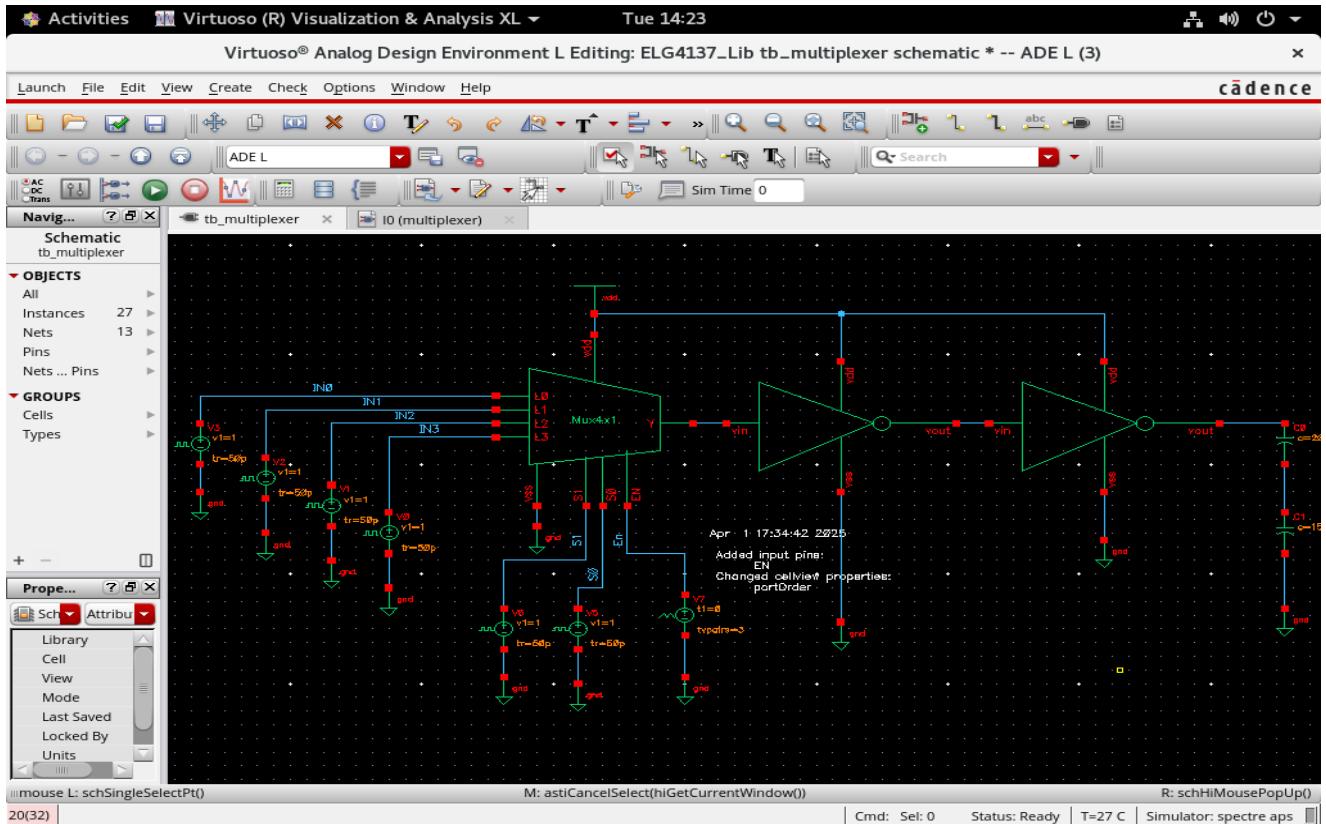


SIMULATION WITH 3 INVERTERS:



SIMULATION WITH 2 INVERTORS:





Calculation of the optimal number of inverters:

Stage 1: ~~inv~~ $\times 2$
 Stage 2: transG $\times 4$
 Stage 3: inv
 Stage 4: ~~inv~~ transG $\times 2$
 Stage 5: NAND2
 Stage 6: inv

$C = 1 \mu F$

$$H = \frac{C_{load}}{C_{in}} = \cancel{\frac{15 \mu F}{3C}} = 5$$

$$B = 2 + 4 + 1 + 2 + 1 = 10$$

$$G = 1 \times \frac{1}{2} \times 1 \times \frac{1}{2} \times \frac{4}{3} = 0.333$$

$$\log_4 (GBH) = 2,0294 \Rightarrow \sqrt[2]{N} \leq 3$$

CONCLUSION

This project allowed us to apply key VLSI concepts through the complete custom design of a 4x1 multiplexer with enable functionality. From paper calculations to schematic and layout implementation, followed by simulation and verification steps (DRC, LVS), each stage reinforced our understanding of digital circuit design and CAD tools. The successful validation of our design confirms both its logical correctness and practical feasibility, providing valuable hands-on experience in the full custom VLSI design flow.