CS344

Construir um roteador de Internet



# Construindo um roteador de Internet

Um dos principais objetivos deste curso é projetar e construir um roteador de internet totalmente funcional. Este documento pretende servir como uma visão geral da abordagem que adotaremos para isso.

# Ferramentas

Utilizaremos o fluxo de trabalho P4->NetFPGA para implementar a parte do plano de dados do roteador. Este fluxo de trabalho tenta abstrair muitos dos detalhes de baixo nível necessários para o desenvolvimento de hardware. Um dos objetivos é que ele seja utilizável por desenvolvedores P4 sem experiência prévia em design HDL.

O plano de controle será escrito em Python sobre a biblioteca de processamento de pacotes Scapy . O Scapy é um gerador, sniffer, analisador e editor de pacotes muito flexível; e é bastante fácil de usar, tornando os desenvolvedores mais produtivos.

# Abordagem

- Entregue o material introdutório completo para configurar tudo o que você precisa.
- Leia e entenda o código inicial fornecido. Aqui está uma breve visão geral.
- Revise os protocolos. Considere rever algumas das aulas do CS144 se precisar de uma atualização sobre os protocolos listados abaixo.
  - IP - entenda como um roteador toma uma decisão sobre o encaminhamento de um pacote IP com base em sua tabela de roteamento
  - ARP
  - ICMP * PWOSPF
- Aprenda a usar P4 e P4->NetFPGA:
  - Exercícios P4 Mininet

    - Exercícios P4->NetFPGA
- Revise os requisitos básicos para o plano de dados e o plano de controle (veja abaixo).
- Desenvolva um plano de interoperabilidade com antecedência! Como turma, vocês precisarão definir um plano concreto para garantir que o roteador de todos se torne interoperável. Recomendamos fortemente que as equipes trabalhem juntas para realizar testes incrementais de suas implementações entre si. Por exemplo, após implementar o protocolo PWOSPF HELLO, certifique-se de que os roteadores entre as equipes consigam realizar a descoberta de vizinhos com sucesso antes de prosseguir com o desenvolvimento das atualizações de estado do link. Testar componentes individualmente proporciona um ambiente de depuração muito mais sensato do que um sistema totalmente construído.
- Divide and conquer. One member from each team will be responsible for the P4 data-plane implementation and the other will be responsible the control-plane. We encourage close collaboration and communication, but team members will need to work in parallel in order to complete the deliverables on time. So make sure to clearly define the interface between the data-plane and control-plane to ensure that integration will proceed smoothly. Clearly document your design decisions in your project's README file. The deliverables listed below are meant to provide a set of initial baseline tests to make sure your data-plane and control-plane implementations are on the right track, but you will still need to define more tests and integrate the two together. * Data-Plane baseline tests
    - Control-Plane baseline tests
- Integrate your data-plane and control-plane implementations. Make sure to run some tests on your own design before attempting to build a multi-router topology. See the hints below for some example tests.
- Interoperate with other teams! As a class, you will need to prove to the instructors that all of your routers are in fact interoperable.
- Celebrate!

# Data-Plane Basic Requirements

- Provide a routing table that can store IP address/prefix pairs with their associated port and next-hop IP address.
- Use the routing table to perform a longest prefix match on destination IP addresses and return the appropriate egress port and next-hop address (or 0.0.0.0 for a directly attached destination).
    - NOTE: We will use a ternary match table for the routing table because LPM tables are not fully supported by SDNet yet.

- Provide an ARP table that can store at least 64 entries. This will accept an IP address as a search key and will return the associated MAC address (if found). This table is modified by the software, which runs its own ARP protocol.
- Provide a “local IP address table”. This will accept an IP address as a search key and will return a signal that indicates whether the correspond address was found. This table is used to identify IP addresses that should be forwarded to the CPU.
- Decode incoming IP packets and perform the operations required by a router. These include (but are not limited to):
  - verify that the existing checksum and TTL are valid
  - look up the next-hop port and IP address in the route table
  - look up the MAC address of the next-hop in the ARP table
  - set the src MAC address based on the port the packet is departing from
  - decrement TTL
  - calculate a new IP checksum
  - transmit the new packet via the appropriate egress port
  - local IP packets (destined for the router) should be sent to the software
  - PWOSPF packets should be sent to the software
  - packets for which no matching entry is found in the routing table should be sent to the software
  - any packets that the hardware cannot deal with should be forwarded to the CPU. (e.g. not Version 4 IP)
- Provide counters for the following:
  - IP packets
  - ARP packets
  - Packets forwarded to the control-plane

# Control-Plane Basic Requirements

- Sending ARP requests
- Updating entries in the hardware ARP cache
- Timing out entries in the hardware ARP cache
- Queuing packets pending ARP replies
- Responding to ICMP echo requests
- Generating ICMP host unreachable packets
- Handling corrupted or otherwise incorrect IP packets
- Building the forwarding table via a dynamic routing protocol (PWOSPF)
- Support static routing table entries in addition to the routes computed by PWOSPF
- Handling all packets addressed directly to the router

# You Decide

- Responding to ARP requests is actually fairly straight forward to express in P4. You can decide whether you want to implement ARP responding in the control-plane or the data-plane.

# Hints and Tips

- Are you handling PWOSPF HELLO packets correctly in the data-plane? What IP address are they sent to?
- Be sure to make use of the CLI tool to add/remove/inspect table entries and read/write counters
- Here is useful command for configuring the tables in your P4 switch:
  - `cat ${P4_PROJECT_DIR}/src/commands.txt | ${P4_PROJECT_DIR}/sw/CLI/P4_SWITCH_CLI.py`
- Possible initial tests:
  - Is your router forwarding correctly with statically configured table entries?
  - Can you ping each of the routers interfaces?
  - Is the router responding to ARP requests?
  - Be careful if you are trying to ping one interface from the other. Unless you are careful, linux will force the traffic to use the loopback interface rather than sending packets out onto the wire. It is possible to do this, but it'll be easier (and less confusing) if you can arrange a time with a neighboring group to use their NIC. Then you can do small tests like sending pings through the router, traceroute to and through the router, send iperf flows through the router, and so on.
- Occassionally the `nf0` - `nf3` network interfaces do not come up after programming the FPGA. Try running the following command to bring it back up:
  - `# ifdown nf0 && ifup nf0`
- Configure interface with IP address:
  - `# ifconfig eth1 1.2.3.4 netmask 255.255.255.0`
- Configure interface with MAC address:
  - `# ifconfig eth1 hw ether 00:11:22:33:44:55`
- Adding routing table entries on Ubuntu:
  - `# route add -net 1.1.1.0 netmask 255.255.255.0 gw 12.12.12.13 dev eth2`
- Show routing table entries:
  - `# route -n`
- Show arp table entries:
  - `# arp -i eth1`

- If you try to program the FPGA and you see something like the following message: `Check programming FPGA or Reboot machine !`, that probably means that the machine has been shut off since the last time the FPGA was programmed. If the links of the SUME board do not come up when the BIOS enumerates the PCIe endpoints then the SUME board will not be detected. The easiest solution to this problem is simply to do a warm reboot after programming the FPGA: `$ sudo reboot now`. Then try programming the FPGA again after the machine comes back up.
- If the `eth1` or `eth2` interfaces are down then you probably just need to configure them with an IP address using the `ifconfig` command as shown above.
- You can safely ignore the following error that you get when programming the FPGA: `rmmod: ERROR: Module sume_riffa is not currently loaded` because the programming script simply always attempts to unload and reload the `sume_riffa` drivers (even if they are not currently loaded).
- We recommend using VNC Viewer if you'd like a graphical desktop:
  - Install VNC Viewer if you don't already have it installed.
  - Start a VNC server on your development machine: `$ vncserver`. This command indicates the port on which the VNC server is running.
  - You can then use VNC Viewer to connect to your development machine on the appropriate display port. To connect to a VNC server running on port 1 of packet-3 connect to `packet-3:1` from within VNC Viewer.
  - You can start multiple vnc servers, in which case the port number would just increment.
  - To kill the VNC server runing on port 1: `$ vncserver -kill :1`

---