$\mu_n C_{ox}$ =200 μA/V^2 , $\mu_p C_{ox}$ =100 μA/V^2 , NMOS V_{TH} =0.4 V, PMOS V_{TH} =−0.4 V,

7.7 We wish to design the stage in Fig 7.40 for a drain current of 0.5 mA. If W/L =50/0.18, calculate the value of R_1 and R_2 such that these resistors carry a current equal to one-tenth of I_{D1}.

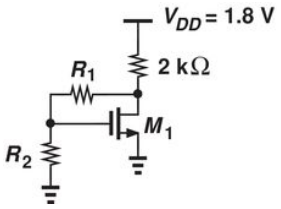

Fig. 7.40

7.17 We wish to design a stage of Fig 7.50 for a voltage gain of 5 with $W/L \leq$ 20/0.18 Determine the required R_D if the power dissipation must not exceed 1 mW.

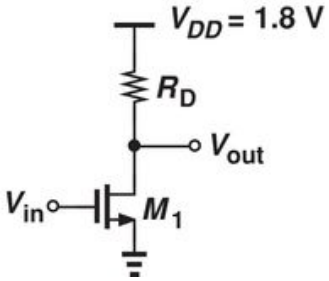

Fig. 7.50

7.21 Explain which one of the topologies shown in Fig. 7.54 is preferred.

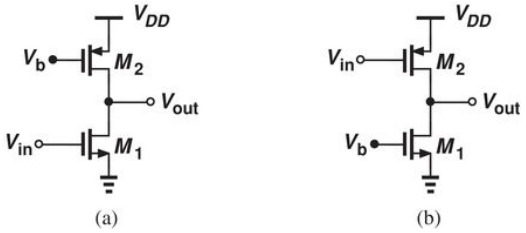

Fig. 7.54

7.23 The CS stage shown in Fig. 7.56 must achieve a gain of 7. If $(W/L)_2$ = 2/0.18, compute the required value of $(W/L)_1$.

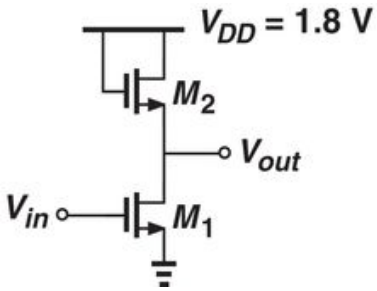

Fig. 7.56