Chapter Exam

Chapter 5-Large and Fast: Exploiting Memory Hierarchy

2012/06/19

1. For a direct-mapped cache design with 32-bit address, the following bits of the address are used to access the cache.

	Tag	Index	Offset
a	31-10	9-4	3-0
b	31-12	11-5	4-0

(1) What is the cache line size (in words)? (10%)
(2) How many entries does the cache have? (10%)
(3) What is the ratio between total bits required for such a cache implementation over the data storage bits? (10%)

2. Caches are important to providing a high performance memory hierarchy to processors. Below is a list of 32-bit memory address references, given as word addresses

a.	1, 134, 212, 1, 135, 213, 162, 161, 2, 44, 41, 221

For each of these references, identify the binary address, the tag, and the index given a direct-mapped cache with 16 one-word blocks. Also list if each reference is a hit or a miss, assuming the cache is initially empty. Please fill the Tag, Index, and Hit/Miss result in the blank. (10%)

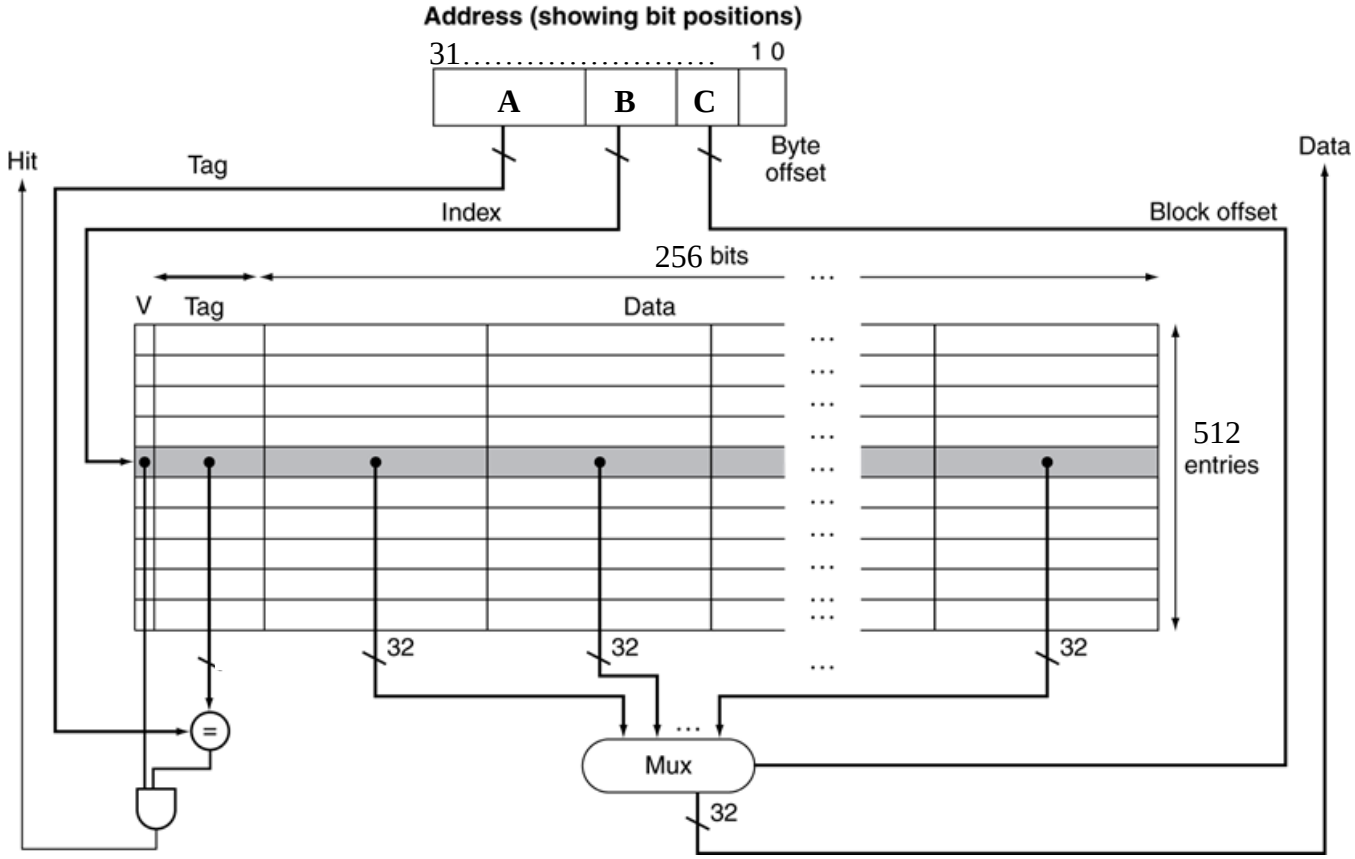
Address		Tag	Index	Hit/Miss
decimal	binary			
1	1	0000	0001	Miss
134	10000110	1000	0110	Miss
212	11010100			
1	1			
135	10000111			
213	11010101			
162	10100010			
161	10100001			
2	10			
44	101100			
41	101001			
221	11011101			

3. Assume that main memory accesses take 70 ns and that memory accesses are 36% of all instructions. The following table shows data for L1 caches attached to each of two processors P1 and P2.

	L1 size	L1 miss rate	L1 hit time
P1	1KB	11.4%	0.62ns
P2	2KB	8.0%	0.66ns

What is the AMAT for each of P1 and P2? (10%)

4. There is a Intrinsity FastMATH data cache in the Figure 1. It can store 256 bits data and has 512 entries. How many bits are Tag (A), Index (B), and Block offset (C) ? (10%)



5. Please explain the difference between write-through and write-back and them advantage and disadvantage. (20%)

6. (1) In virtual memory system, how many memory references are performed per load/store operation? Explain the purpose of these memory references. (10%)

(2) What is the translation lookaside buffer (TLB) ? What is it purpose? (10%)

7. The textbook presents the following development issues in a specific sequence (from simple to complex), in order to show a typical research and development (R&D) process. Please fill in the sequence number for the corresponding issue (1 being the simplest and 5 being the most complex). (10%)

Development Issue	Sequence (1…5)
Translation Lookaside Buffer (TLB)	
Memory hierarchy	
Directed mapped cache	
Set associative cache	
Virtual memory	