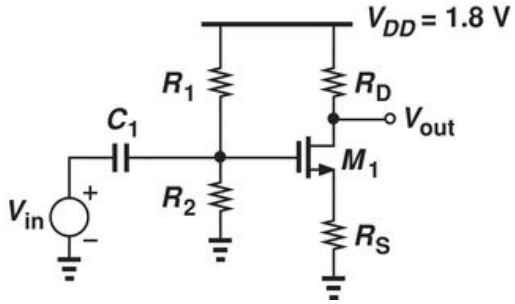
Digital Electronics Final Homework Due : 4PM, June 21st

$\mu_n C_{ox}$ =200 μA/V^2 , $\mu_p C_{ox}$ =100 μA/V^2 , NMOS V_{TH} =0.4 V, PMOS V_{TH} =–0.4 V,

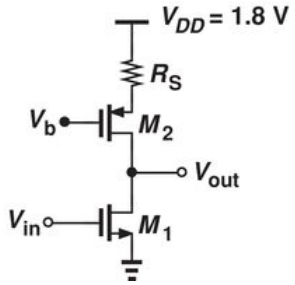
1 (40%) The degenerated stage showing below need to provide a voltage gain of 4 with a power budget of 2 mW. The voltage drop on the R_s is equal to 200 mv. Assume λ=0, If the overdrive voltage of the transistor is set to 100 mv and R_1 and R_2 must consume 5% of the allocated power, design the circuit by finding (1) I_{DS} of M_1, (2) R_S, (3) R_D , (4) R_2 , (5) R_1 , (6) (W/L) of M_1.



2. (40%) A CS stage with a degenerated PMOS current source. The degeneration must raise the output impedance of the current source to about 10r_{o1} such that the voltage gain remains nearly equal to the intrinsic gain of M_1. Assume λ=0.1V^{-1} for both transistors and a power budget of 2mW.

(a) (20%) If V_B=1V, determine the values of $(W/L)_2$ and R_s so that the impedance seen into the drain of M_2 is equal to 10 r_{o1}.

(b) (10%) Determine $(W/L)^1$ to achieve a voltage gain of 10.



3. (40%) Design a CG stage shown below such that it can accommodate an output swing of 500mV_{pp} i.e. V_{out} can fall below its bias value by 250mV without driving M_1 into the triode region. Assume a voltage gain of 4 and an input impedance of 50Ω. Select $R_S \approx 10/g_m$ and $R_1 + R_2$ =20kΩ. Please find the (1)g_m, (2)R_s, (3)(W/L) of M_1, (4) R_D, (5) R_1, (6) R_2, (7) I_{DS} of M_1.

(Hint: Since M_1 is biased 250mV away from the triode region, we have $R_S I_D + V_{GS} - V_{TH} + 250\text{mV} = V_{DD} - I_D R_D$)