Chapter Exam

Chapter 4-The Processor

2012/05/22

1. Different instructions utilize different hardware blocks in the basic single-cycle implementation. The next three problems in this exercise refer to the following instruction.

	Instruction	Interpretation
a	add Rd, Rs, Rt	Reg[Rd] = Reg[Rs] + Reg[Rt]
b	lw Rt, Offs(Rs)	Reg[Rt] = Mem[Reg[Rs] + Offs]

(1) What are the values of control signals generated by the control in Figure 1 for this instruction? (The ALU operation writes Sub, Add, AND and OR directly) (10%)

(2) Which resources (blocks) produce outputs, but their outputs are not used for this instruction? Which resources produce no outputs for this instruction? (10%)

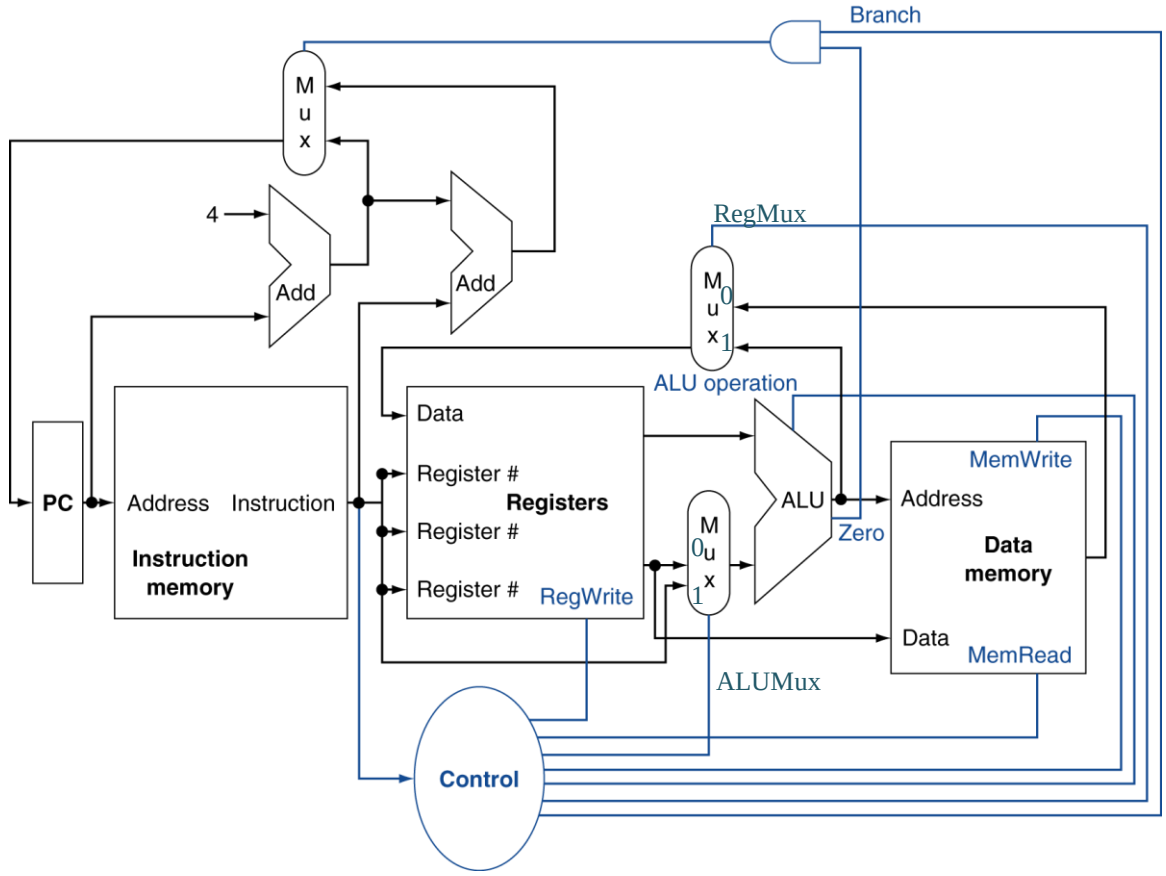

Figure 1 The basic implementation of the MIPS

2. In this exercise we examine how latencies of individual components of the datapath affect the clock cycle time of the entire datapath, and how these components are utilized by instructions. For problems in this exercise, assume the following latencies for logic blocks in the datapath:

	I-Mem	Add	Mux	ALU	Regs	D-Mem	Sign-extend	Shift-left-2
a.	400ps	100ps	30ps	120ps	200ps	350ps	20ps	0ps
b.	500ps	150ps	100ps	180ps	220ps	1000ps	90ps	20ps

(1) What is the clock cycle time in figure 2 datapath if the only type of instructions we need to support are ALU instructions (add, and, etc)?

(2) What is the clock cycle time in figure 2 datapath if we only had to support lw instruction?

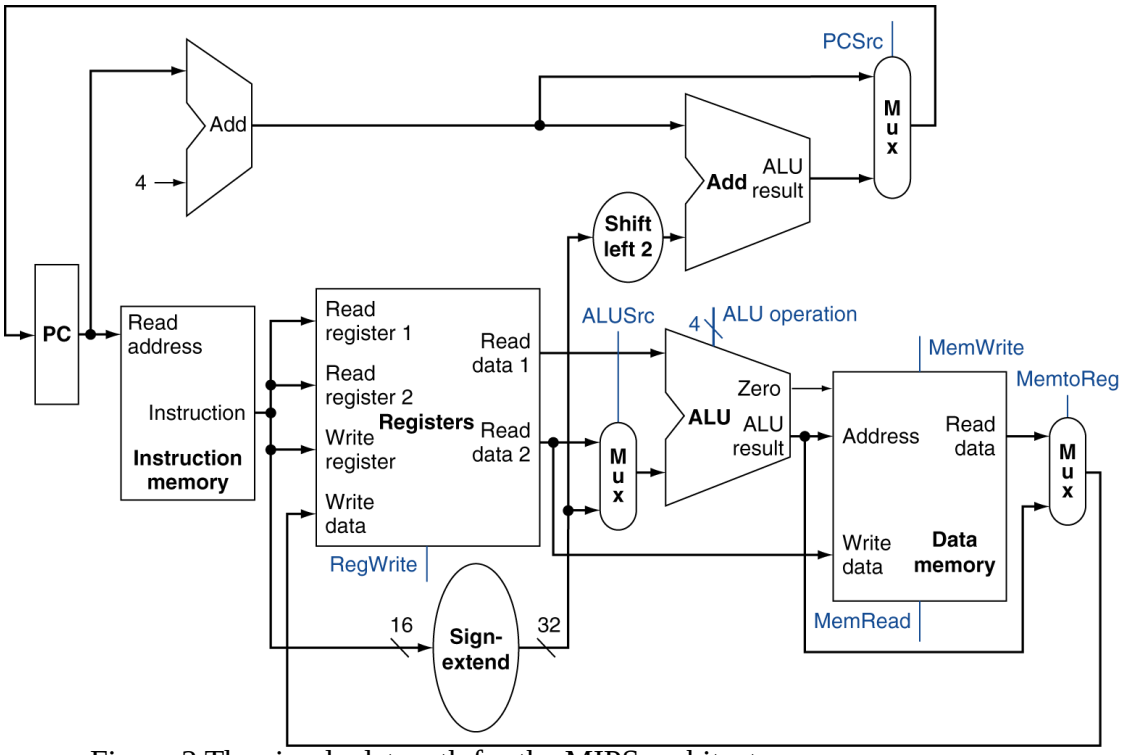

Figure 2 The simple datapath for the MIPS architecture

3. For the remaining problems in this exercise, assume that there are no pipeline stalls and that the breakdown of executed instructions is as follows:

	add	addi	not	beq	lw	sw
a.	30%	15%	5%	20%	20%	10%
b.	25%	5%	5%	15%	35%	15%

(1) In what fraction of all cycles is the input of the sign-extend circuit needed? (10%)

(2) If we can improve the latency of one of the given datapath components by 10%, which component should it be? what is the speed-up from this improvement? (10%)

4. According Figure 3, Figure 4 and Figure 5, please fill the results in the blank (1)~(36) in the Table 1. And there is an instruction that it is “add $s0, $s3, $s4 ” and its binary code is “ 0000000 10011 10100 10000 00000 100000”. Please fill the results in the blank (37)~(40) according points A~D in the Table 2. Assume that $s3 = 8, $s4 = 10 and pc = 16. (You must draw the Table on your answer paper and fill the results) (44%)

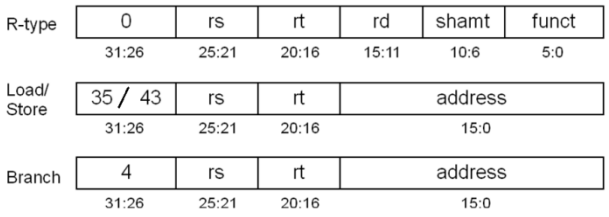

Figure 3

opcode	ALUOp	Operation	funct	ALU function	ALU control
lw	00	load word	XXXXXX	add	0010
sw	00	store word	XXXXXX	add	0010
beq	01	branch equal	XXXXXX	subtract	0110
R-type	10	add	100000	add	0010
		subtract	100010	subtract	0110
		AND	100100	AND	0000
		OR	100101	OR	0001
		set-on-less-than	101010	set-on-less-than	0111

Figure 4

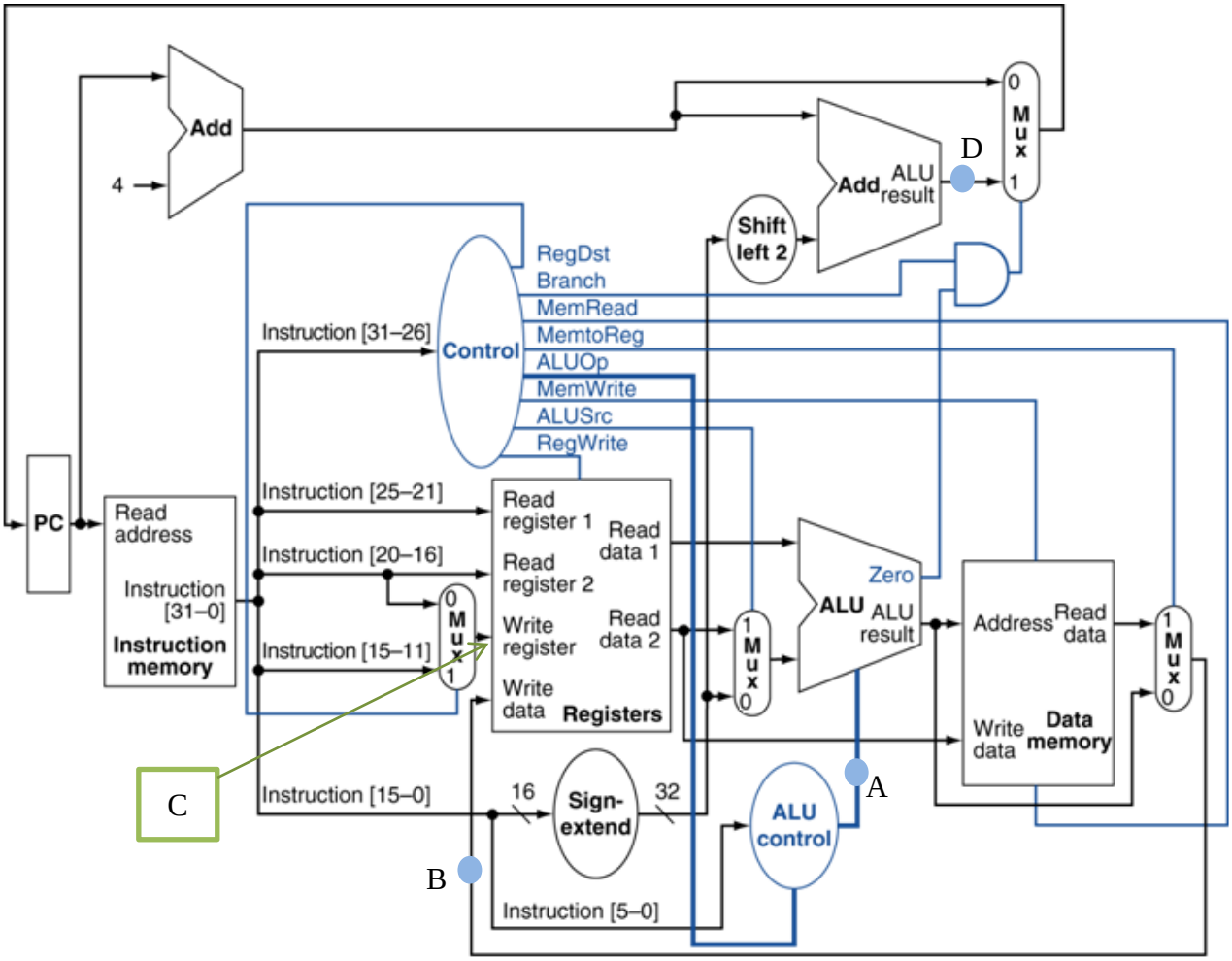

Figure 5

instruction	RegDst	ALUSrc	Memto-Reg	Reg Write	Mem Read	Mem Write	Branch	ALU Op1	ALU Op0
R-format	(1)	(2)	(3)	(4)	(5)	(6)	(7)	(8)	(9)
lw	(10)	(11)	(12)	(13)	(14)	(15)	(16)	(17)	(18)
sw	(19)	(20)	(21)	(22)	(23)	(24)	(25)	(26)	(27)
beq	(28)	(29)	(30)	(31)	(32)	(33)	(34)	(35)	(36)

Table 1

point	Value
A	(37)
B	(38)
C	(39)
D	(40) (5%)

Table 2

5. The MIPS processor uses multiple level control units that are main control and ALU control in Figure5. What is the advantage of multiple level control unit? (6%)