Chapter Exam

Chapter 4-The Processor

2012/06/05

1. Problems in this exercise assume that individual stages of the datapath have the following latencies:

	IF	ID	EX	MEM	WB
a	300ps	400ps	350ps	500ps	100ps
b	200ps	150ps	120ps	190ps	140ps

(1) What is the clock cycle time in a pipelined and nonpipelined processor? (10%)

(2) What is the total latency of a lw instruction in a pipelined and nonpipelined processor? (10%)

2. Problems in this exercise refer to the following instruction sequences:

	Instruction sequence

a.	lw $1, 40 ($2)
	add $2, $3, $3
	add $1, $1, #2
	sw $1, 20 ($2)

b.	add $1, $2, $3
	sw $2, 0 ($1)
	lw $1, 4 ($2)
	add $2, $2, $1

(1) Find all data dependences in this instruction sequence. (Hint: data dependences involve RAW, WAR, WAW)(10%)

(2) Find all hazards in this instruction sequence for a five-stage pipeline with and then without forwarding. (10%)

3. This exercise examines the accuracy of various branch predictors for the following repeating pattern (e.g., in a loop) of branch outcomes: (T: taken, NT: not taken)

	Branch outcomes
a.	T, T, NT, T
b.	T, T, T, NT, NT

(1) What is the accuracy of always-taken and always-not-taken predictors for this sequence of branch outcomes (10%)

(2) What is the accuracy of the two –bit predictor if this pattern is repeated forever?(10%)

4. Consider executing the following code on the pipeline in Fig. 1:

```
lw    $2, 10($1)
sub   $4, $3, $2
add   $5, $6, $7
and   $8, $4, $5
or    $9, $8, $3
```

(1) At the end of the fifth cycle of execution, what instruction will be in each of the MIPS pipeline stages (IF, ID, EXE, MEM, WB)? (10%)

(2) If the forwarding unit is not available, what instruction will be in each of the pipeline stages at the end of the fifth cycle for this instruction sequence to be executed correctly? (10%)

5. For the pipeline in Fig1, please complete following conditions, [1]~[4]? (20%)

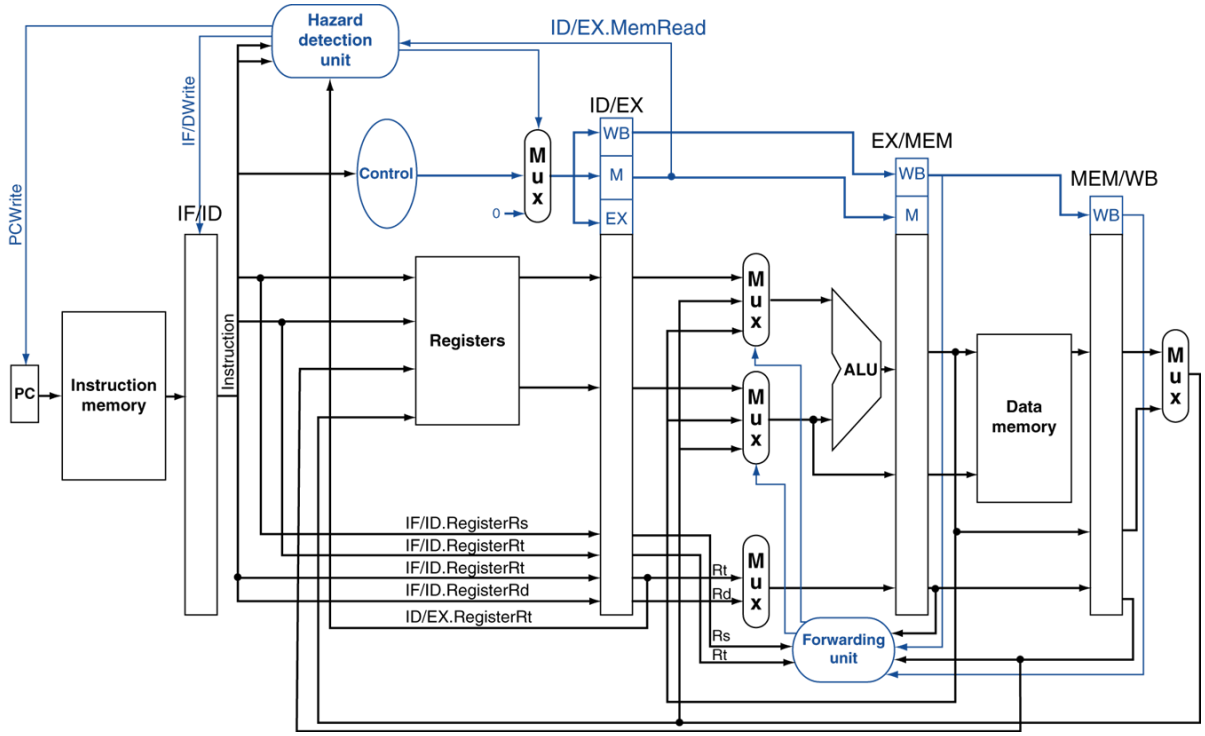

Fig1: the MIPS 5-stage (IF/ID/EX/MEM/WB) pipeline with the hazard detection unit and the forwarding unit

ForwardingA = 00	**ID/EX**	The first ALU operand comes from the register file
ForwardingA = 10	**EX/MEM**	The first ALU operand is forwarded from prior ALU result
ForwardingA = 01	**MEM/WB**	The first ALU operand is forwarded from data memory or an earlier ALU result
ForwardingB = 00	**ID/EX**	The second ALU operand comes from the register file
ForwardingB = 10	**EX/MEM**	The second ALU operand is forwarded from prior ALU result
ForwardingB = 01	**MEM/WB**	The second ALU operand is forwarded from data memory or an earlier ALU result

Forwarding conditions of EX hazard

if (EX/MEM.RegWrite and (EX/MEM.RegisterRd ≠ 0)
and (EX/MEM.RegisterRd = **[1]**)) ForwardA = 10

if (EX/MEM.RegWrite and (EX/MEM.RegisterRd ≠ 0)
and (EX/MEM.RegisterRd = **[2]**)) ForwardB = 10

Forwarding conditions of MEM hazard

if (MEM/WB.RegWrite and (MEM/WB.RegisterRd ≠ 0)
and (MEM/WB.RegisterRd = **[3]**)) ForwardA = 01

if (MEM/WB.RegWrite and (MEM/WB.RegisterRd ≠ 0)
and (MEM/WB.RegisterRd = **[4]**)) ForwardB = 01

6. The textbook presents the following development issues in a specific sequence (from simple to complex), in order to show a typical research and development (R&D) process. Please fill in the sequence number for the corresponding issue (1 being the simplest and 5 being the most complex). (10%)

Development Issue	Sequence (1…5)
Exception handling	
Single cycle implementation	
Data hazards	
Forwarding (bypassing) Unit	
Pipelining	
Hazard Detection Unit	
Control Hazards	
Delayed Branch	
2-bit Dynamic Branch Prediction	