課程: Computer Organization,
國立中山大學資訊工程學系, 教師：黃英哲

Chapter Exam

Chapter 4-The Processor

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1. Assume individual stages (IF,ID,EX,MEM,WB) of the datapath have the following latencies :

IF	ID	EX	MEM	WB
200ps	150ps	120ps	300ps	130ps

What is the **total execution time** in a 5-stage pipelined processor and in a non-pipelined single cycle processor to finish execute the following assembly codes ? **(20%)**

```
lw    $t0 ,0($s0)
sll   $t1, $t1, 2
sub   $t2,$t2,$t3
add   $t0 , $t0,$t3
sw    $t0 ,0($s0)
sub   $t4, $t0,$t2
```

2. According **Figure 1**, **Figure 2** and **Figure 3**, please fill the results in the blank (1)~(32) in the **Table 1**. And there is an instruction that it is "**sub $s0, $s3, $s4** " and its binary code is " 000000 10011 10100 10000 00000 100010". Please fill the results in the blank (33)~(35) according points A~C in the **Table 2**. Assume that $s3 =10 , $s4 = 2 and pc = 80. (You must draw the Table on your answer paper and fill the results) **(35%)**

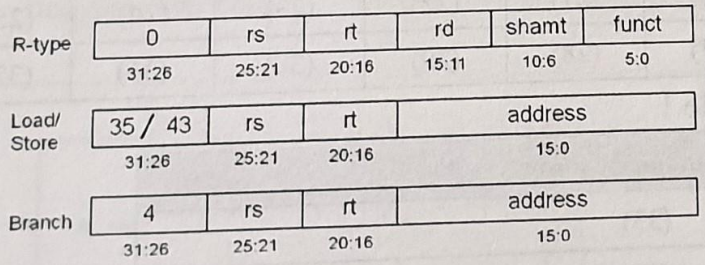


Figure 1

opcode	ALUOp	Operation	funct	ALU function	ALU control
lw	10	load word	XXXXXX	add	0010
sw	10	store word	XXXXXX	add	0010
beq	01	branch equal	XXXXXX	subtract	0110
R-type	00	add	100000	add	0010
		subtract	100010	subtract	0110
		AND	100100	AND	0000
		OR	100101	OR	0001
		set-on-less-than	101010	set-on-less-than	0111

Figure 2

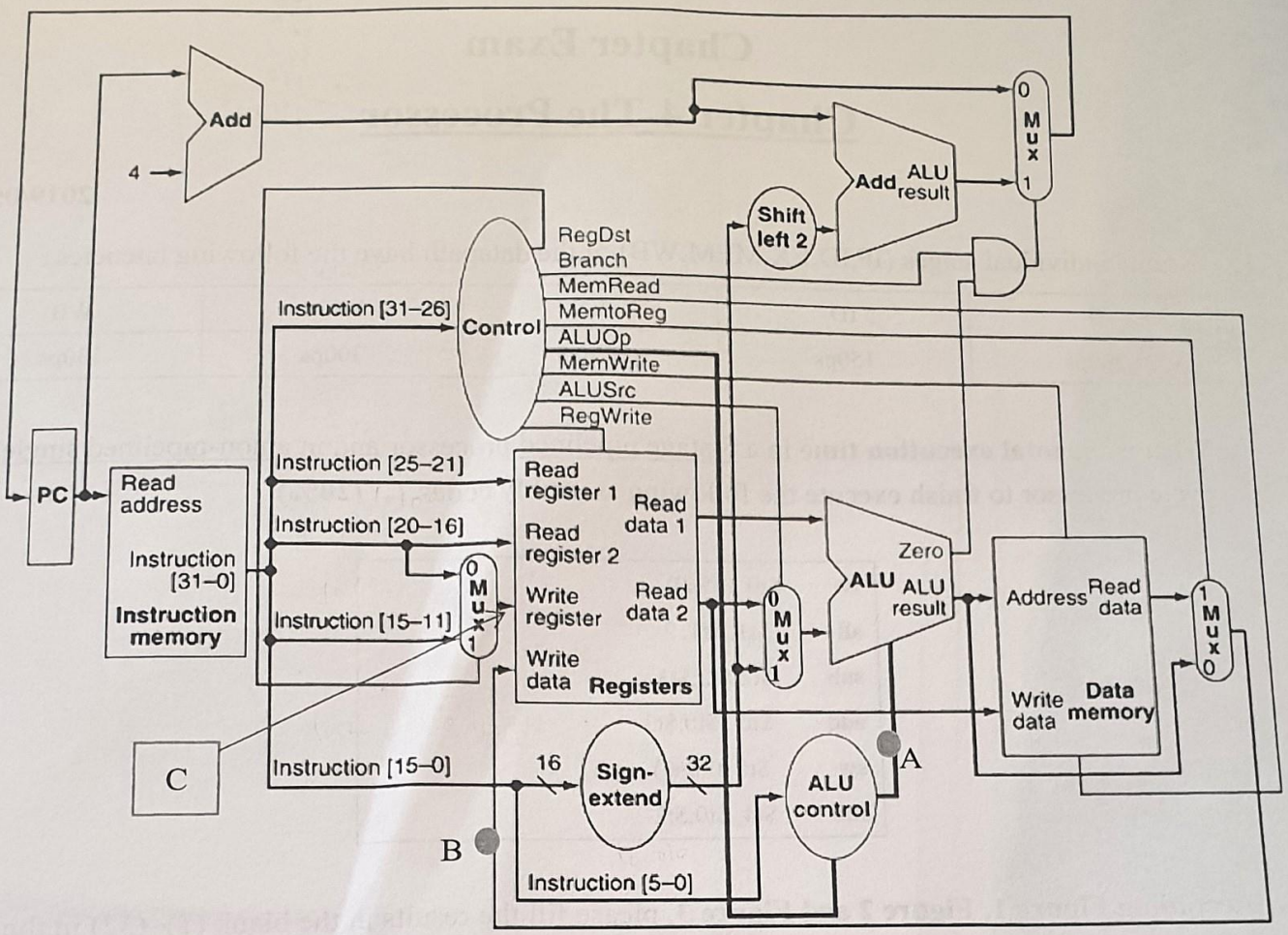


Figure 3

instruction	RegDst	ALUSrc	Memto-Reg	Reg Write	Mem Read	Mem Write	Branch	ALU Op1	ALU Op0
R-format	(1)	(2)	(3)	(4)	(5)	(6)	(7)	(8)	(9)
lw	(10)	(11)	(12)	(13)	(14)	(15)	(16)	(17)	(18)
sw	X	(19)	X	(20)	(21)	(22)	(23)	(24)	(25)
beq	X	(26)	X	(27)	(28)	(29)	(30)	(31)	(32)

Table 1

point	Value (in binary format)
A	(33)
B	(34)
C	(35)

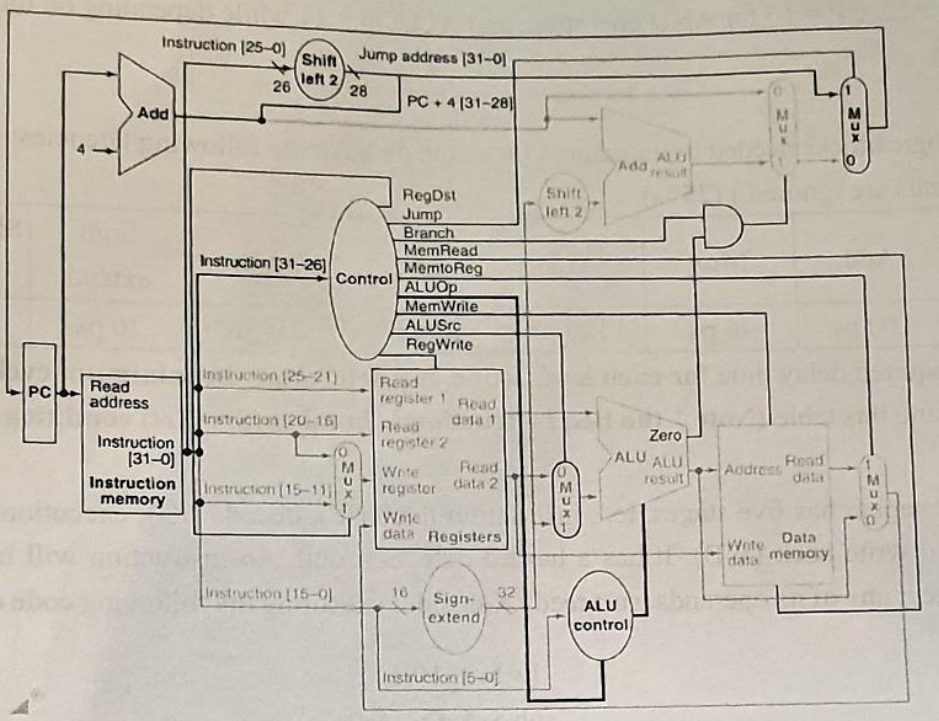
Table 2

sub $s0, $s3, $s4

3. Problem in this exercise refer to a clock cycle in which the processor fetches the following instruction word :

Instruction word
0001 0000 0010 0100 0000 0000 0000 1000

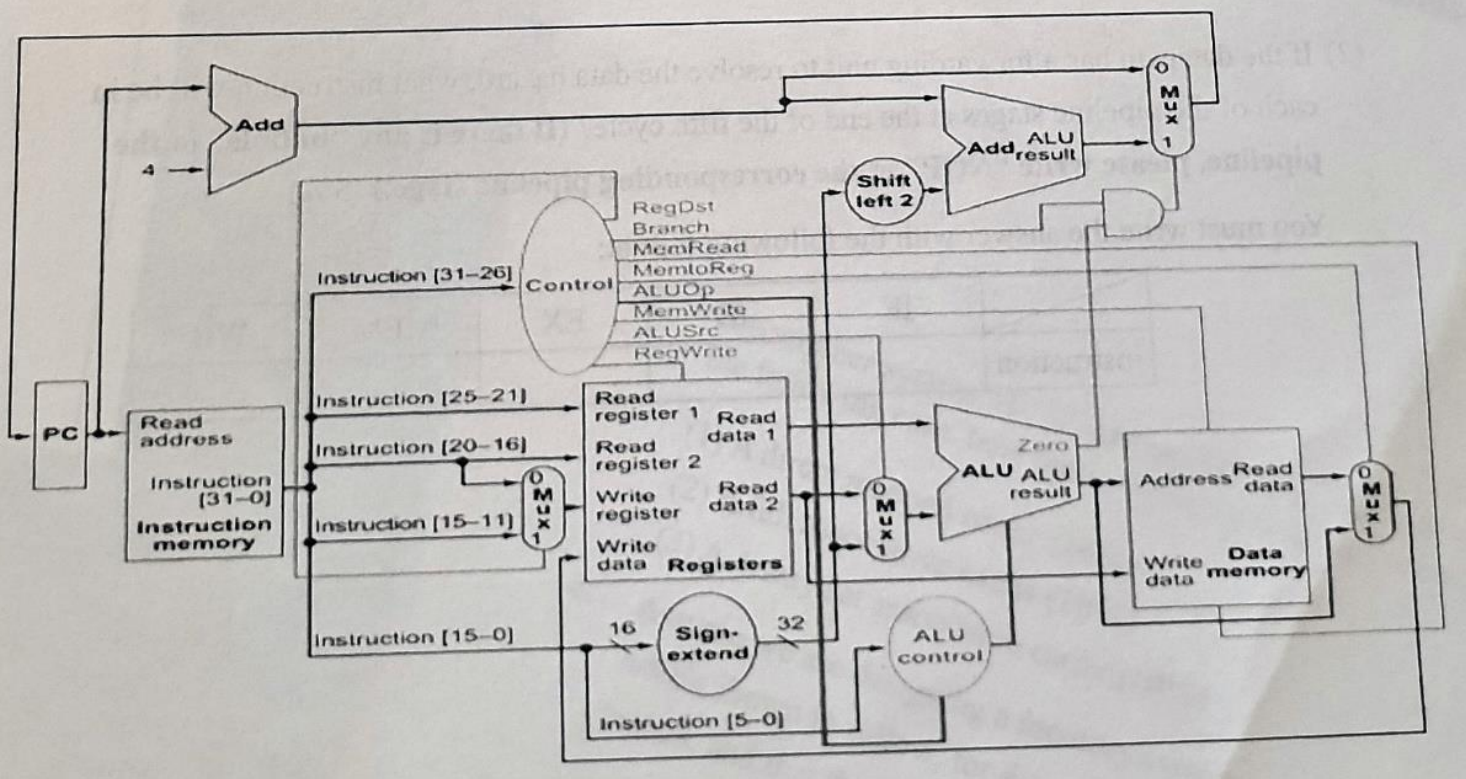
Figure 4.



What are the outputs of the **sign-extend** and the **jump "Shift left 2" unit** (in **Figure 4**)for this instruction words ? Please refer to Figure 1. and Figure 2. **(20%)**

4. A Give the datapath for a single-cycle implementation of a computer and the definition and formats of its instructions as follows:

add $rd, $rs, $rt	#$rd = $rs + $rt	R-format
lw $rt, addr($rs)	#$rt = Memory[$rs + sign-extend address]	I-format
sw $rt, addr($rs)	#Memory[$rs + sign-extend address] = $rt	I-format
beq $rs, $rt, addr	#if ($rs == $rt) then go to PC + 4 + 4×address	I-format



Assume that control signal ALUOp = 01 for performing addition of the ALU unit, ALUOp = 00 for subtraction, ALUOP = 10 for AND operation, and ALUOp = 11 while depending on the ***funct*** field of the instruction.

Assume that logic blocks needed to implement the datapath have the following latencies: (Delays for other components are ignored.) **(25%)**

I-Mem	Add	Mux	ALU	Regs	D-Mem	Sign extend	Shift-left-2 bits
400 ps	100 ps	40 ps	120 ps	200 ps	350 ps	20 ps	10 ps

Compute the required delay time **for each instruction** and **determine the minimum cycle time** of the computer by using this table:**(Note：the Beq instruction is in taken($rs=$rt) condition.)**

5. Pipelined datapath has five stages, ie. , instruction fetch (IF), decode (ID), execution (EX), memory (MEM), and write back (WB). It has a hazard detection unit. An instruction will be stalled at the decode stage if any of its operands isn't ready. Consider executing the following code on this datapath：

```
lw $r2, 10($1)
sub $r4, $r3, $r2
add $r5, $r6, $7
and $r8, $r4,$r5
```

(1) At the end of fifth cycle of execution, what instruction will be in each of the pipeline stages?**(If there is any "bubble" in the pipeline, please write "NOP" in the corresponding pipeline stage.) (5%)**

You must write the answer with the following format.

	IF	ID	EX	MEM	WB
instruction					

(2) If the datapath has a forwarding unit to resolve the data hazard, what instruction will be in each of the pipeline stages at the end of the fifth cycle? **(If there is any "bubble" in the pipeline, please write "NOP" in the corresponding pipeline stage.) (5%)**

You must write the answer with the following format:

	IF	ID	EX	MEM	WB
instruction					