Chapter Exam

Chapter 3-Arithmetic for Computers

2012/05/02

1. The following table shows pairs of decimal numbers.

	A	B
a	70	90
b	104	44

(1) Assume A and B are unsigned 8-bit decimal integers. Calculate A – B. Is there overflow, underflow, or neither? Why? (10%)

(2) Assume A and B are signed 8-bit decimal integers stored in sign-magnitude format. Calculate A + B. Is there overflow, underflow, or neither? Why? (10%)

2. Let's look in more detail at multiplication. We will use the numbers in the following table

A	B
101000 bin	010011 bin

the hardware described in Figure 1 to calculate the product of two unsigned 6-bits binary numbers A and B. Complete the contents of each register on each step list on the following table. (20%)

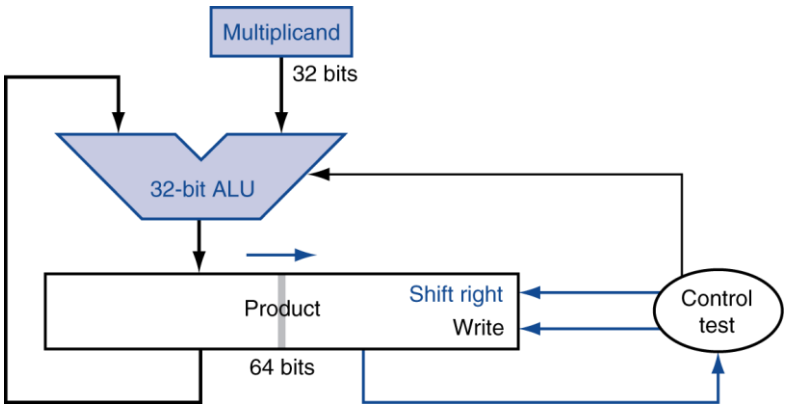

Figure 1 An improved version of the division hardware

step	Action	Multiplicand	Product/Multiplier
0	Initial value	101 000	(1)
1	Prod = Prod + Mcand		(2)
	Rshift Product	101 000	(3)
2	Prod = Prod + Mcand		(4)
	Rshift Mplier	101 000	(5)
3	lsb = 0, no op		
	Rshift Mplier	101 000	(6)
4	lsb = 0, no op		
	Rshift Mplier	101 000	(7)

5	Prod = Prod + Mcand		(8)
	Rshift Mplier	101 000	(9)
6	lsb = 0, no op		
	Rshift Mplier	101 000	(10)

3. What decimal number does the bit pattern represent if it is a floating-point number? Use the IEEE 754 standard.

The following table shows decimal numbers

a.	-160.5
b.	118.75

Write down the binary representation of the decimal number, assuming the IEEE 754 single precision format. (20%)

4. (1) What is the different between integer and float number in conditional branch? (5%) (2) How to compare with variable? Please show an example and describe it clearly (10%)

5. **C**onsider a two-dimensional array (A [*i*][*j*]), which *i* and *j* are 5. Draw how the array elements are stored in memory if it is row major? Also indicate the starting and ending address in element A[*i*][*j*], if the starting address is 0 and each element occupies a memory line. (5%)

6. Comparing the original hardware design (Figure 2) and the optimized hardware (Figure 3) design of the multiplier, please specify the features that have been optimized and explain why. (10%)

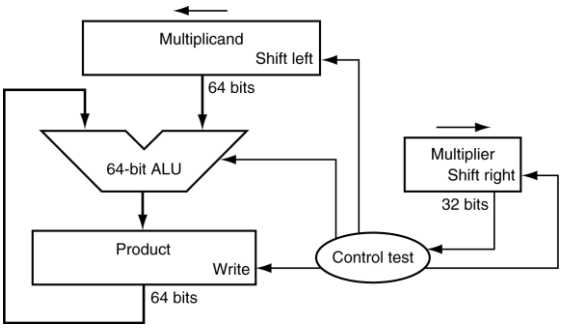

Figure 2 original hardware

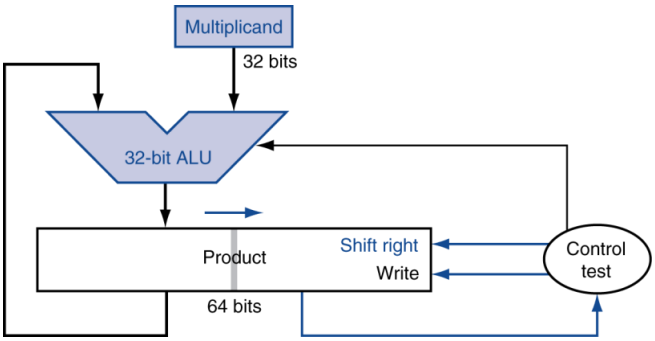

Figure 3 optimized hardware

7. In the IEEE-754 32-bit floating point format, why the exponent is biased and why the exponent field [30-23] is placed in the higher significant bits than the fraction field [22-0]? (10%)