課程: Computer Organization,
國立中山大學資訊工程學系, 教師：黃英哲

Chapter Exam

Appendix C-The Basics of Logic Design

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1. What are the differences between combinational logics and sequential logics? **(10%)**

2. What is the difference between Moore and Mealy machine? **(10%)**

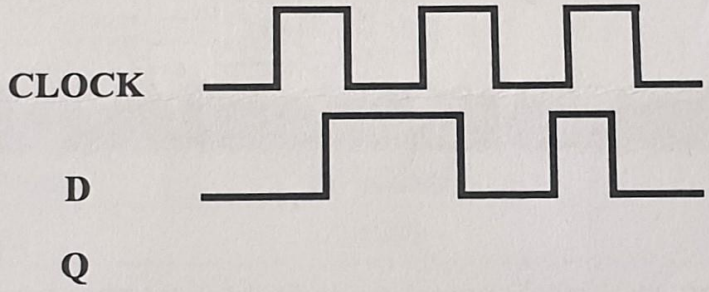
3. Prove that the two equations E1, E2 are equivalent **(10%)**

   $E1 = ((A \cdot B) + (B \cdot C)) \cdot \overline{(A \cdot B \cdot C)}$

   $E2 = (A \cdot B \cdot \overline{C}) + (\overline{A} \cdot B \cdot C)$

4. Explain the function of the following circuit. **(10%)**

5. Complete timing diagram according to CLOCK、D(input)、Q(output) signals.
   Each timing diagram should include CLOCK、D(input)、Q(output).**(20%)**



   i) D latch : **(10%)**

   ii) D flip-flop : **(10%)**

6. What's the most significant difference between C programing and digital logic design? **(5%)**

7. Derive the logic equations (5.a, 5.b, 5.c, 5.d and 5.e) of a 16-bit CLA (carry look ahead) adder below. There is no need to simplify the equations. **(30%)**

$gi = ai \cdot bi$ $\quad pi = ai + bi$

$P0 = p3 \cdot p2 \cdot p1 \cdot p0$

$P1 = p7 \cdot p6 \cdot p5 \cdot p4$

$P2 = p11 \cdot p10 \cdot p9 \cdot p8$

$P3 =$ [5.a]

$G0 = g3 + (p3 \cdot g2) + (p3 \cdot p2 \cdot g1) + (p3 \cdot p2 \cdot p1 \cdot g0)$

$G1 = g7 + (p7 \cdot g6) + (p7 \cdot p6 \cdot g5) + (p7 \cdot p6 \cdot p5 \cdot g4)$

$G2 =$ [5.b]

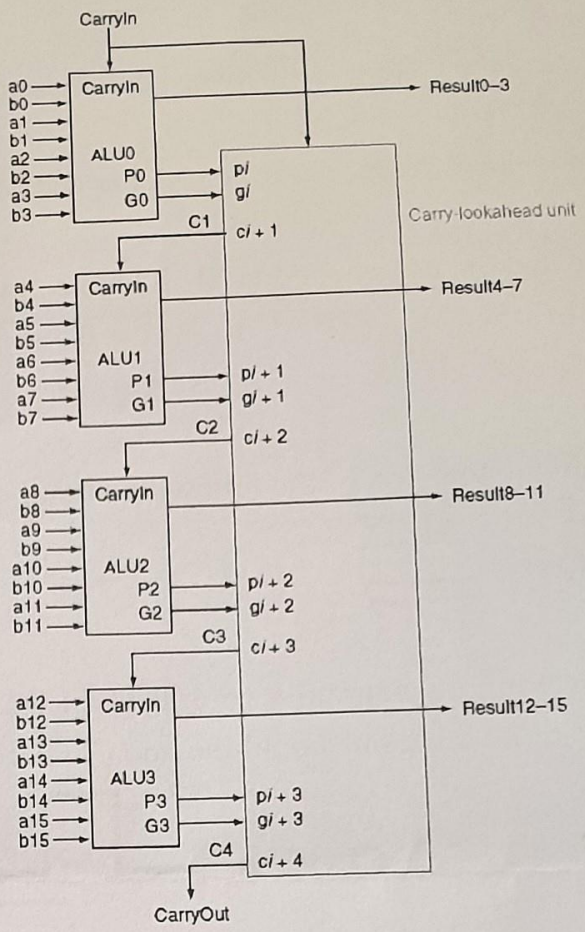
$G3 =$ [5.c]

$C1 = G0 + (P0 \cdot c0)$ $\quad G_1 + P_1(C1)$

$C2 = G1 + (P1 \cdot G0) + (P1 \cdot P0 \cdot c0)$

$C3 =$ [5.d]

$C4 =$ [5.e]



8. Prove that the NOR gate is universal by showing how to build the AND, OR, and NOT functions using a two-input NOR gate. **(15%)**

i) AND gate

ii) OR gate

iii) NOT gate

$(A'+B')' = AB$

$((A+B)')' = (A'B')' = A+B$