課程: Computer Organization,
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Chapter Exam

Chapter 1-Computer Abstractions and Technology

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1. Consider two different implementations of the same instruction set architecture. There are four classes of instructions, A, B, C, and D. The clock rate and CPI of each implementation are given in the following table.

	Clock rate	CPI Class A	CPI Class B	CPI Class C	CPI Class D
P1	1.4 GHz	4	3	2	1
P2	2 GHz	2	2	4	2

(1) Given a program with 10^6 instructions divided into classes as follows: 10% class A, 20% class B, 50% class C and 20% class D, which implementation is faster? **(5%)**

(2) Which is the global CPI for each implementation? **(10%)**

2. Consider the following performance measurements of a program, which computer has the higher MIPS rating? **(5%)**

Measurement	Computer A	Computer B
Instruction count	10 billion	8 billion
Clock rate	5 GHz	3GHz
CPI	1	2

3. Consider two different processor P1 and P2 executing the same instruction set with the clock rates and CPIs given in the following table.

Processor	Clock Rate	CPI
P1	1.5 GHz	0.5
P2	2 GHz	2.0

(1) Which processor has the highest performance? **(5%)**

(2) If the processors each execute a program in 10 seconds, find the number of execution cycles and the number of execution instructions. **(10%)**

(3) We are trying to reduce the time by 10% but this leads to an increase of 20% in the CPI. What clock rate (for each processor) should we have to get this time reduction? **(10%)**

4. (1) Describe the definition of Amdahl's law **(5%)**

(2) Suppose we enhance a machine making all floating-point instructions run 10 times faster. If the execution time of some benchmark before the floating-point enhancement is 30 seconds, what will the speed up if $\frac{2}{3}$ of the 60 seconds are spent executing floating-point instructions? **(10%)**

time = cc × ct → 1/rate

5. A base processor and two options for improving its hardware and compiler design described as follows :

I. The base machine, Mbase :

Mbase has a clock rate of 250 MHz and the following measures :

Instruction class	CPI	Frequency
A	1	40%
B	2	20%
C	3	40%

II. The machine with improved hardware, Mhw :

Mhw has a clock rate of 400 MHz and the following measures :

Instruction class	CPI	Frequency
A	2	50%
B	2	20%
C	3	30%

III. The combination of the improved compiler and the base machine, Mcomp :

The instruction improvements from this enhanced compiler are as follows :

Instruction class	Percentage of instructions executed vs. Mbase
A	80%
B	70%
C	60%

(1) What is the CPI(clock cycles per instruction) for each machine? **(15%)**

(2) How much faster is each of Mhw and Mcomp than Mbase? **(10%)**

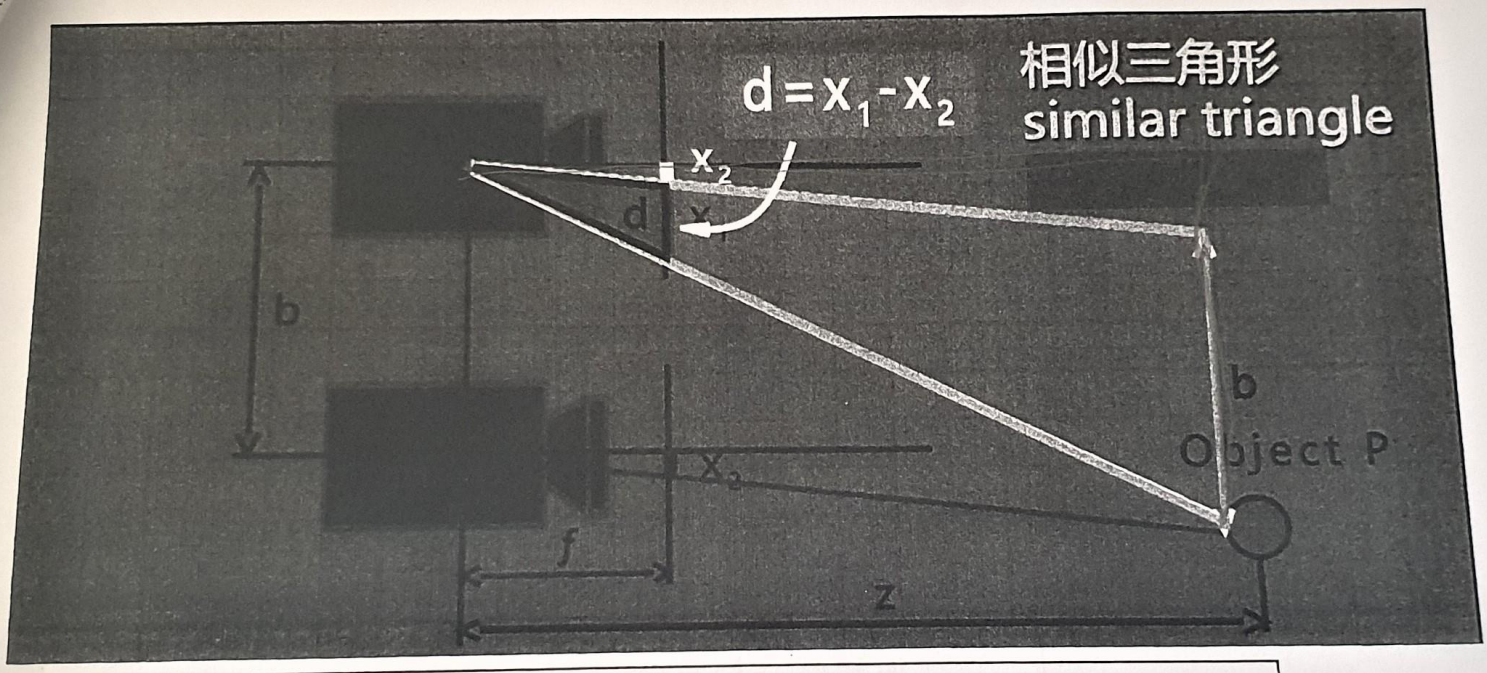
6. The following table shows results for SPEC2006 benchmark programs running on an AMD Bracelona.

Name	Intr. Count x10^9	Execution time (seconds)	Reference time (seconds)
perl	3000	1500	45000

(1) Find the CPI if the clock cycle time is 0.333 ns. **(5%)**

(2) Find the SPEC ration. **(5%)**

7. In the depth camera diagram, describe the relationship between the four variables f, b, z, d in the form of "p : q = x : y", based on the similar triangle principle. (5%)



b：照相機間距(Camera Distance)	f：焦距(Focus Distance)
z：物件深度(Object Depth)	d：視差(Disparity)

8. PID is a popular automatic control mechanism, which consists of P (proportional) unit, I (integral) unit and D (derivative) unit. What's the purpose of I unit and D unit, respectively? (10%)