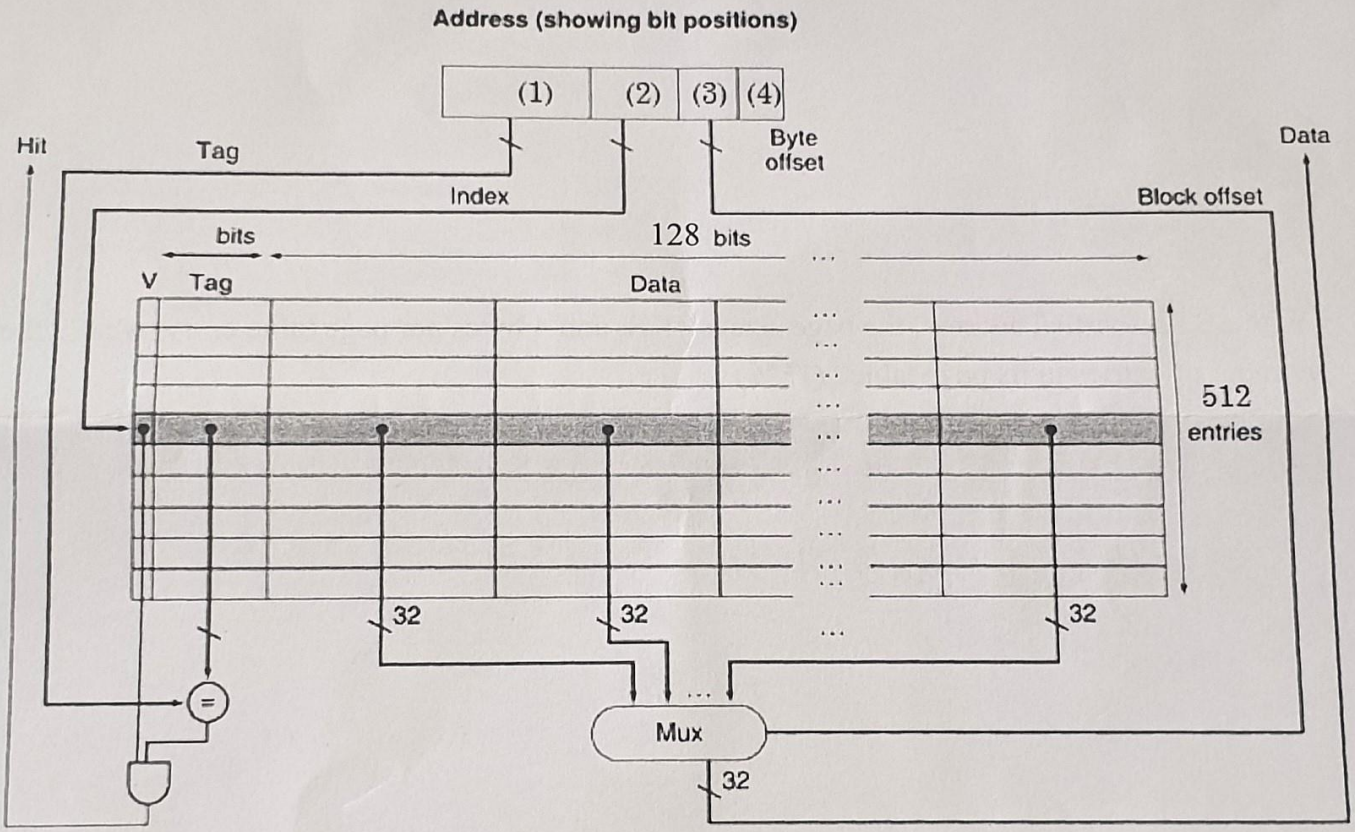
Chapter Exam

Chapter 5 – Memory Hierarchy

2019/06/18

1. For a Direct-mapped cache design with 32-bit address, how many total bits required with 64KB of data, 1-bit tag and 1-word block? **(15%)**

2. Consider a Direct-mapped cache as shown below, assume a **32-bit address**, 512 entries, and can store 128 bits data per block (1 word consists of 4 byte). How many bits are required for (1) Tag (2) Index (3) Block offset and (4) Byte offset ? **(20%)**



3. A computer system has 32 address line and 16K byte cache. Each cache block size is 32bytes. For the following case, how many *tag-bit* is required for each cache block?

   (1) A direct mapped cache **(10%)**

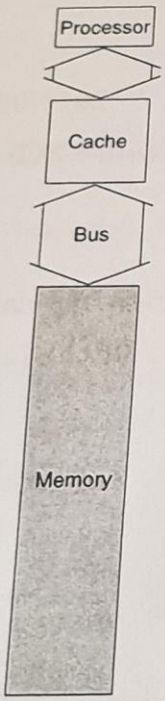
   (2) A full associative cache **(10%)**

   (3) A 4-way set associative cache **(10%)**

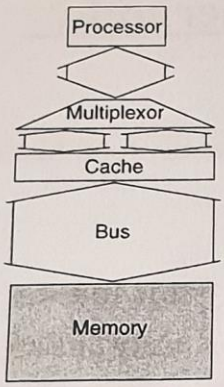
4. Assume we are designing a memory system and there are there architecture we considered, which shown in follow, for 4-word block, the width of organization of the figure (b) is four words, and that the number of banks in organization of the figure (c) is four.

   A cache block read operation needs: (1) 1 bus cycle for address transfer. (2) 15 bus cycles per DRAM access(for initiation). (3) 1 bus cycle per data transfer.

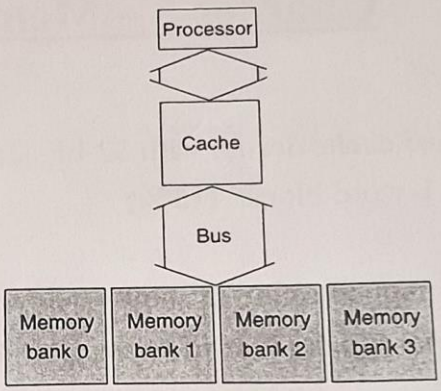
Calculate the time for reading a block from memory to cache by these three architectures (a), (b), (c). **(30%)**



a. One-word-wide memory organization



b. Wider memory organization



c. Interleaved memory organization

5. With a 32-bit virtual address, the page size is 4KB, and 4 bytes per page table entry, what's the number of entries in its page table? **(15%)**