數位電子學 第七章 習題

μnCox =200 μA/V2 , μpCox =100 μA/V2 , NMOS *VTH* =0.4 V, PMOS *VTH* =−0.4 V,

7.3 The circuit of Fig 7.37 must be designed for a voltage drop of 200 mV across *RS*. (a) Calculate the minimum allowable value of W/L if M1 must remain in saturation. (b) What are the required value of *R1*and *R2*if the input impedance must be at least 30 kΩ.

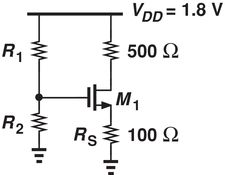


Fig. 7.37

7.6 The self-biased stage of Fig 7.39 must be designed for a drain current of 1 mA. If M1 is to provide a transconductance of 1/(100Ω), calculate the required *RD*.

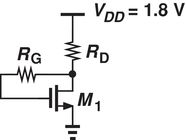


Fig. 7.39

7.12 Consider the circuit shown in Fig. 7.45 where (W/L)1 = 10/0.18 and (W/L)2 = 30/0.18. If λ = 0.1 V-1, calculate *VB* such that *VX* = 0.9 V.

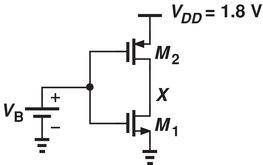


Fig. 7.45

7.16 In the common-source stage of Fig. 7.49, W/L = 30/0.18 and λ = 0. (a) What gate voltage yields a drain current of 0.5 mA? (Verify that M1 operates In saturation.) (b) With such a drain bias current, calculate the voltage gain of the stage.

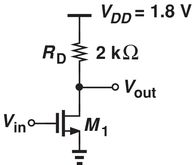


Fig. 7.49

7.23 The CS stage shown in Fig. 7.56 must achieve a gain of 7. If (W/L)2 =2/0.18, compute the required (W/L)1.

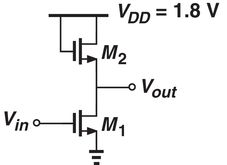


Fig. 7.55

7.26 For the circuit shown in. Fig.7.59, which should give gain of 5 with a bias current of 0.5 mA. Assume a drop of 250 mV across *RS* and λ = 0. (a) If *RD* = 2kΩ, determine the required (W/L). (b) If (W/L) = 40/0.18, determine the value of *RD*.

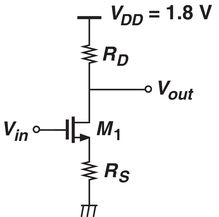


Fig. 7.59

7.32 For a circuit in Fig. 7.65, for λ = 0, *I1* = 2 mA, what is the maximum value of *RD* for M1 to be in saturation.

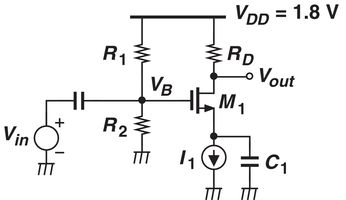


Fig. 7.65

7.45 Calculate voltage gain of circuit as shown in Fig. 7.76.

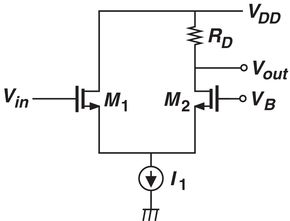


Fig. 7.76

7.47 For the circuit shown in Fig. 7.78, *AV* = 0.85, power budget 2 mW, determine required (W/L) ratio. C is very large and λ= 0.

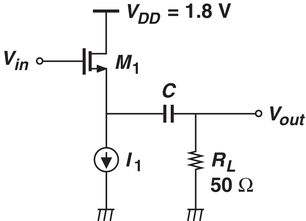


Fig. 7.78