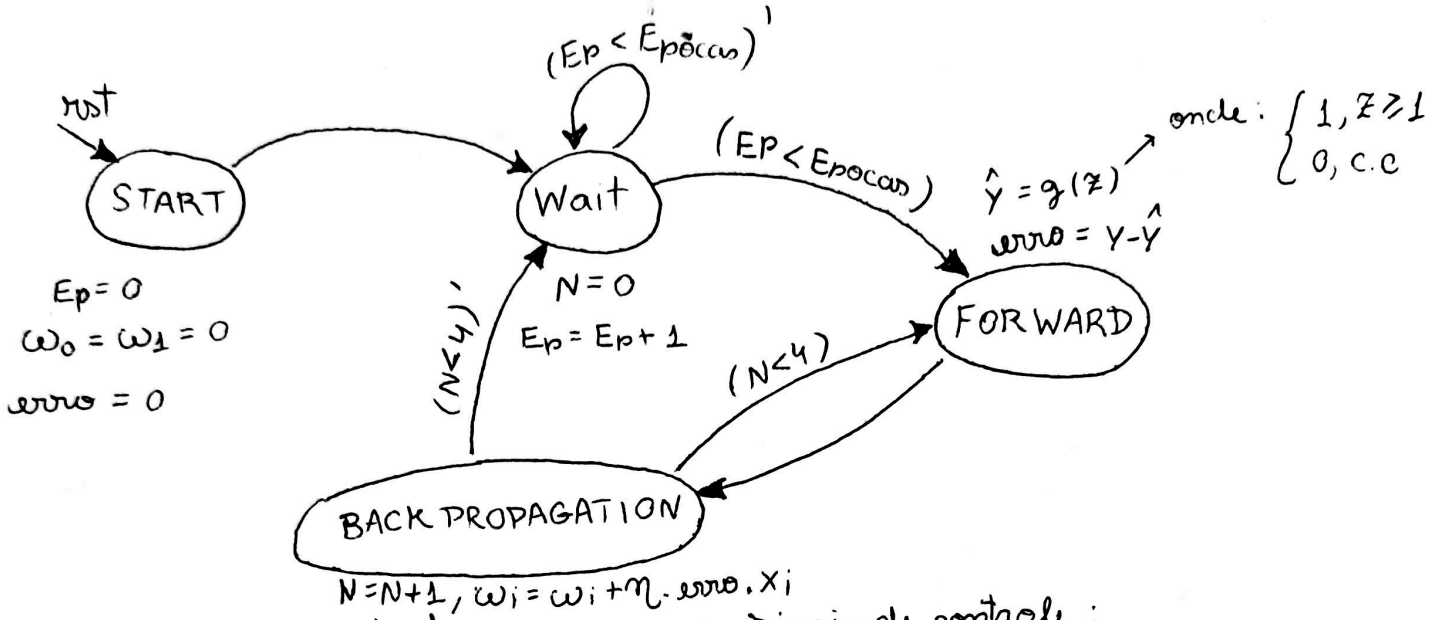
⊙ Projeto RTL

(1) FSM - Máquina de Estados



* Codificação dos estados

00 → START
01 → WAIT
10 → FORWARD
11 → BACKPROPAGATION

* Sinais de status:

> Epm = 1 (Ep < Epocas)

> Nm = 1 (N < 4)

* Sinais de controle:

> ld_n = 1 (N = N+1) → carrega + 1 amostra

> clr_n = 1 (N = 0) → limpa as amostras

> ld_Ep = 1 (Ep = Ep+1) → carrega + 1 época

> clr_Ep = 1 (Ep = 0) → limpa as épocas

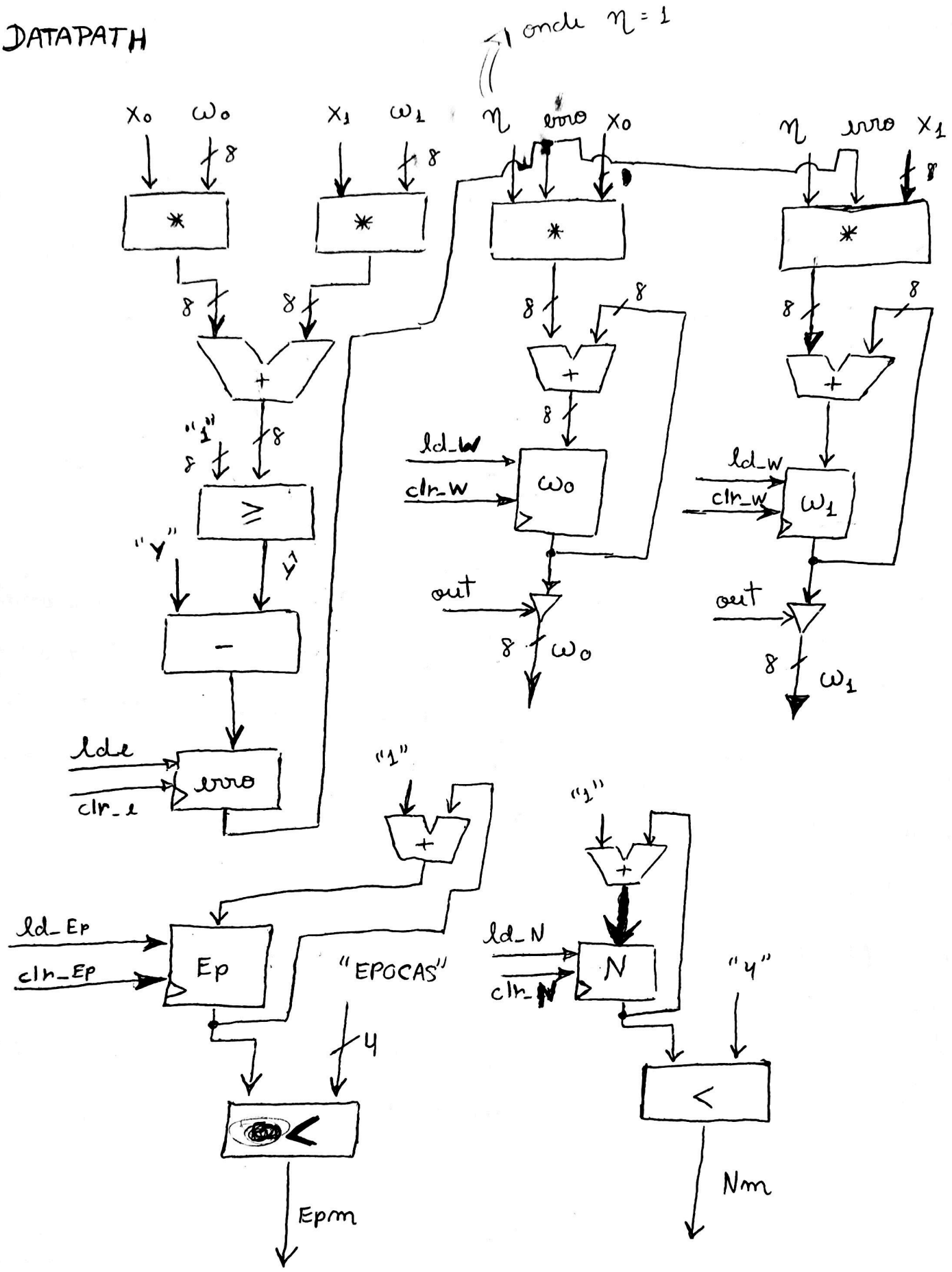
> clr_w = 1 (ω0 = ω1 = 0) → limpa os pesos

> ld_w = 1 (ωi = ωi + η . erro . Xi) → carrega os pesos rebalanceados

> ld_e = 1 (erro = Y - ŷ) → carrega o erro atualizado.

> clr_e = 1 (erro = 0) → limpa o registrador de erro

(2) DATAPATH



onde: $\hat{y}$ = y_pred

Controle (3)

Estados: $2^n \geq 4 \rightarrow n = 2$ bits

* Codificação

S_1 S_0	ESTADO
0 0	START
0 1	WAIT
1 0	FOWARD
1 1	B.PROP

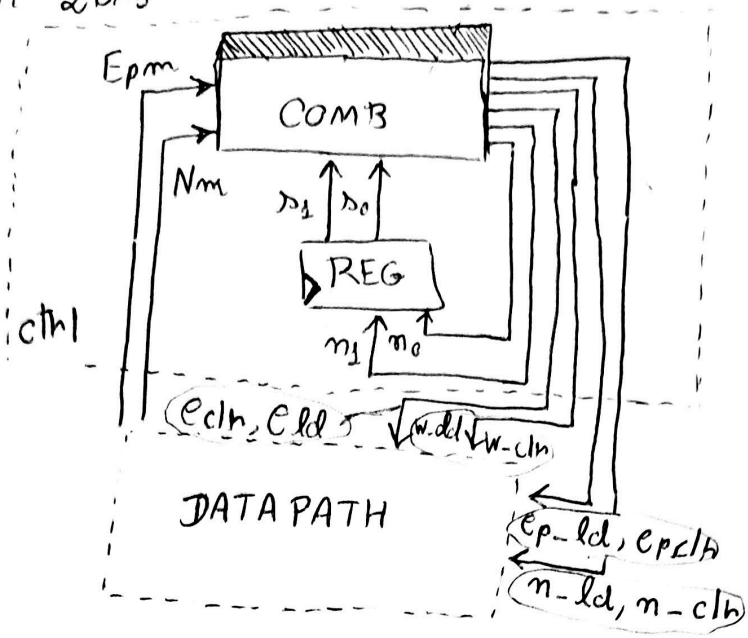


TABELA DE TRANSIÇÃO DE ESTADOS

ld, clr

	INPUTS				OUTPUTS									
	S_1	S_0	Epm	Nm	n_1	n_0	e_ld	e_clr	w_ld	w_clr	ep_ld	ep_clr	n	n
(START)	0	0	X	X	0	1	0	1	0	1	0	1	0	0
(WAIT)	0	1	0	X	0	1	0	0	0	0	1	0	0	1
(WAIT)	0	1	1	X	1	0	0	0	0	0	1	0	0	1
(FOWARD)	1	0	X	X	1	1	1	0	0	0	0	0	0	0
(B.PROP)	1	1	X	0	0	1	0	0	1	0	0	0	1	0
(B.PROP)	1	1	X	1	1	0	0	0	1	0	0	0	1	0