Assignment2 Report

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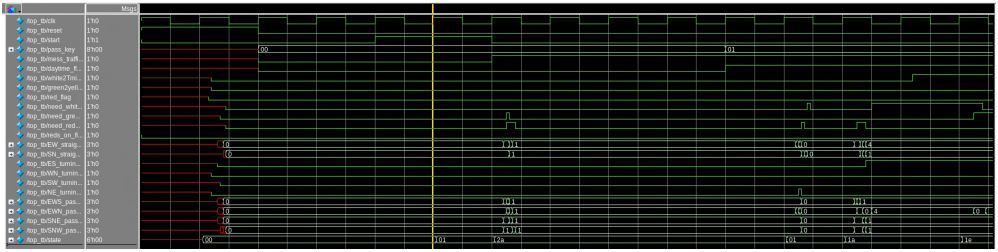
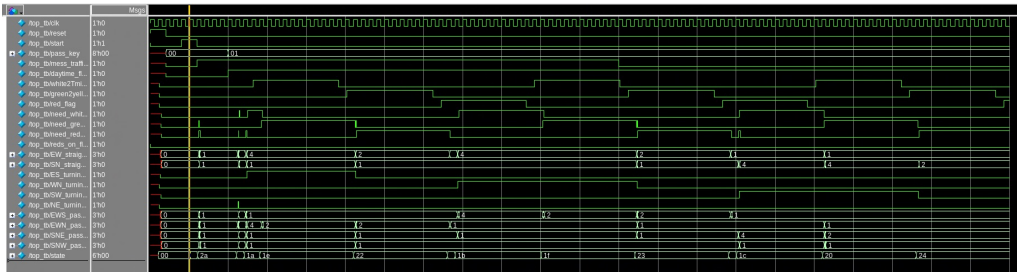
Following are state transition from mapped verilog



We can see the delay between posedge of clk and the change position of state



For large scale the whole system working properly

All input files are included in “in” and output files are included in “out”