CHAPTER 7 Basic Op-Amp Circuits

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CHAPTER 7 Basic Op-Amp Circuits

7.1 Comparators

7.2 Summing Amplifiers

7.3 Integrators and Differentiators

7.1 Comparators

- A **comparator** is a specialized op-amp circuit that compares two input voltages and produces an output that is always at either one of two states, indicating the greater or less than relationship between the inputs.
- **Zero-Level Detection**
- Figure 7–1(a) shows a zero-level detector. Notice that the inverting(-) input is grounded to produce a zero level and that the input signal voltage is applied to the noninverting (+) input.
- Because of the high open-loop voltage gain, a very small difference voltage between the two inputs drives the amplifier into saturation, causing the output voltage to go to its limit.

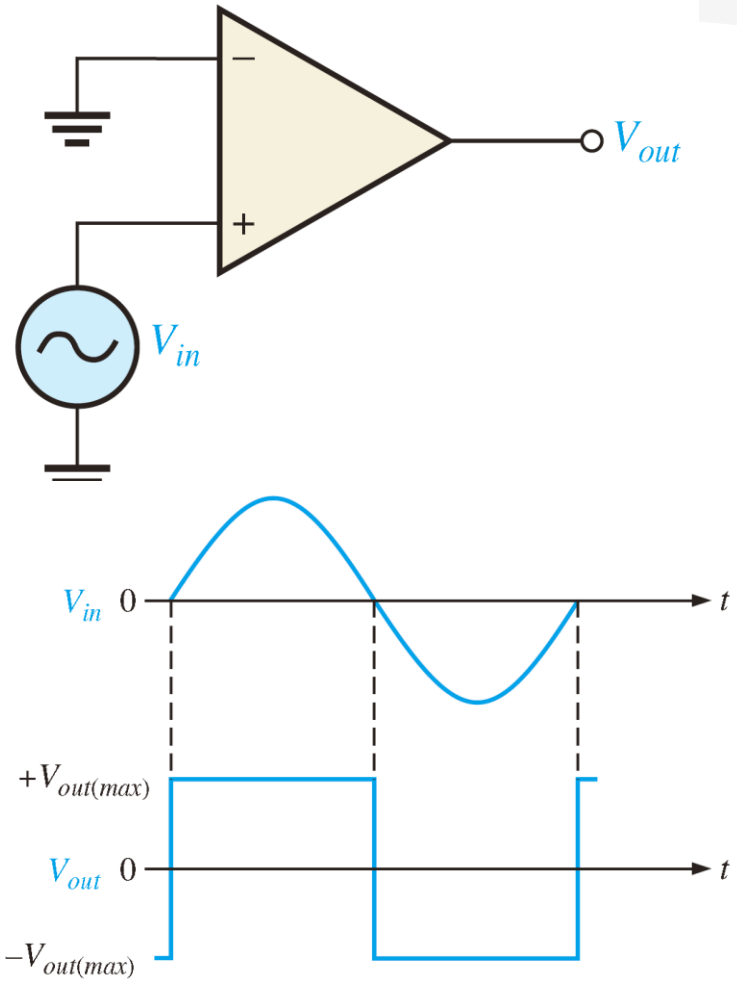


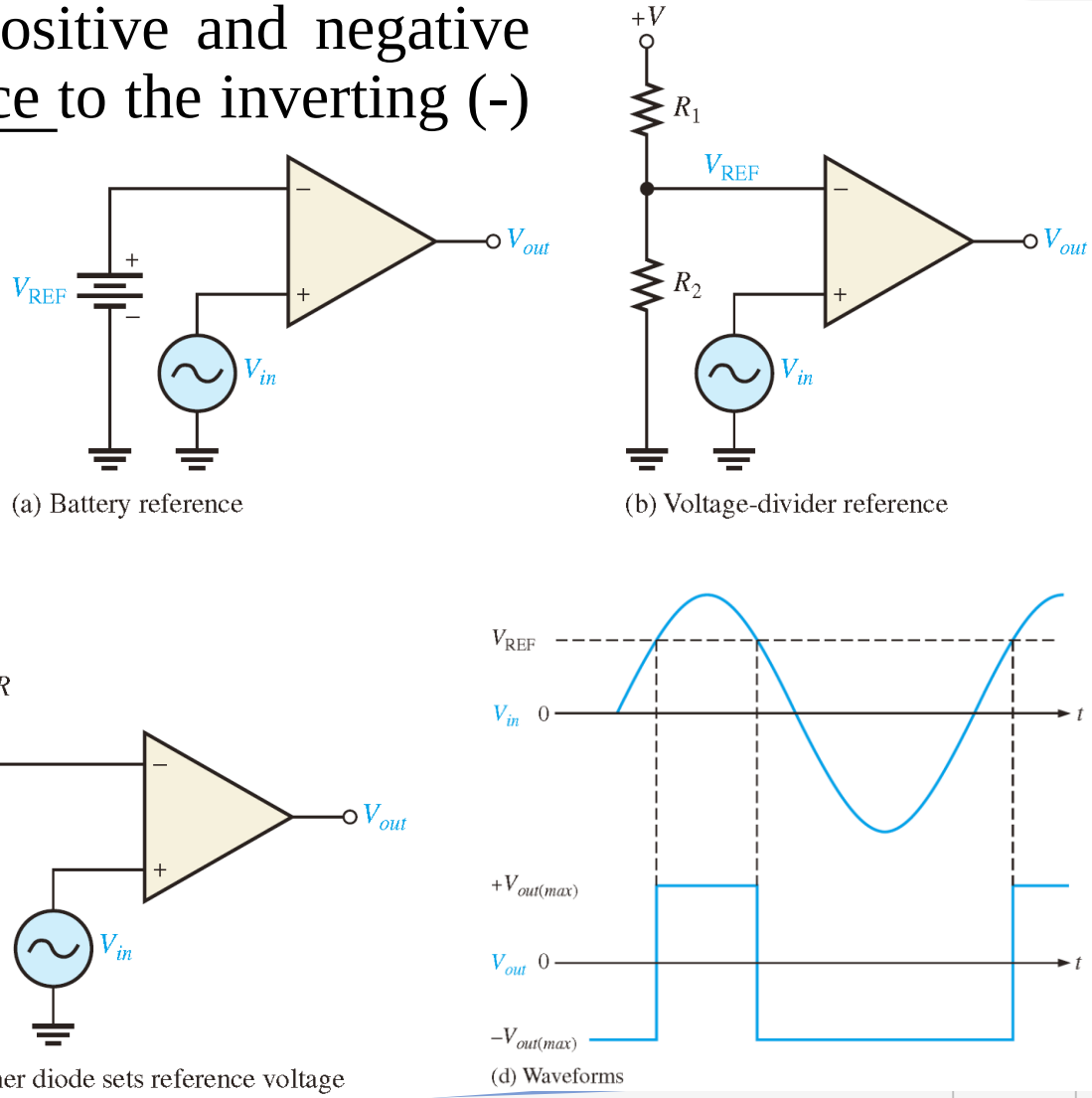
FIGURE 7-1
The op-amp as a zero-level detector.

Nonzero-Level Detection

- The zero-level detector can be modified to detect positive and negative voltages by connecting a fixed reference voltage source to the inverting (-) input, as shown in Figure 7–2(a).
- A more practical arrangement is shown in Figure 13–2(b) using a voltage divider to set the reference voltage, V_{REF}, as follows:

$$V_{REF} = \frac{R_2}{R_1 + R_2}(+V)$$

- The circuit in Figure 7–2(c) uses a zener diode to set the reference voltage ($V_{REF} = V_Z$).
- As long as V_{in} is less than V_{REF}, the output remains at the maximum negative level. When the input voltage exceeds the reference voltage, the output goes to its maximum positive voltage.



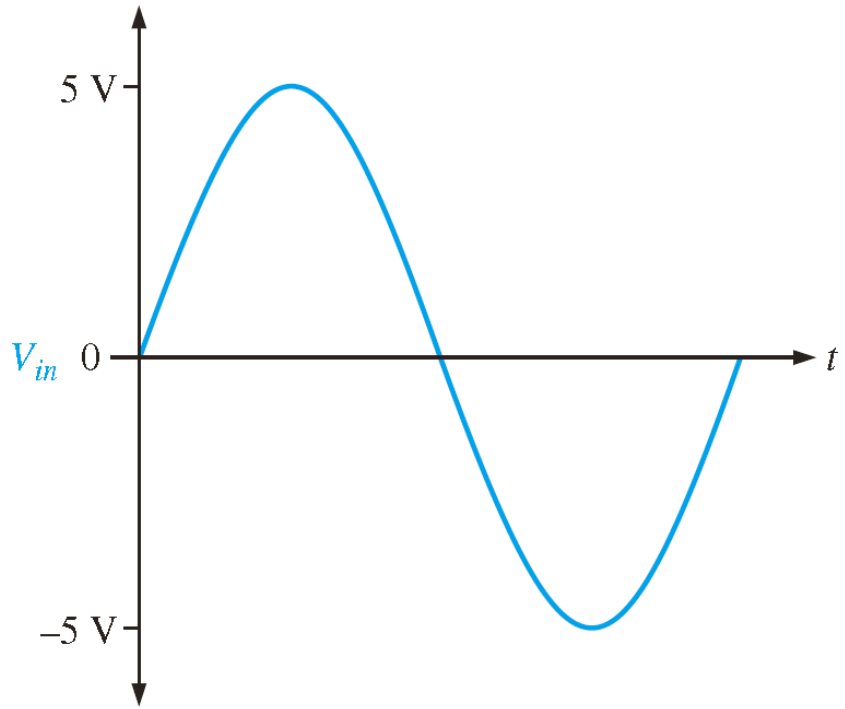
(a) Battery reference (b) Voltage-divider reference

(c) Zener diode sets reference voltage (d) Waveforms

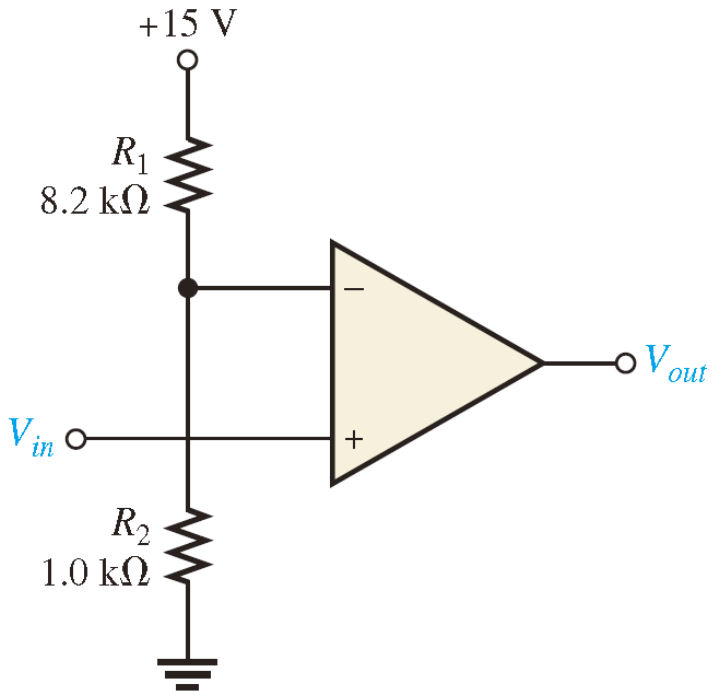
FIGURE 7-2 Nonzero-level detectors.

Example

The input signal in Figure 13–3(a) is applied to the comparator in Figure 13–3(b). Draw the output showing its proper relationship to the input signal. Assume the maximum output levels of the comparator are ±14 V.



(a)



(b)

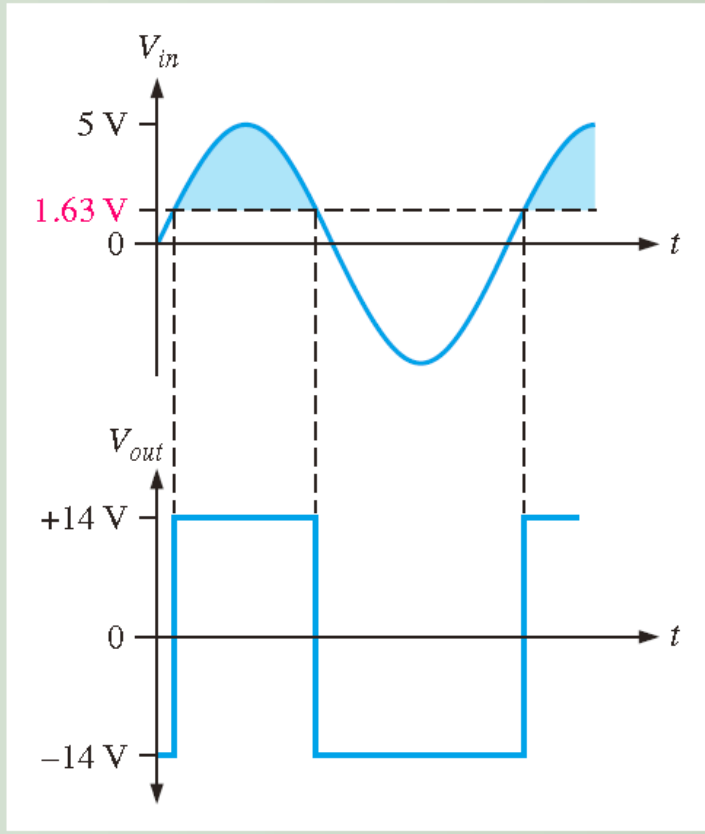
Example

Solution The reference voltage is set by R_1 and R_2 as follows:

$$V_{REF} = \frac{R_2}{R_1 + R_2}(+V) = \frac{1.0\,\text{k}\Omega}{8.2\,\text{k}\Omega + 1.0\,\text{k}\Omega}(+15\text{ V}) = 1.63\text{ V}$$

As shown in Figure 13–4, each time the input exceeds +1.63 V, the output voltage switches to its +14 V level, and each time the input goes below +1.63 V, the output switches back to its −14 V level.

▶ FIGURE 13–4



Effects of Input Noise on Comparator Operation

- In many practical situations, noise (unwanted voltage fluctuations) appears on the input line. This noise voltage becomes superimposed on the input voltage

- The figure shows the input sine wave plus noise and the resulting output. When the sine wave approaches 0, the fluctuations due to noise may cause the total input to vary above and below 0 several times, thus producing an erratic output voltage.

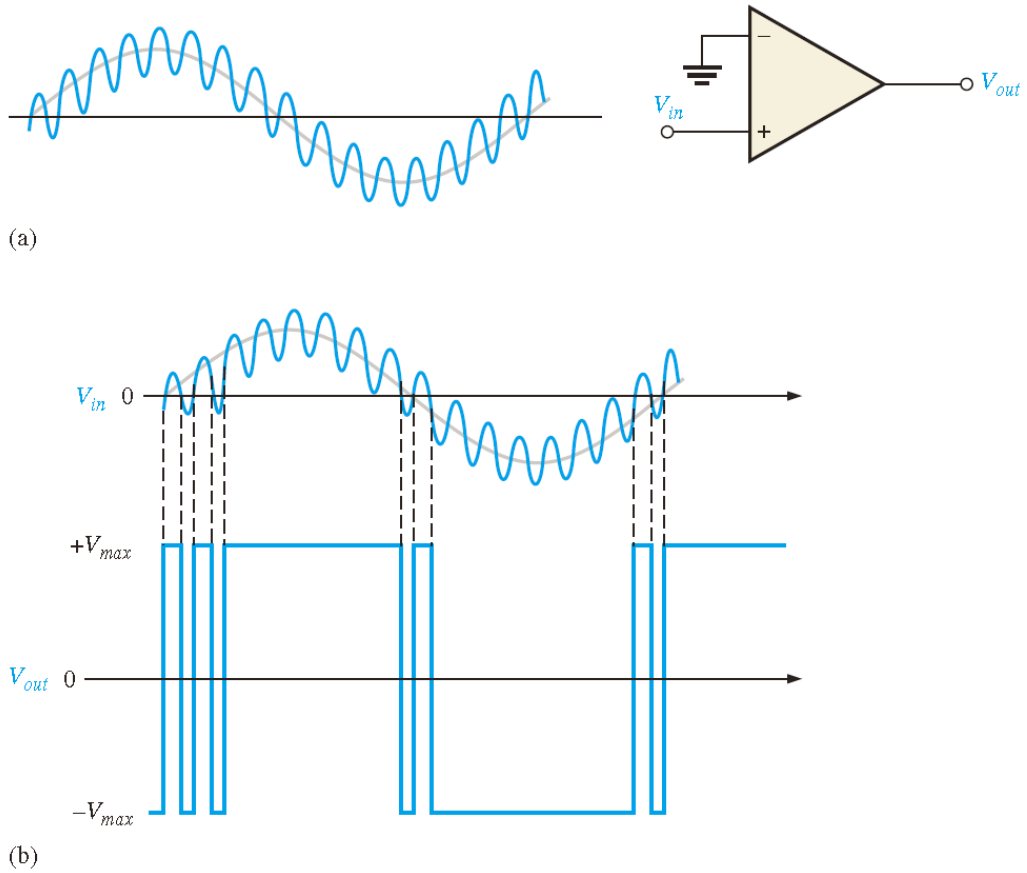


FIGURE 7-3 Effects of noise on comparator circuit.

Hysteresis

- In order to make the comparator less sensitive to noise, a technique incorporating positive feedback, called hysteresis, can be used. Basically, hysteresis means that there is a higher reference level when the input voltage goes from a lower to higher value than when it goes from a higher to a lower value.

- The two reference levels are referred to as the upper trigger point (UTP) and the lower trigger point (LTP). This two-level hysteresis is established with a positive feedback arrangement, as shown in Figure 7–4.

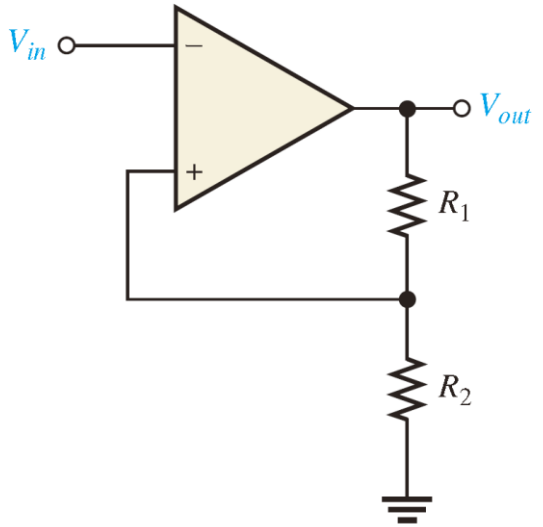
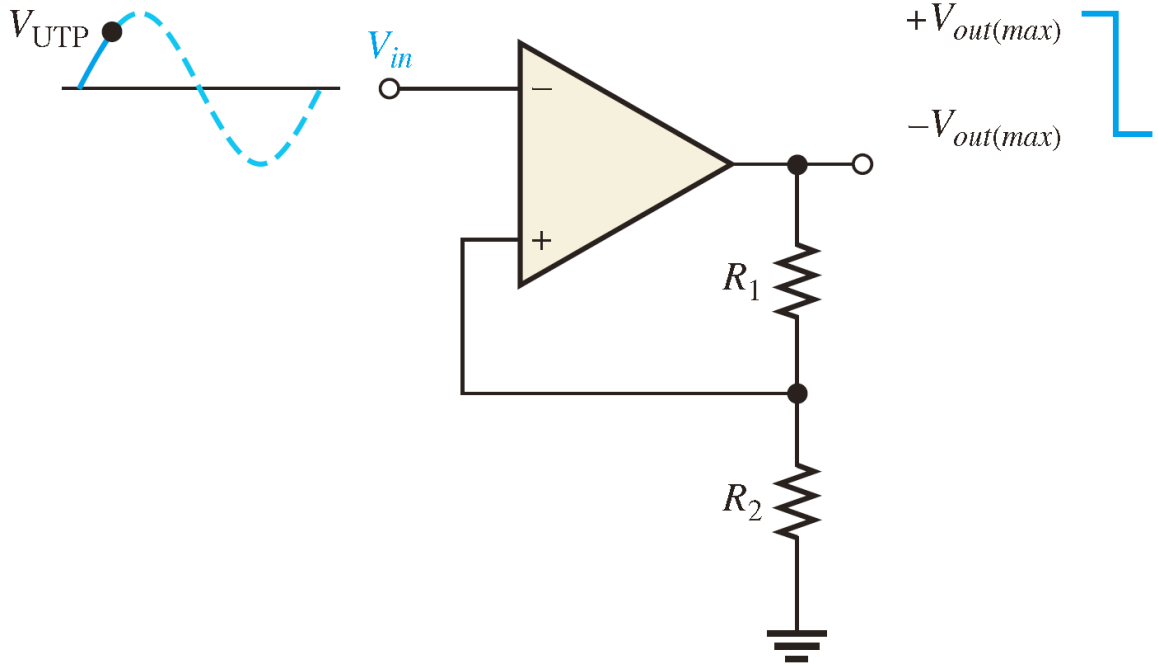


FIGURE 7-4 Comparator with positive feedback for hysteresis.

Hysteresis

- The basic operation of the comparator with hysteresis is illustrated in Figure 7–5.
- Assume that the output voltage is at its positive maximum, $+V_{out(max)}$. The voltage fed back to the noninverting input is V_{UTP} and is expressed as

$$V_{UTP} = \frac{R_2}{R_1 + R_2}(+V_{out(max)})$$



(a) When the output is at the maximum positive voltage and the input exceeds UTP, the output switches to the maximum negative voltage.

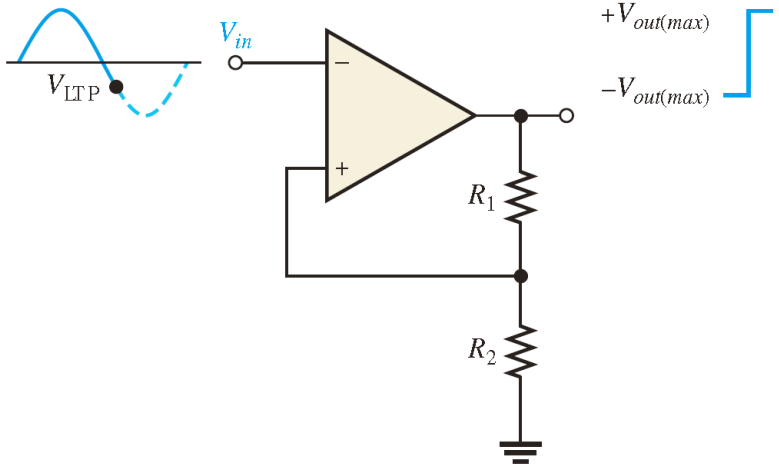
FIGURE 7-5 Operation of a comparator with hysteresis.

Hysteresis

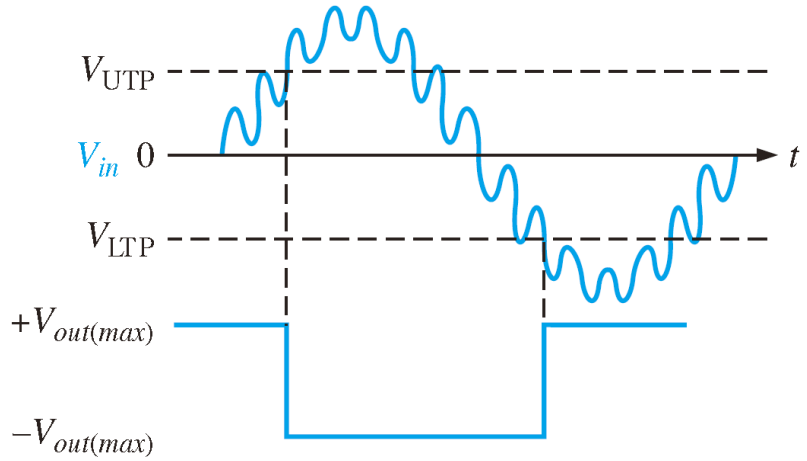
- When V_{in} exceeds V_{UTP}, the output voltage drops to its negative maximum, $-V_{out(max)}$, as shown in part (a). Now the voltage fed back to the noninverting input is V_{LTP} and is expressed as

$$V_{LTP} = \frac{R_2}{R_1 + R_2}(-V_{out(max)})$$

- The input voltage must now fall below V_{LTP}, as shown in part (b), before the device will switch from the maximum negative voltage back to the maximum positive voltage. This means that a small amount of noise voltage has no effect on the output.



(b) When the output is at the maximum negative voltage and the input goes below LTP, the output switches back to the maximum positive voltage.



(c) Device triggers only once when UTP or LTP is reached; thus, there is immunity to noise that is riding on the input signal.

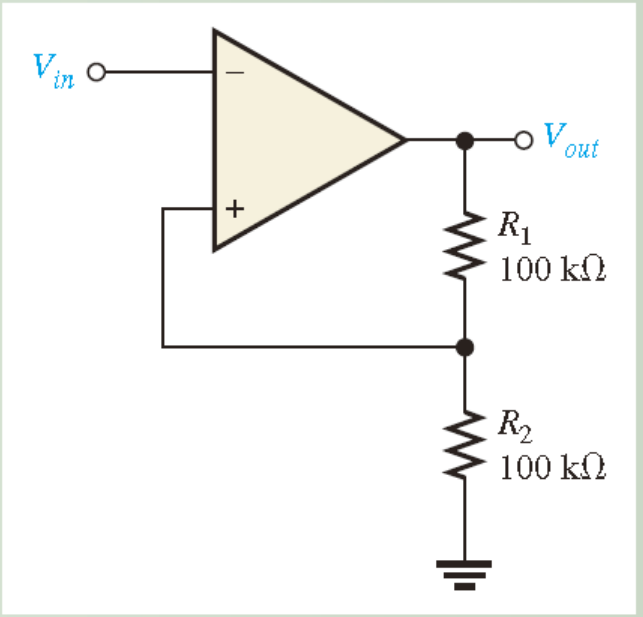
FIGURE 7-6 Operation of a comparator with hysteresis.

Example

EXAMPLE 13–2

Determine the upper and lower trigger points for the comparator circuit in Figure 13–9. Assume that $+V_{out(max)} = +5$ V and $-V_{out(max)} = -5$ V.

▶ FIGURE 13–9



Solution

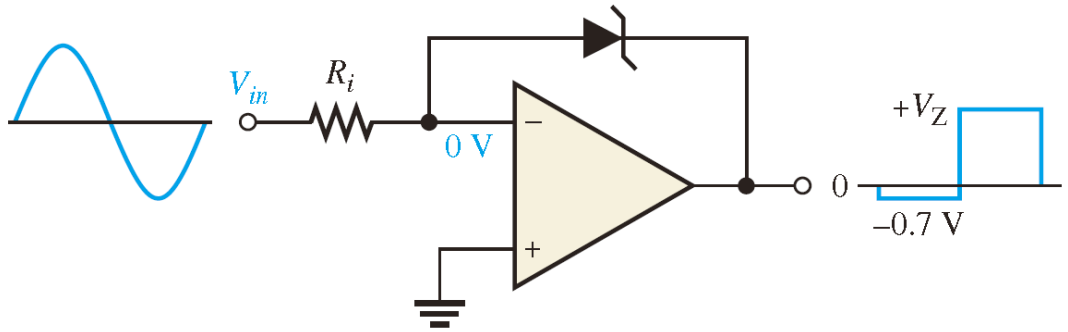
$$V_{UTP} = \frac{R_2}{R_1 + R_2}(+V_{out(max)}) = 0.5(5\text{ V}) = \mathbf{+2.5\text{ V}}$$

$$V_{LTP} = \frac{R_2}{R_1 + R_2}(-V_{out(max)}) = 0.5(-5\text{ V}) = \mathbf{-2.5\text{ V}}$$

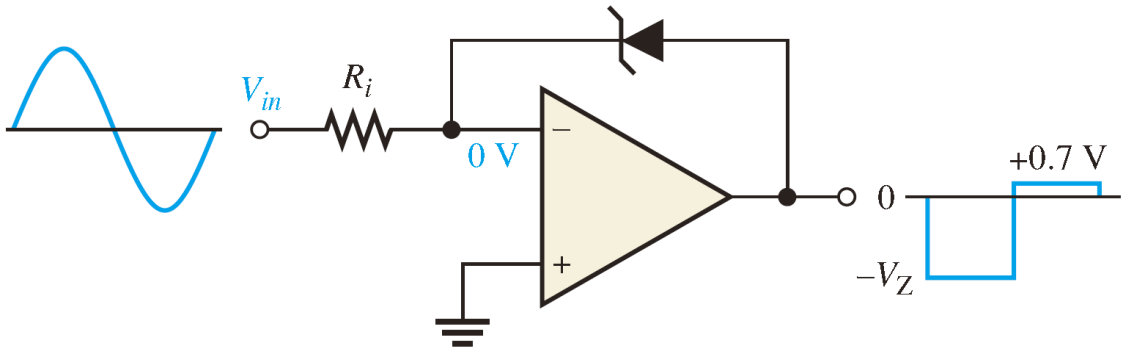
Output Bounding

- In some applications, it is necessary to limit the output voltage levels of a comparator to a value less than that provided by the saturated op-amp. A single zener diode can be used, as shown in Figure 13–10, to limit the output voltage to the zener voltage in one direction and to the forward diode voltage drop in the other. This process of limiting the output range is called bounding.

- When the output voltage reaches a positive value equal to the zener voltage, it limits at that value, as illustrated in Figure 7–7(a). When the output switches negative, the zener acts as a regular diode and becomes forward biased at 0.7 V, limiting the negative output voltage to this value, as shown in part (b). Turning the zener around limits the output voltage in the opposite direction.



(a) Bounded at a positive value



(b) Bounded at a negative value

FIGURE 7-7 Operation of a bounded comparator.

Output Bounding

- Two zener diodes arranged as in Figure 7–8 limit the output voltage to the zener voltage plus the forward voltage drop (0.7 V) of the forward-biased zener, both positively and negatively, as shown.

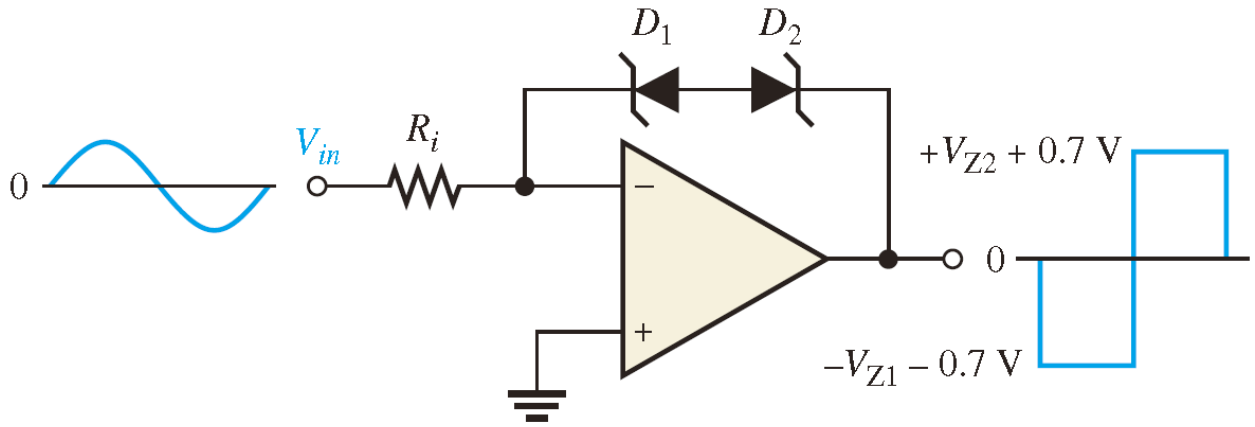
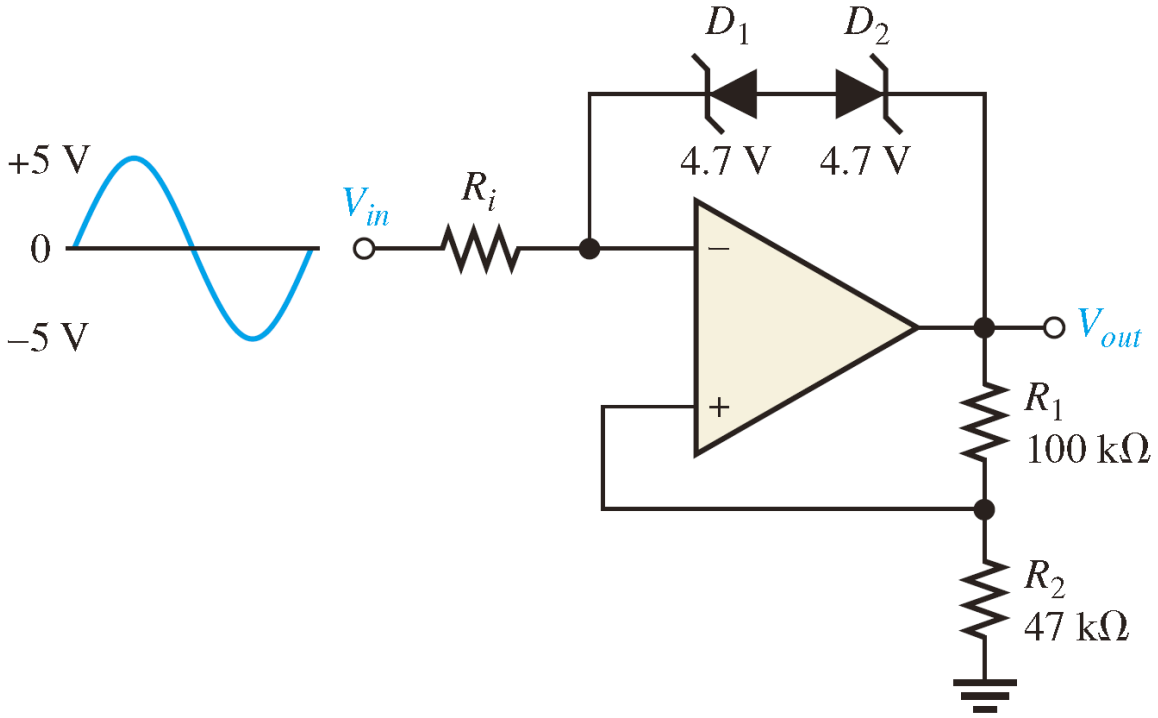


FIGURE 7-8 Operation of a bounded comparator.

Example

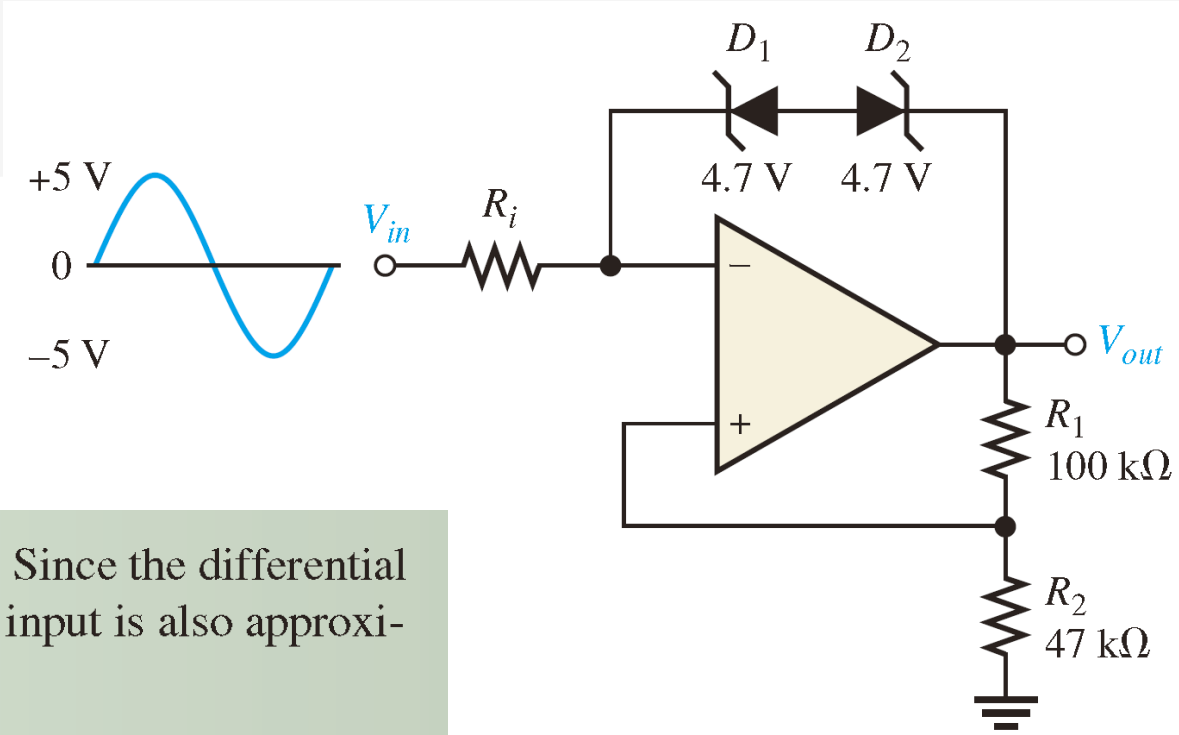
- Determine the output voltage waveform



Solution This comparator has both hysteresis and zener bounding. The voltage across D_1 and D_2 in either direction is 4.7 V + 0.7 V = 5.4 V. This is because one zener is always forward-biased with a drop of 0.7 V when the other one is in breakdown.

Example

- Determine the output voltage waveform



The voltage at the inverting (−) op-amp input is $V_{out} \pm 5.4$ V. Since the differential voltage is negligible, the voltage at the noninverting (+) op-amp input is also approximately $V_{out} \pm 5.4$ V. Thus,

$$V_{R1} = V_{out} - (V_{out} \pm 5.4\text{ V}) = \pm 5.4\text{ V}$$

$$I_{R1} = \frac{V_{R1}}{R_1} = \frac{\pm 5.4\text{ V}}{100\text{ k}\Omega} = \pm 54\ \mu\text{A}$$

Since the noninverting input current is negligible,

$$I_{R2} = I_{R1} = \pm 54\ \mu\text{A}$$

$$V_{R2} = R_2 I_{R2} = (47\text{ k}\Omega)(\pm 54\ \mu\text{A}) = \pm 2.54\text{ V}$$

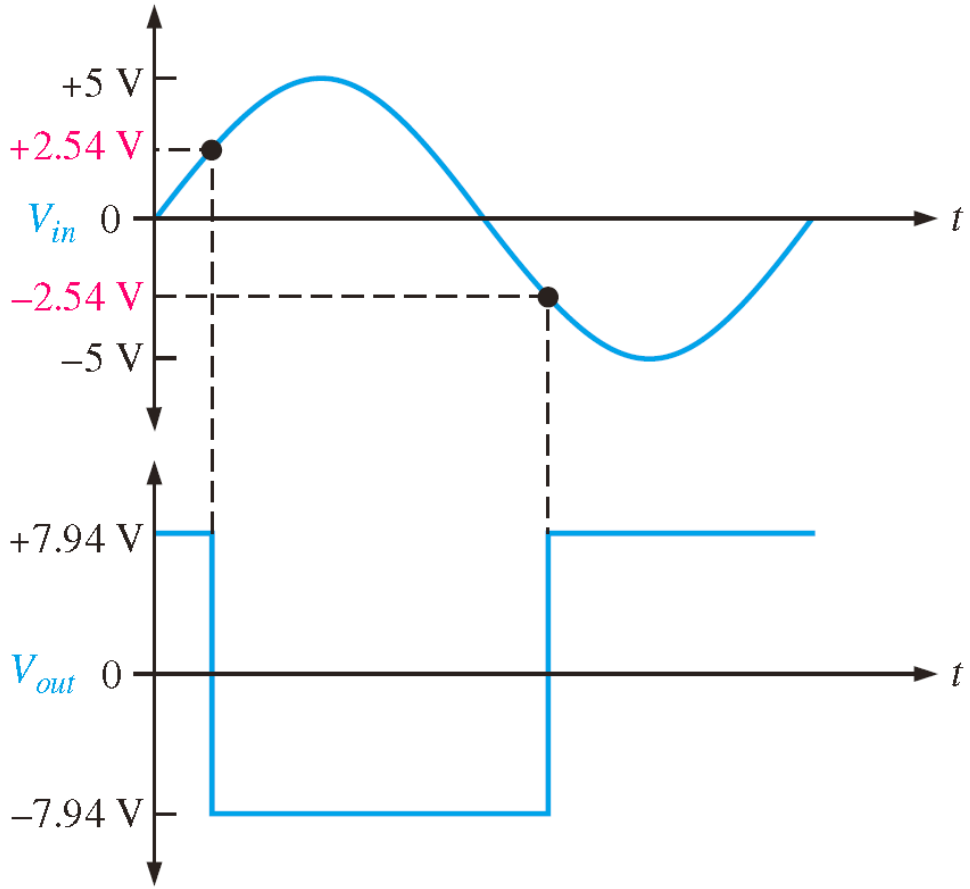
$$V_{out} = V_{R1} + V_{R2} = \pm 5.4\text{ V} \pm 2.54\text{ V} = \pm 7.94\text{ V}$$

Example

The upper trigger point (UTP) and the lower trigger point (LTP) are as follows:

$$V_{\text{UTP}} = \left(\frac{R_2}{R_1 + R_2}\right)(+V_{out}) = \left(\frac{47\ \text{k}\Omega}{147\ \text{k}\Omega}\right)(+7.94\ \text{V}) = +2.54\ \text{V}$$

$$V_{\text{LTP}} = \left(\frac{R_2}{R_1 + R_2}\right)(-V_{out}) = \left(\frac{47\ \text{k}\Omega}{147\ \text{k}\Omega}\right)(-7.94\ \text{V}) = -2.54\ \text{V}$$



7-2 Summing Amplifiers

- **Summing Amplifier with Unity Gain**
  - A **summing amplifier** has two or more inputs, and its output voltage is proportional to the negative of the algebraic sum of its input voltages.

- A two-input summing amplifier is shown in Figure 7–9, but any number of inputs can be used.
- Using the concepts of infinite input impedance and virtual ground, you can determine that the inverting (-) input of the op-amp is approximately 0 V and has no current through it.

$$I_T = I_1 + I_2$$

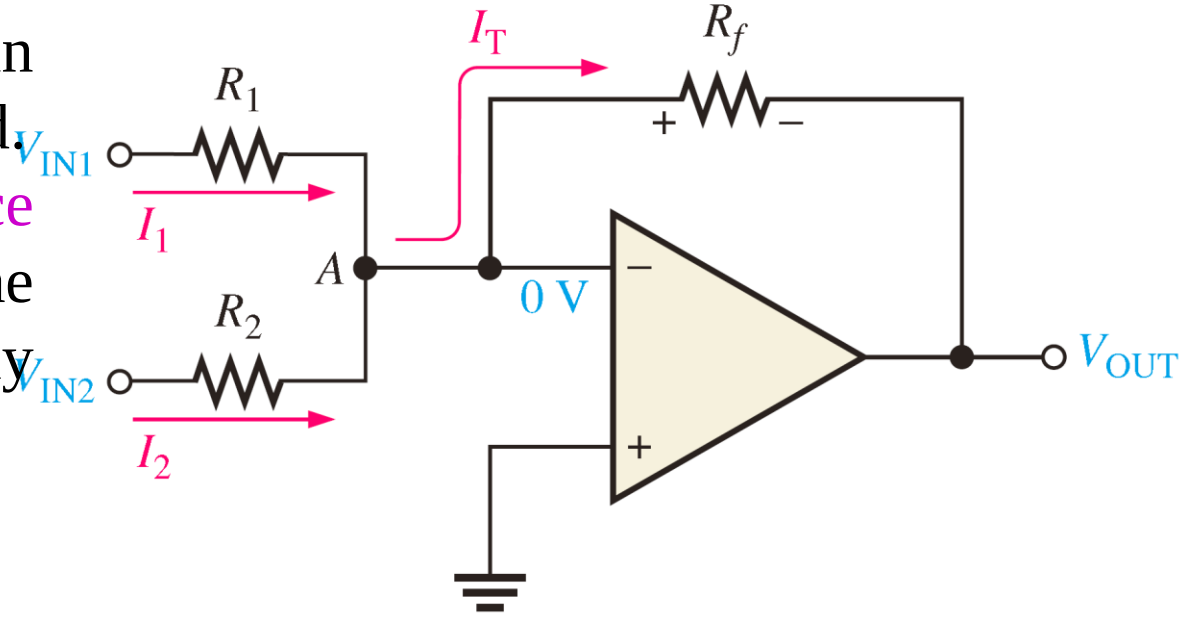


FIGURE 7-9 Two-input inverting summing amplifier.

Summing Amplifiers

$$I_T = I_1 + I_2$$

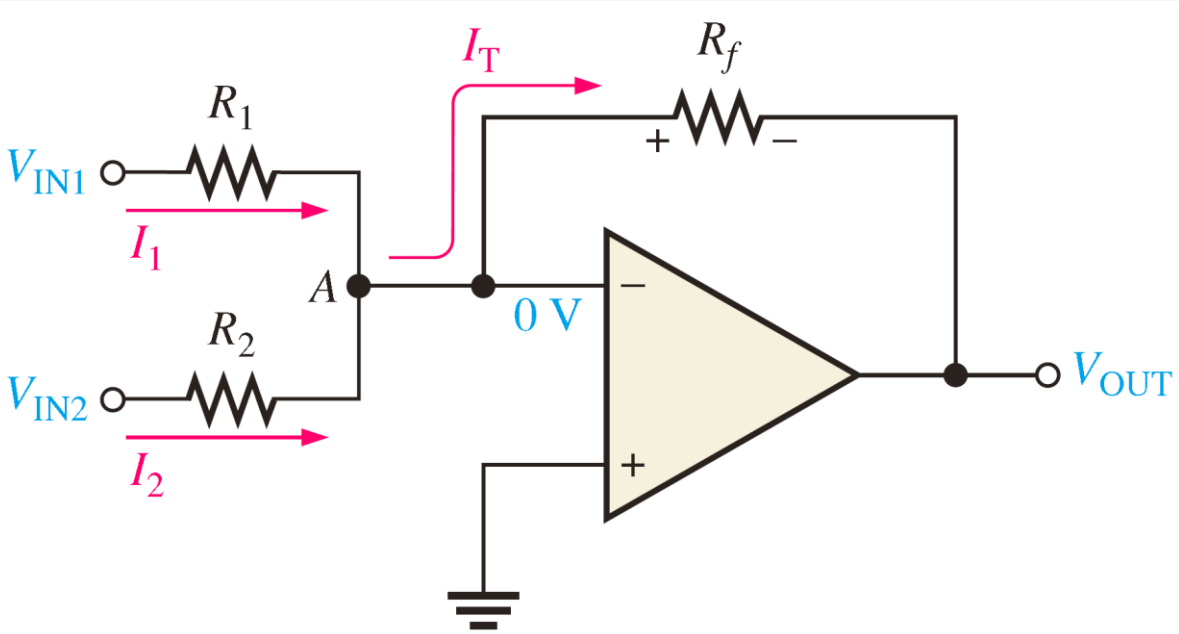


FIGURE 7-9 Two-input inverting summing amplifier.

Since $V_{OUT} = -I_T R_f$, the following steps apply:

$$V_{OUT} = -(I_1 + I_2)R_f = -\left(\frac{V_{IN1}}{R_1} + \frac{V_{IN2}}{R_2}\right)R_f$$

If all three of the resistors are equal ($R_1 = R_2 = R_f = R$), then

$$V_{OUT} = -\left(\frac{V_{IN1}}{R} + \frac{V_{IN2}}{R}\right)R = -(V_{IN1} + V_{IN2})$$

Summing Amplifiers

- A general expression is given for a unity-gain summing amplifier with *n* inputs, as shown in Figure 7–10 where all resistors are equal in value.

$$V_{OUT} = -(V_{IN1} + V_{IN2} + V_{IN3} + \cdots + V_{INn})$$

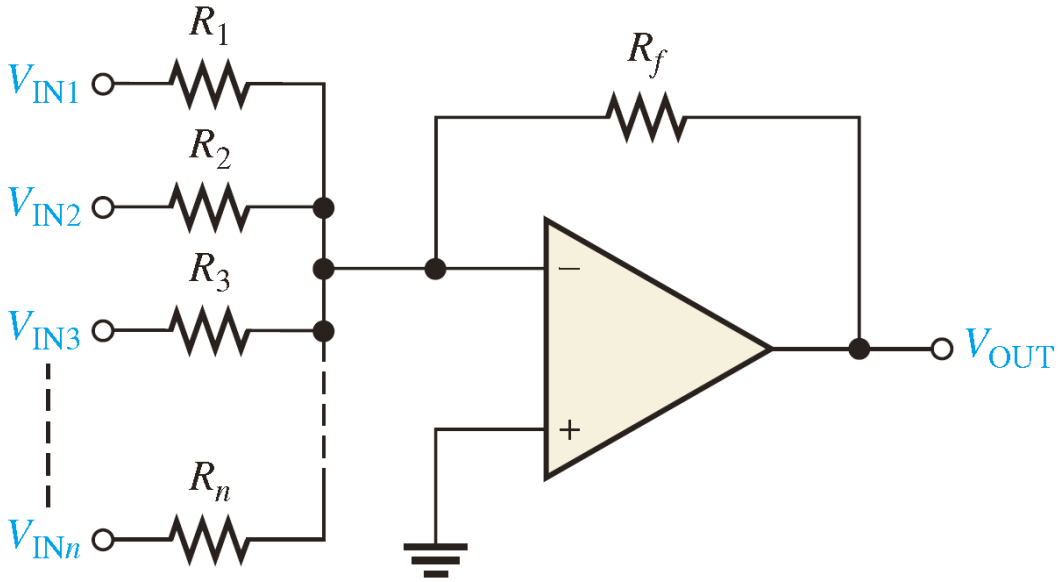
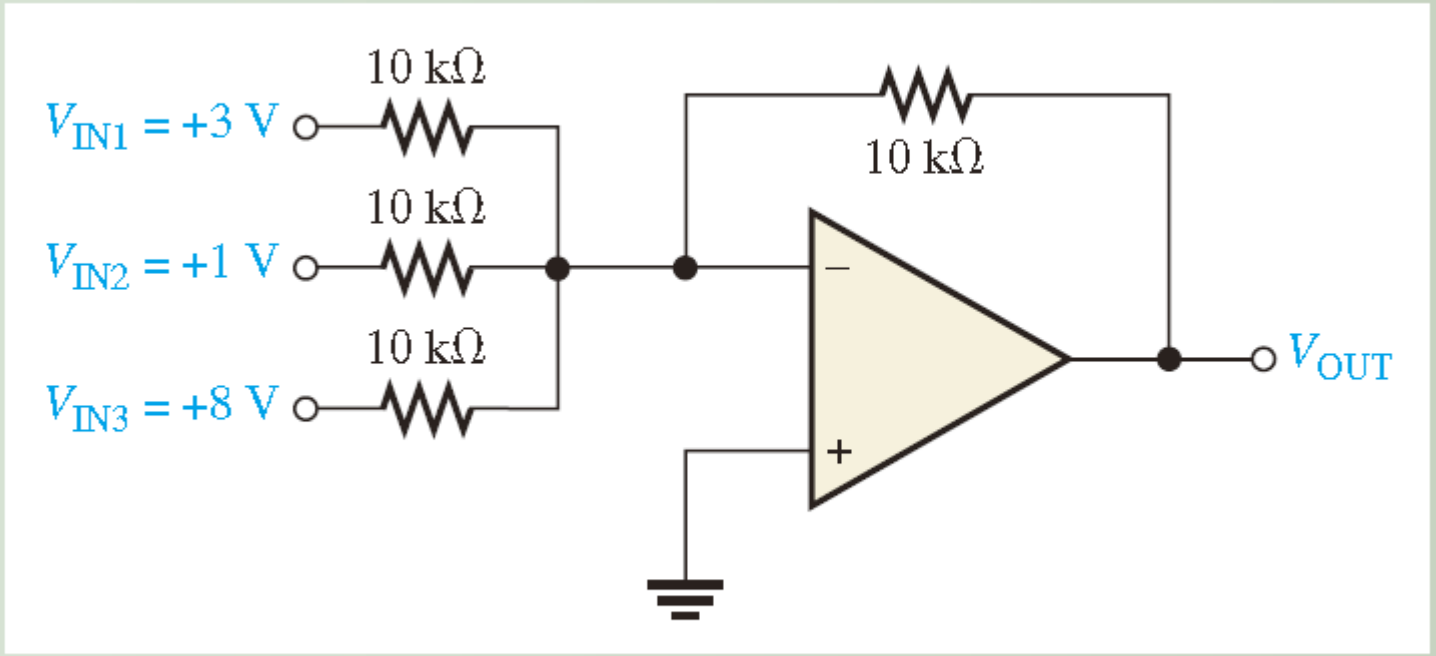


FIGURE 7-10 Summing amplifier with *n* inputs. All resistors have the same value.

Example

Determine the output voltage in Figure 13–22.

▶ FIGURE 13–22



Solution

$$V_{OUT} = -(V_{IN1} + V_{IN2} + V_{IN3}) = -(3\text{ V} + 1\text{ V} + 8\text{ V}) = \mathbf{-12\text{ V}}$$

Summing Amplifier with Gain Other Than Unity

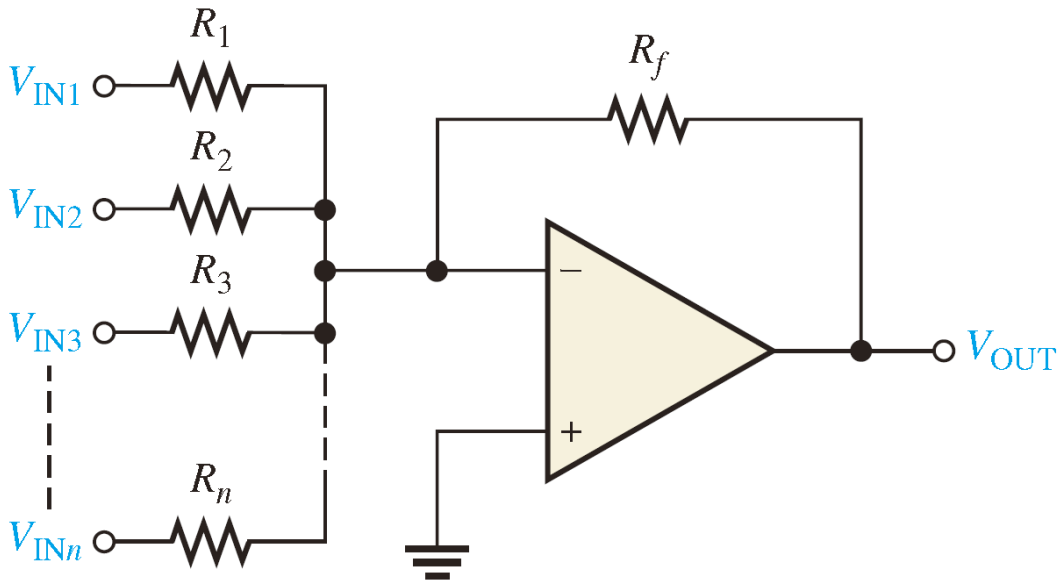


FIGURE 7-10 Summing amplifier with *n* inputs.

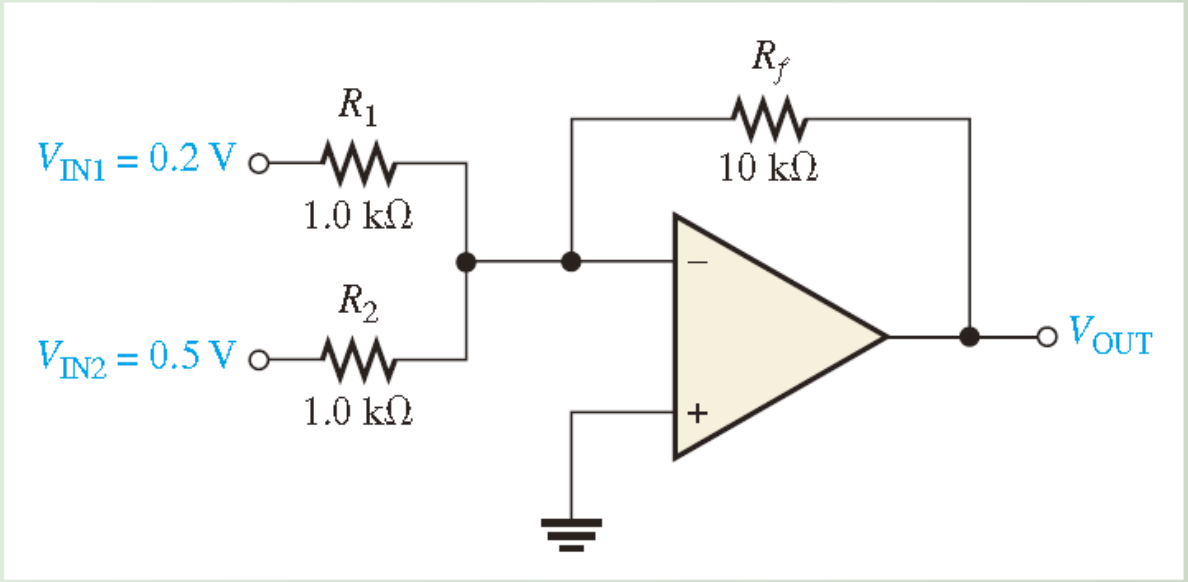
When R_f is different from the input resistors, the amplifier has a gain of R_f/R, where R is the value of each equal-value input resistor. The general expression for the output is

$$V_{OUT} = -\frac{R_f}{R}(V_{IN1} + V_{IN2} + \cdots + V_{INn})$$

As you can see, the output voltage has the same magnitude as the sum of all the input voltages multiplied by a constant determined by the ratio $-(R_f/R)$. The gain can be greater or less than unity, depending on the ratio of R_f/R.

Example

Determine the output voltage for the summing amplifier in Figure 13–23.



Solution $R_f = 10\,\text{k}\Omega$ and $R = R_1 = R_2 = 1.0\,\text{k}\Omega$. Therefore,

$$V_{OUT} = -\frac{R_f}{R}(V_{IN1} + V_{IN2}) = -\frac{10\,\text{k}\Omega}{1.0\,\text{k}\Omega}(0.2\,\text{V} + 0.5\,\text{V}) = -10(0.7\,\text{V}) = \mathbf{-7\,V}$$

Averaging Amplifier

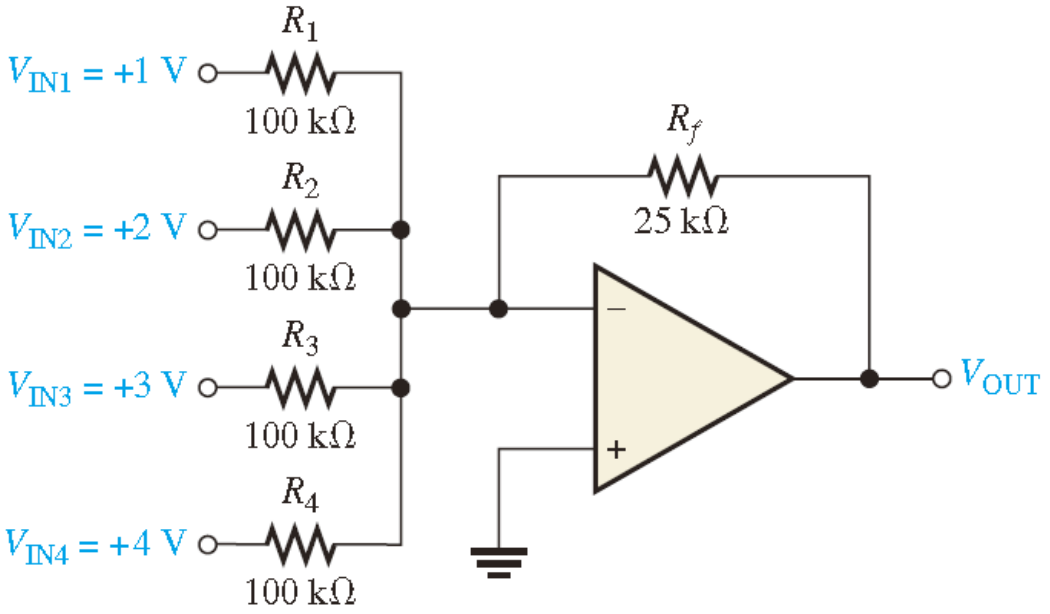
Averaging Amplifier

A summing amplifier can be made to produce the mathematical average of the input voltages. This is done by setting the ratio R_f/R equal to the reciprocal of the number of inputs (n).

$$\frac{R_f}{R} = \frac{1}{n}$$

Example

Show that the amplifier in Figure 13–24 produces an output whose magnitude is the mathematical average of the input voltages.



Solution Since the input resistors are equal, $R = 100\ \text{k}\Omega$. The output voltage is

$$V_{OUT} = -\frac{R_f}{R}(V_{IN1} + V_{IN2} + V_{IN3} + V_{IN4})$$

$$= -\frac{25\ \text{k}\Omega}{100\ \text{k}\Omega}(1\ \text{V} + 2\ \text{V} + 3\ \text{V} + 4\ \text{V}) = -\frac{1}{4}(10\ \text{V}) = \mathbf{-2.5\ V}$$

Scaling Adder

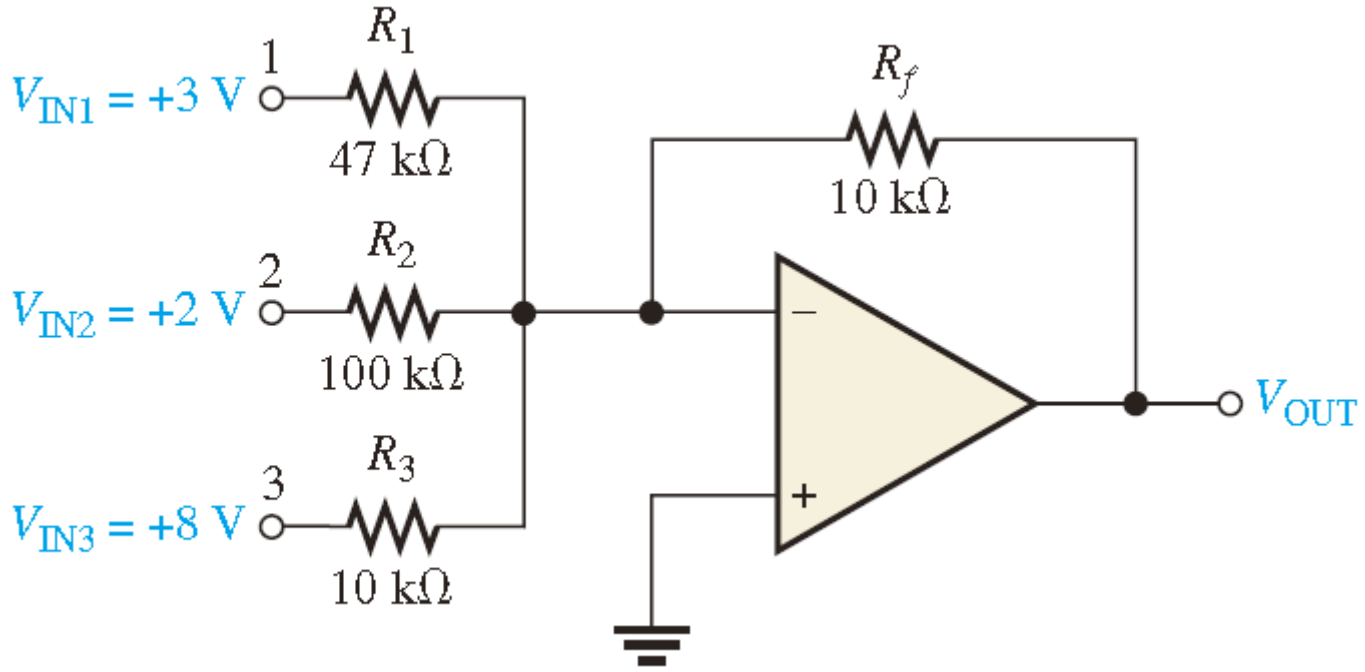
A different weight can be assigned to each input of a summing amplifier by simply adjusting the values of the input resistors. As you have seen, the output voltage can be expressed as

$$V_{OUT} = -\left(\frac{R_f}{R_1}V_{IN1} + \frac{R_f}{R_2}V_{IN2} + \cdots + \frac{R_f}{R_n}V_{INn}\right)$$

The weight of a particular input is set by the ratio of R_f to the resistance, R_x, for that input ($R_x = R_1, R_2, \ldots R_n$). For example, if an input voltage is to have a weight of 1, then $R_x = R_f$. Or, if a weight of 0.5 is required, $R_x = 2R_f$. The smaller the value of input resistance R_x, the greater the weight, and vice versa.

Example

Determine the weight of each input voltage for the scaling adder in Figure 13–25 and find the output voltage.



Example

Solution

Weight of input 1: $\frac{R_f}{R_1} = \frac{10\,\text{k}\Omega}{47\,\text{k}\Omega} = \mathbf{0.213}$

Weight of input 2: $\frac{R_f}{R_2} = \frac{10\,\text{k}\Omega}{100\,\text{k}\Omega} = \mathbf{0.100}$

Weight of input 3: $\frac{R_f}{R_3} = \frac{10\,\text{k}\Omega}{10\,\text{k}\Omega} = \mathbf{1.00}$

The output voltage is

$$V_{\text{OUT}} = -\left(\frac{R_f}{R_1}V_{\text{IN1}} + \frac{R_f}{R_2}V_{\text{IN2}} + \frac{R_f}{R_3}V_{\text{IN3}}\right)$$

$$= -[0.213(3\text{ V}) + 0.100(2\text{ V}) + 1.00(8\text{ V})]$$

$$= -(0.639\text{ V} + 0.2\text{ V} + 8\text{ V}) = \mathbf{-8.84\text{ V}}$$

7-3 Integrators and Differentiators

- **The Op-Amp Integrator**

- The Ideal Integrator An ideal integrator is shown in Figure 7–11. Notice that the feedback element is a capacitor that forms an *RC* circuit with the input resistor.
- **How a Capacitor Charges** To understand how an integrator works, it is important to review how a capacitor charges. Recall that the charge Q on a capacitor is proportional to the charging current (I_C) and the time (t).

$$Q = I_C t$$

- Also, in terms of the voltage, the charge on a capacitor is

$$Q = CV_C$$

- From these two relationships, the capacitor voltage can be expressed as

$$V_C = \left(\frac{I_C}{C}\right)t$$

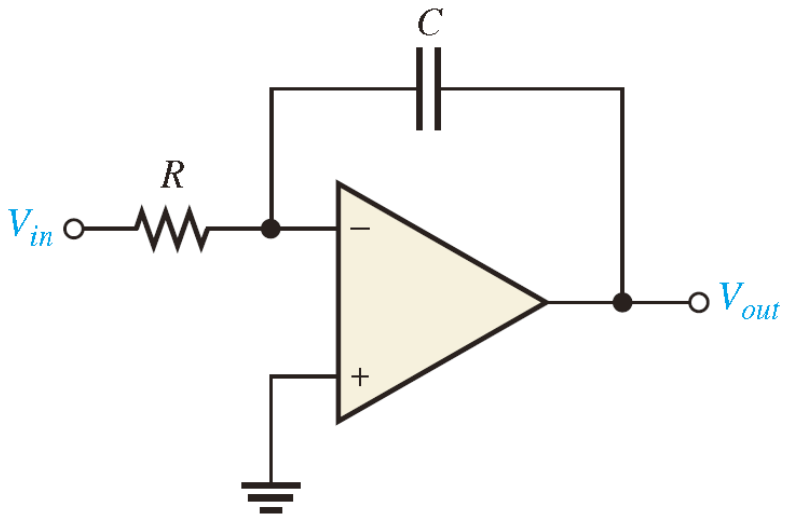


FIGURE 7-11 An ideal op-amp integrator.

Integrators

- Recall that the capacitor voltage in a simple *RC* circuit with a constant input voltage is not linear but is exponential. This is because the charging current continuously decreases as the capacitor charges and causes the rate of change of the voltage to continuously decrease.
- The key thing about using an op-amp with an *RC* circuit to form an integrator is that if the capacitor's charging current is made constant, the output will be a straight-line (linear) voltage rather than an exponential voltage.
- In Figure 7–12, the inverting input of the op-amp is at virtual ground (0 V), so the voltage across R_i equals V_{in}. Therefore, the input current is

$$I_{in} = \frac{V_{in}}{R_i}$$

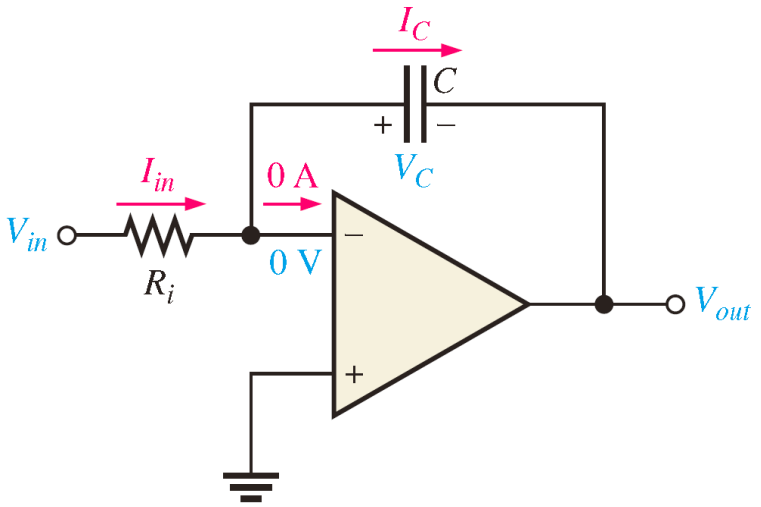


FIGURE 7-12 Currents in an integrator.

Integrators

- If V_{in} is a constant voltage, then I_{in} is also a constant because the inverting input always remains at 0 V, keeping a constant voltage across R_i.
- Because of the very high input impedance of the op-amp, there is negligible current at the inverting input. This makes the constant input current charge the capacitor, as indicated in Figure 7–12

$$I_{in} = \frac{V_{in}}{R_i} \qquad I_C = I_{in}$$

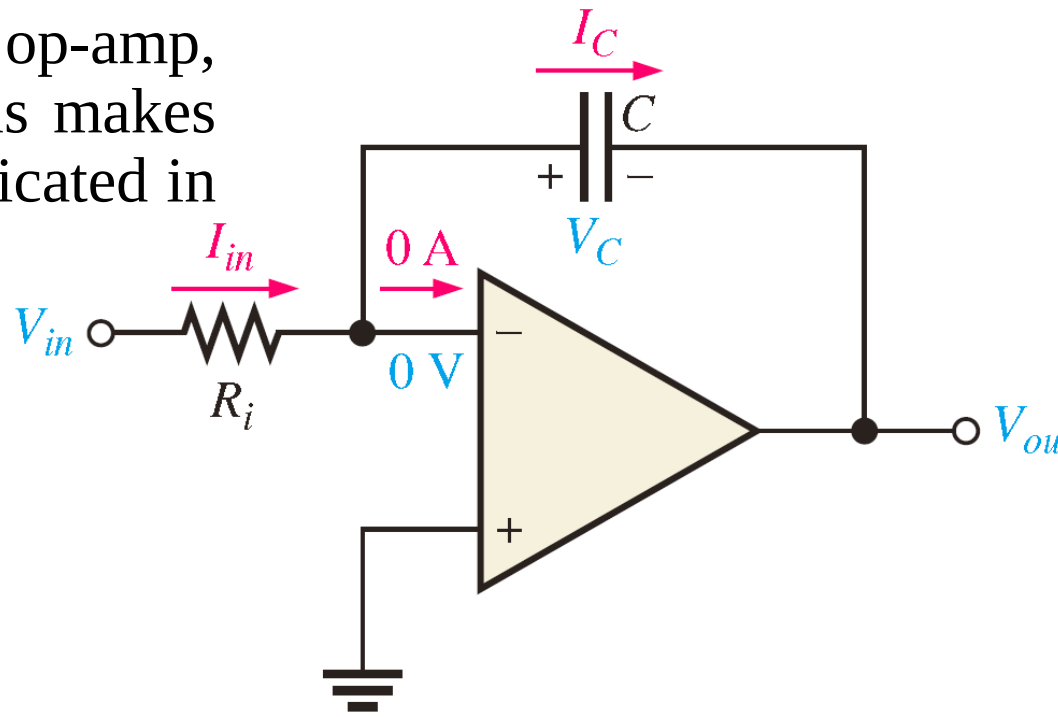


FIGURE 7-12 Currents in an integrator.

Integrators

- **The Capacitor Voltage**
- Since I_{in} is constant, so is I_C. The constant I_C charges the capacitor linearly and produces a linear voltage across C. The positive side of the capacitor is held at 0 V by the virtual ground of the op-amp. The voltage on the negative side of the capacitor, which is the op-amp output voltage, decreases linearly from zero as the capacitor charges, as shown in Figure 7–13. This voltage, V_C, is called a negative ramp and is the consequence of a constant positive input.

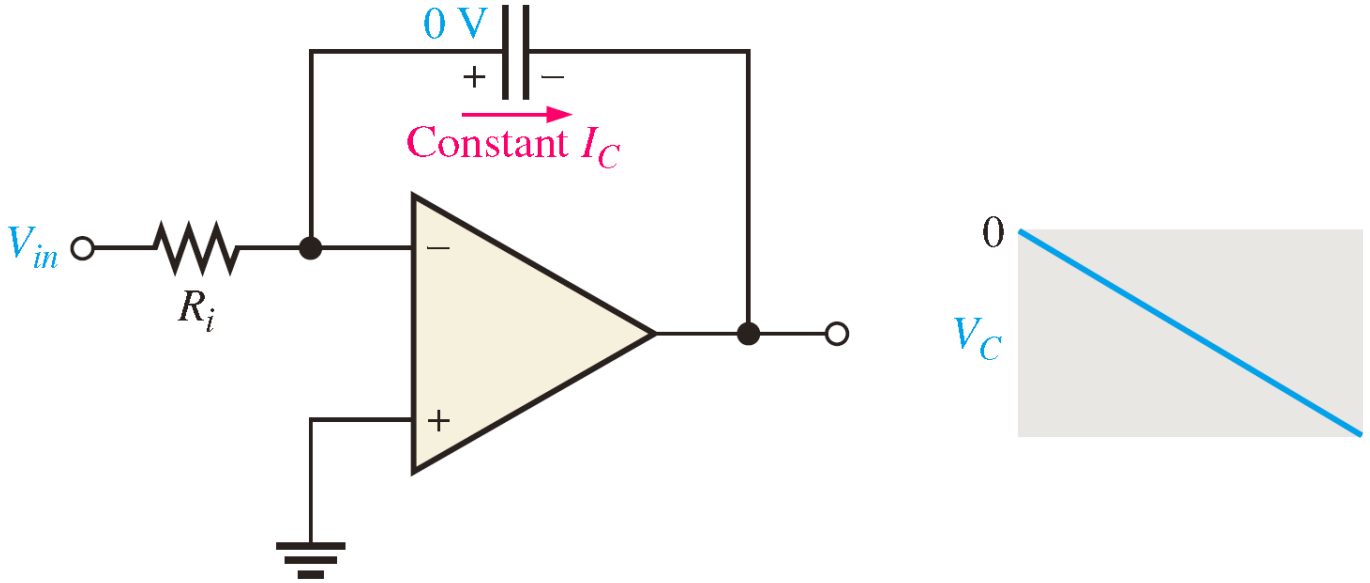


FIGURE 7-13 A linear ramp voltage is produced across the capacitor by the constant charging current.

Integrators

- **The Output voltage**
- V_{out} is the same as the voltage on the negative side of the capacitor. When a constant positive input voltage in the form of a step or pulse (a pulse has a constant amplitude when high) is applied, the output ramp decreases negatively until the op-amp saturates at its maximum negative level.

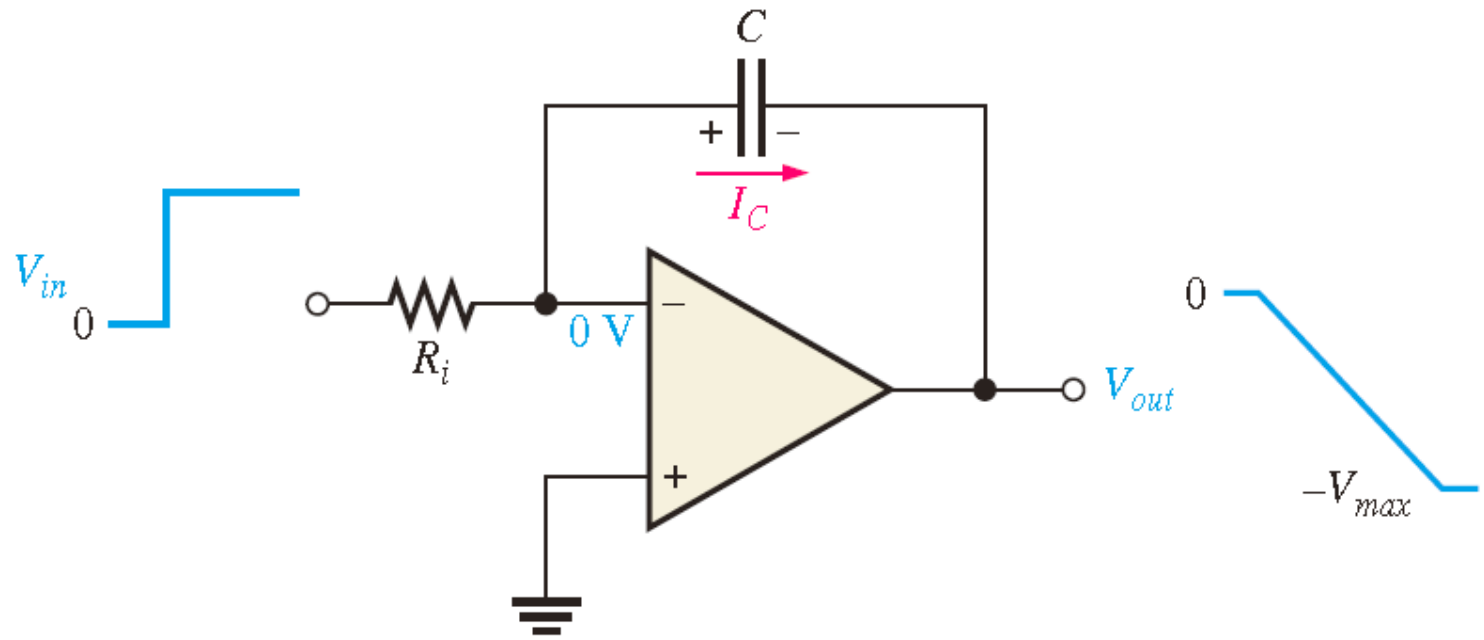


FIGURE 7-13 A constant input voltage produces a ramp on the output of the integrator.

Rate of Change of the Output Voltage

Rate of Change of the Output Voltage The rate at which the capacitor charges, and therefore the slope of the output ramp, is set by the ratio I_C/C, as you have seen. Since $I_C = V_{in}/R_i$, the rate of change or slope of the integrator's output voltage is $\Delta V_{out}/\Delta t$.

$$\frac{\Delta V_{out}}{\Delta t} = -\frac{V_{in}}{R_i C}$$

The Practical Integrator

- In a practical integrator, any dc error voltage due to offset error will cause the output to produce a ramp that moves toward either positive or negative saturation (depending on the offset), even when no signal is present.

- The simplest effective solution of overcoming the effects of offset and bias current is to use a resistor in parallel with the capacitor in the feedback path, as shown in Figure 7–14. The feedback resistor, R_f, should be large compared to the input resistor R_{in}, in order to have a negligible effect on the output waveform.

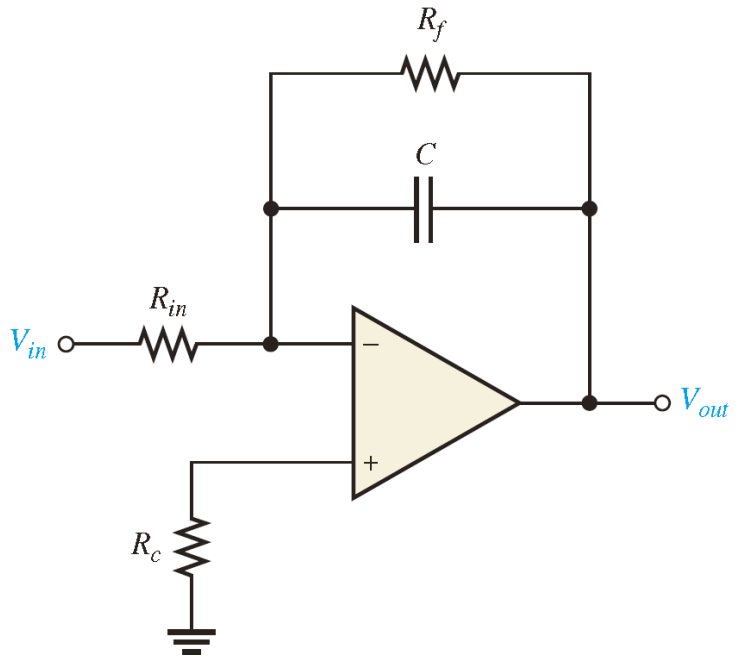


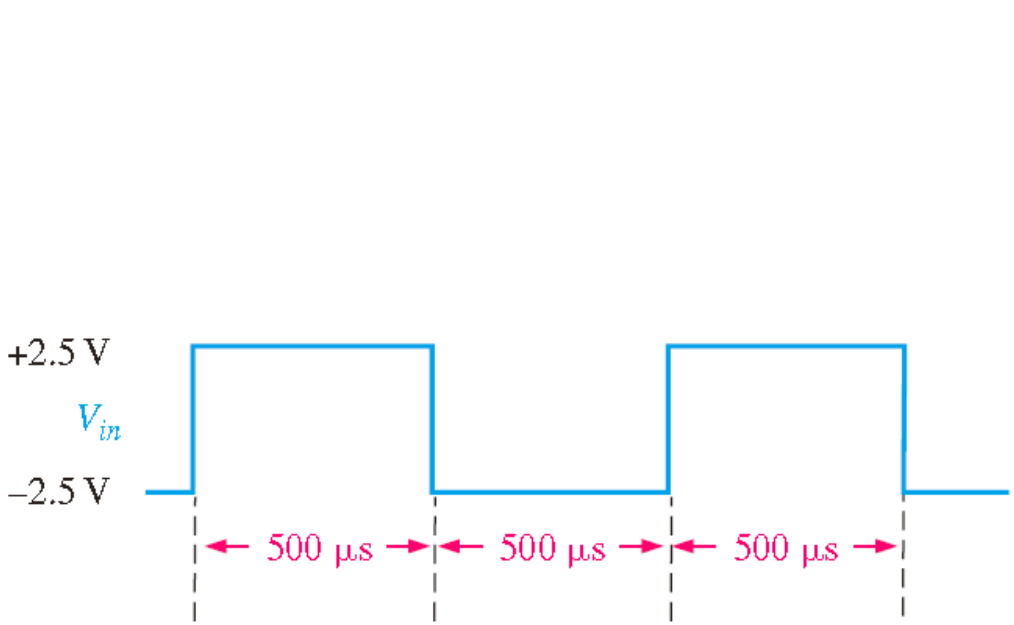
FIGURE 7-14 Practical Integrator.

Example

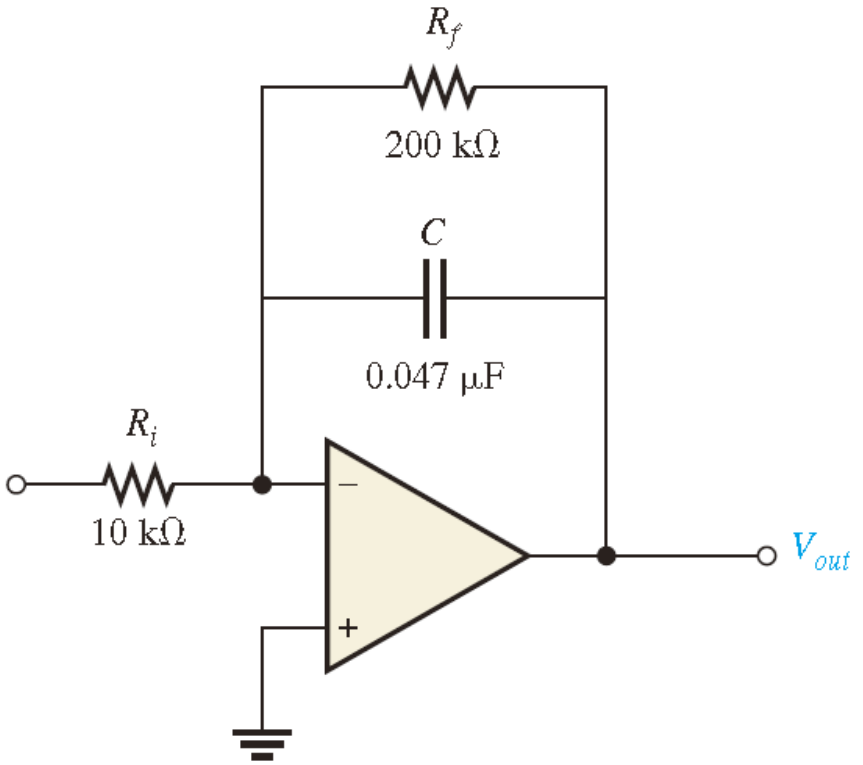
MPLE 13–10

(a) Determine the rate of change of the output voltage in response to the input square wave, as shown for the practical integrator in Figure 13–36(a). Assume steady state conditions have been reached. The input is a 1.0 kHz, 5 V_{pp} square wave centered at 0 V.

(b) Draw the output waveform.



(a)



Example

Solution (a) The rate of change of the output voltage during the time that the input is at +2.5 V (capacitor charging) is

$$\frac{\Delta V_{out}}{\Delta t} = -\frac{V_{in}}{R_i C} = -\frac{2.5\text{ V}}{(10\text{ k}\Omega)(0.047\ \mu\text{F})} = -5.32\text{ kV/s} = \mathbf{-5.32\ mV/\mu s}$$

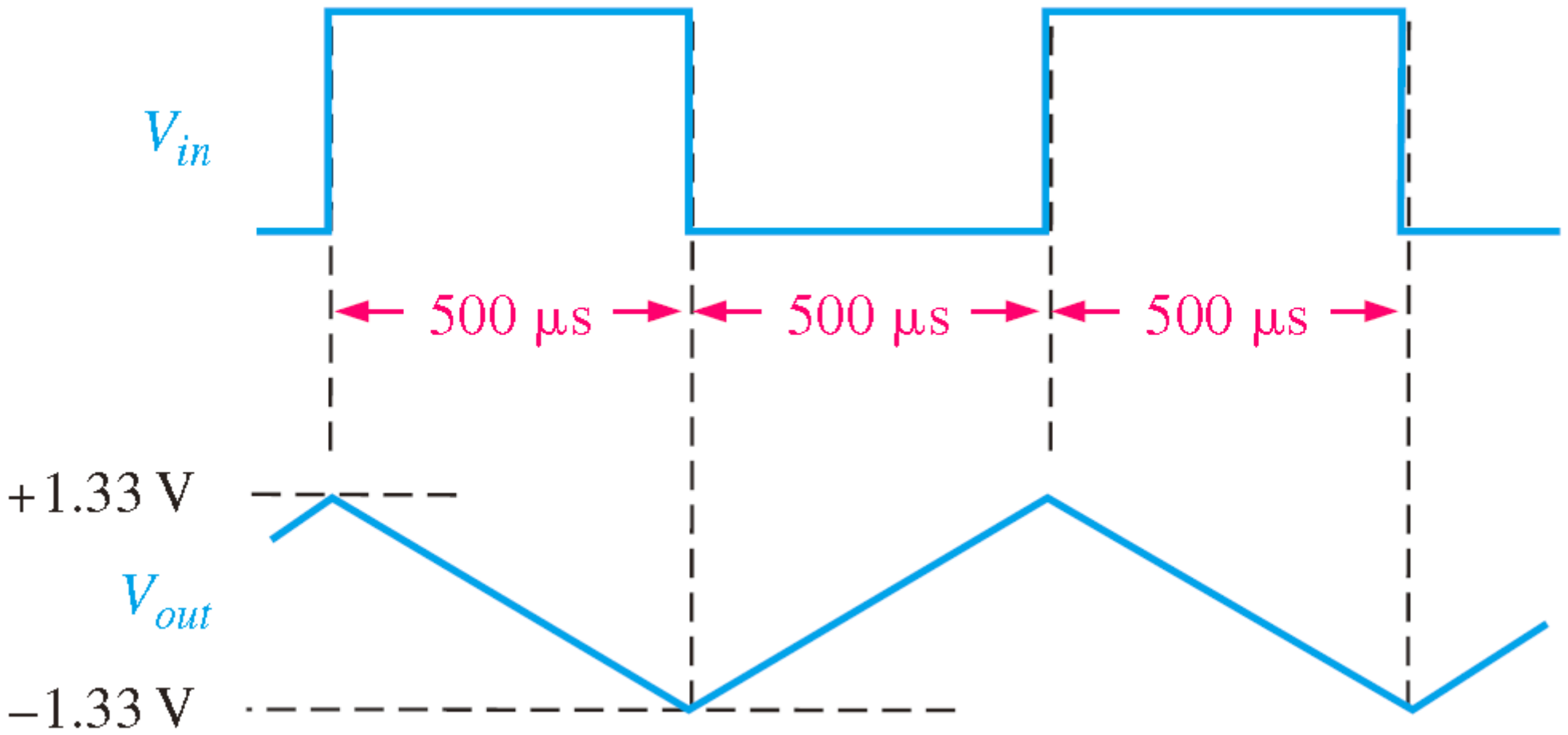
(b) In 500 μs (the time the pulse is high), the output changes by

$$\Delta V_{out} = (-5.32\text{ mV/}\mu\text{s})(500\ \mu\text{s}) = -2.66\ V$$

Because the output has had time to reach steady state conditions, it is centered on 0 V and thus goes from +1.33 V to −1.33 V.

The time that the input is −2.5 V is also 500 µs and the charging rate is the same as before but of opposite sign. Therefore, the ΔV_{out} = +2.66 V. The output will go from −1.33 V to +1.33 V as shown in Figure 13-36(b).

Example



The Op-Amp Differentiator

- ***The Ideal Differentiator*** An ideal differentiator is shown in Figure 7–15. Notice how the placement of the capacitor and resistor differ from the integrator. The capacitor is now the input element, and the resistor is the feedback element. A differentiator produces an output that is proportional to the rate of change of the input voltage.

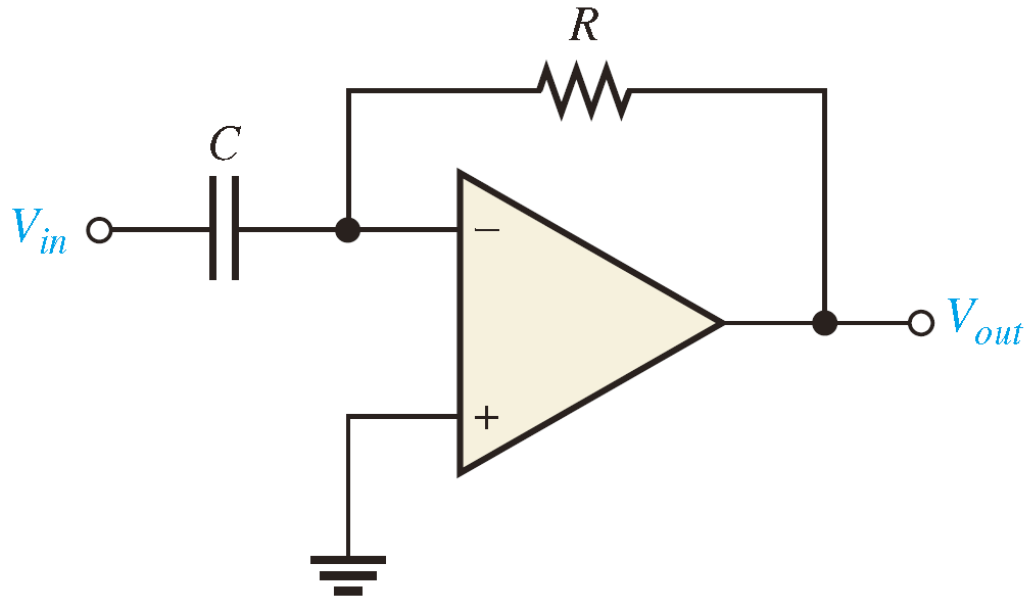


FIGURE 7-15 An ideal op-amp differentiator.

The Op-Amp Differentiator

- Apply a positive-going ramp voltage to the input as indicated in Figure 7–16. In this case, $I_C = I_{in}$ and the voltage across the capacitor is equal to V_{in} at all times ($V_C = V_{in}$) because of virtual ground on the inverting input.

From the basic formula, $V_C = (I_C/C)t$, the capacitor current is

$$I_C = \left(\frac{V_C}{t}\right)C$$

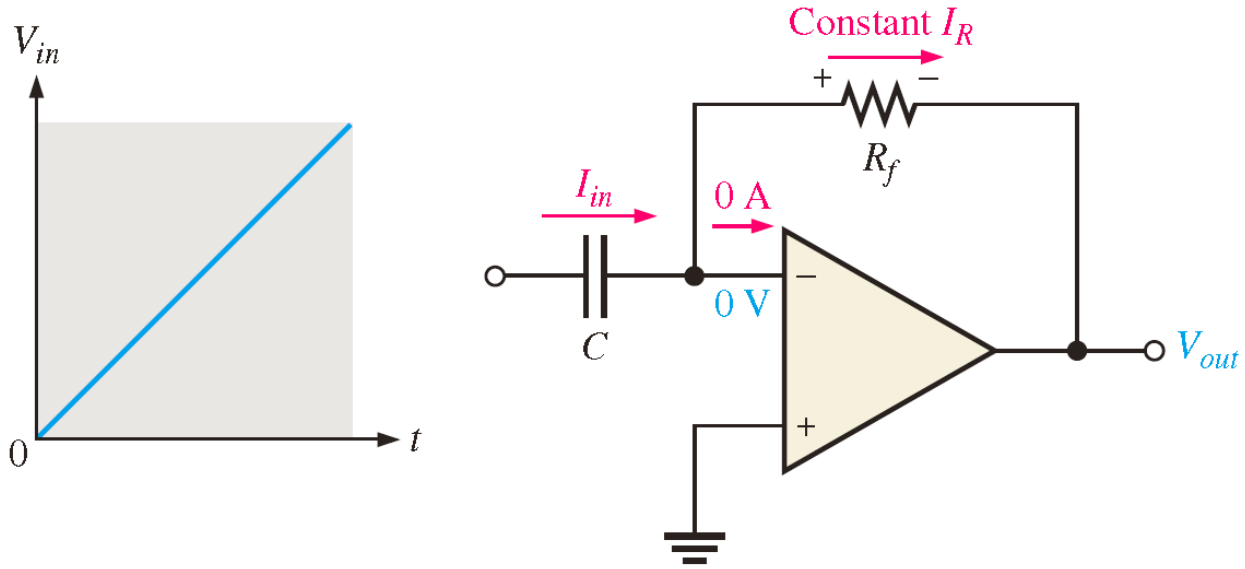


FIGURE 7-16 A differentiator with a ramp input.

The Op-Amp Differentiator

- Since the current at the inverting input is negligible, $I_R = I_C$. Both currents are constant because the slope of the capacitor voltage (V_C/t) is constant. The output voltage is also constant and equal to the voltage across R_f because one side of the feedback resistor is always 0 V (virtual ground).

$$V_{out} = -\left(\frac{V_C}{t}\right)R_f C$$

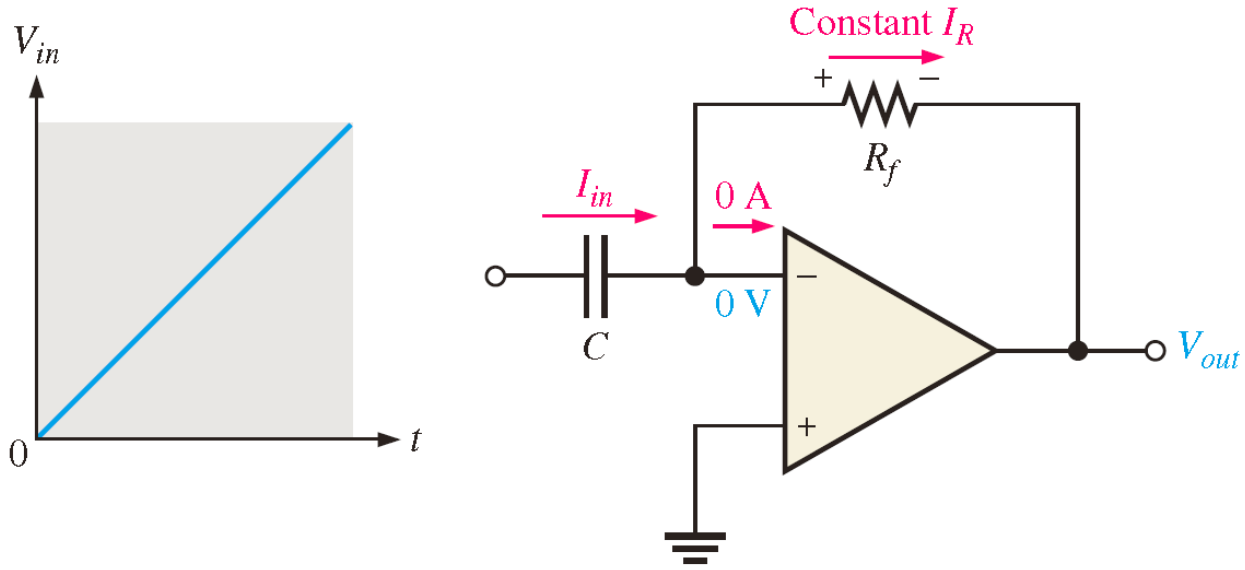


FIGURE 7-16 A differentiator with a ramp input.

The Op-Amp Differentiator

- The output is negative when the input is a positive-going ramp and positive when the input is a negative-going ramp, as illustrated in Figure 7–17. During the positive slope of the input, the capacitor is charging from the input source and the constant current through the feedback resistor is in the direction shown. During the negative slope of the input, the current is in the opposite direction because the capacitor is discharging.

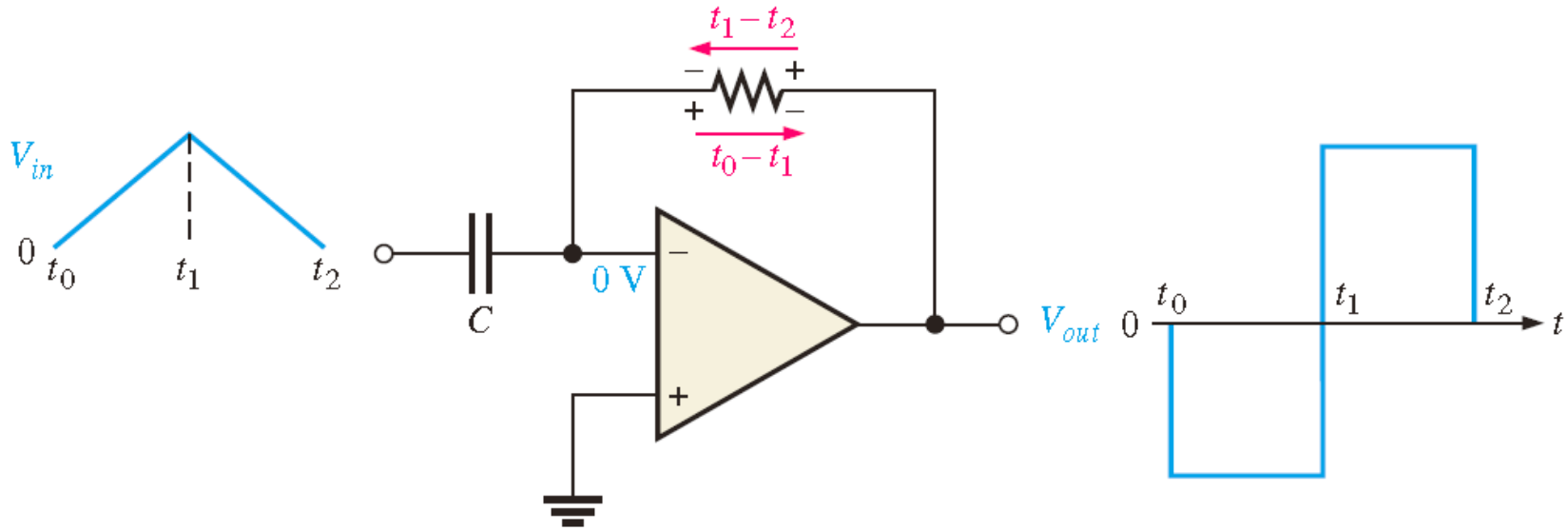


FIGURE 7-17 Output of a differentiator with a series of positive and negative ramps (triangle wave) on the input.

The Practical Differentiator

- Because The capacitor of ideal differentiator has very low impedance at high frequencies, the combination of R_f and C form a very high gain amplifier at high frequencies.
- This means that a differentiator circuit tends to be noisy because electrical noise mainly consists of high frequencies. The solution to this problem is simply to add a resistor, R_{in}, in series with the capacitor to act as a low-pass filter and reduce the gain at high frequencies.

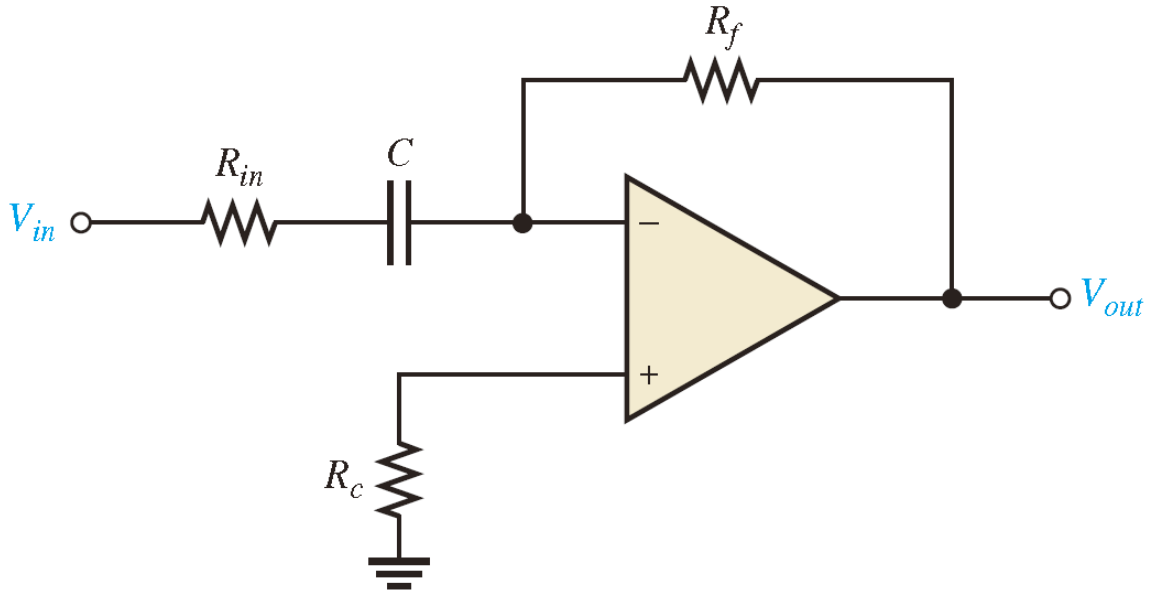
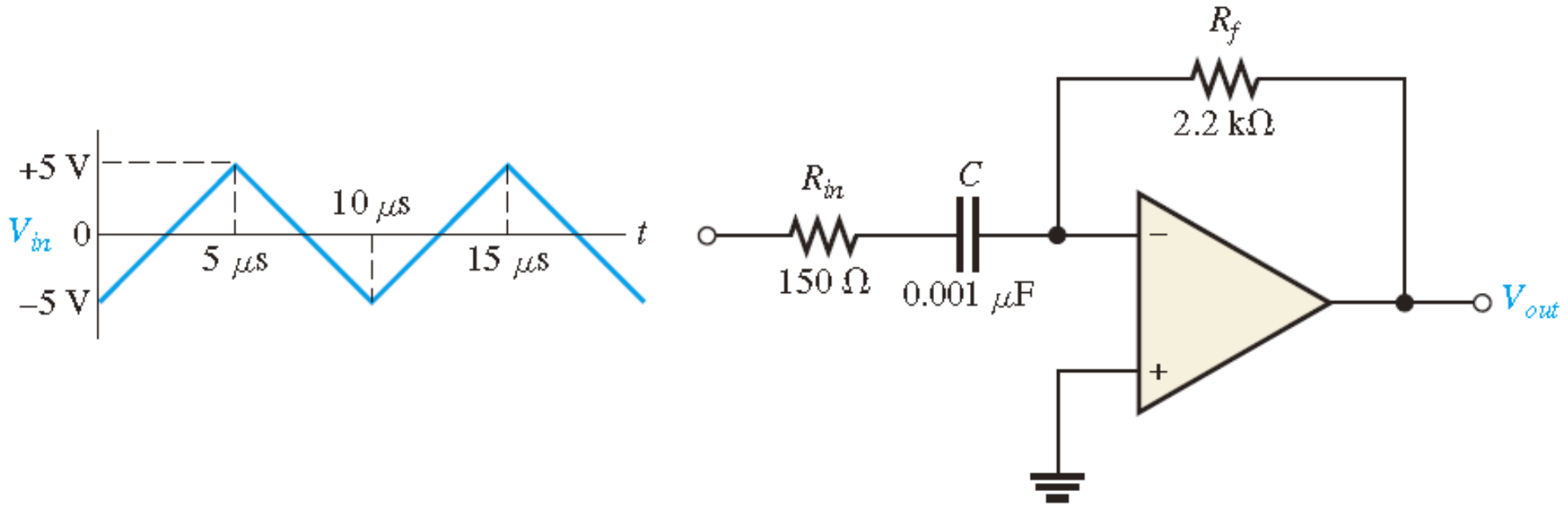


FIGURE 7-18 Practical Differentiator.

Example

Determine the output voltage of the practical op-amp differentiator in Figure 13–42 for the triangular-wave input shown. The input resistor can be ignored as it is small compared to R_f.



Example

Solution Starting at $t = 0$, the input voltage is a positive-going ramp ranging from -5 V to $+5$ V (a $+10$ V change) in 5 μs. Then it changes to a negative-going ramp ranging from $+5$ V to -5 V (a -10 V change) in 5 μs.

The time constant is

$$R_f C = (2.2\ \text{k}\Omega)(0.001\ \mu\text{F}) = 2.2\ \mu\text{s}$$

Determine the slope or rate of change (V_C/t) of the positive-going ramp and calculate the output voltage as follows:

$$\frac{V_C}{t} = \frac{10\ \text{V}}{5\ \mu\text{s}} = 2\ \text{V}/\mu\text{s}$$

$$V_{out} = -\left(\frac{V_C}{t}\right)R_f C = -(2\ \text{V}/\mu\text{s})2.2\ \mu\text{s} = \mathbf{-4.4\ V}$$

Likewise, the slope of the negative-going ramp is -2 V/μs, and the output voltage is

$$V_{out} = -(-2\ \text{V}/\mu\text{s})2.2\ \mu\text{s} = \mathbf{+4.4\ V}$$

Example

Figure 13–42 shows a graph of the output voltage waveform relative to the input.