Quantum Hardware Overview

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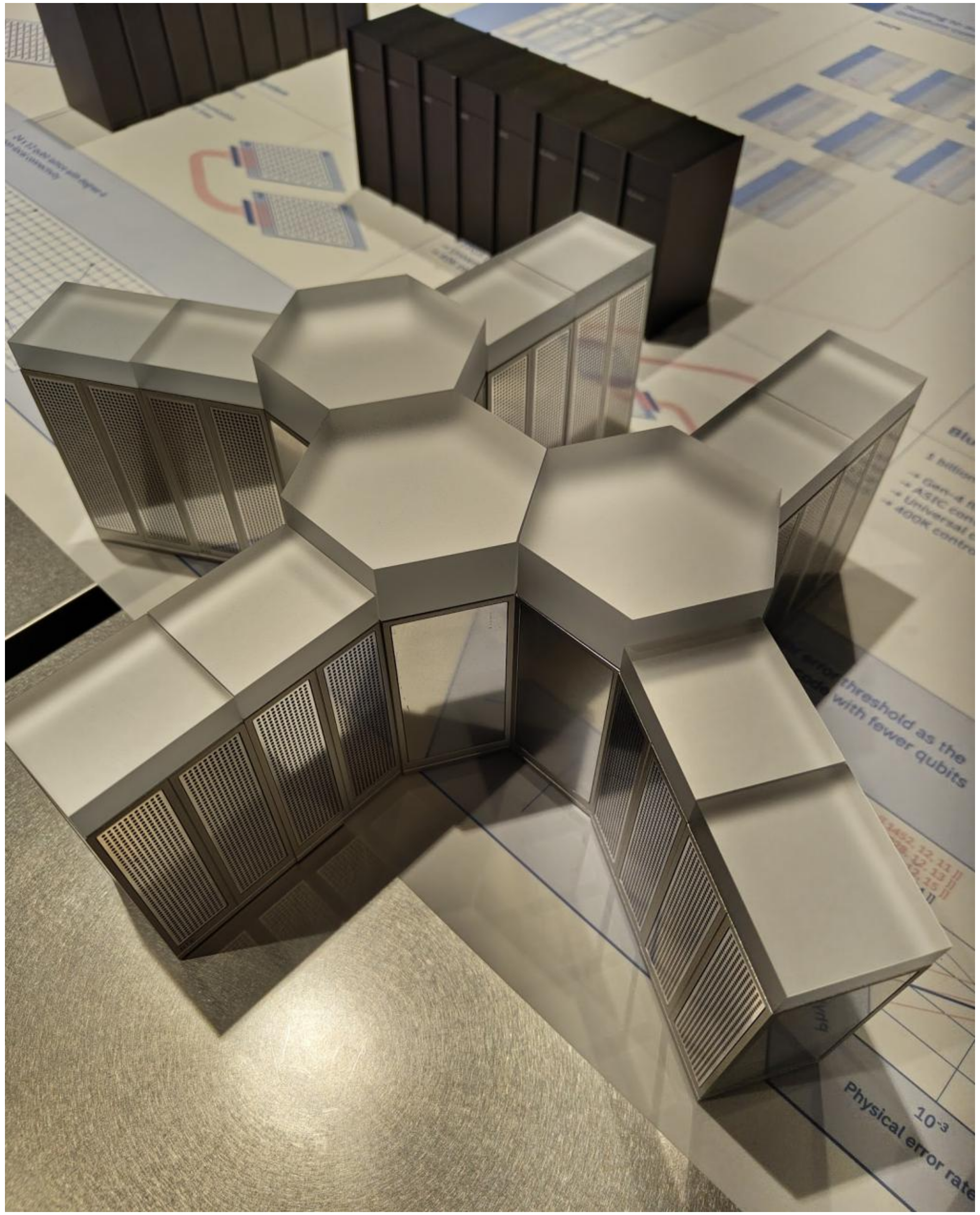
Background & Motivation

Background & Motivation



A Practical Description of Quantum Computing Workflow

In quantum computing, a large class of quantum algorithms prepares superpositions, encodes problem structure as phases (or amplitudes) via unitaries, and engineers interference so that informative outcomes become likely. High-sensitivity measurements (often phase-sensitive in hardware) then sample those outcomes enough times to estimate the desired quantity. **Interferometry** and **metrology** thus provide both the metaphors and many of the tools, even though not every algorithm or platform reduces purely to phase readout.

For the ideal case, in hardware, this would be done in a single shot and should closely match a reference analytical model for a system of interest. In the realistic case, this requires more than a single shot and systematic refinements to get closer to a chosen analytical reference model.

Background & Motivation (Related Repositories)

OJB-Quantum/QC-Hardware-How-To

Everything you need for quantum **hardware** engineering in the field. Curated by Onri Jay Benally.

sustainability · quantum · quantum-mechanics · quantum-computing · qed

Jupyter Notebook · ☆ 65 · Updated 6 hours ago

Unstar

OJB-Quantum/Qiskit-Metal-to-Litho

From **Qiskit Metal** to pattern generation to real nanofabrication demo. Here, quantum devices on a chip are patterned via direct-write elec...

quantum · quantum-computing · manufacturing · hardware-designs · quantum-information

Jupyter Notebook · ☆ 45 · Updated 24 days ago

Unstar

OJB-Quantum/Generative-Layout-Notebooks

GDSII/OASIS **layouts**, including fractals, generated in working Google Colab **notebooks**. **Layout** previews are plotted as 2D graphics before e...

open-source · automation · google · layout · quantum

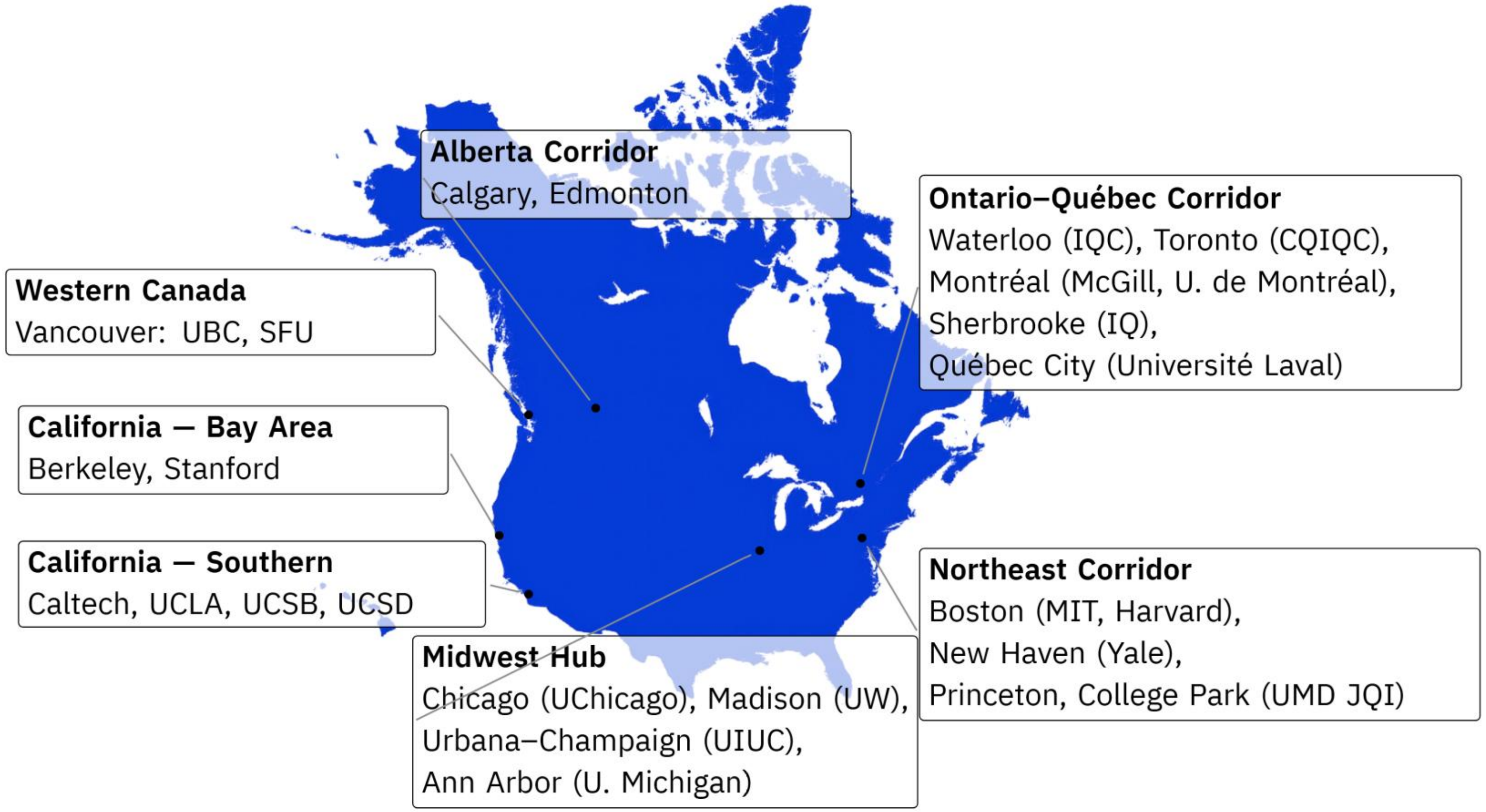
Jupyter Notebook · ☆ 6 · Updated on Aug 14

Unstar

Available at: github.com/OJB-Quantum

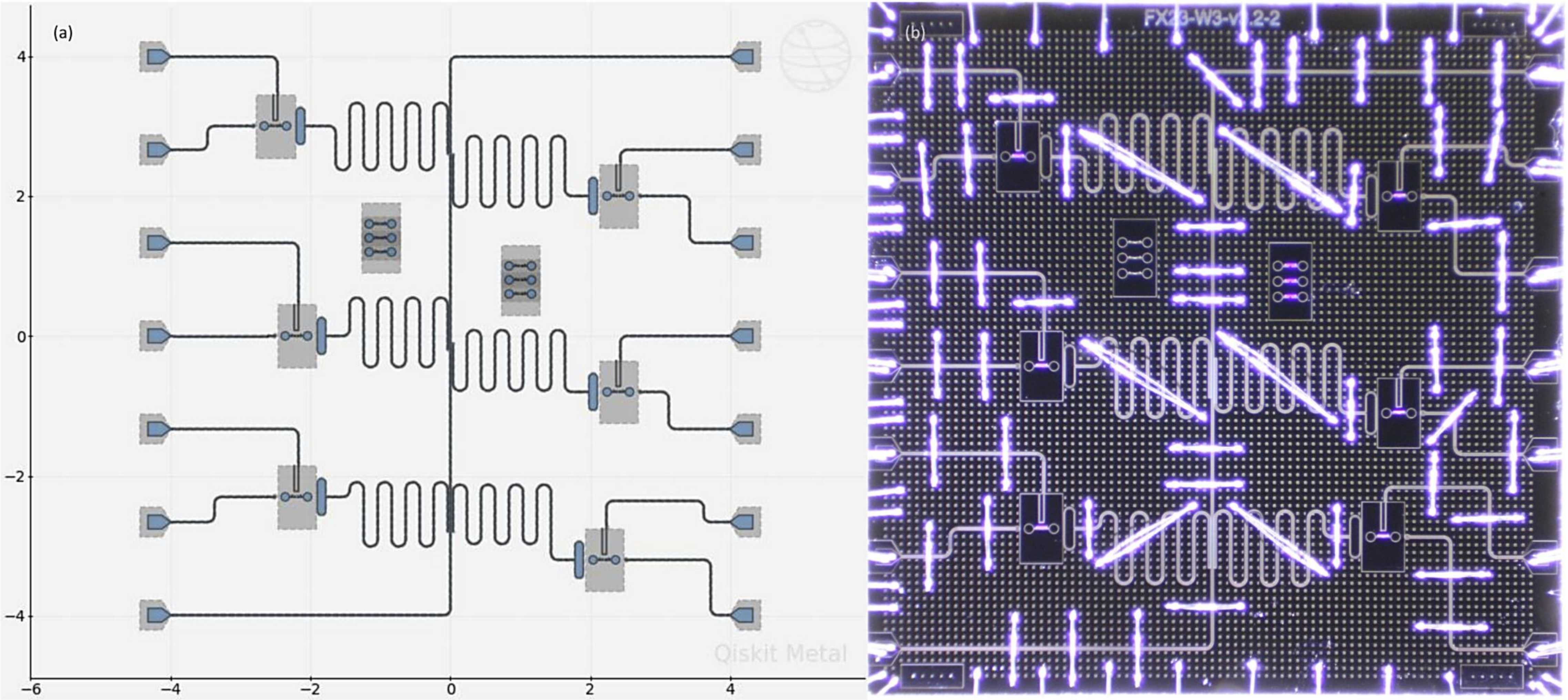
Background & Motivation

Geographic View: Major U.S. Hubs and the Canadian Corridor



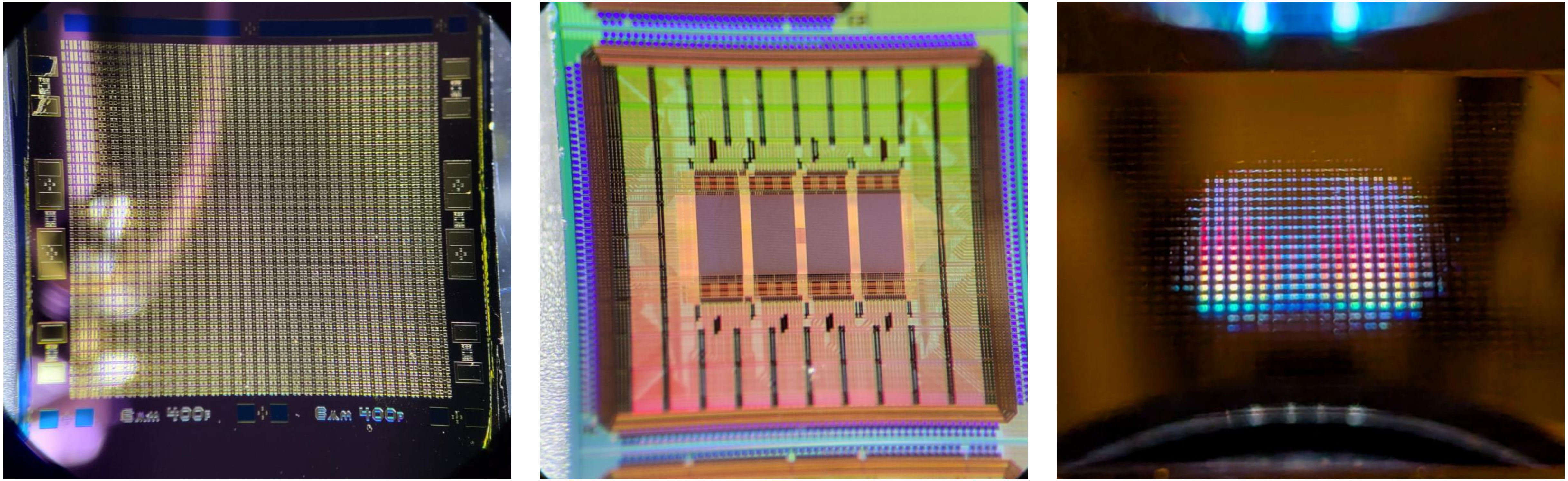
As quantum hardware training infrastructure and programs develop, more major hubs will show up on the map. Eventually, UMN may join the Midwest Hub as well.

Background & Motivation



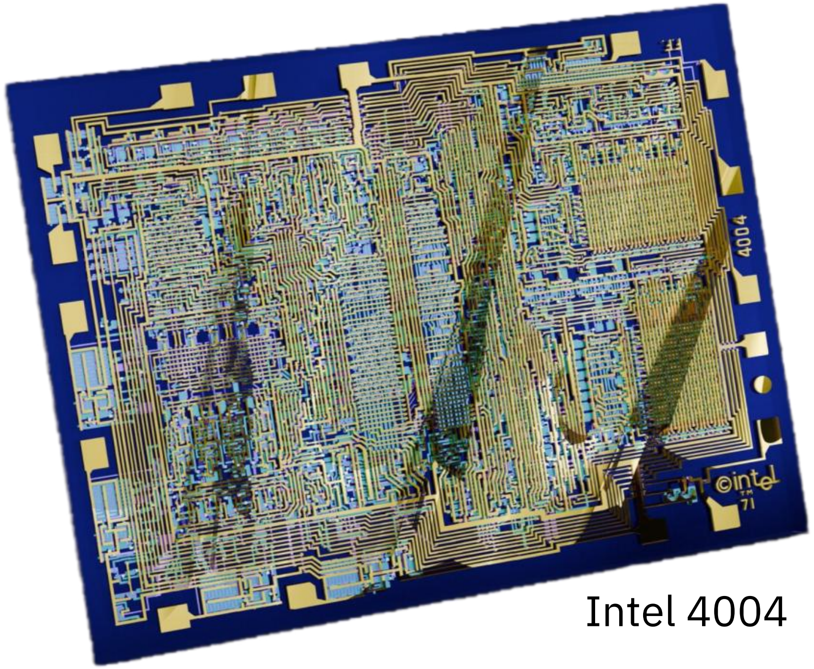
1. Yilmaz, et al., *arXiv* 2411.15039 (2024)

Background & Motivation

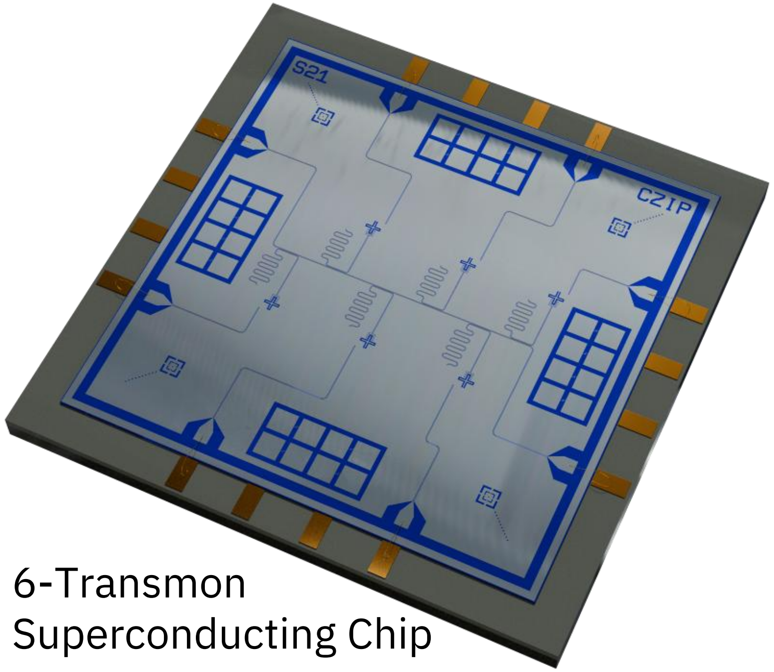


Some images of cryogenically compatible memory chips fabricated by me
(taken through an optical microscope + phone camera).

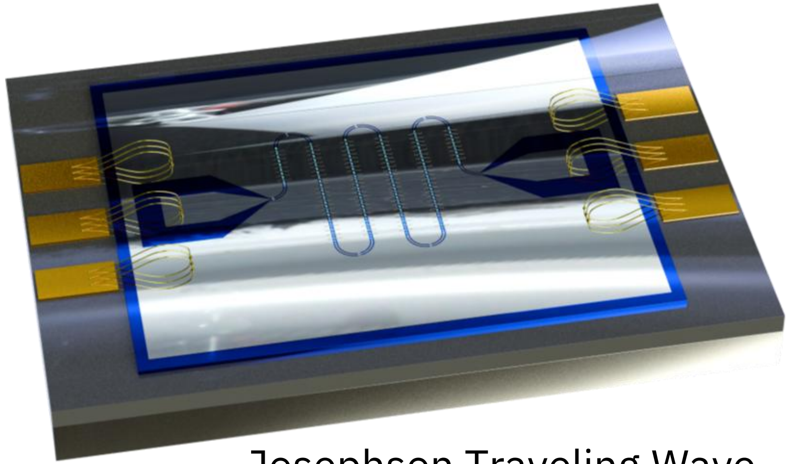
Examples at the Chip Level (Rendered with Blender)



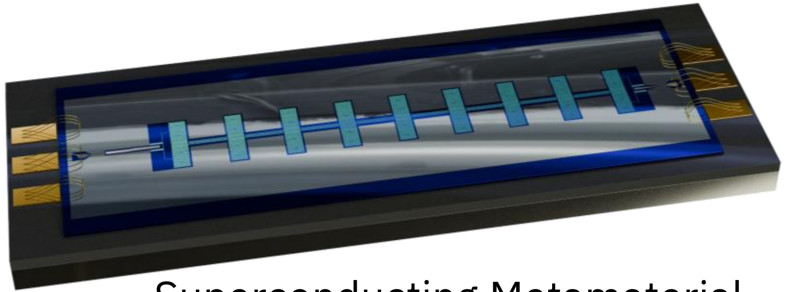
Intel 4004



6-Transmon
Superconducting Chip



Josephson Traveling Wave
Parametric Amplifier Chip



Superconducting Metamaterial
Waveguide Resonator Chip

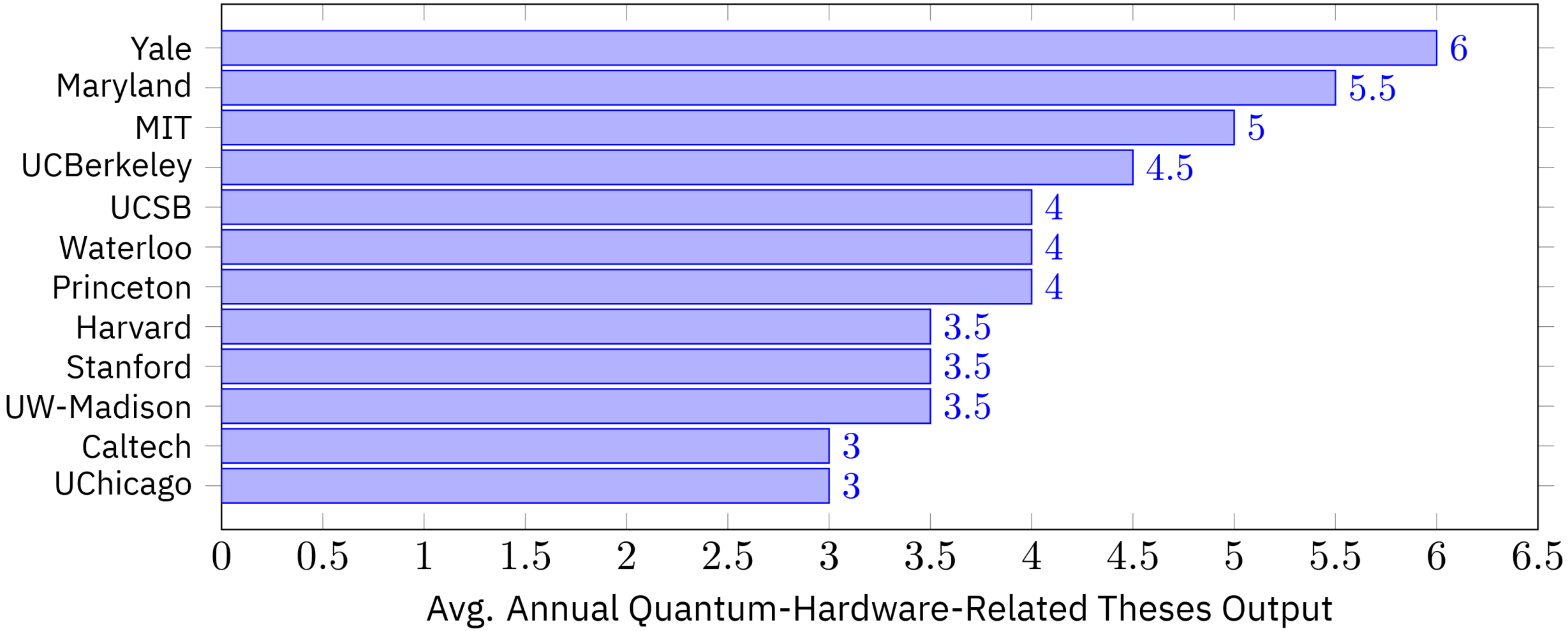
Coplanar Waveguide
Single Resonator Chip

Classical Chips

Quantum Chips

Now available in high resolution on [Wikimedia Commons]

Quantum Hardware Related Graduate Research in the US & Canada



Extensive List of Quantum Hardware Categories

```
+-- I. Quantum-Core Hardware
|   +-- A. Qubit Technologies
|   |   +-- 1. Superconducting Qubits
|   |   |     - Transmon, Fluxonium, Flux qubit
|   |   |     - Cavity-protected (cat, binomial, GKP-encoded)
|   |   +-- 2. Spin-Based Qubits
|   |   |   +-- a. Semiconductor Spins (Si/SiGe, GaAs, donors, NV)
|   |   |   +-- b. Magnetic and Molecular Spins
|   |   |         - Magnetic clusters (Fe8, Mn12, heterometallic rings, other candidates)
|   |   |         - Magnetic nanodisks (meron/skyrmion qubits)
|   |   +-- 3. Bosons (microwave photons, phonons, magnons)
|   |   +-- 4. Topological/Majorana Candidates
|   +-- B. Quantum Interconnects ("Buses")
|   |   +-- 1. Planar Resonators (CPW lambda/4, lambda/2, lumped, stripline)
|   |   +-- 2. 3-D Superconducting Cavities
|   |   +-- 3. Metamaterial Waveguides & Resonators
|   |   +-- 4. Photonic Waveguides & Ring-resonator PICs
|   |   +-- 5. Hybrid Quantum Transducers (electro-optic, electro-acoustic, magnonic)
|   +-- C. Quantum-Limited & Quantum-Enhanced Detectors
|   |   +-- 1. SNSPD
|   |   +-- 2. KID/MKID
|   |   +-- 3. Josephson Photomultipliers (JPM) & Photonics
|   |   +-- 4. Quantum-optimized Bolometers/Calorimeters
|   +-- D. Quantum Memories
|   |   +-- 1. Rare-earth AFC crystals
|   |   +-- 2. Magnon memories
|   |   +-- 3. 3-D Cat-code cavities
|   |   +-- 4. Nuclear-spin ensembles
|   +-- E. Quantum Photonic Integrated Circuits (QPICs)
|       +-- 1. SiN/Si/SiO2 wafer-scale
|       +-- 2. III-V hybrids (GaAs, InP)
|       +-- 3. Diamond & LiNbO3
```

```
+-- II. Quantum-Adjacent Hardware
    +-- A. Cryogenic Digital Control Logic
    |   +-- 1. Single-Flux-Quantum families (RSFQ, RQL, AQFP, eSFQ)
    |   +-- 2. Deep-Cryo CMOS (4 K)
    |   +-- 3. Milli-Kelvin CMOS (<= 100 mK)
    +-- B. Cryogenic Mixed-Signal & RF ICs
    |   +-- 1. Time-interleaved DAC/ADC
    |   +-- 2. RF Transceiver SoCs (2-18 GHz I/Q)
    |   +-- 3. Cryo Class-D Drivers/Piezo
    +-- C. Cryogenic Amplifiers, Filters, & Passive Components
    |   +-- 1. mK Parametric Pre-Amplifiers
    |   |     a. Flux-pumped Josephson Parametric Amplifier/Converter (JPA/JPC)
    |   |     b. Josephson Traveling-Wave Parametric Amplifier (JTWPA)
    |   |     c. Kinetic-Inductance Traveling-Wave Parametric Amplifier (KI-TWPA)
    |   |     d. Nanobridge Kinetic Parametric Amplifier (NKPA)
    |   |     e. Quantum Capacitance Parametric Amplifier (QCPA)
    |   |     f. SNAIL-based Parametric Amplifier (SPA/SNAIL-TWPA)
    |   +-- 2. 4 K HEMT LNAs (octave-wide, high dynamic range)
    |   +-- 3. RF Isolators/Circulators (ferrite or on-chip)
    |   +-- 4. Superconducting & SAW Filters
    +-- D. Cryogenic Packaging & Interconnects
    |   +-- 1. Flex-print & interposer tiles
    |   +-- 2. 3-D cavities w/ cryogenic bump-bonds/ interconnects
    |   +-- 3. Coax/waveguide/stripline wiring (NbTi, Nb, CuNi)
    |   +-- 4. Optical fiber feedthroughs (1-4 K)
    |   +-- 5. Magnetic & vibration shielding, radiation hardeners
    +-- E. Cryogenic Memory & Storage
        +-- 1. SRAM (FinFET 14-nm & 5-nm cryo-SRAM)
        +-- 2. Floating-Body RAM (FBRAM) at 77 K
        +-- 3. Capacitor-less eDRAM/DRAM benchmarks (2T0C, 4 K)
        +-- 4. JJ-based RAM (JJ-RAM, JMRAM)
        +-- 5. Spin-orbit-torque (SOT) MRAM at 4 K
```

Available at: github.com/OJB-Quantum/QC-Hardware-How-To

Some Portmanteaus

```
Portmanteaus
├── Transistor
│   ├── transconductance + varistor
│   │   └── transconductance + variable + resistor
│   └── transfer + resistor (widely accepted)
│
├── Spintronics
│   ├── spin + transport + electronics
│   └── spin + electronics
│
├── Qubits
│   └── quantum + bit
│       └── quantum + binary + digit
│
└── Qudits
    └── quantum + digit
```

Qubit Classification Trees

```
Qudit-Related Relationships of Quantum Information Carriers
└─ Terminology
   ├─ Qubit = dimension-2 qudit
   ├─ Qutrit = dimension-3 qudit
   ├─ Ququart = dimension-4 qudit
   └─ Qudit = quantum digit (general dimension)
```

Qubit Classification Trees

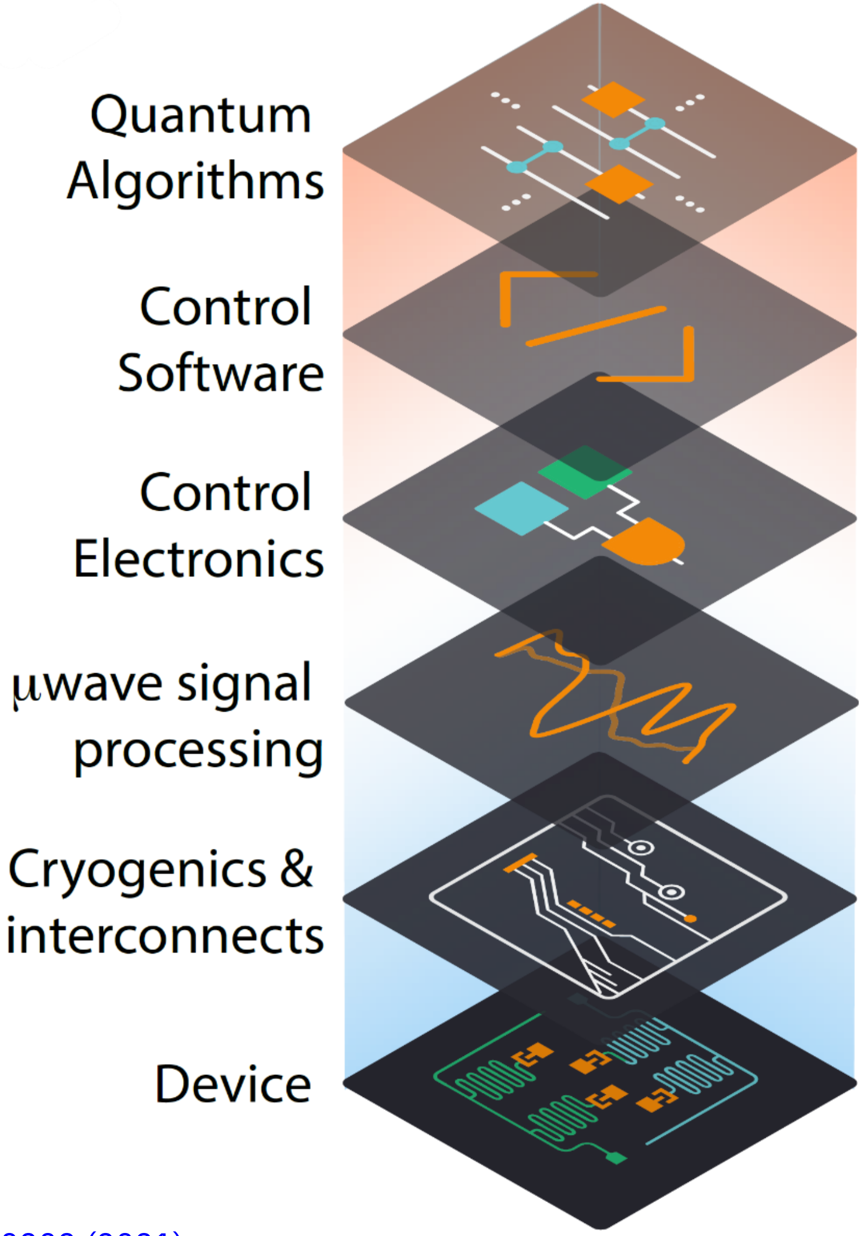
```
└ Noisy Intermediate-Scale Quantum (NISQ) Era
   ├ Abstraction Level
   │  ├ Physical Qubit
   │  └ Logical Qubit  (≈1 logical : 1 physical today)
   ├ Origin
   │  ├ Natural Qubit
   │  └ Synthetic Qubit
   ├ Spectral Control
   │  ├ Fixed-Frequency Qubit
   │  └ Tunable Qubit
   ├ Mobility
   │  ├ Stationary Qubit
   │  └ Flying Qubit
   └ Functional Role
      ├ Data Qubit
      └ Ancilla Qubit
```

```
└ Fault-Tolerant (FT) Era
   ├ Abstraction Level
   │  ├ Physical Qubit
   │  └ Logical Qubit  (>1,000 physical per logical)
   ├ Origin
   │  ├ Natural Qubit
   │  └ Synthetic Qubit
   ├ Spectral Control
   │  ├ Fixed-Frequency Qubit
   │  └ Tunable Qubit
   ├ Mobility
   │  ├ Stationary Qubit
   │  └ Flying Qubit
   └ Functional Role
      ├ Data Qubit
      └ Ancilla Qubit
```

Quantum Stack

Software

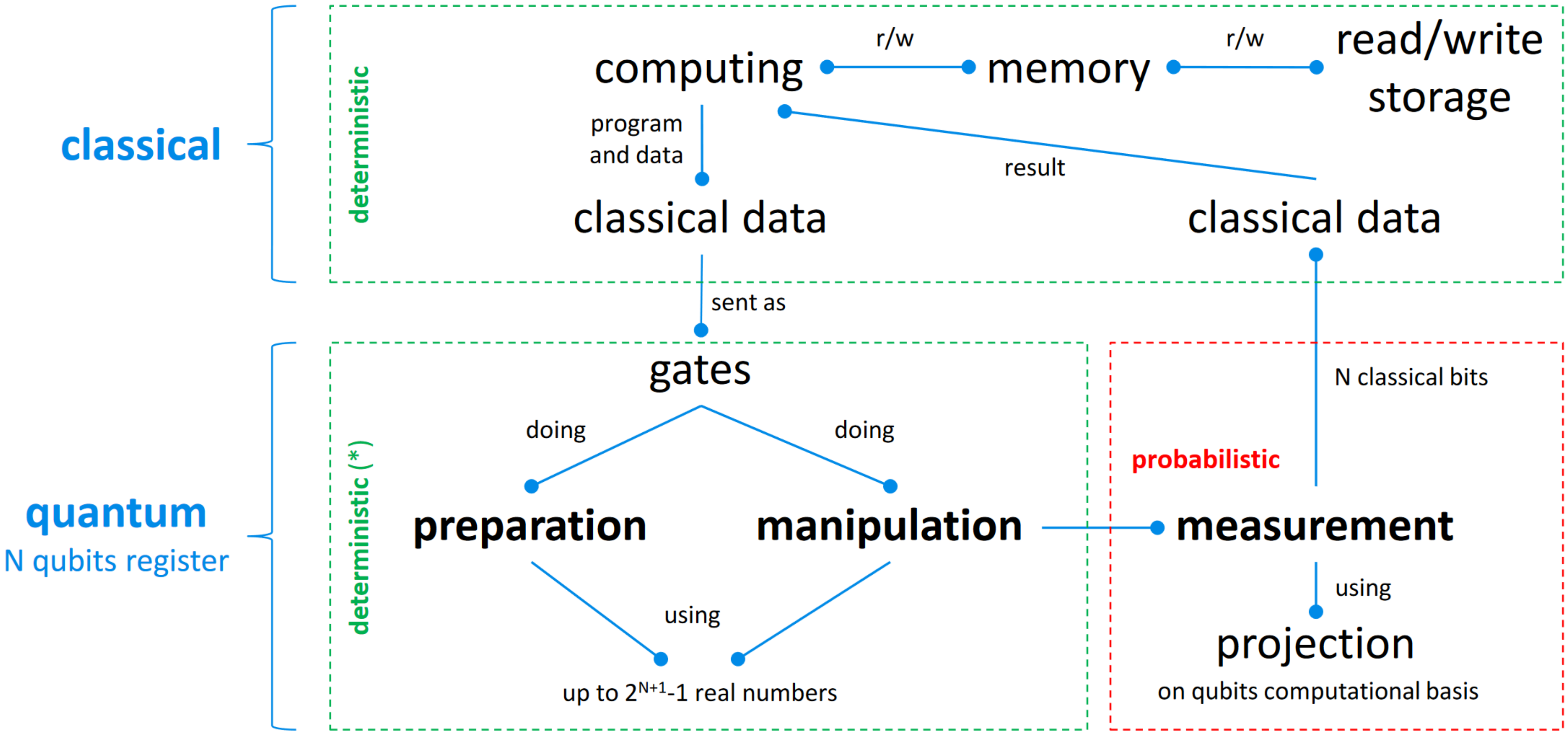
Hardware



1. Gao et al., *PRX Quantum* 2, 040202 (2021)

Workflow for Gate-Based Quantum Computing

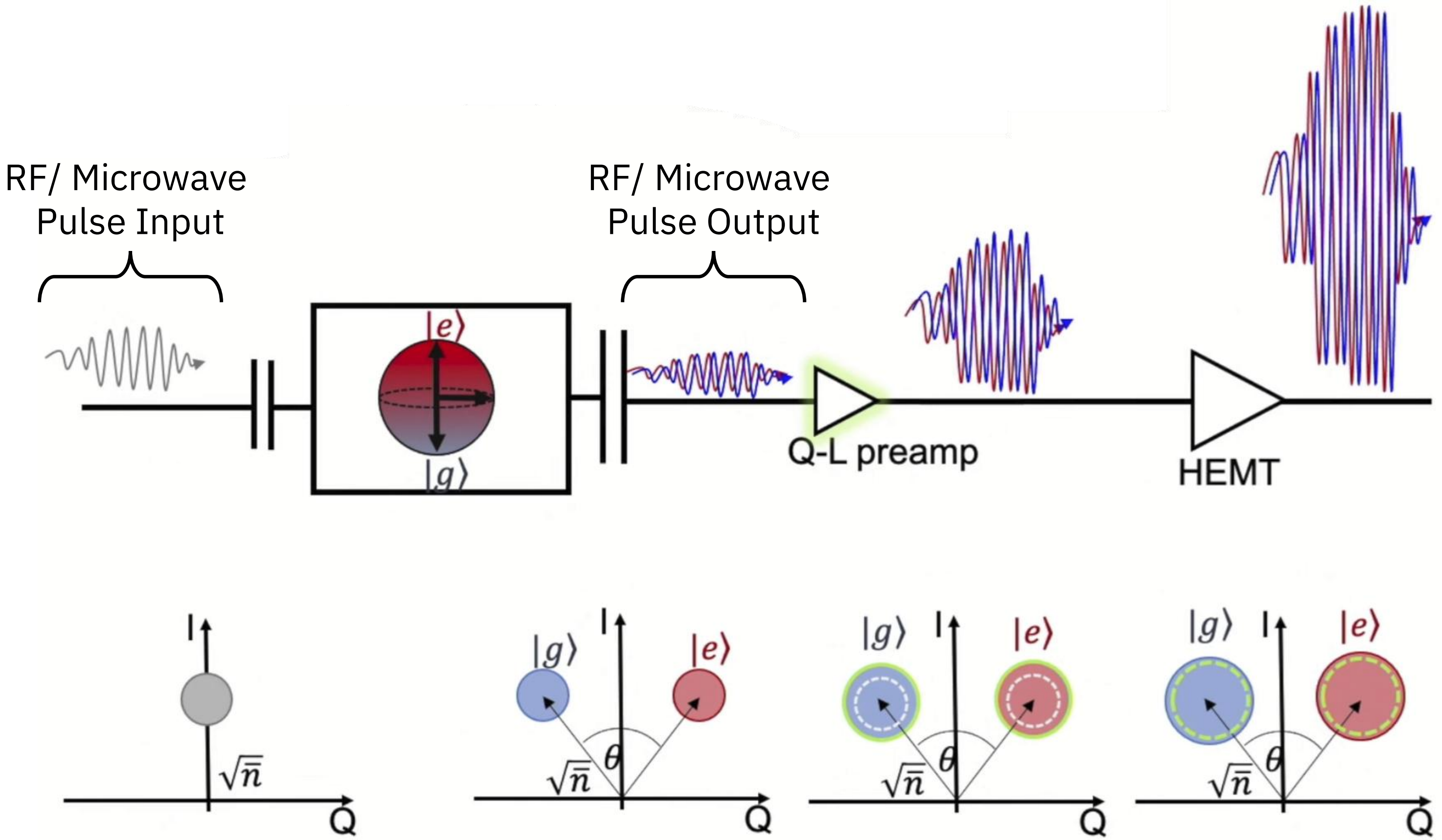
- Every quantum gate has a unique waveform for every physical gate supported by the system.



(*) module noise and decoherence effects, and some probabilistic gates like with some quantum photonic settings (MZI, KLM).

1. Ezratty et al., *arXiv* 2111.15352 (2024)

Context: A Conventional Quantum System Workflow (w/ Quantum-Limited Amplification)



Note: this workflow is generally applicable for quantum computing hardware, although the output signal may differ (RF/MW vs. charge steps)

HEMT = High Electron Mobility Transistor [Amp.]

[Courtesy of Dr. Olivia Lanes from IBM, via Qiskit on YouTube]

How to Think About The Outcome of Qubits Based on Their Classification

Model	Target p	Shots	(Successes)	(Failures)	Successes Fraction (Observed p)	Wilson CI 95% Low	Wilson CI 95% High	CI Width (95%)	Required Shots for ±2%	Required Shots for ±1%	Required Shots for ±0.5%
Toy working qubit	0.50	10,000	5,025	4,975	0.5025	0.4927	0.5123	0.0196	2,401	9,604	38,415
NISQ qubit	0.60	10,000	6,010	3,990	0.6010	0.5914	0.6105	0.0191	2,305	9,220	36,878
Fault-tolerant (logical)	0.90	10,000	9,013	987	0.9013	0.8956	0.9067	0.0111	865	3,458	13,830
Topologically protected	0.98	10,000	9,797	203	0.9797	0.9769	0.9822	0.0053	189	753	3,011
Ideal qubit	1.00	10,000	10,000	0	1.0000	0.9996	1.0000	0.0004	1	1	1

- **Toy working qubit** — Simple demonstrator; about half shots meet the criterion.
- **NISQ qubit** — Noisy Intermediate-Scale Quantum device; modest success rate above chance.
- **Fault-tolerant (logical)** — Error-corrected logical qubit; high single-shot success probability.
- **Topologically protected** — Intrinsic protection; very high single-shot success probability.
- **Ideal qubit** — Theoretical perfect qubit; always successful in a single shot.

A Note About Truly Perfect/ Ideal Qubits

Would a **truly** perfect qubit behave almost deterministically?

Instead of directly deterministic outcomes like a digital transistor is capable of, a truly perfect qubit would exhibit indirect near-deterministic outcomes "the long way"(yet efficiently) if scaled up to its advantage or utility threshold.

```
"Determinism" in Quantum Computing
├─ Physics limit (Born rule)
│   └─ Single shot random unless in eigenstate.
├─ Make success likely → 1
│   ├─ In-circuit: amplitude amplification (Grover angle, fixed-point variants).
│   ├─ Estimation: quantum amplitude estimation (QAE) reduces samples.
│   └─ Statistics: Hoeffding/Chernoff majority/CI boosts.
├─ Make errors vanishingly rare
│   ├─ Active: Fault-tolerant QEC (e.g., bicycle code); logical p_L ↓ ~ exp(-α·d) below threshold.
│   └─ Passive: Topological protection (hardware)
│       ├─ Non-Abelian anyons/ Majorana zero modes → non-local encoding, braiding
│       ├─ Splitting ΔE(L) ~ e^{-L/ξ}; thermal errors ~ e^{-Δ/kT}
│       └─ Limits: QP poisoning; 2D self-correction no-go → combine with active QEC
└─ Special cases
    └─ Exact algorithms (Deutsch-Jozsa, Bernstein-Vazirani) → deterministic on ideal hardware.
```

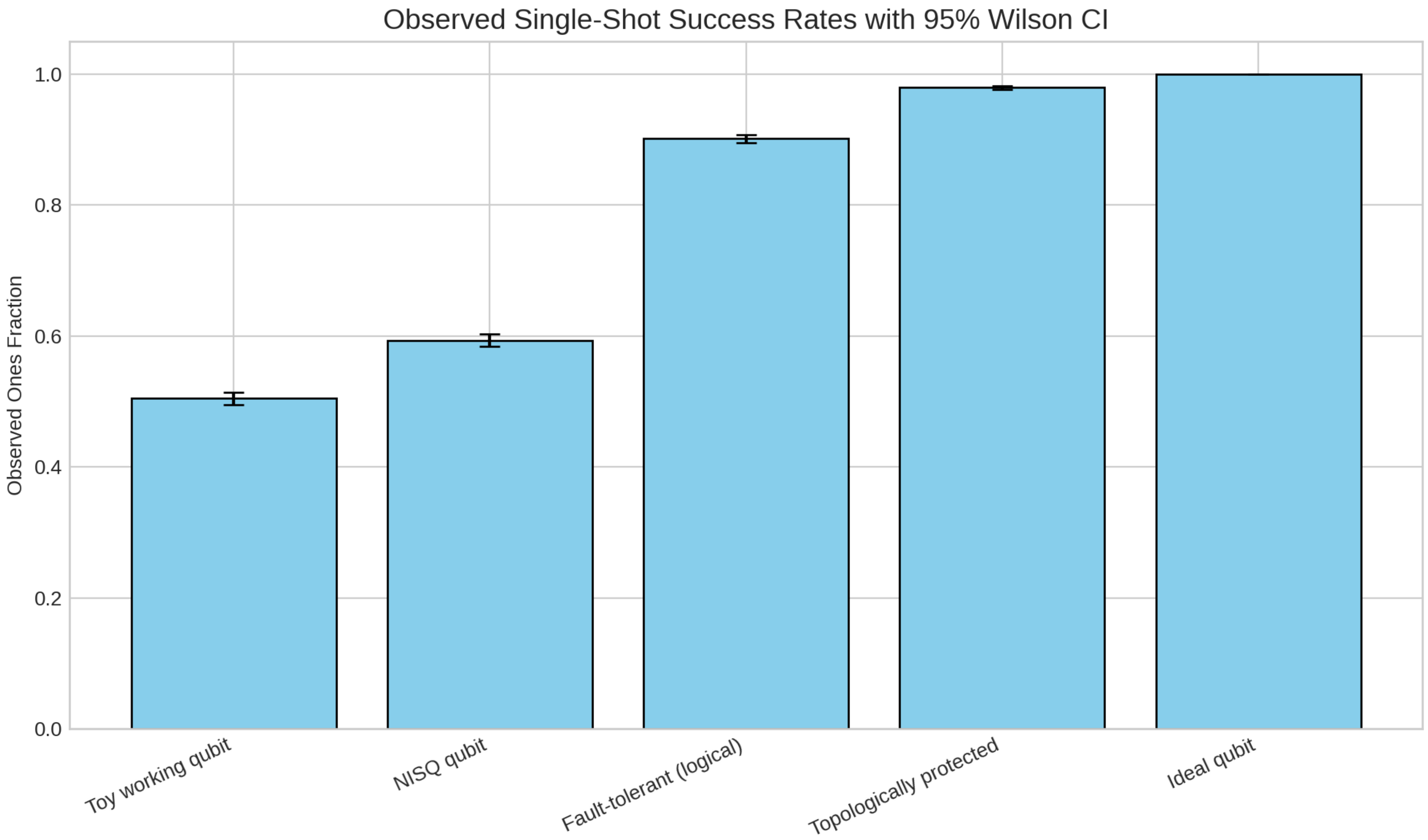

1. Neumaier, *Entropy 27*(4), 415 (2025)
2. Brassard et al., Contemp. Math. 305 05215 (2002)
3. Aliferis et al., *Quant. Inf. Comput.* 6(2) 97-165 (2006)
4. Alicea, Rep. Prog. Phys. 75 076501 (2012)

The Top 2 Qubit Regimes for the Long Term

Mechanism	What protects information	Characteristic scaling	What you tune	Practical caveats
Active fault-tolerant QEC (e.g., bicycle code)	Repeated syndrome extraction + decoding; logical information is spread over many qubits	For $p < p_{\text{th}}$, $p_L \sim e^{-\alpha(p)d}$ (often fit as $A(p/p_{\text{th}})^{(d+1)/2}$)	Lower physical error rate p; raise code distance d	Requires fast, reliable measurements and decoding; overhead is large but scaling is systematic.
Passive topological protection (hardware)	Non-local ground-state manifold (e.g., Majorana/anyons)	Ground-state splitting $\Delta E(L) \propto e^{-L/\xi}$; thermal errors $\propto e^{-\Delta/kT}$	Increase separation L; increase gap Δ; reduce temperature T	Quasiparticle poisoning not automatically suppressed; finite-size hybridization. 2D self-correction is a no-go at finite T $\rightarrow$ often paired with active QEC.

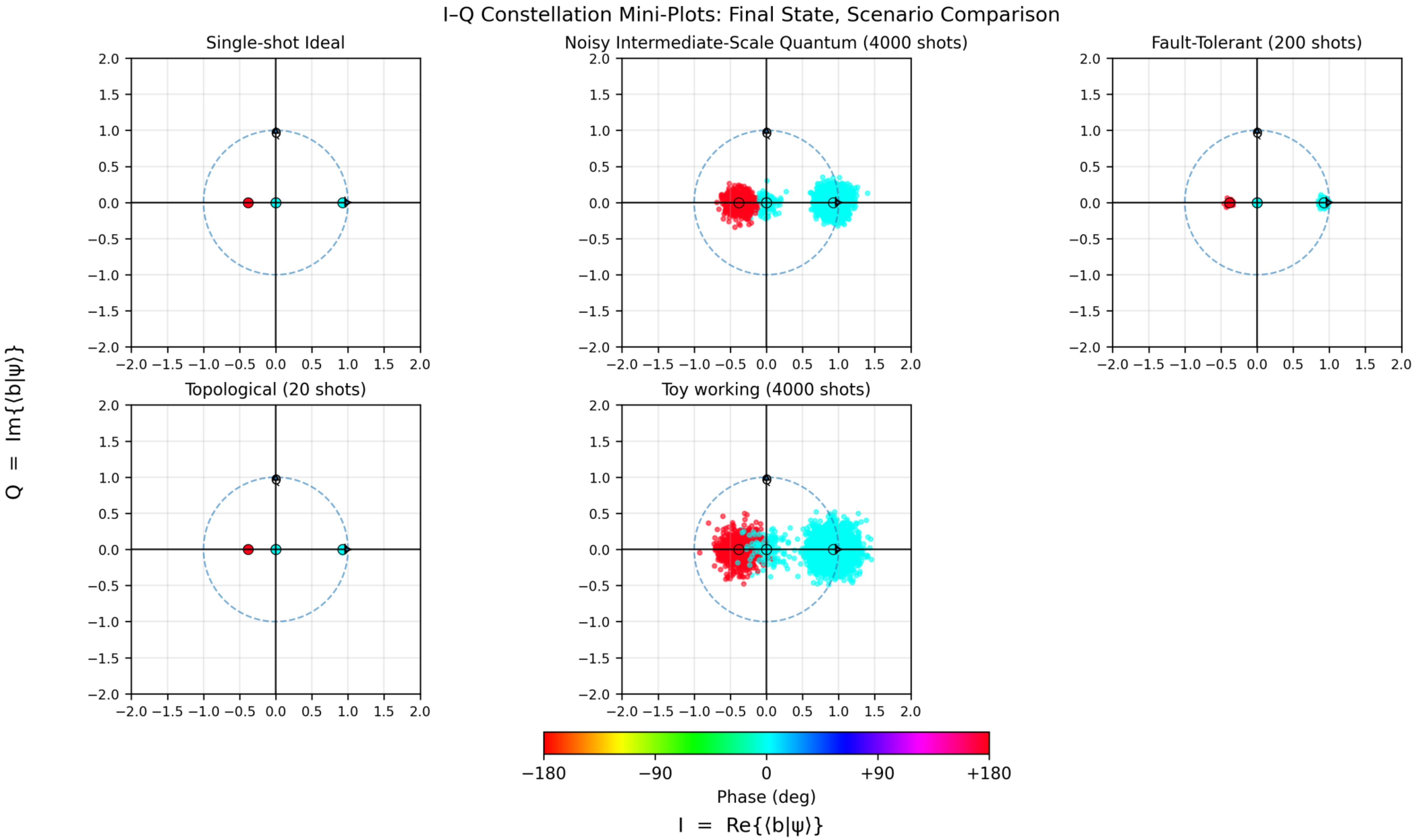
1. Neumaier, *Entropy 27*(4), 415 (2025)
2. Brassard et al., Contemp. Math. 305 05215 (2002)
3. Aliferis et al., *Quant. Inf. Comput.* 6(2) 97-165 (2006)
4. Alicea, Rep. Prog. Phys. 75 076501 (2012)

Illustrative Single-Shot Success Rates for Qubit Types



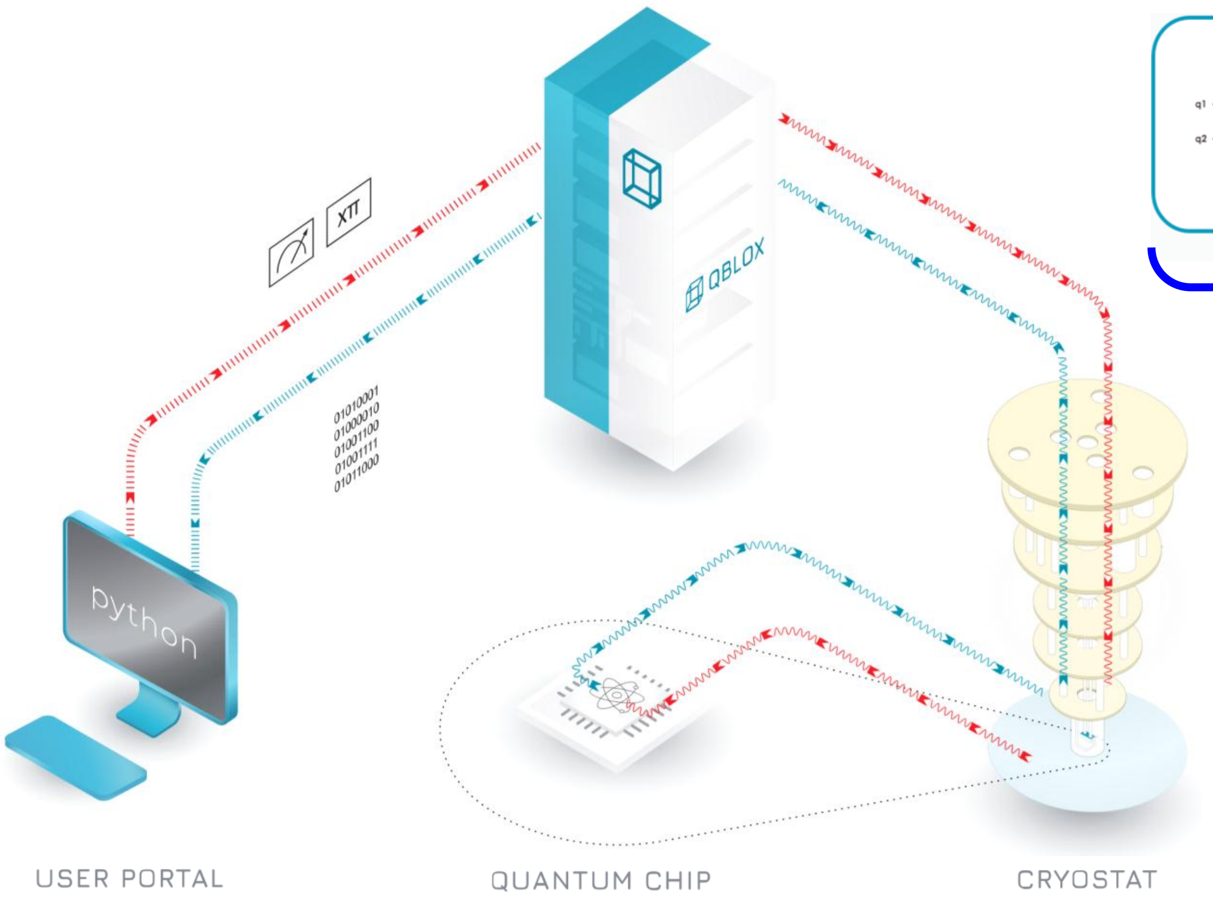
Available at: github.com/OJB-Quantum/QC-Hardware-How-To

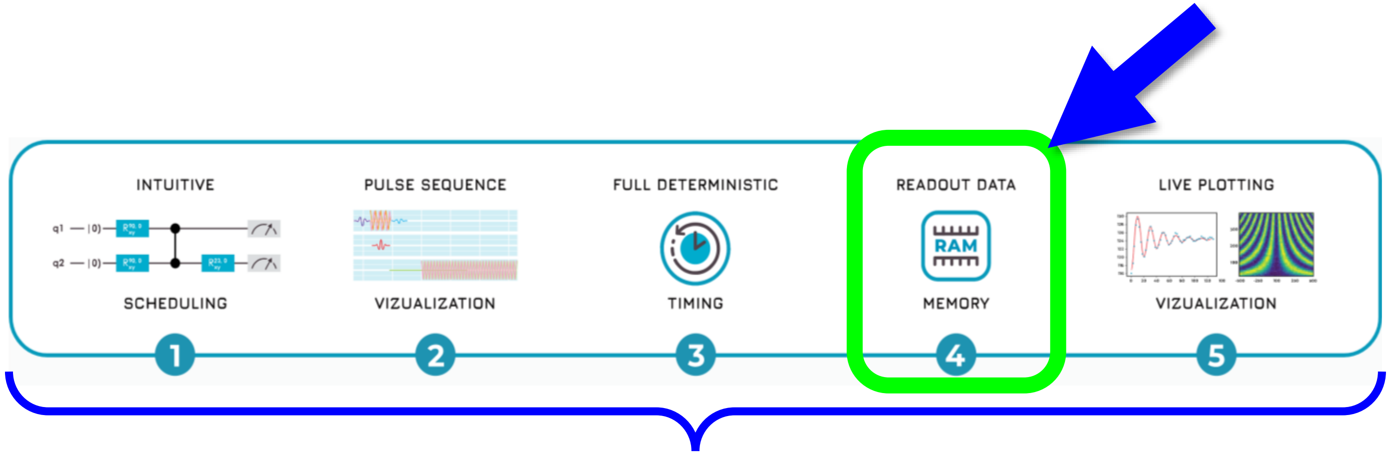
Illustrative Single-to-Multi-Shot Success Rates for Qubits

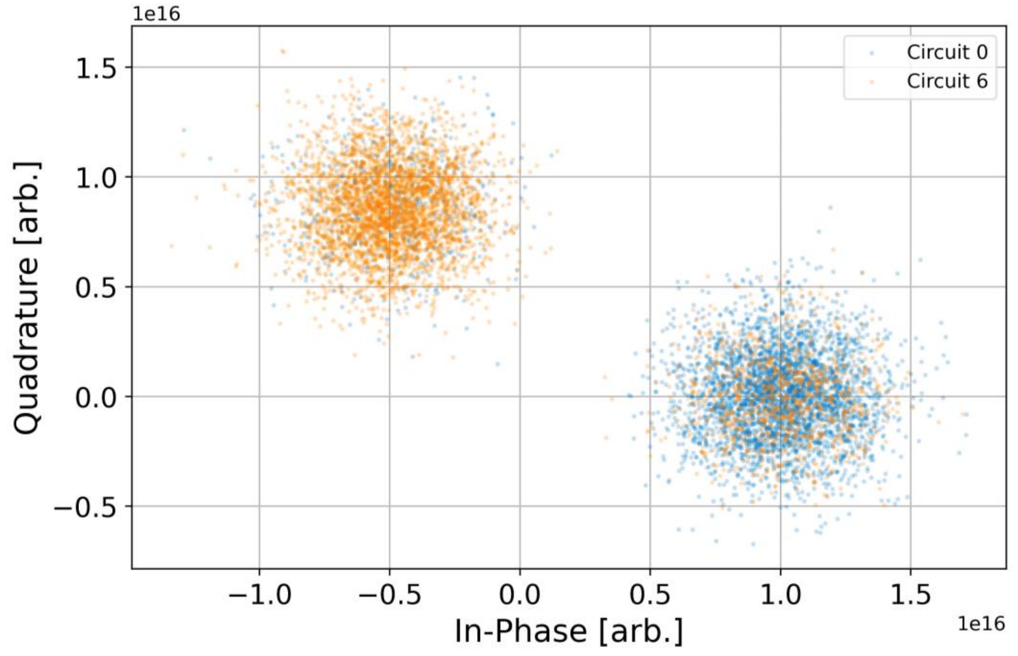


Available at: github.com/OJB-Quantum/QC-Hardware-How-To

Generic Qubit Drive & Readout Workflow w/ Example

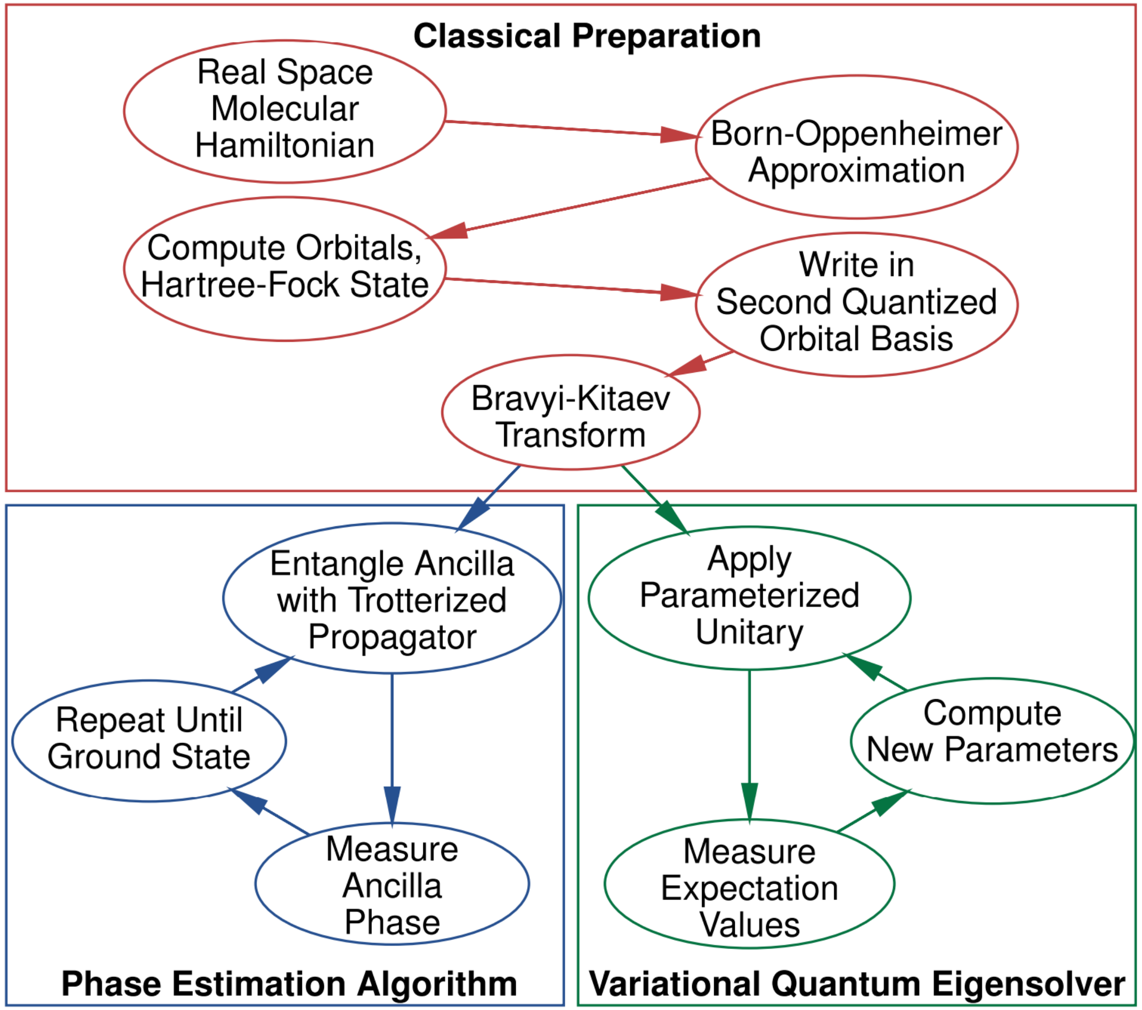


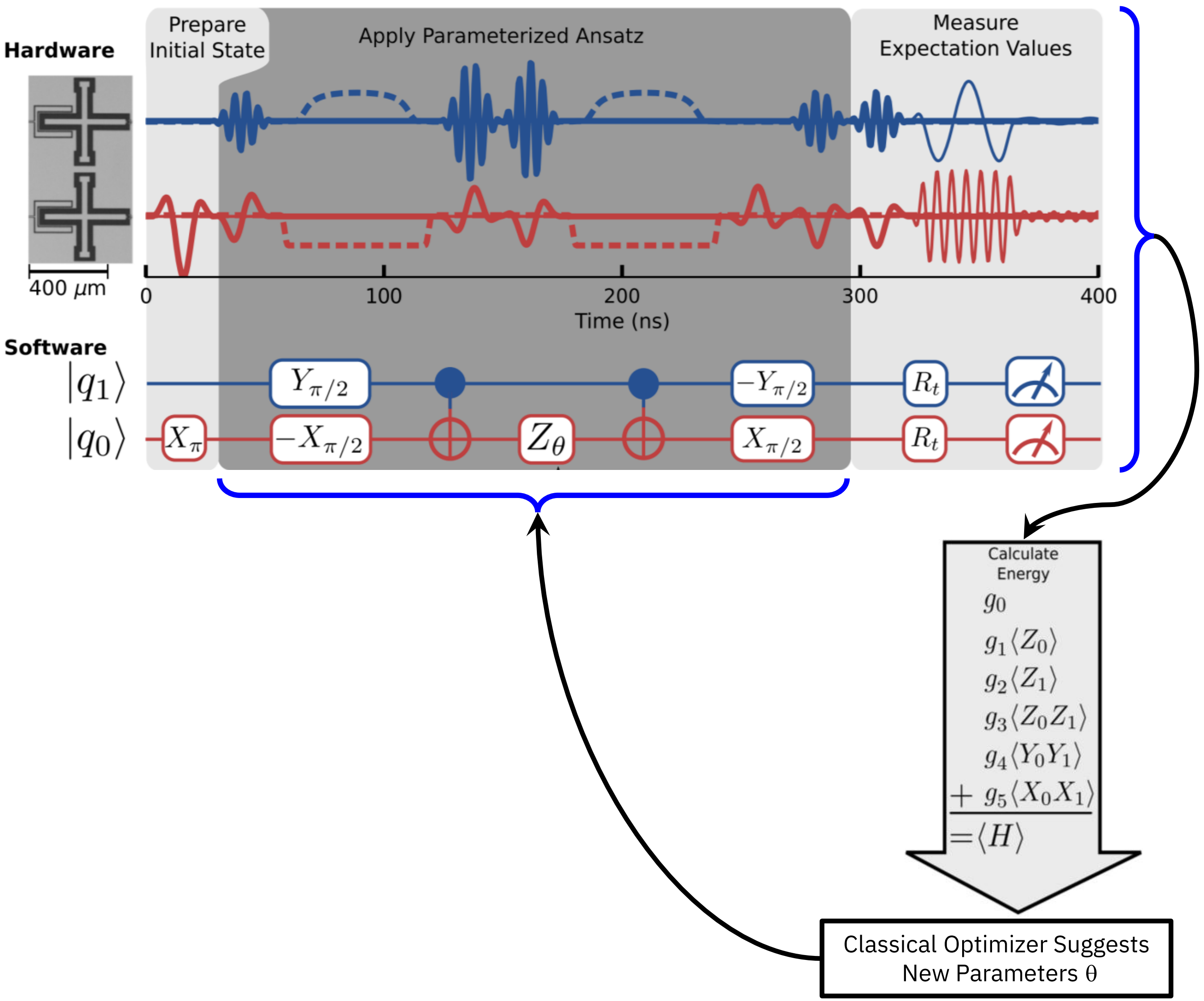




1. Qblox Quantum, *Documentation and Tutorials* (2022)

Example of Required Steps to Compute Molecular Energies





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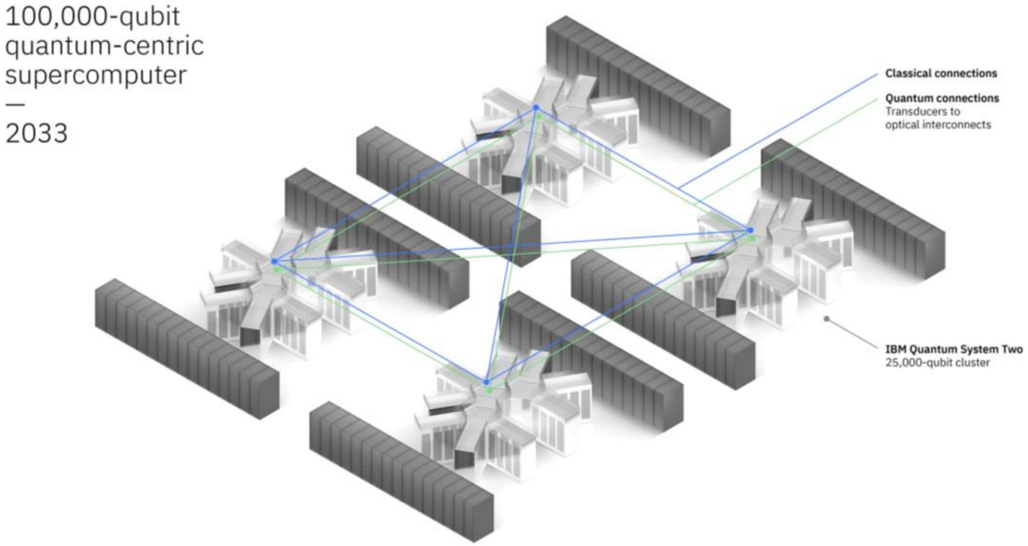
1. van Dijk et al., *Microprocessors and Microsystems* 6, 2019.02.004 (2019)
2. Adapted from: O'Malley et al., *Phys. Rev. X*, 6 031007 (2016)

Quantum Systems Range in Size

- In configuring quantum machines, it is useful to know that **control components** have been made available in various sizes and formfactors.
- Control components for qubits can take up a lot of hardware space/ footprint.
    - However, an effort has been made to miniaturize them using cryo-compatible:
        - Complementary Metal Oxide Semiconductor (CMOS) chips.
        - Application Specific Integrated Circuit (ASIC) or Field-Programmable Gate Array (FPGA) chips.

Up to 3-qubit desktop quantum PC (novelty)
Price ≈ $5,000
FPGA-controlled NMR



More Desktop-Like ⟷ ***More Server-Farm-Like**

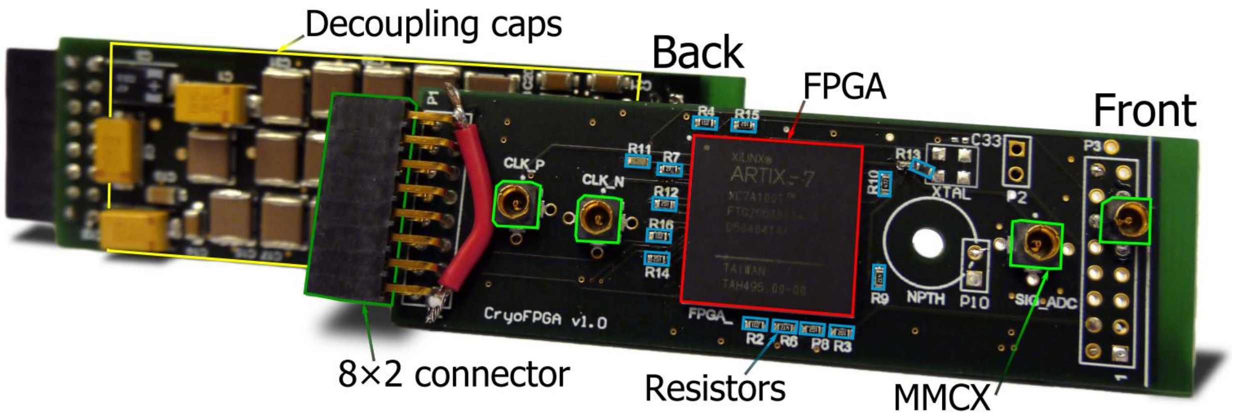
1. SpinQ, *Gemini 2 [2-Qubit System]* (2022)
2. IBM Research

*Also called server-clusters

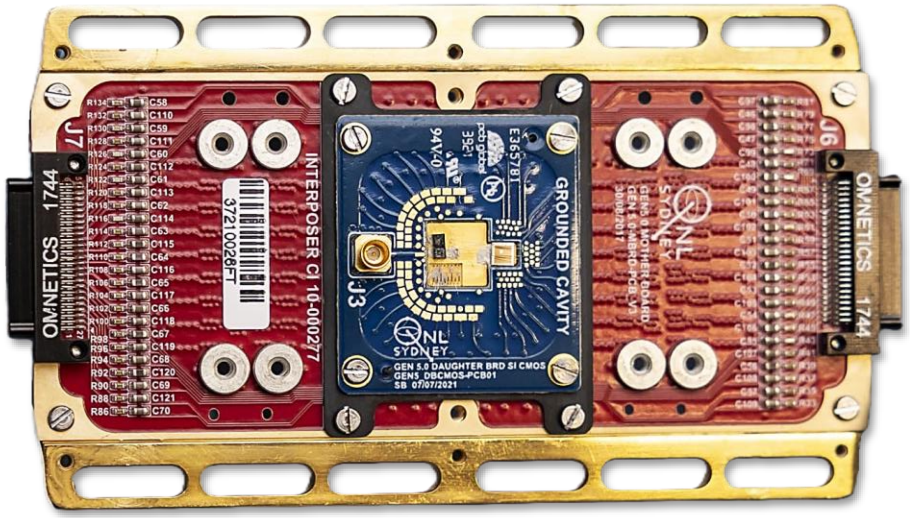
Advanced Quantum Computers Are Controlled Using 2 Approaches

Controller Type	Full Name	Description
Cryo-FPGA	Cryogenic Field Programmable Gate Array	A reconfigurable logic device designed to operate at cryogenic temperatures, used for flexible signal processing and control of qubits.
Cryo-ASIC	Cryogenic Application Specific Integrated Circuit	A custom-designed integrated circuit optimized for cryogenic operation, tailored for efficient and low-power qubit control and readout.

Cryogenic FPGA & ASIC Qubit Controller Examples



Xilinx FPGA Artix 7



Diraq-USydney Cryo CMOS ASIC

1. Homulle et al., 1854 IEEE Trans. Circuits and Sys–I 63, 11 7593301 (2016)
2. Diraq & University of Sydney

Room Temp. Control vs. Embedded Cryogenic Control of Qubits

RT Qubit Controller
[Built-In (Memory + ADC + DAC)]

Room Temperature
Control Approach

Embedded Qubit Controller
[Built-In (Memory + ADC/ DAC)]

ASIC or FPGA

-OR-

Embedded Qubit Controller
[Built-In Memory]
+ [Separate ADC/ DAC]

Multi-Chip

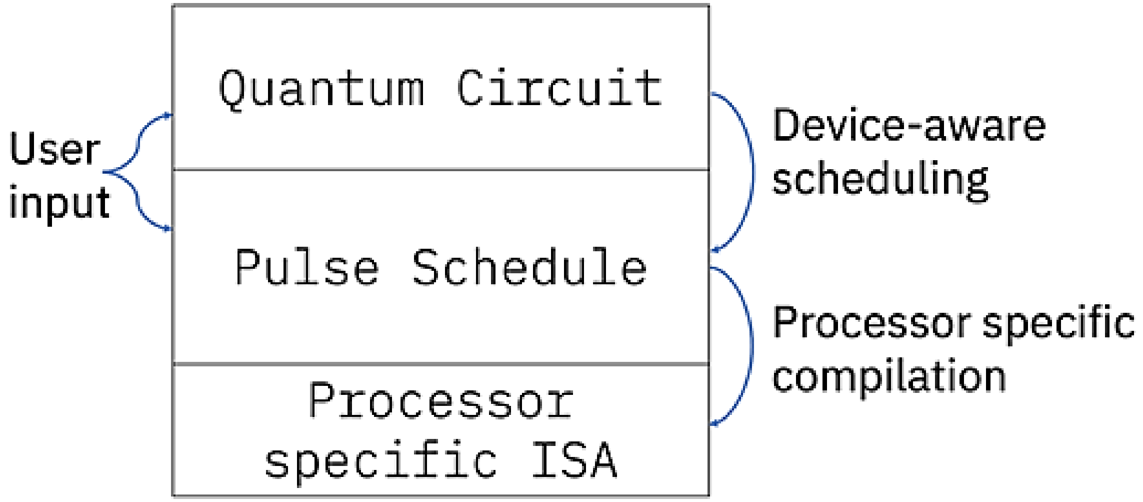
Cryogenic Temperature
Embedded Control Approach

Note: Here, cryogenic is referred to as being below 123 K.
*SoC: System on a Chip

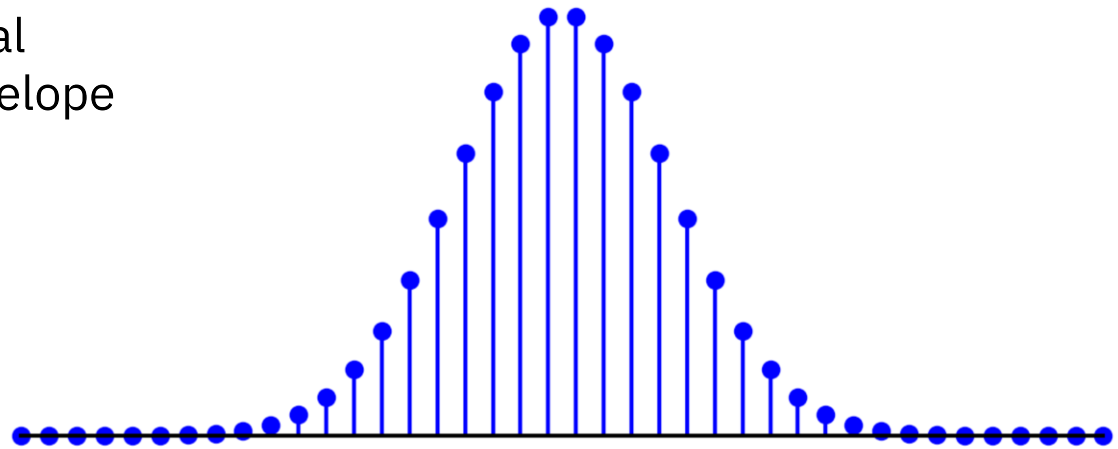
1. Pobell, Matter and Methods at Low Temp. 3rd ed. Springer, 978-3-540-46360-3 (2007)

Current Memory & Waveform Use Flowchart for Quantum

- Leading to the comparison between specialized waveform memory and the use of RAM for wave encoding.
- Every quantum gate has a unique waveform for every physical gate supported by the system. The data points along the envelope are something that can be stored in classical memory.



- ISA = Instruction Set Architecture



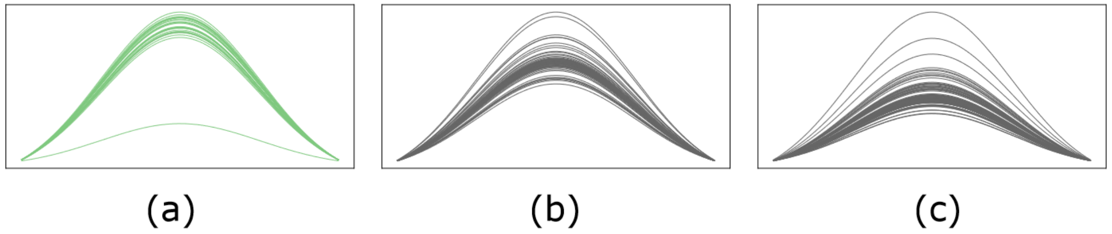
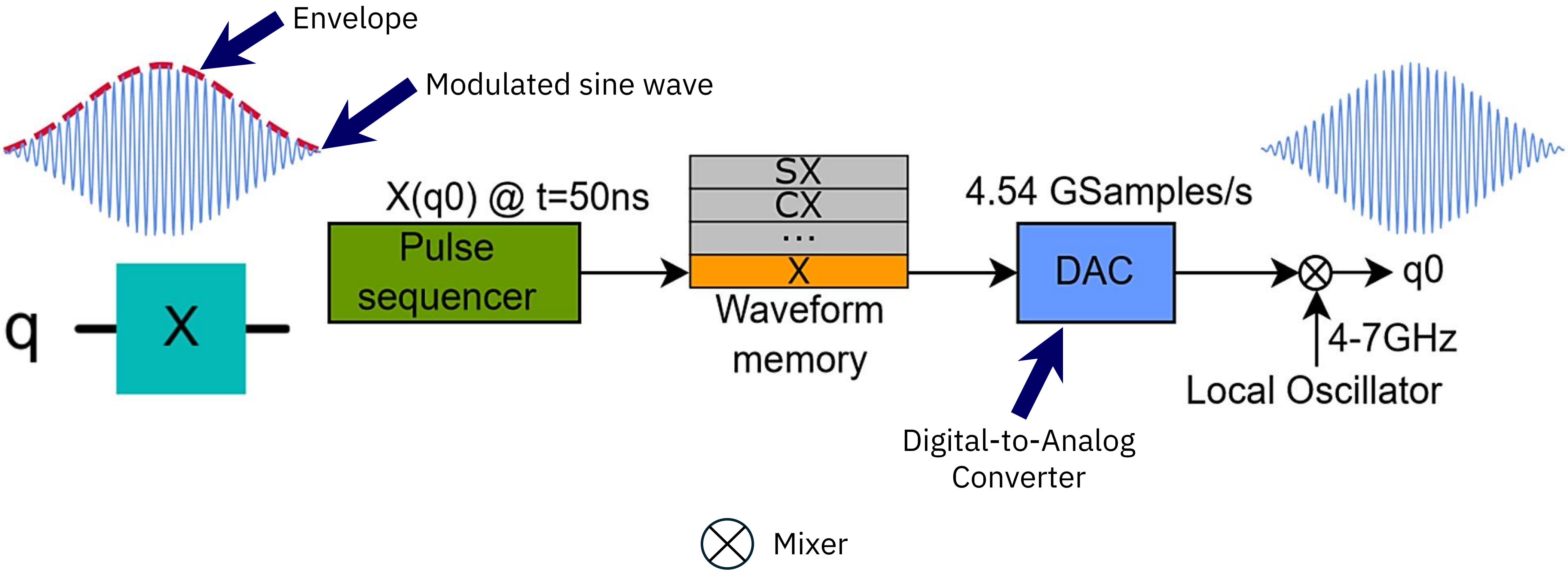


Figure 4. π-pulse shapes of all (a) 27 qubits on IBM Toronto (b) 65 qubits on IBM Brooklyn (c) 127 qubits on IBM Washington machines.

1. Alexander et al., *Quantum Sci. Technol. 5, 044006* (2020)
2. Maurya & Tannu, *arXiv* 2212.03897 (2022)

Qubit Control Pulse Generation Pipeline

- Every quantum gate has a unique waveform for every physical gate supported by the system.
- In this example, the mixer helps with up-conversion (from MHz tone to suitable GHz tones).



1. Maurya & Tannu, *arXiv* 2212.03897 (2022)

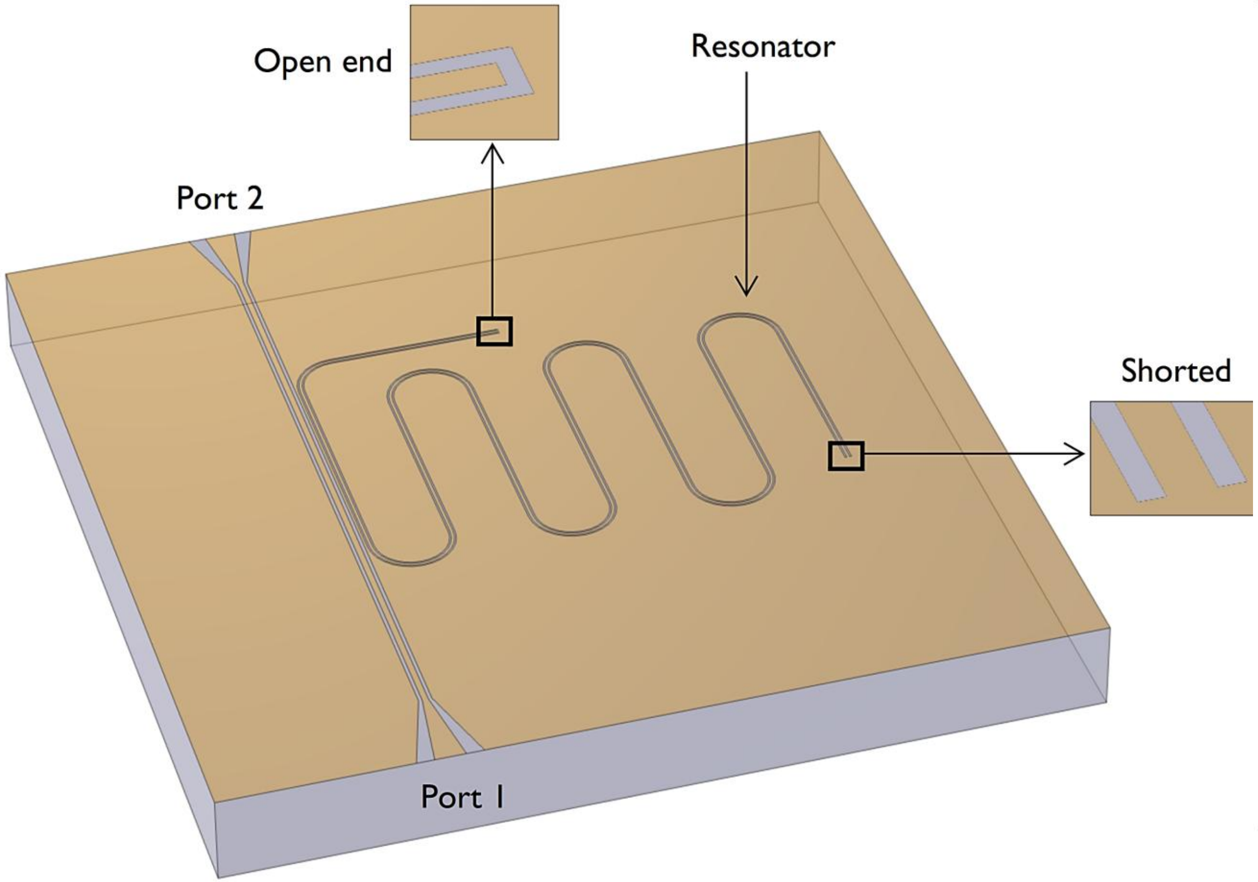
Sampling Snapshots & Buffering

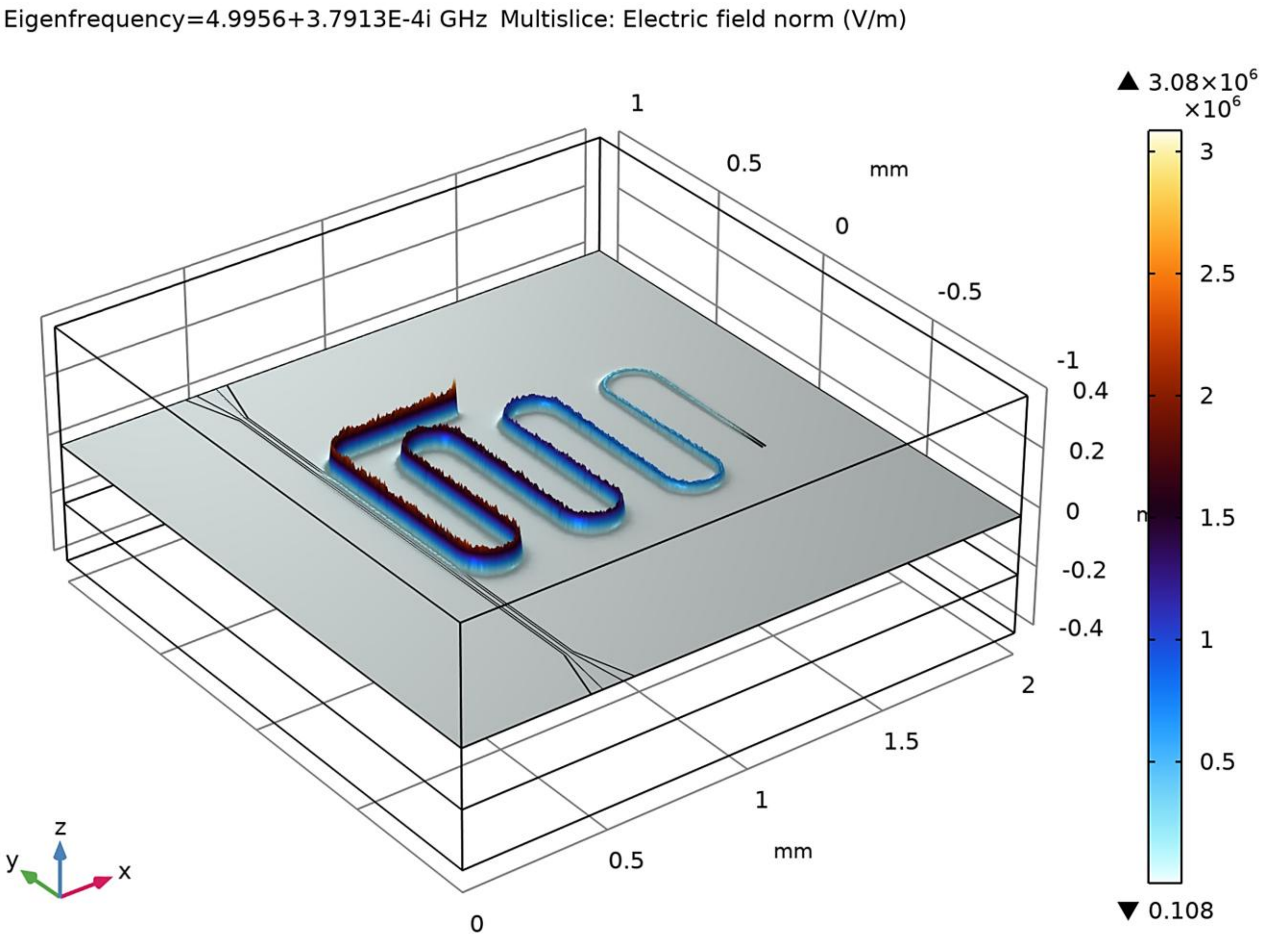
Stage	Does *sampling*?	What memory does here	Notes
I/Q mixer + baseband filter	No (continuous-time analog)	None	Analog down-conversion only
ADC (e.g., cryo SAR)	**ADC samples & quantizes**	Writes discrete samples to a small **FIFO/SRAM window**	Proven **1 GS/s, 6–8-bit Cryo-CMOS SAR ADC** for quantum readout; digitization moves inside the cryostat
Digital DDC/ integrator/ discriminator	No sampling; DSP on ADC stream	Uses **SRAM/FIFO** for short windows, accumulators, and classifier parameters	System papers describe a **digital state discriminator** that consumes the **digitizer output**; buffers are small (windowed) and power-aware

- 1 classical memory chip or macro is a buffer for sending quantum gate waveforms.
- 1 classical memory chip or macro is a buffer for receiving digitized quantum gate waveforms from the DAC. This is pretty much the reverse process.

1. Maurya & Tannu, *arXiv* 2212.03897 (2022)

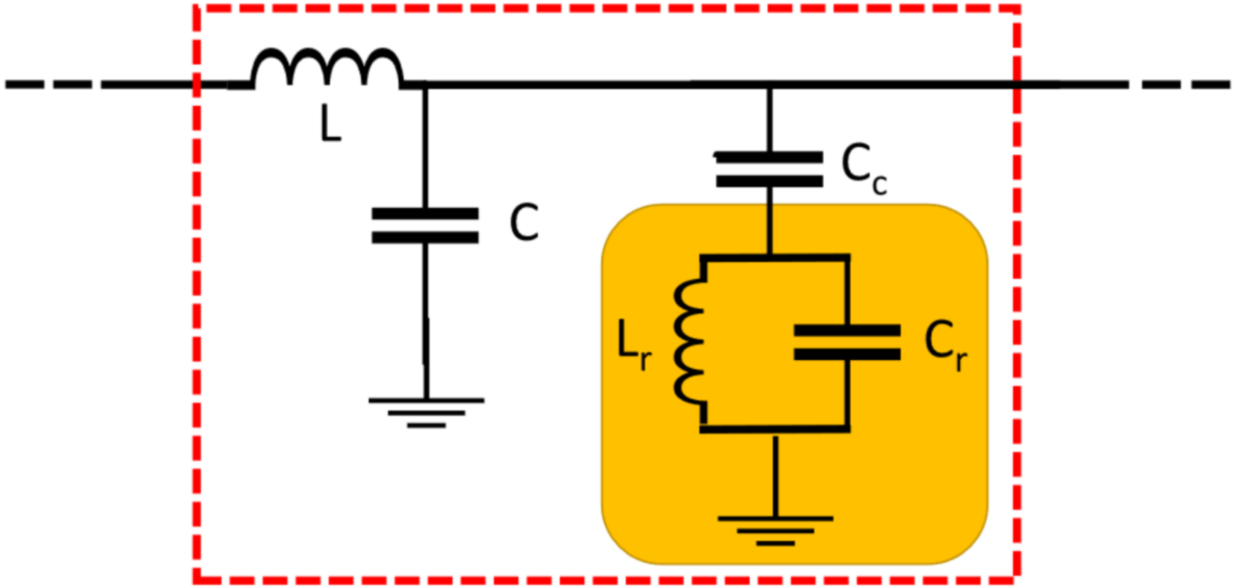
The Beauty of Abstractions in Superconducting Circuits



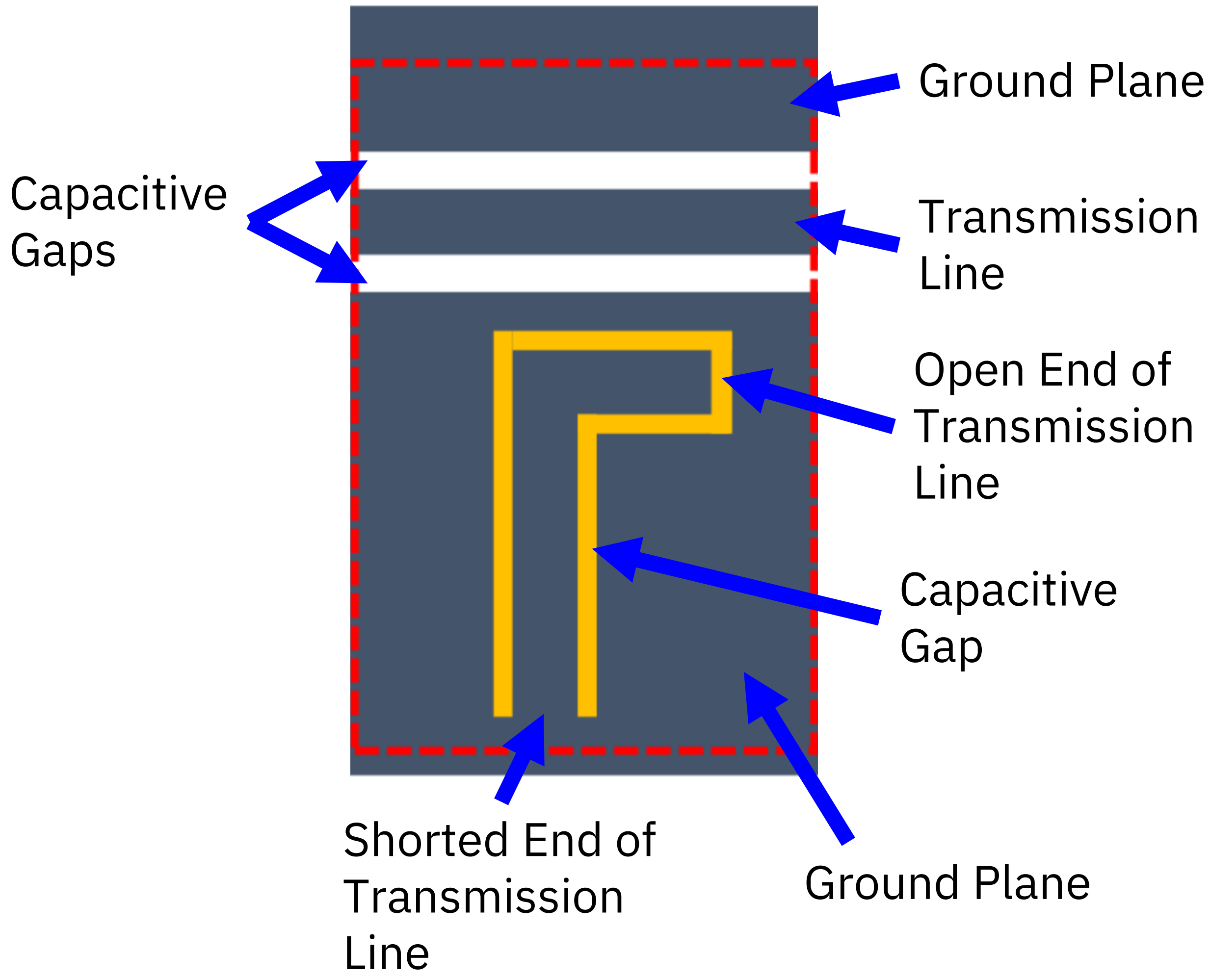


1. COMSOL: CPW Resonator for Circuit Quantum Electrodynamics

Coupled Coplanar Waveguide Resonator (Elbow)

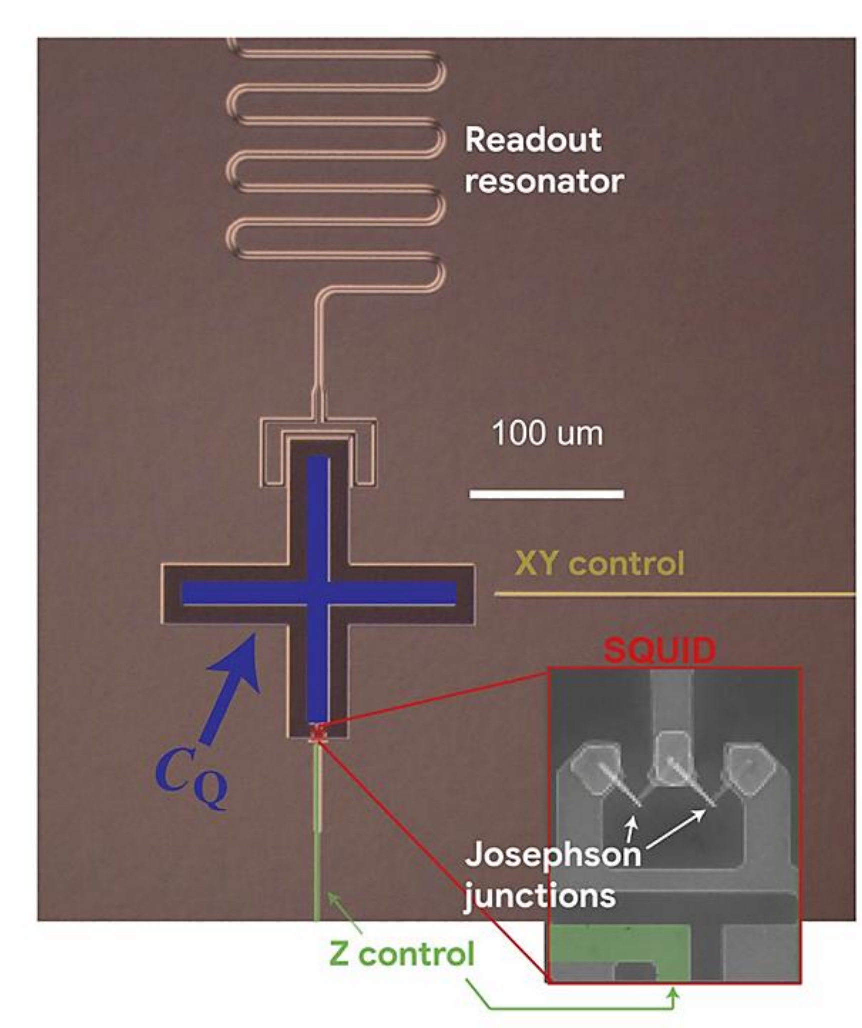


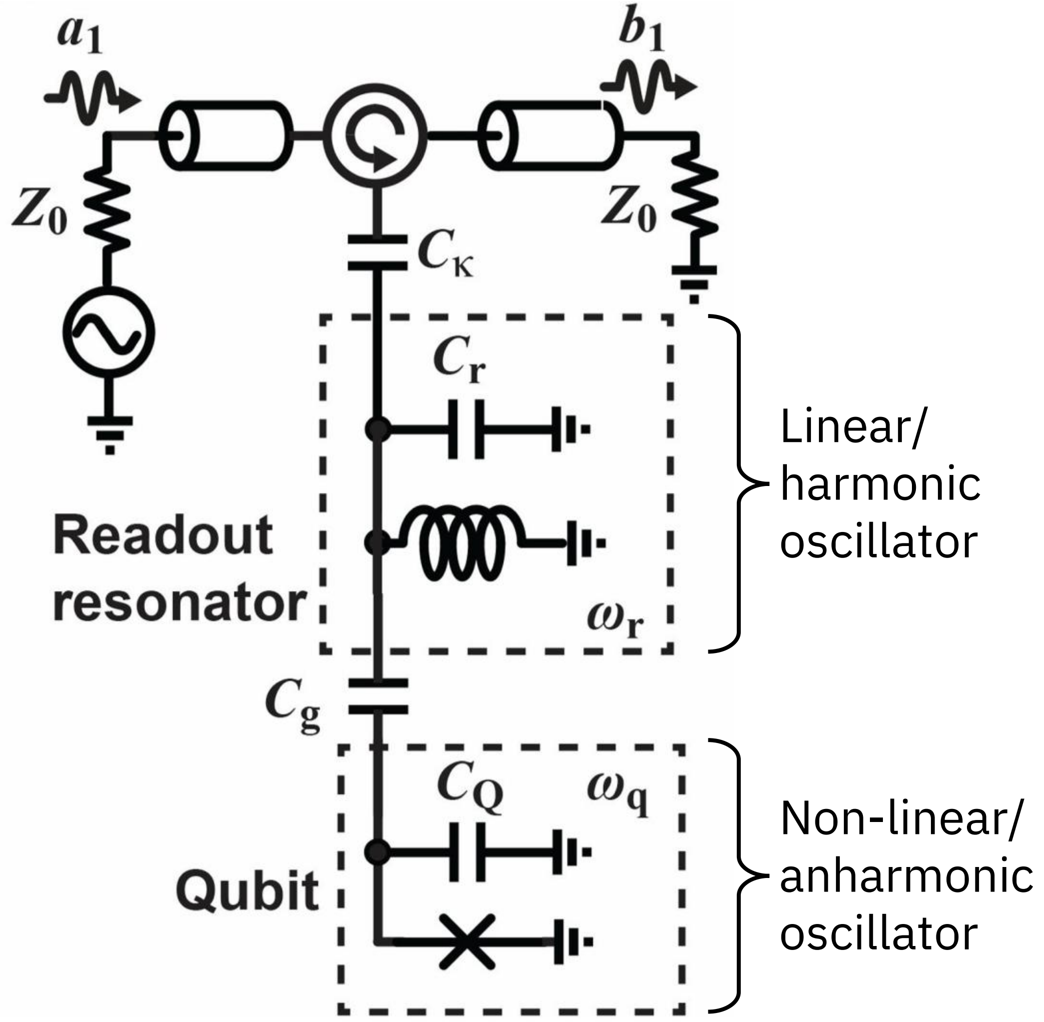
Lumped element equivalent circuit



1. Adapted from Sweetnam et al., *Supercond. Sci. Technol.* 35 095011 (2022)

Linear & Non-Linear Elements of a Superconducting Qubit





Achieves control of **collective phase-plasma-like excitations** (Cooper pairs)

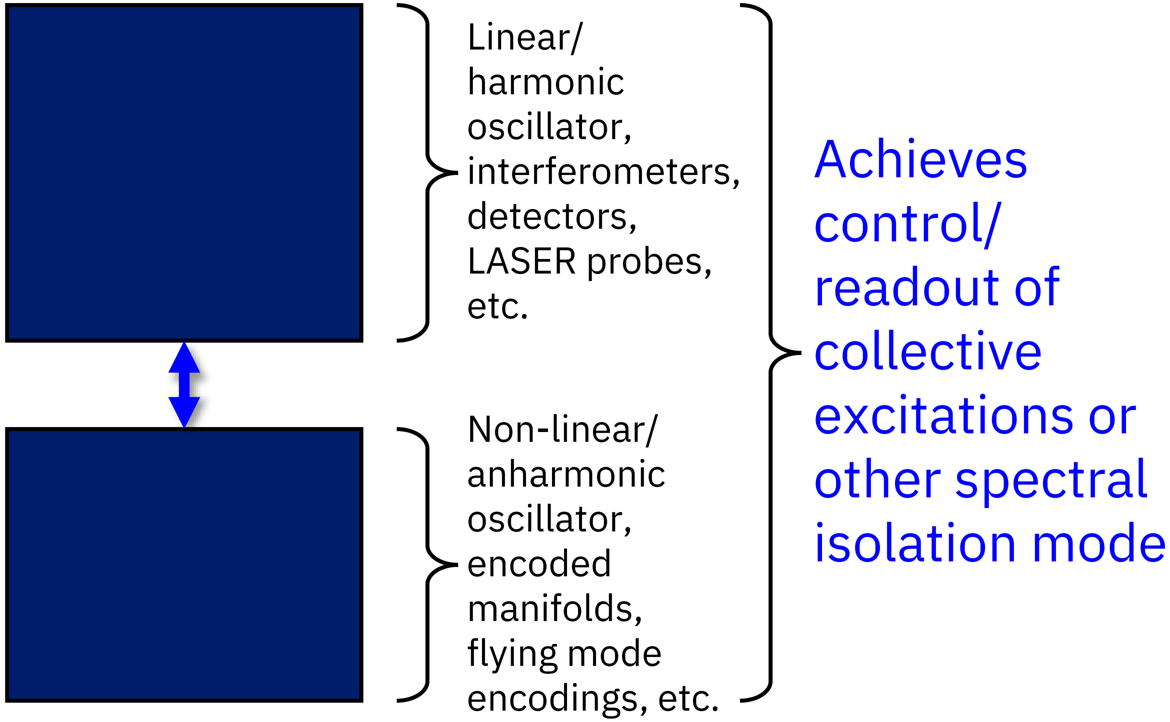
This is one way to physically simulate or mimic the excitation of a single atom.

1. Bardin et al., *IEEE J. Microw.* 1, 1 (2021)

Mechanism-Agnostic Elements of a Qubit

You will notice that **practical** selection and usage of a physical qubit requires for it to:

- Achieve spectral isolation so that T_1, T_2 comfortably exceed gate and measurement times
    - Examples under isolation: anharmonicity, selection rules, encoded manifolds, mode orthogonality, etc.
- Allow coherence engineering
- Allow scaling up
    - Often enabled through buses, memory, & transducers
- Be controllable of its quantum states using tailored electromagnetic (EM) fields (DC, RF, microwave, or optical) or magnetization fields/ textures with the carrier being of appropriate wavelength & noise levels



Practical Requirements For Qubit Implementation

```
Qubit-as-Mode
├─ Spectral isolation (mechanism-agnostic requirement)
│  A) Intrinsic anharmonicity (nonlinear oscillators/ circuits)
│  B) Selection rules & internal level structure
│  C) Interaction-induced blockade/ many-body protection
│  D) Confinement & quantization (spatial/ orbital/ band)
│  E) Encoded manifolds (bosonic/stabilizer protected subspaces)
│  F) Topological protection (gap + nonlocal encoding)
│  G) Mode orthogonality & interferometric isolation (photonic/flying-mode encodings)
│  H) Dispersion-/bandgap-engineered quasiparticles (frequency-k isolation)
│  I) Spin-texture doublets (prospective; texture-defined manifolds)
├─ Control & readout (pick mechanisms appropriate to each row)
│  ├─ Microwaves/flux (SC circuits) → dispersive cQED
│  ├─ Lasers (ions/atoms) → fluorescence, shelving
│  ├─ Photonics → interferometers + detectors
│  └─ Magnetization fields & spin textures (spintronics) → STT/SOT/VCMA, TMR/GMR, AHE/THE, MOKE, ISHE, FMR/BLS
├─ Coherence engineering (T1, T2 ≫ t_gate, t_read)
│  ├─ Materials & surfaces, filtering, shielding; sweet spots; dynamical decoupling
│  └─ From physical quality → QEC thresholds (surface code, bicycle/QLDPC, cat/GKP hybrids)
└─ Scale-up
   ├─ Connectivity graphs & couplers/buses
   ├─ Calibration stability & crosstalk control
   └─ Logical qubits via codes (surface, QLDPC/bicycle, cat/GKP hybrids)
```

Quantum Computing That Can Be Achieved Without Nanofabrication

Qubit carrier (microscopic)	Gate mechanism	Typical "lab-bench" hardware (macroscopic)	Measurement
Liquid-state NMR (nuclear spins in molecules floating in a beaker)	RF pulse sequences implement universal gates on nuclear spins	Commercial NMR spectrometer, 10–30 MHz RF coils; no vacuum, no cryogenics if you use a permanent-magnet benchtop unit	Inductive voltage in same RF coil (macroscopic signal from $\gtrsim 10^{18}$ molecules)
Trapped ions (e.g. $^{40}Ca^{+}$, $^{171}Yb^{+}$)	Laser-driven stimulated-Raman or Mølmer–Sørensen gates	Millimetre-scale metal-rod Paul trap, table-top lasers (~100 µm beam waist), vacuum at 10^{-9} mbar	Fluorescence counted by photomultiplier/APD
Neutral atoms in optical tweezers / optical lattices	Rydberg blockade or spin-exchange gates	Commercial diode lasers & objective lens; glass vacuum cell; spatial-light-modulator for tweezer array	Fluorescence imaging onto a CCD
Linear-optics quantum computing	Hong–Ou–Mandel interference; wave-plate phase shifters	Off-the-shelf mirrors, beamsplitters, Pockels cells, optical fibres	Single-photon avalanche diodes
NV centres in bulk diamond	Microwave pulses + optical spin-selective shelving	One diamond crystal; microwave stripline printed on FR-4; 532 nm laser; room-temperature operation	Spin-dependent fluorescence into an objective

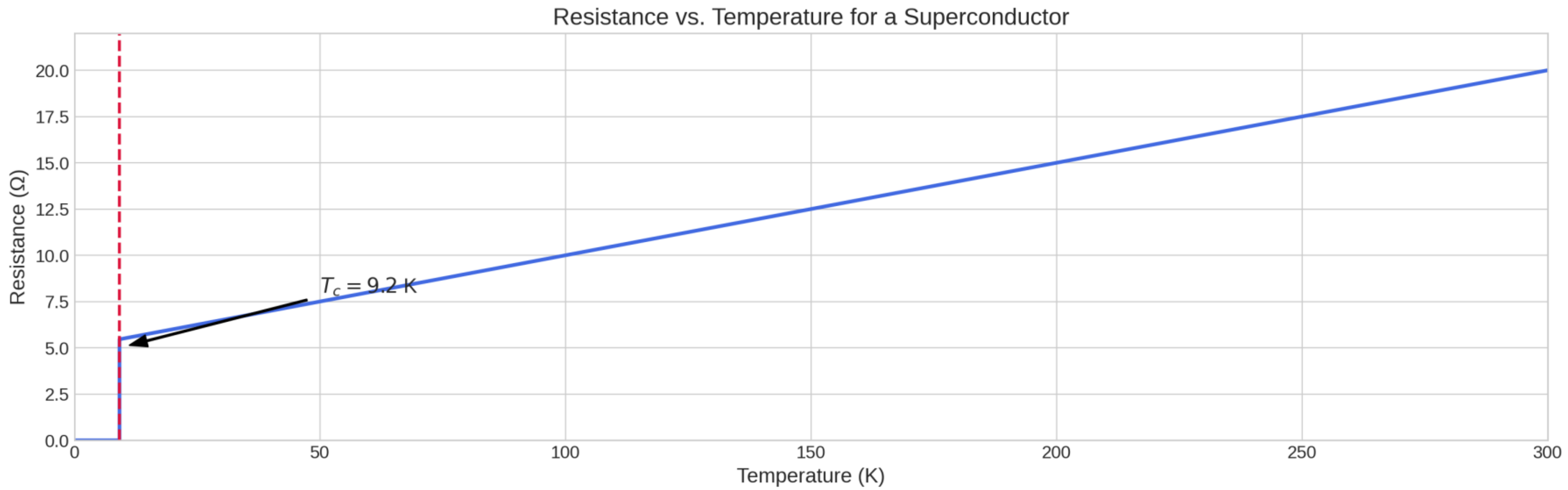
Key limitation is solid-state scalability, lack of strong on-chip coupling.

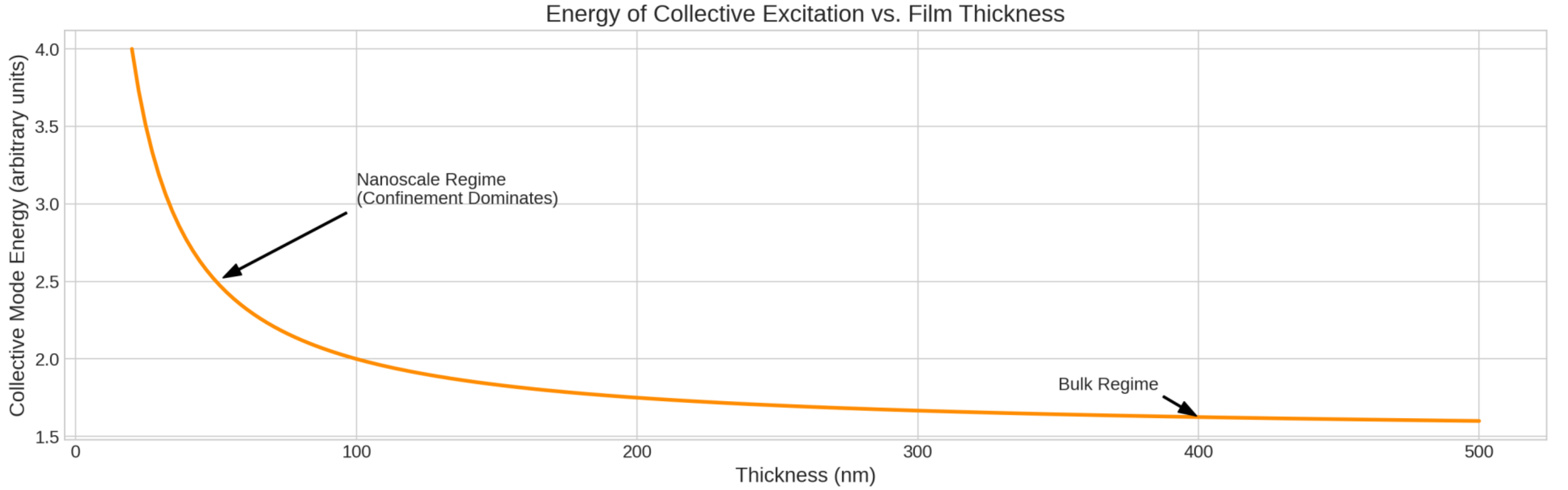
Quantum Computing That Can Be Achieved With Nanofabrication

Feature	Description
DiVincenzo Criteria + Precision Apparatus + Memory (classical + quantum)	The foundational requirements for a scalable quantum system: the DiVincenzo criteria, high-precision measurement/control apparatus, and both classical and quantum memories.
System Stack	Microscopic qubit carrier (programmable 2-level atom [natural or synthetic]) → apparatus → control/sampling (mixed-signal components) → memories.
Embedded Chip Components	All layers except the qubit carrier are chip-integrated, enabling precise control/observation and the ability to tie thousands to millions of qubits into a fault-tolerant system.
On-Chip Metrology	Integrated, real-time quantum-adjacent device health monitoring for in-situ metrology and device-level diagnostics.
Quantum Memory ↔ Transducer Coupling	Fabricated quantum memories interface with quantum transducers to enable long-range QPU-to-QPU coupling (entanglement bus) for modular quantum computing architectures.

Key advantage is solid-state scalability, strong on-chip coupling.

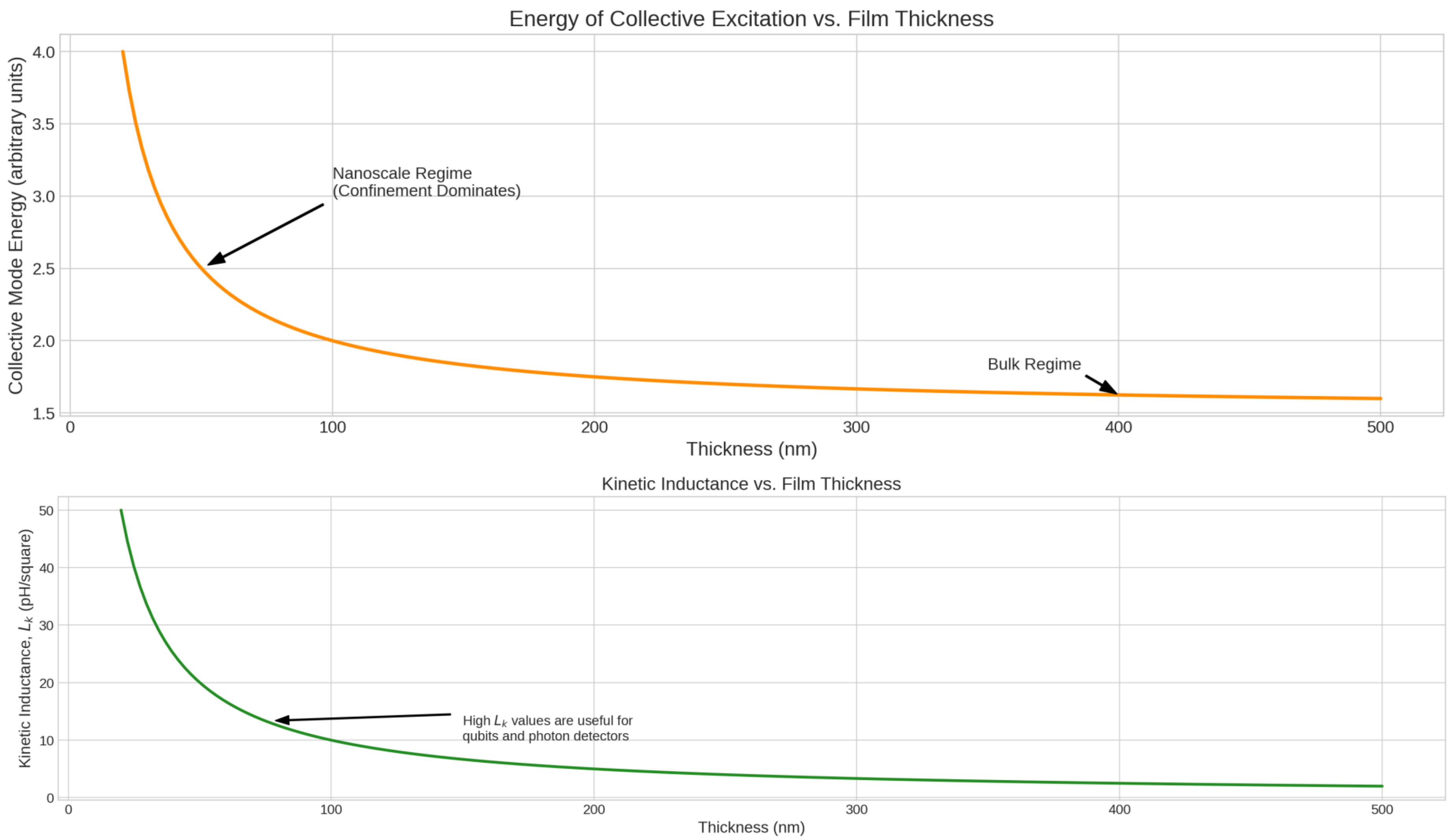
Towards Collective Excitations in a Superconductor





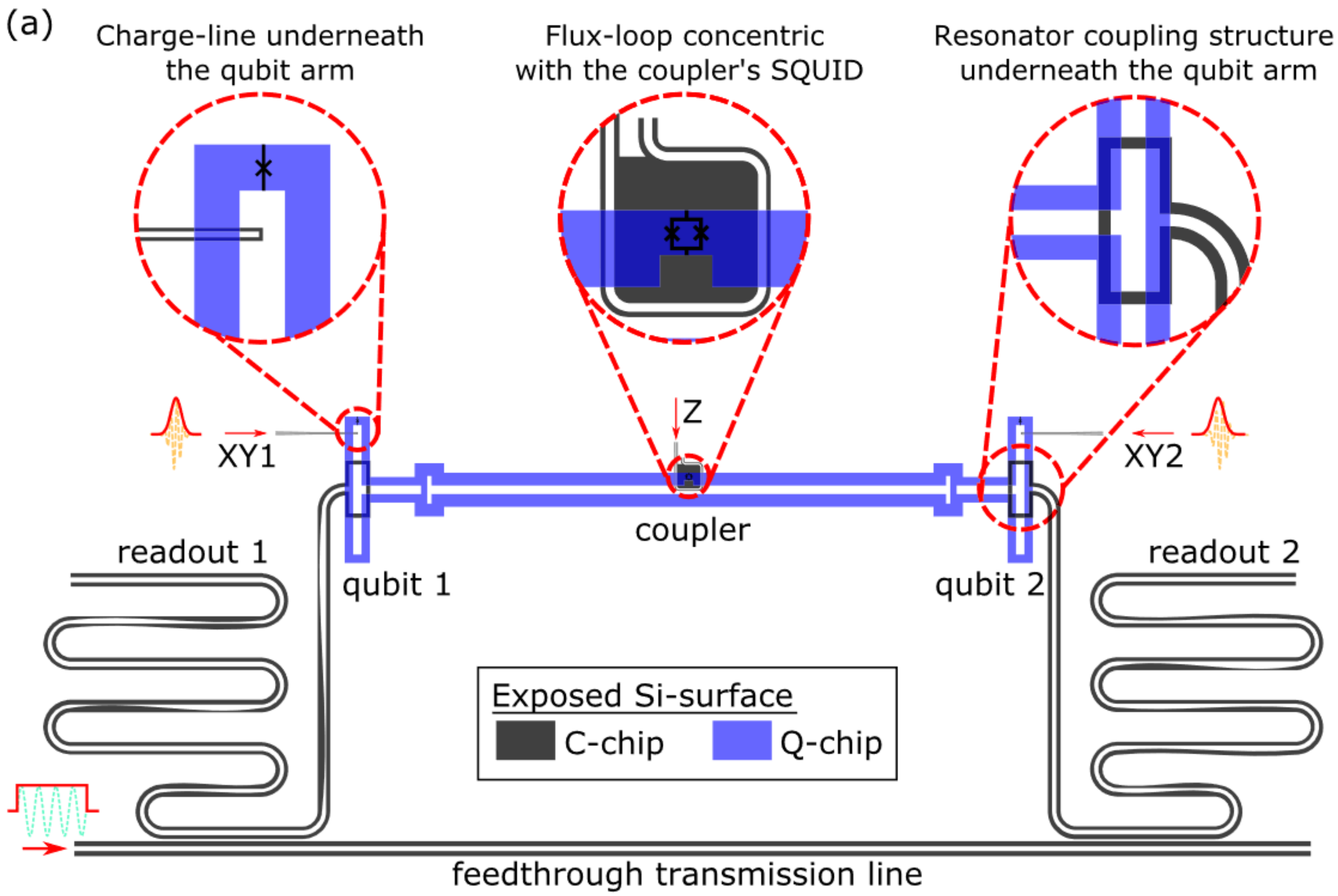
Collective excitations are very important for solid-state. As shown in the example above, it can be achieved by reducing the thickness and lowering the temperature of a quantum material (to its critical temperature).

Towards Collective Excitations in a Superconductor



Collective excitations are very important for solid-state. As shown in the example above, it can be achieved by reducing the thickness and lowering the temperature of a quantum material (to its critical temperature).

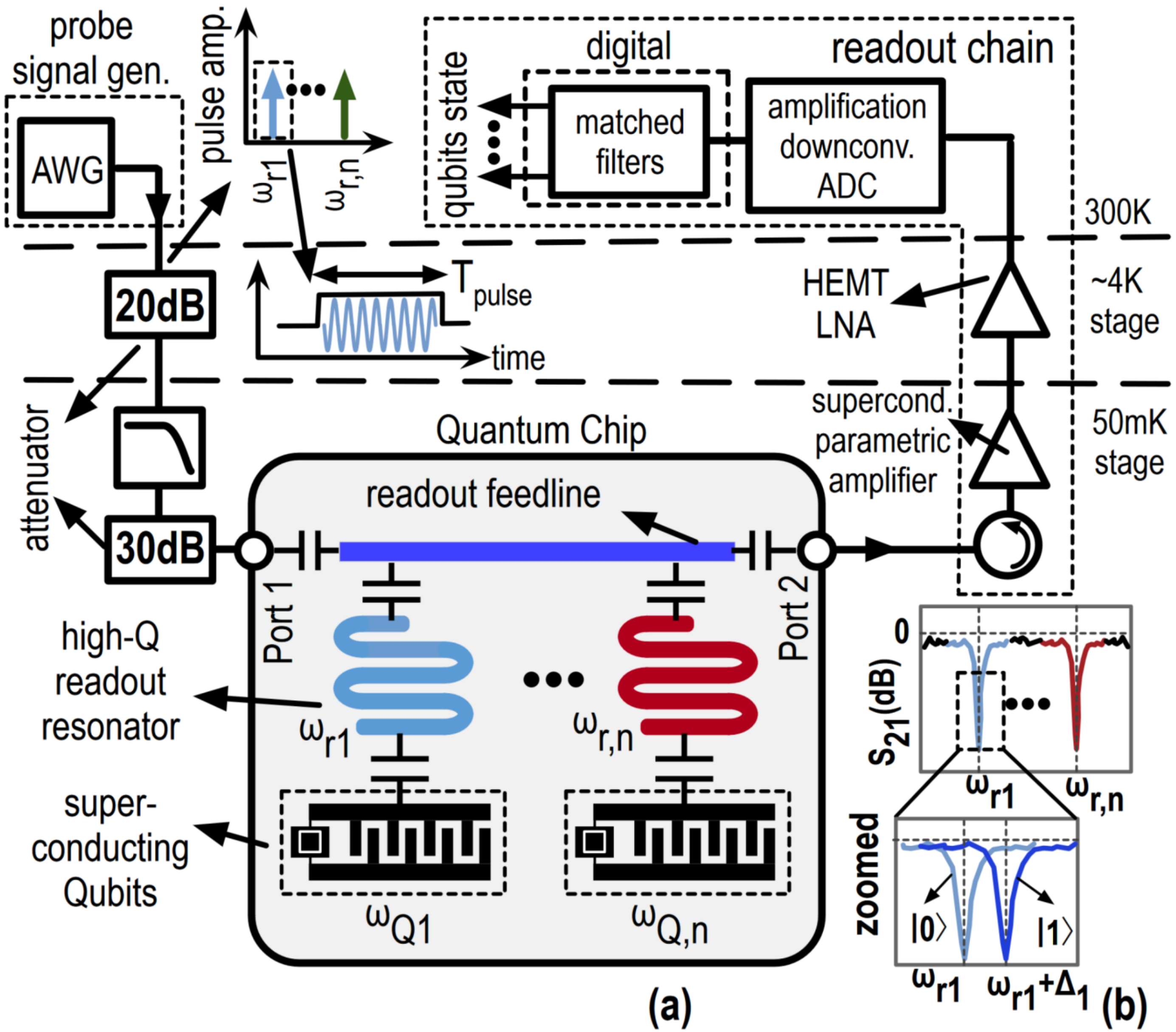
Linkable Quantum Computing Systems



Momentary flux tuning of the coupler temporarily turns on an entangling two-qubit interaction, then returns to idle to minimize ZZ. Here, ZZ is an undesired static two-qubit interaction (cross-Kerr).

1. Kosen et al., *Quantum Sci. Technol.* 7 035018 (2022)

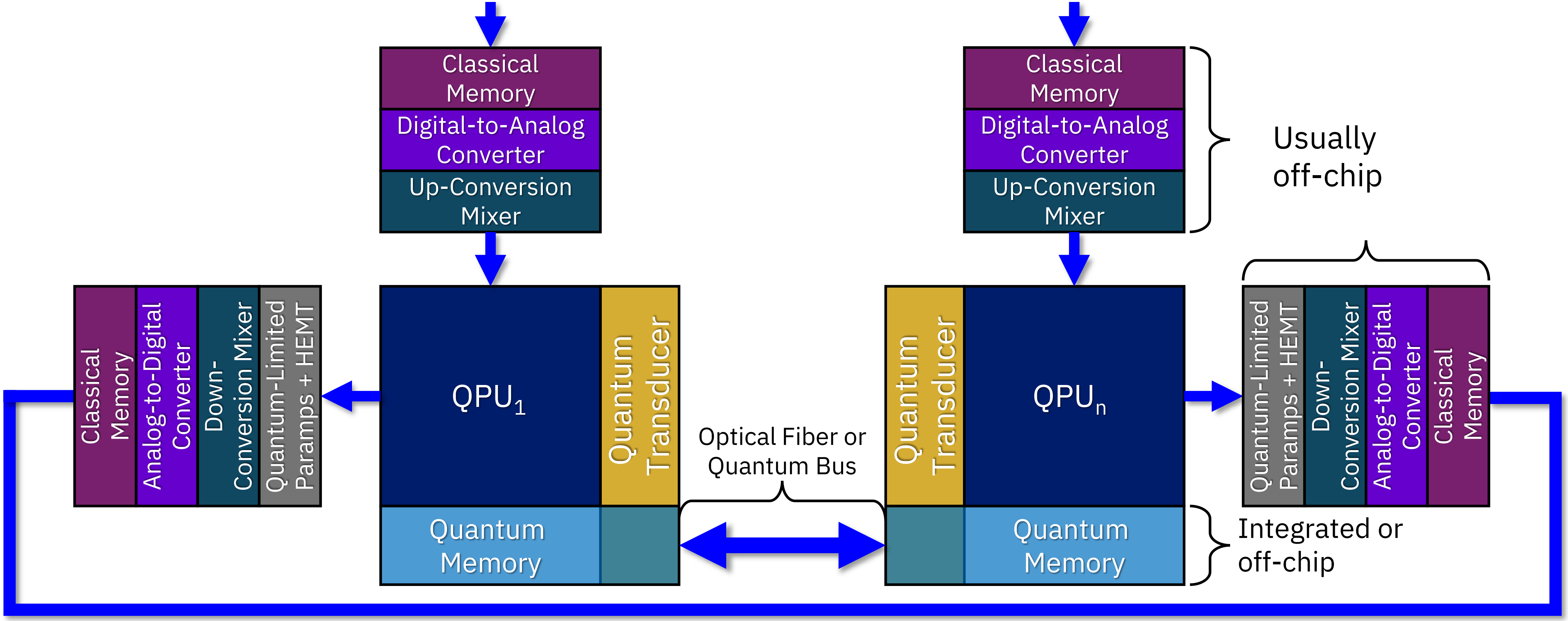
Linkable Quantum Computing Systems



Other Entangling Mediators Per Qubit Platform Based on Hardware Scaling Requirements

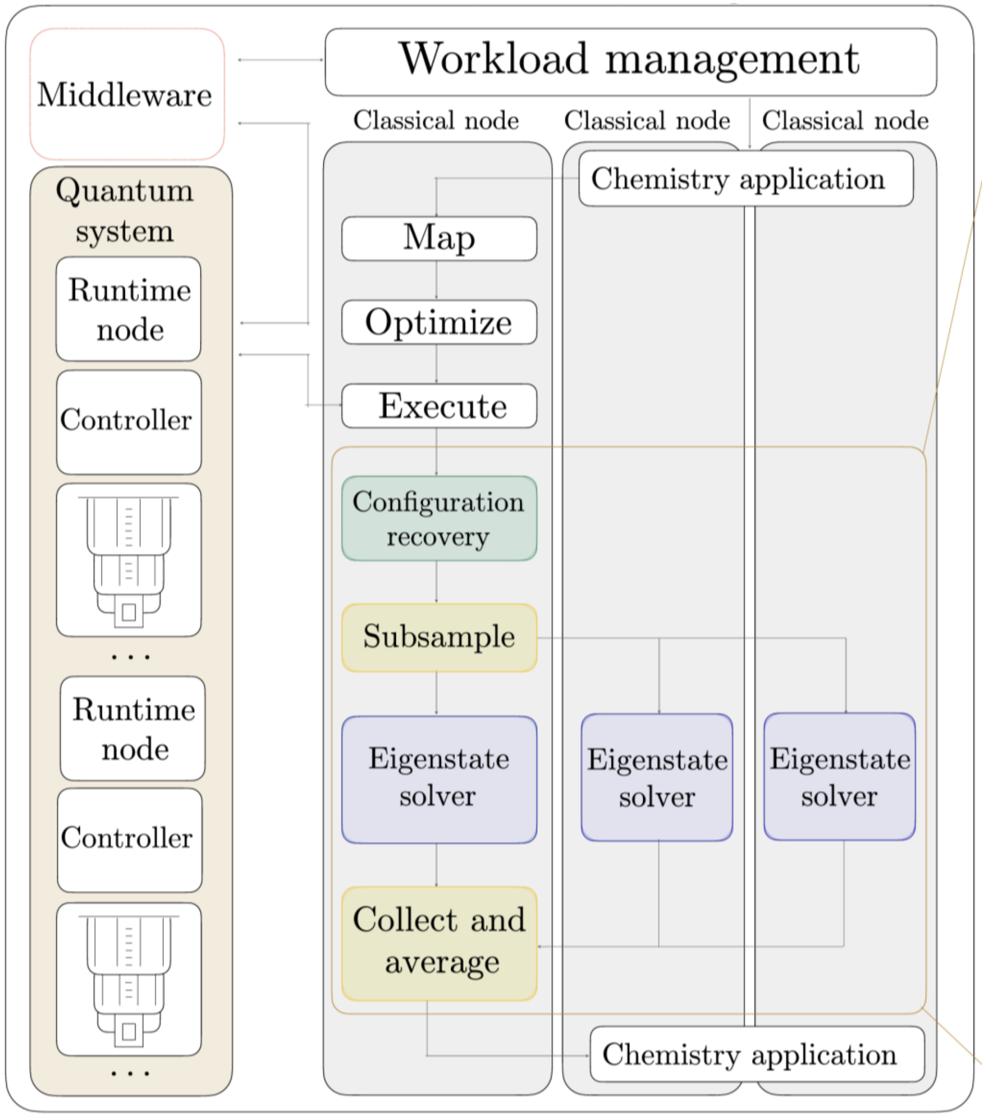
```
├─ Superconducting
│  ├─ Cross-Resonance →  ZX (drive-induced dispersive) → CNOT/eCR
│  ├─ Tunable Coupler  →  exchange/ZZ (flux or parametric) → CZ, iSWAP, fSim
│  ├─ Bus-RIP         →  dispersive ZZ (driven resonator) → CZ, multi-qubit phase
│  └─ MAP/CCR         →  engineered higher-levels/ exchange → CPHASE, iSWAP
├─ Trapped Ions
│  ├─ Mølmer-Sørensen →  XX/YY (spin-dep. force via phonons) → CNOT-equiv.
│  └─ Cirac-Zoller    →  sideband-mediated (phonon bus)      → CNOT
├─ Neutral Atoms
│  └─ Rydberg blockade → Ising-like ZZ (vdW shift)            → CZ/CNOT
├─ Semiconductor Spins
│  ├─ Exchange J(V)     →  Heisenberg/Ising-like              → CZ/CNOT/(√)iSWAP
│  ├─ Capacitive        →  dipole-dipole (charge-assisted)    → CZ/iSWAP-like
│  └─ cQED resonator    →  exchange via virtual photons       → iSWAP/fSim
├─ NV Centers
│  ├─ Spin-photon link →  heralded entanglement               → Bell/parity ops
│  └─ Dipolar (local)  →  secular dipole terms                → CZ/SWAP-like
└─ Photonics
   ├─ Linear optics     →  measurement-induced nonlinearity   → CZ/CNOT (prob.)
   └─ CV squeezing      →  Gaussian entanglers                → MBQC two-mode ops
```

QPU-to-QPU Connections for Quantum Supercomputing

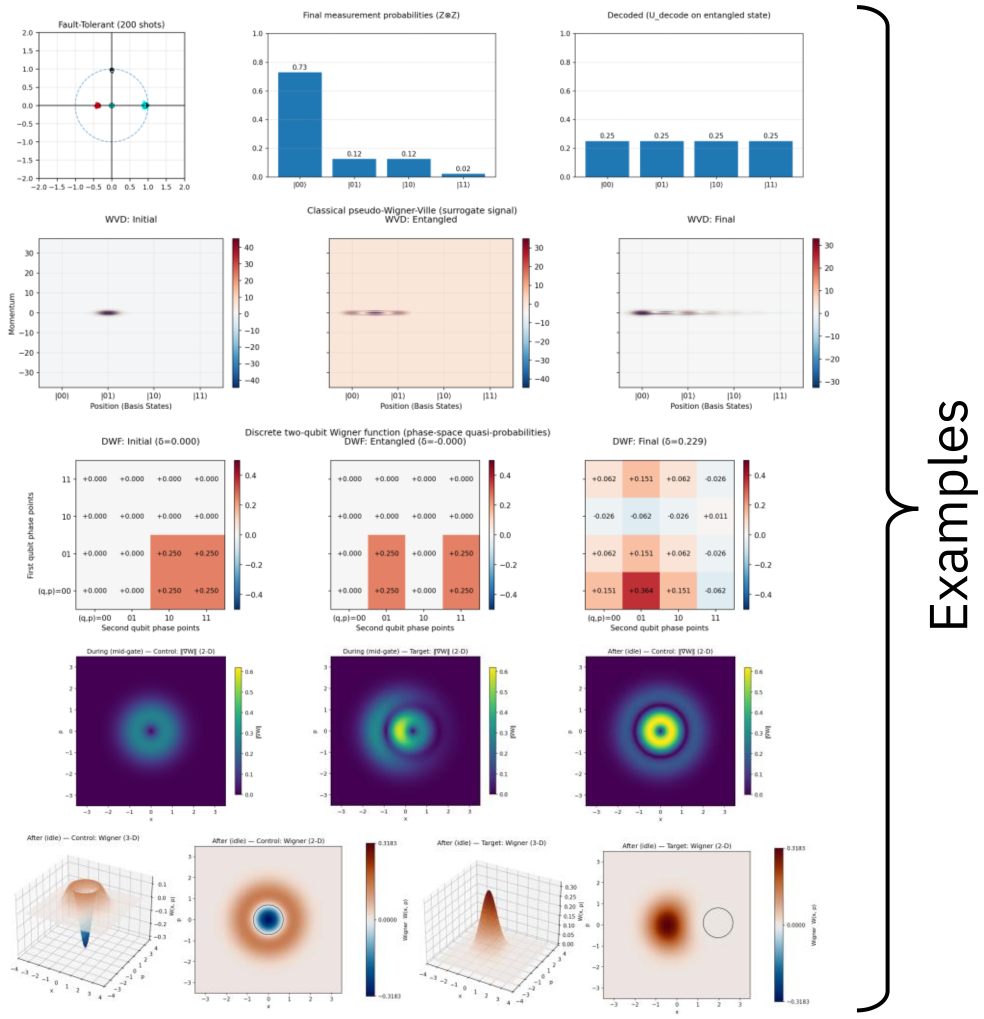


- Note that the quantum transducer chip here typically contains interfacial **metamaterial waveguide** structures that allow transmission of quantum information over a cable/wire (optical fiber or other quantum bus).
- The purpose of the classical memory is to store sampled quantum gate waveform data for feedback looping or data acquisition after it has been down-converted.

Quantum-Centric Supercomputing Cluster

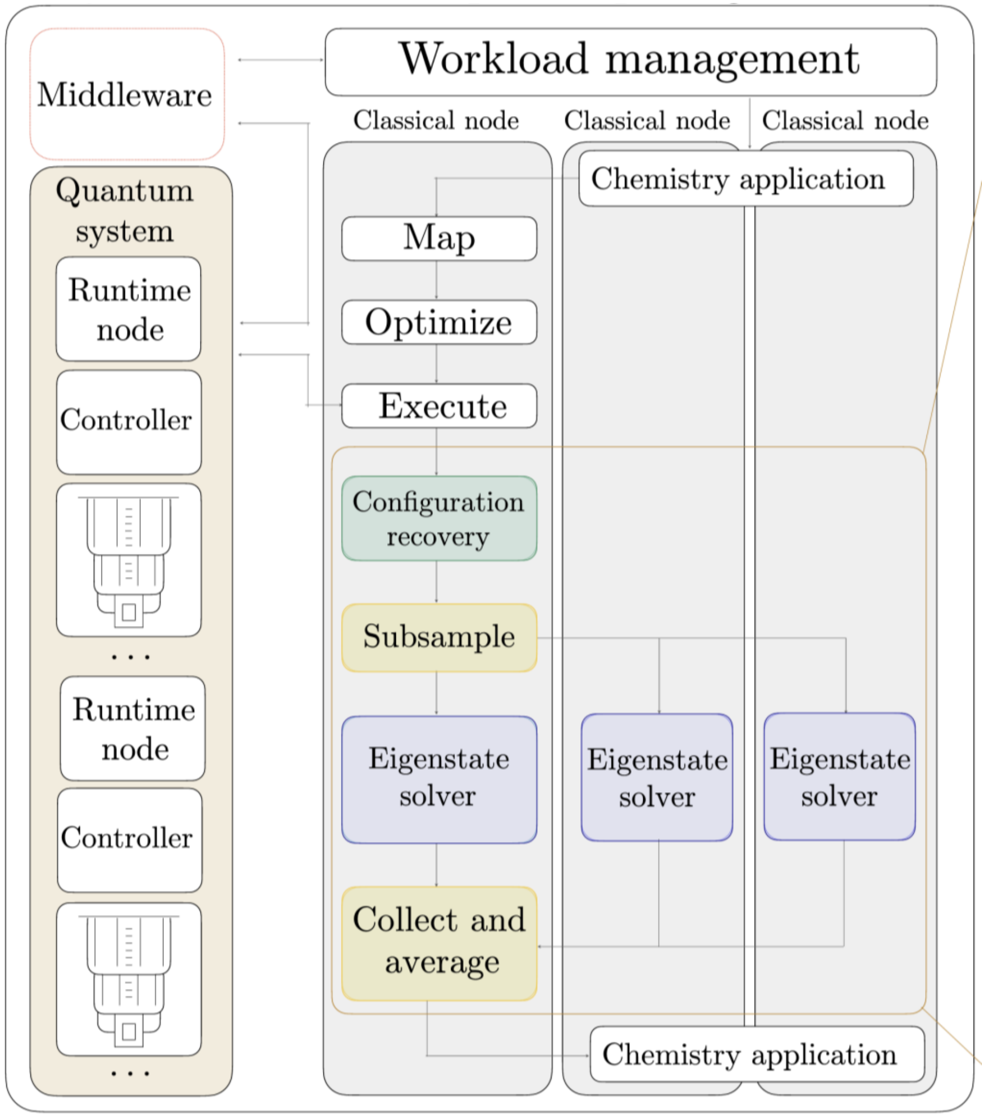


Post-Processing Results

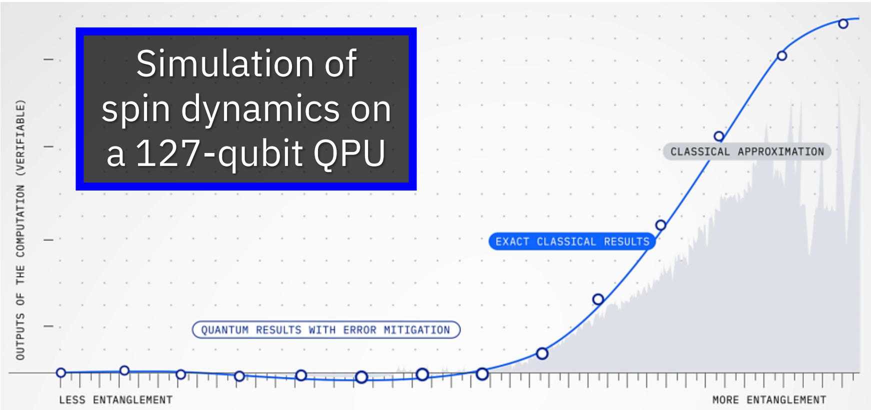


1. Adapted from Robledo- Moreno et al., *Sci. Adv.* 11, eadu9991 (2025)

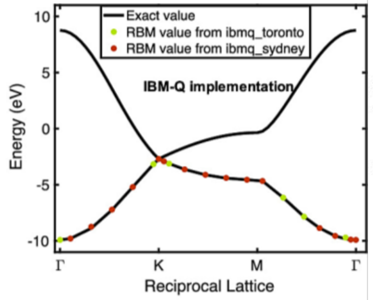
Quantum-Centric Supercomputing Cluster



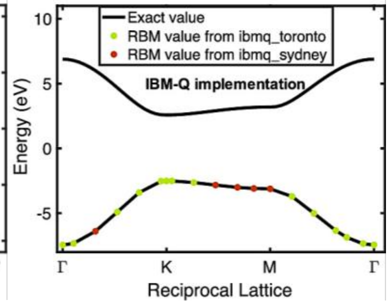
Post-Processing Results



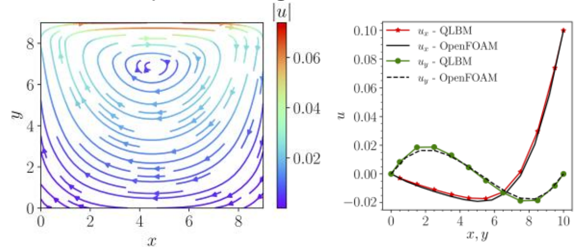
Simulation of Graphene Electronic Band Structure



Simulation of h-BN Electronic Band Structure



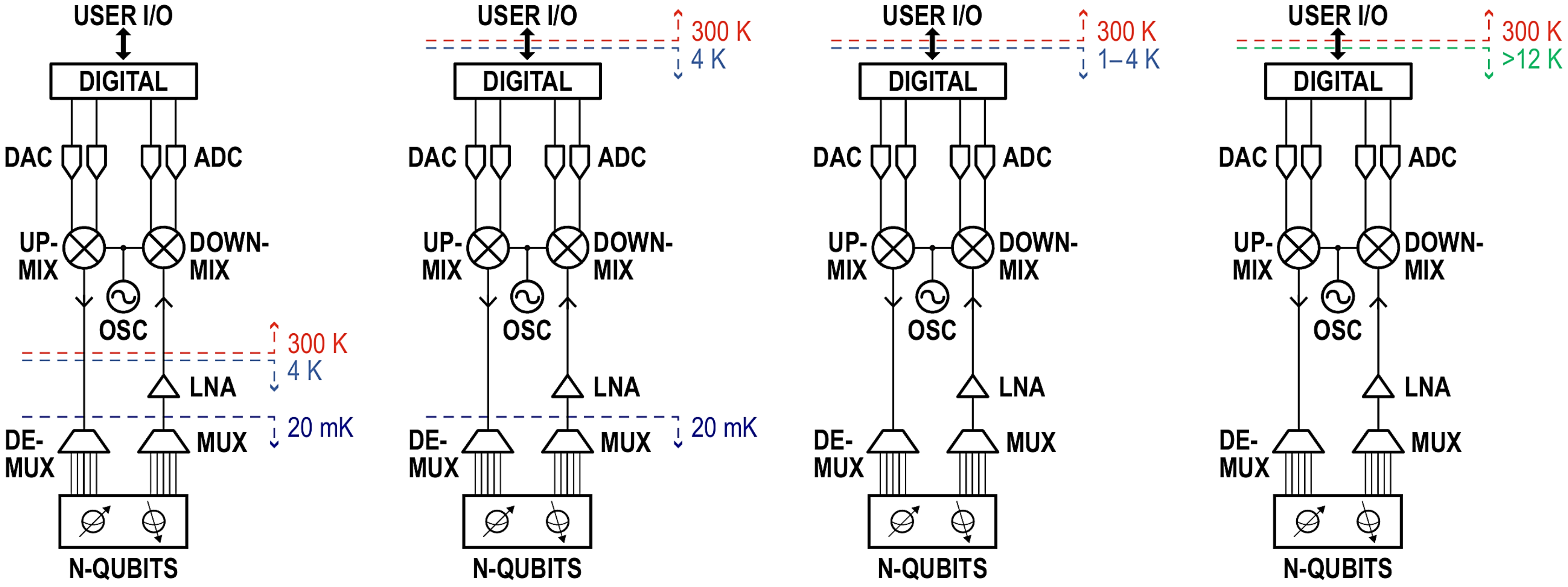
Simulation of Fluid Dynamics using Quantum Lattice Boltzmann Method



Examples

1. Adapted from Robledo- Moreno et al., *Sci. Adv.* 11, eadu9991 (2025)
2. Kim et al., *Nature* 618, 500–505 (2023)
3. Sureshbabu et al., *J. Chem. Inf. Model.* 61, 6, 2667–2674 (2021)
4. Kumar et al., *arXiv* 2405.08669 (2024)

Linkable Quantum Computing Systems (Architecture Level)



Currently Available | Short Term | Near Future | Distant Future

1. Alakusu, et al., *PhD Thesis* (2021)

Common Cryostat Formfactors

Item	
Large-frame dilution refrigerator (DR).	DR available (Integrated or insert attachment)
Floor standing cryostat (cryogen-free PPMS-type).	
Floor standing cryostat (liquid cryogen Dewar type).	No DR available

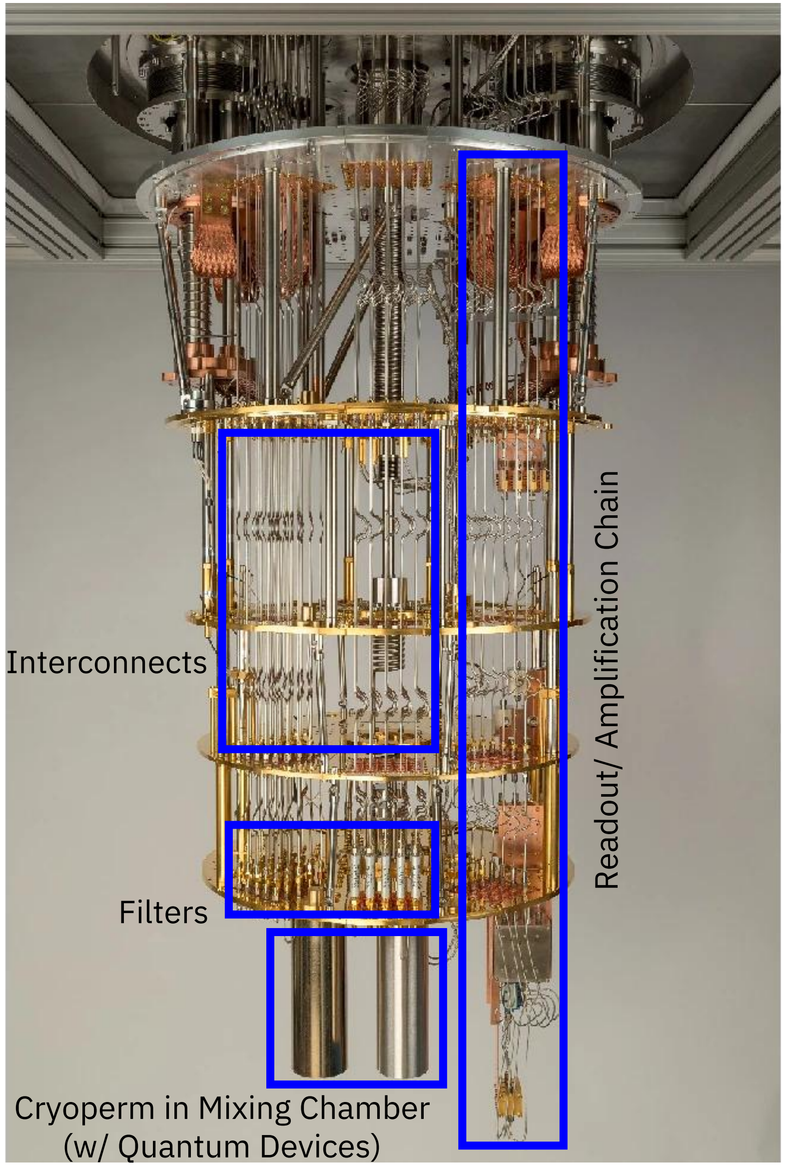
Can be rendered in 3D and with ray tracing in **Blender** for educational purposes.

Dilution Fridge Measurement System

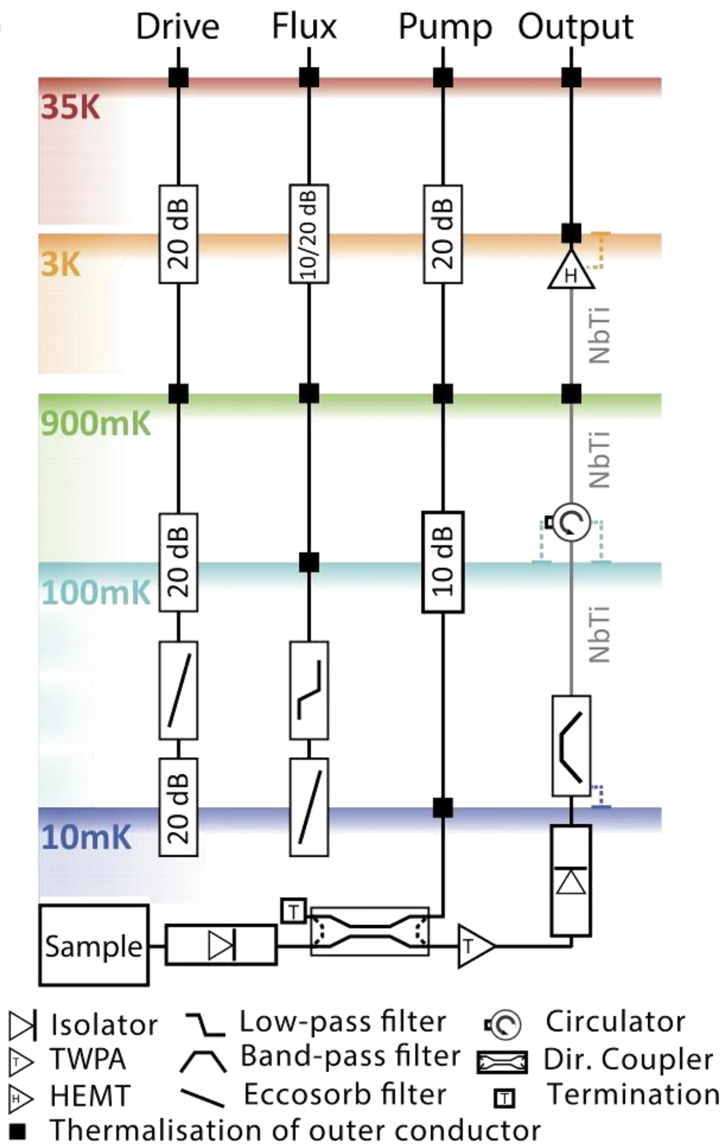
Measurement System

Mixing Chamber

a)

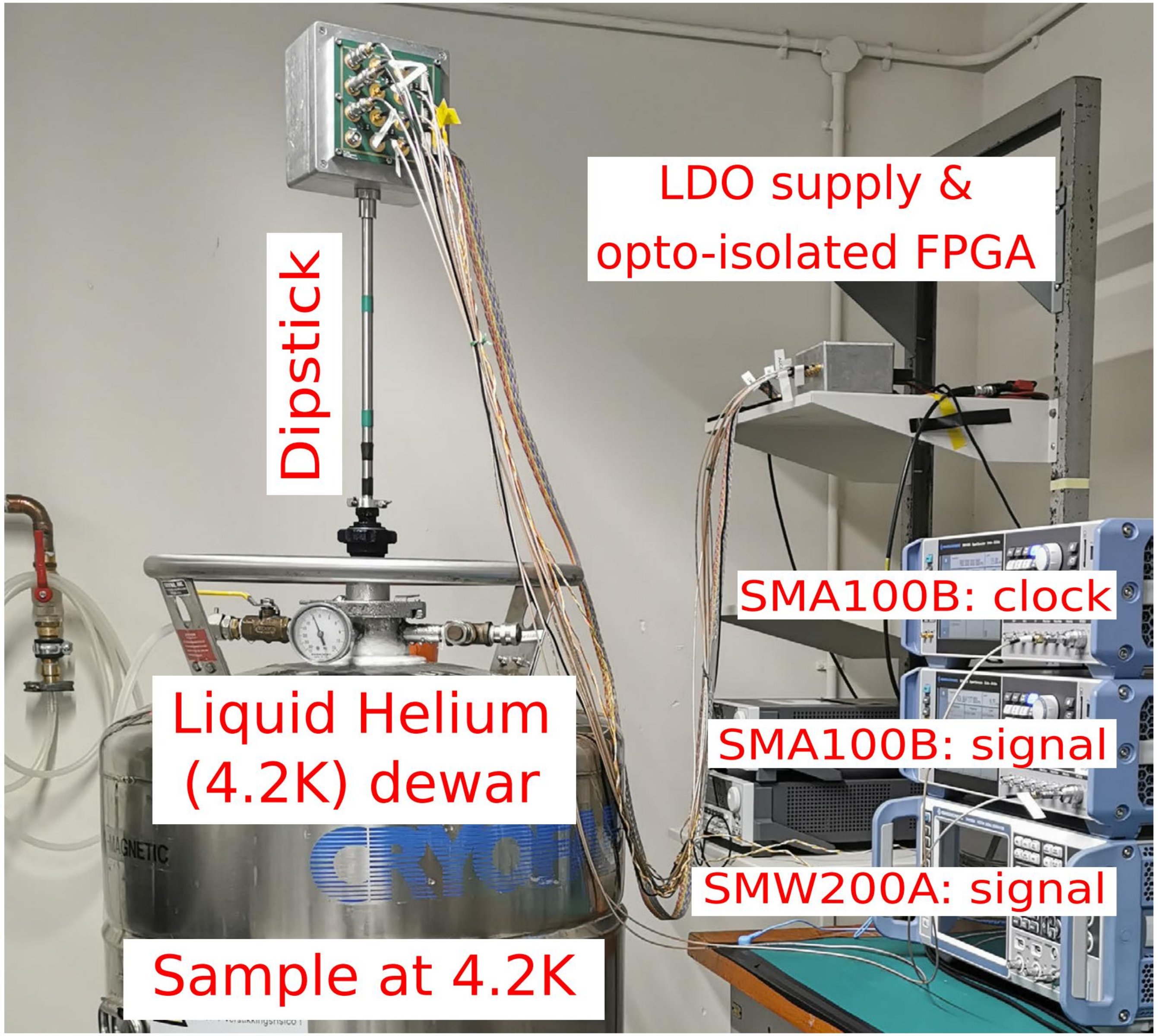


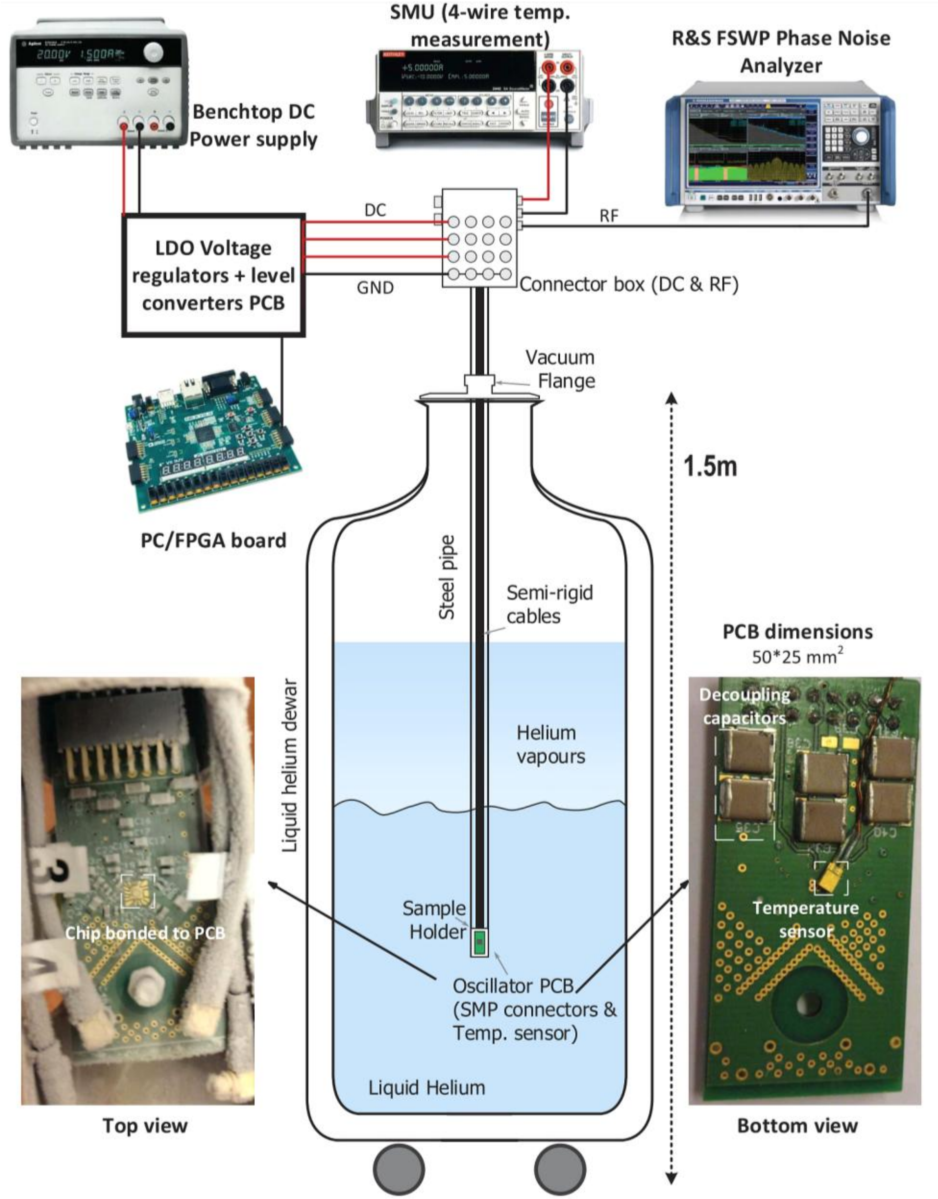
b)



1. Krinner et al., *EPJ Quantum Technol.* 6, 2 (2019)
2. Hollister, SQMS (2023)

External FPGA & Cryo-CMOS Control/Readout





1. Patra et al., *IEEE J. Solid-State Circuits* (2018)
2. Kiene et al., *IEEE J. Solid-State Circuits* (2023)

*LNA: Low Noise Amplifier

Cabling Options
(Depending on Signal Traffic/ Bandwidth Requirements)

Standard Coaxial Wiring

High-Density Coaxial Wiring

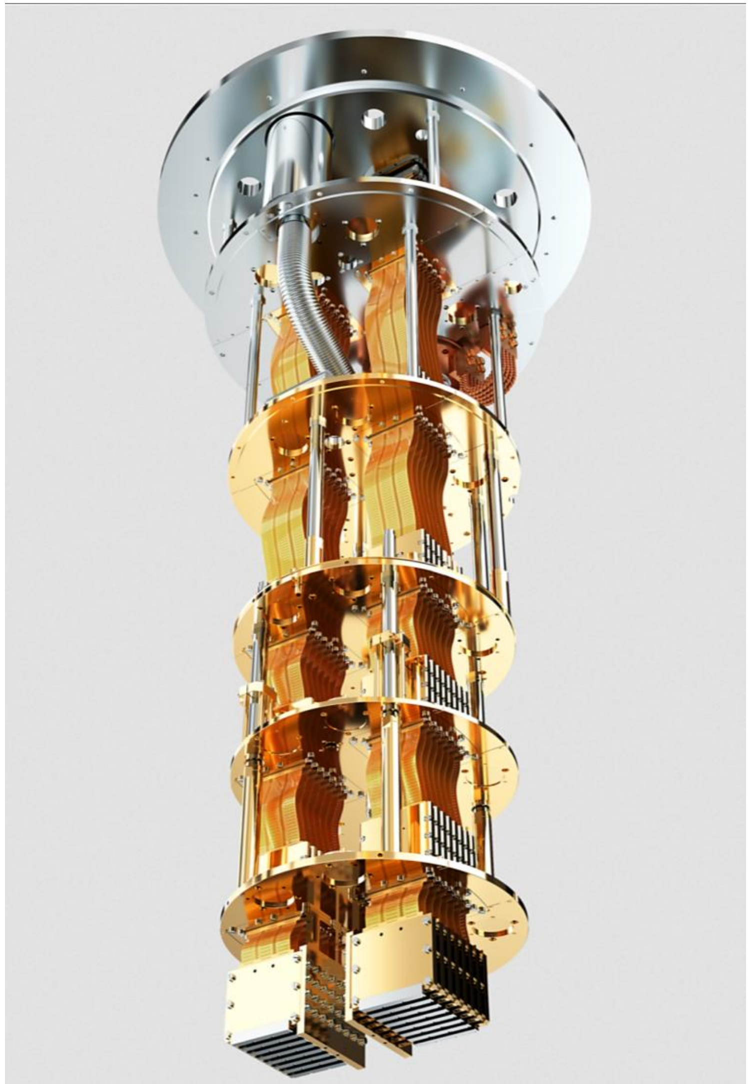
High-Density 'Ribbon' Flex Wiring

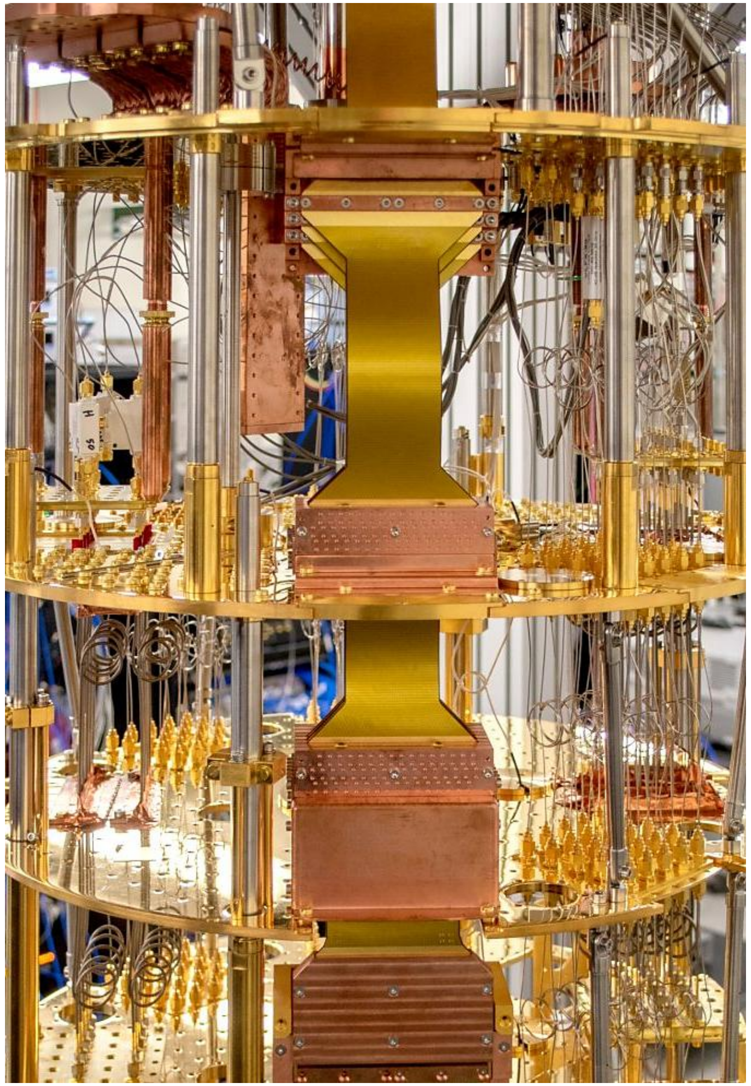
Cryogenic Optical Fiber

Increased Bandwidth Capability

1. Bluefors
2. Ardent Concepts

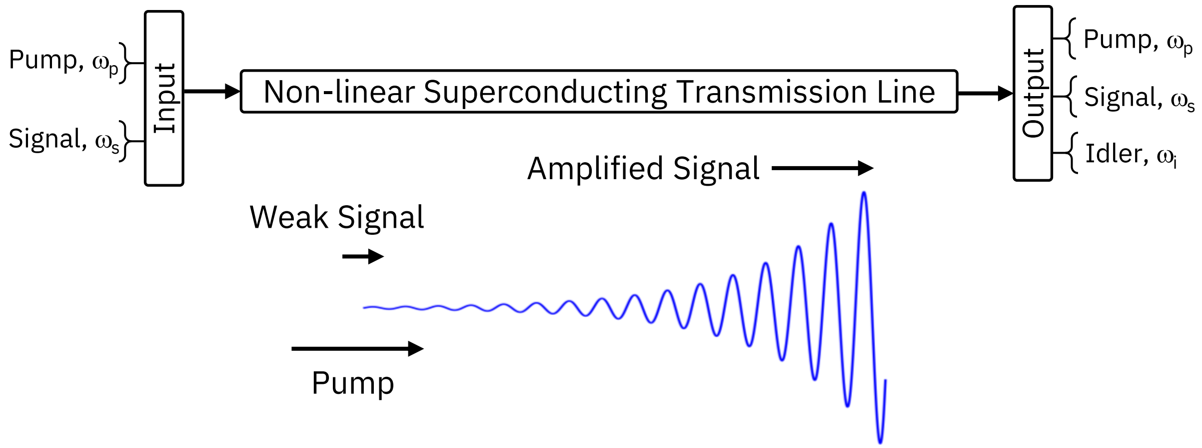
Closer Look at IBM & Bluefors High Bandwidth ‘Ribbon’ Flex Cables



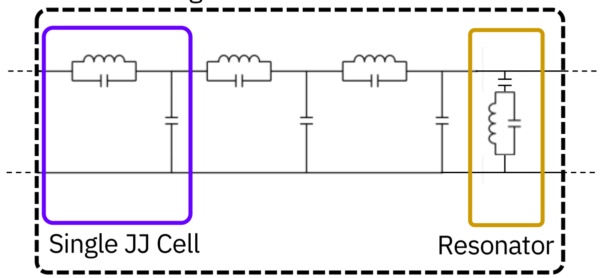


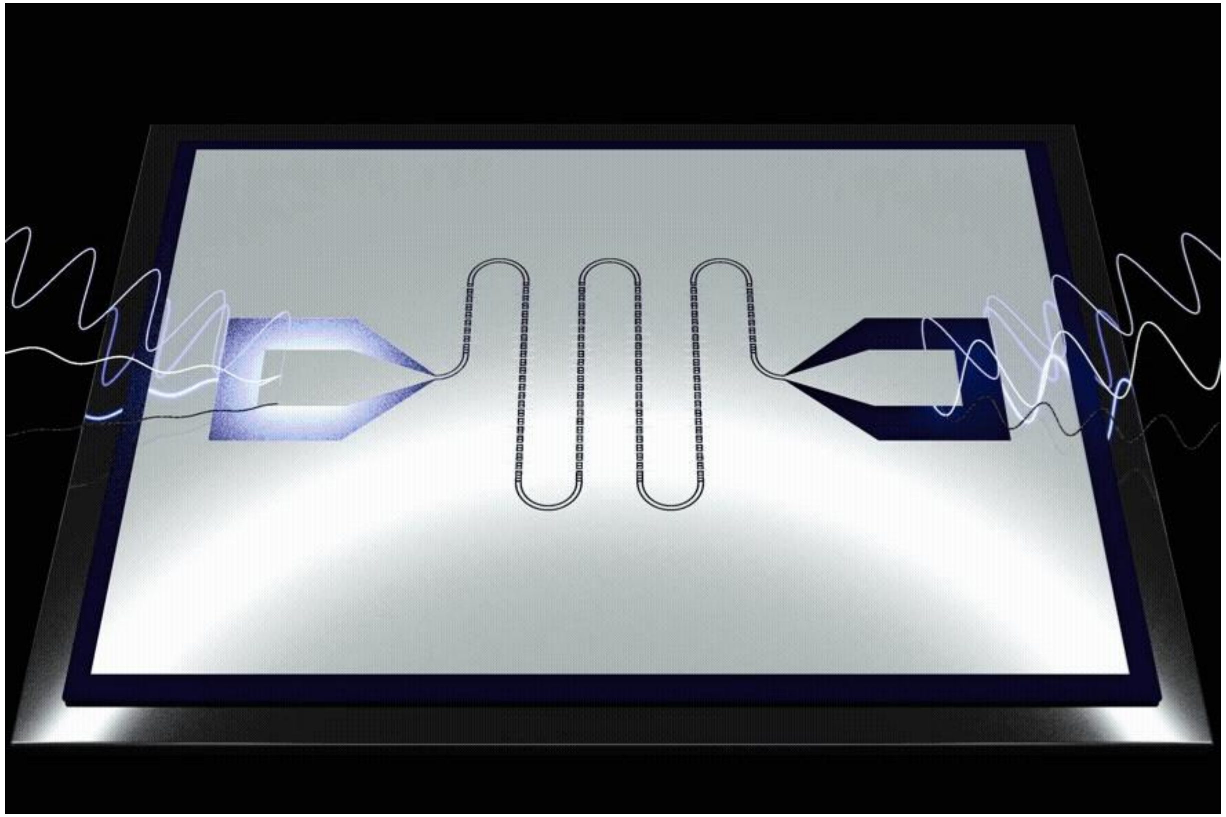
1. Bluefors
2. IBM Research

Josephson Traveling Wave Parametric Amplifiers (J-TWPAs)



Traveling Wave Parametric Amplifier



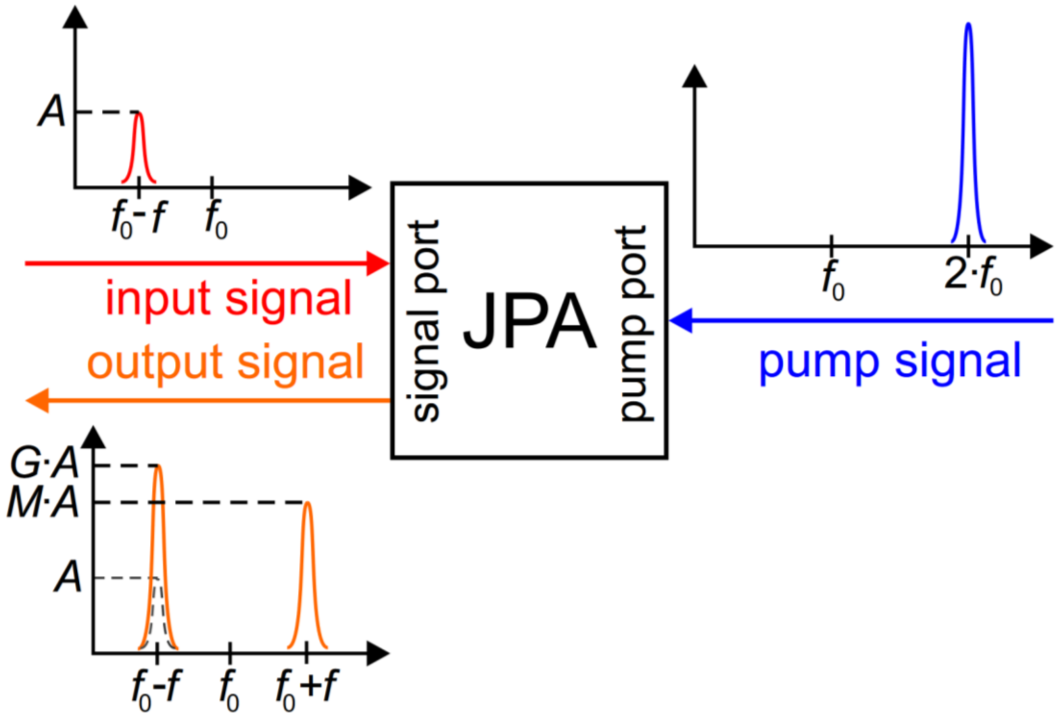


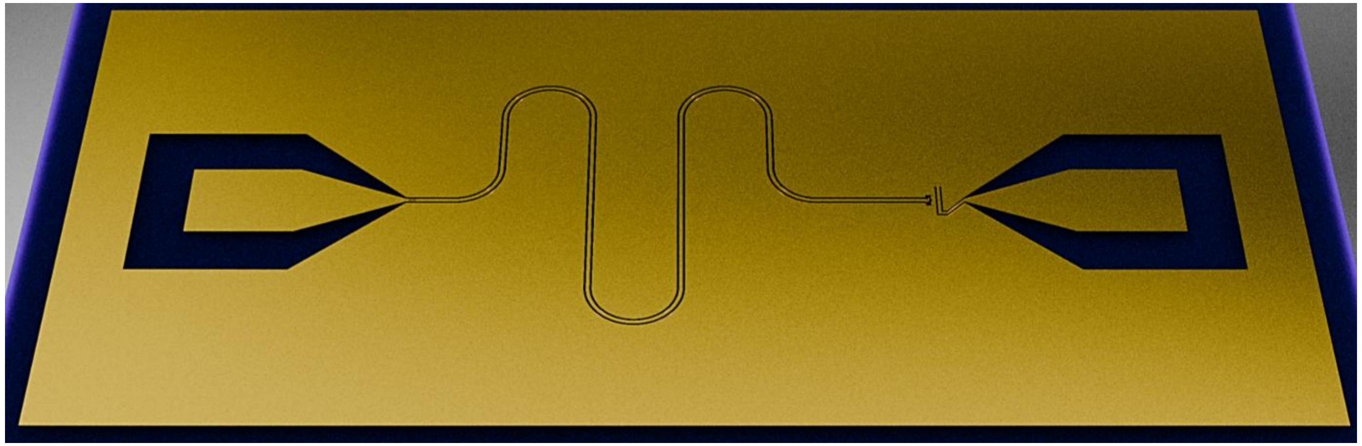
Blender Rendering of a J-TWPA Performing 3-Wave Mixing

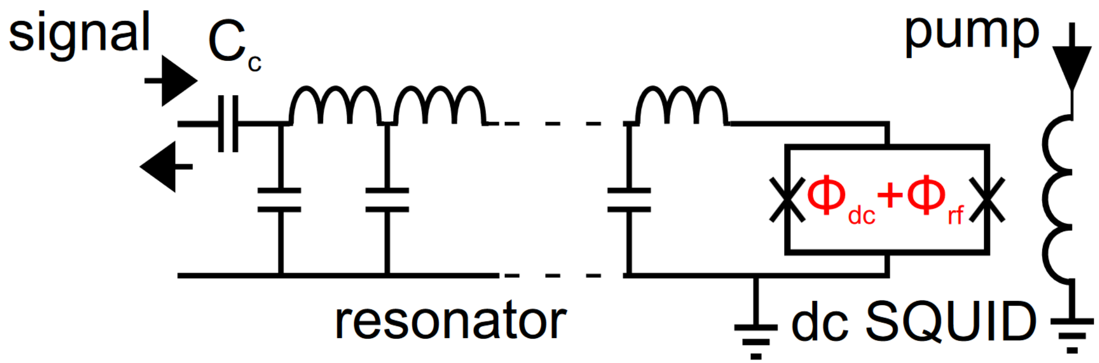
J-TWPA is transmissive mode device with high bandwidth.
It can perform 3 or 4 wave mixing (3WM or 4WM).

1. For more, check: Tan et al., UCMMT 8068511 (2017)

Josephson Parametric Amplifiers (JPAs)



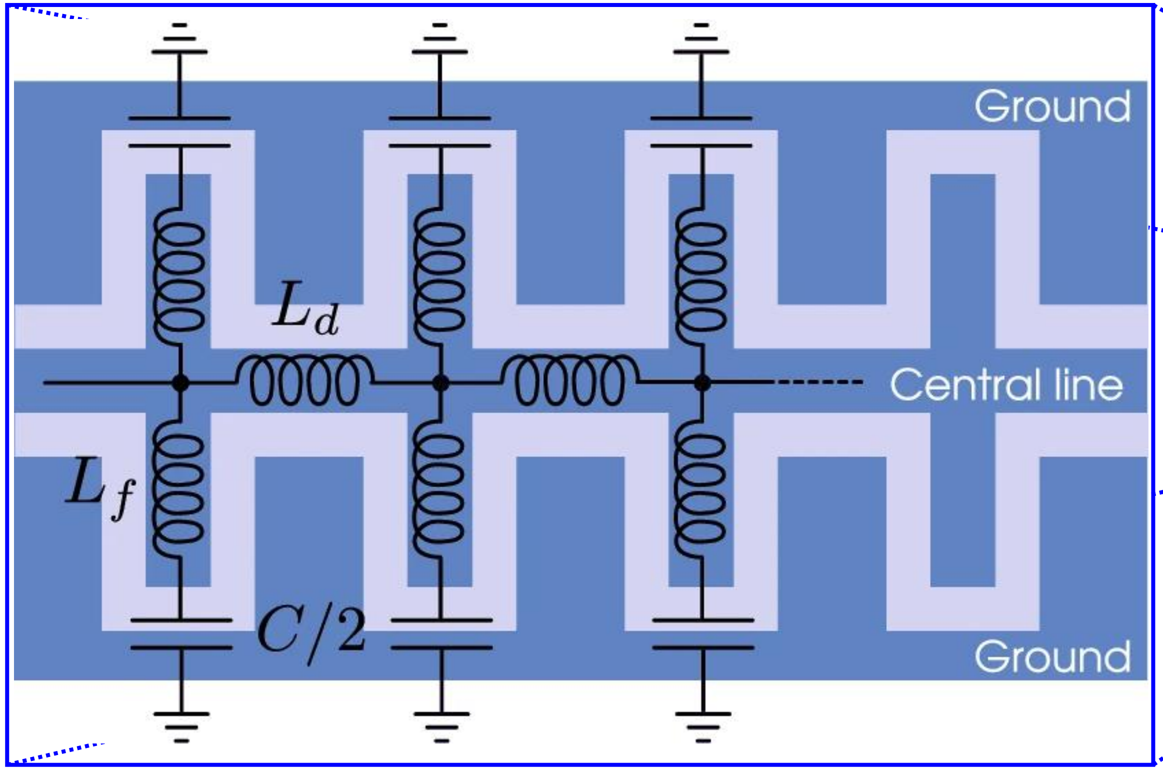


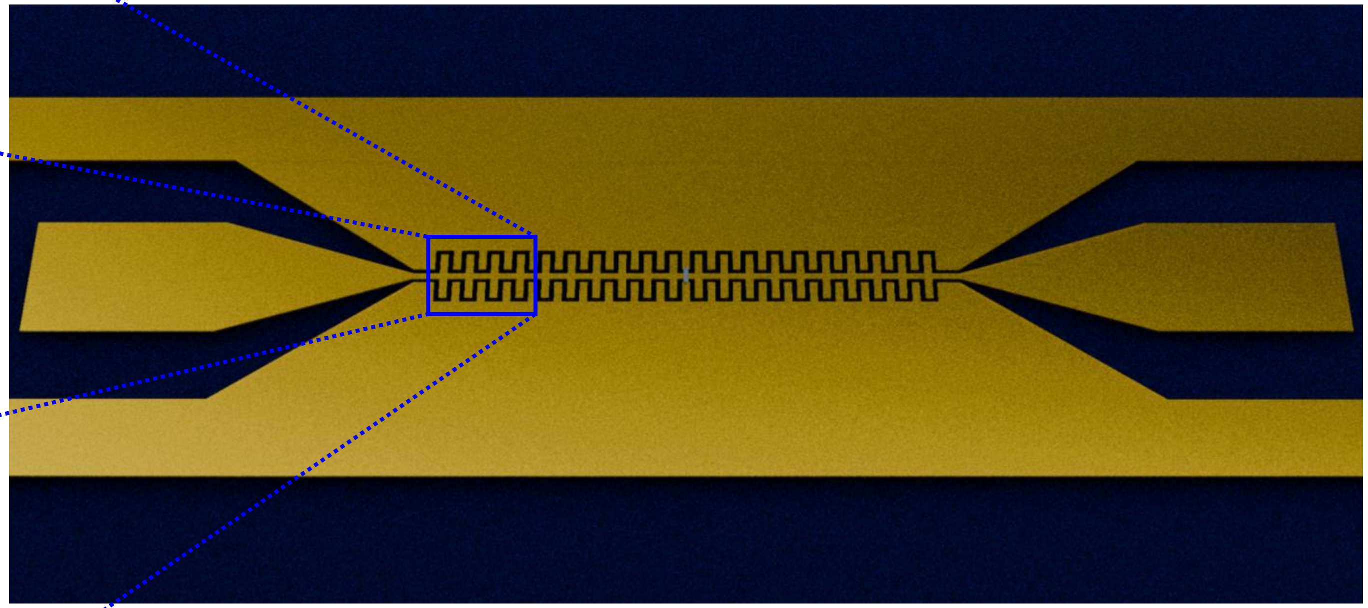


JPA is reflective mode device with low to 'medium' bandwidth.
It can perform 3 or 4 wave mixing (3WM or 4WM).

1. Zhong et al., *New J. Phys.* 15 125013 (2013)

Kinetic Inductance Traveling Wave Parametric Amplifiers (KI-TWPAs)





KI-TWPA is transmissive mode device with high bandwidth.
It can perform 3 or 4 wave mixing (3WM or 4WM).

1. Adapted from: Giachero et al., *J Low Temp Phys* 209, 658–666 (2022)

Deployment of Quantum Processors (Academic vs. Corporate)

```
└ Small-scale/ Academic-lab chips  (few traffic lanes)
  ├ Fixed-frequency transmons on single dies
  │   └ Cross-resonance & sideband gates, 2-to-10-qubit testbeds
  ├ Fluxonium qubits
  │   └ >100 μs coherence; microwave-only CZ studies
  ├ NV-center diamond qubits
  │   └ Two-qubit entanglement & sensor-LASER hybrids
  ├ Semiconductor spin quantum dots
  │   └ 2-to-4-qubit Si/SiGe or MOS devices (TU Delft, UNSW/ Diraq)
  ├ Photonic linear-optics benches
  │   └ Dual-rail photons, Hong-Ou-Mandel, teleportation demos
  └ Superconducting flux qubits (annealing physics)
      └ Non-stoquastic Hamiltonian & prime-factor test circuits
```

```
├ Large-scale/ Data-center-oriented  (≈10²-10⁶ physical qubits, many lanes)
│ ├ Superconducting transmon lattices
│ │  ├ IBM "Heron-class" tunable-coupler tiles (modular roadmap)
│ │  │  ├ 133-qubit Heron r1/r2 chips (baseline fidelity node)
│ │  │  ├ Crossbill prototype: 3 Herons + on-package m-couplers
│ │  │  ├ 462-qubit Flamingo module: l-couplers for ~1 m links
│ │  │  ├ 1,386-qubit Flamingo tri-module demonstration (2026)
│ │  │  ├ Starling fault-tolerant block (≈200 logical qubits, 10⁸ gates, 2029)
│ │  │  └ Blue Jay quantum-centric supercomputer (≈2,000 logical qubits, 10⁹ gates, 2033)
│ │  ├ IBM 127-qubit Eagle → 1,386-qubit Kookaburra (legacy multi-chip)
│ │  ├ Rigetti modular tiles
│ │  │  ├ 84-qubit Ankaa-3 (99.5 % CZ fidelity, 2024)
│ │  │  ├ 36-qubit chiplet prototype (halved error, Jul 2025)
│ │  │  └ 336-qubit Lyra target (narrow quantum advantage, 2026)
│ │  ├ Google Quantum AI
│ │  │  ├ 53-qubit Sycamore (2019)
│ │  │  ├ 105-qubit Willow logical-scaling chip (2024)
│ │  │  └ Roadmap toward ~1 M physical qubits & fault-tolerance (~2033)
│ │  └ Fujitsu-RIKEN superconducting platform (hybrid AI-HPC)
│ │     ├ 256-qubit RQC-Fujitsu machine, external access via hybrid platform (Q1 FY2025)
│ │     ├ 1,000-qubit facility under construction (availability target: FY2026)
│ │     └ ≥10,000-qubit development program, system completion targeted around 2030, aligned with FugakuNEXT AI-HPC
│ ├ Superconducting bosonic/cat-code processors (oscillator-encoded)
│ │  └ AWS Center for Quantum Computing (Caltech)
│ │     ├ Ocelot cat-qubit chip (Feb 2025)
│ │     └ Blueprint: concatenated cat codes + repetition/ surface code stack (2020→2022)
│ ├ Neutral-atom arrays
│ │  ├ QuEra Aquila 256-qubit Rydberg computer (2022 cloud)
│ │  ├ Atom Computing "Phoenix" 1,225-qubit ytterbium array (2023)
│ │  └ Pasqal roadmap to 10,000-qubit array (2026)
│ ├ Photonic cluster-state processors
│ │  ├ PsiQuantum Omega silicon-photonics chiplets, mass-fab (2025)
│ │  └ Xanadu Borealis 216-mode Gaussian-boson-sampler (2022)
│ ├ Trapped-ion modular racks
│ │  └ IonQ Forte (35 algorithmic qubits) + cryptographically relevant quantum computer roadmap (2028)
│ ├ Silicon spin-qubit tiles
│ │  ├ Intel "Tunnel Falls" 12-qubit chip, 300 mm CMOS fab (2023)
│ │  ├ Horse Ridge II 4 K cryo-CMOS controller (wiring cutback)
│ │  └ Pando Tree mK cryo-CMOS fan-out (10-20 mK stage)
│ └ Flux-qubit quantum annealers
│    └ D-Wave Advantage2 (≈7,000 flux qubits, Zephyr topology, 2025 general availability)
```

Quantum Computing Signal Chain Example (w/ RT Control)

A × B Single-Shot Signal Chain — 2 Qubits, Room-Temperature Controllers

Algorithm: $H(q_0)$, $\mathrm{CNOT}(q_0 \to q_1)$, $R_y(\pi/4)$ on q_1, Z on q_1
$\to$ Transpile & schedule (calibrations, virtual-Z)
$\to$ Gate-to-pulse map (DRAG, CR/CZ)

Algorithm & Scheduling

$\Longrightarrow$

Pulse synthesis (I/Q envelopes, pre-distortion)
$\to$ DAC sampling (2--10 GS/s)
$\to$ On-AWG interpolation (fractional delays)
$\to$ IF $\to$ RF up-conversion
$\to$ Heterodyning (LO/NCO planning)
$\to$ Control-line multiplexing

Pulse Synthesis & Up-Conversion

$\Downarrow$

Init to $|00\rangle$ (passive T_1/ active reset)
$\to$ Coherent qubit operations (timed pulses)
$\to$ Entanglement window (CR or CZ)

On-Chip Initialization & Gates

$\Longleftarrow$

Thermal attenuation ladders (300 K $\to$ 50 K $\to\to$ 4 K $\to$ mK)
$\to$ Band-limit filtering (room-T & cryo)
$\to$ Purcell filters & IR Eccosorb

Cryogenic Delivery & Protection

$\Downarrow$

Readout drive injection (multiplexed tones)
$\to$ Single-shot observation (state-dependent field)
$\to$ mK JPA/JPC/J-TWPA $\to$ 4 K HEMT (preamp)
$\to$ Readout-line multiplexing

Readout Injection & Pre-Amplification

$\Longrightarrow$

RF $\to$ IF down-conversion
$\to$ ADC sampling (1--5 GS/s)
$\to$ Interpolation/decimation (CIC/FIR)
$\to$ Digital homodyne/heterodyne
$\to$ Post-DSP filtering checks
$\to$ Decode, plots, histograms

Down-Conversion & DSP Decode

Quantum Computing Signal Chain Example (w/ Cryo-ASIC Control)

A × B Single-Shot Signal Chain — 2 Qubits, Cryogenic ASIC Controllers

$$\underbrace{\begin{array}{c}\text{Algorithm: } H(q_0),\ \text{CNOT}(q_0 \to q_1),\ R_y(\pi/4) \text{ on } q_1,\ Z \text{ on } q_1 \\ \to \text{Transpile \& schedule (virtual-Z placement)} \\ \to \text{Cryo-aware compilation (latency/power caps)} \\ \to \text{Digital command packets to cryo-ASIC}\end{array}}_{\text{Algorithm}\to\text{Cryo Packetization}} \Longrightarrow \underbrace{\begin{array}{c}\text{On-ASIC DAC sampling (1--4 GS/s)} \\ \to \text{On-ASIC interpolation \& pre-distortion} \\ \to \text{On-ASIC NCO/IQ up-conversion} \\ \to \text{Local heterodyning (shared cryo-LO/ digital SSB)} \\ \to \text{Near-chip fanout/multiplex}\end{array}}_{\text{Cryo Up-Conversion \& Fanout}}$$

$$\Downarrow$$

$$\underbrace{\begin{array}{c}\text{Minimal thermal attenuation (short mK run)} \\ \to \text{Cryo filtering: band-limit, Purcell, IR Eccosorb}\end{array}}_{\text{Delivery \& Protection}} \Longleftarrow \underbrace{\begin{array}{c}\text{Initialize to } |00\rangle \text{ (passive } T_1 \text{ or active reset)} \\ \to \text{Gate window } (H \approx R_z(\pi)\, R_y(\pi/2) \text{ with VZ}) \\ \to \text{Entanglement (CR or CZ)}\end{array}}_{\text{On-Chip Execution}}$$

$$\Downarrow$$

$$\underbrace{\begin{array}{c}\text{Readout pulse generated on ASIC} \\ \to \text{State-dependent imprint on resonator field} \\ \to \text{mK JPA/JPC/J-TWPA} \ \to\ \text{4 K HEMT}\end{array}}_{\text{Readout Generation \& Preamp}} \Longrightarrow \underbrace{\begin{array}{c}\text{On-ASIC down-conversion} \\ \to \text{On-ASIC ADC \& decimation} \\ \to \text{On-ASIC digital homodyne/heterodyne} \\ \to \text{Room-T validation \& formatting} \\ \to \text{Final decode, storage, plots}\end{array}}_{\text{Cryo Down-Conv, ADC, DSP, Host Decode}}$$

Bonus: Do I Need Cryogenic Equipment for My Quantum Photonic Chip (If I Have One)?

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├ A) Are you talking about a QUANTUM PHOTONIC QUBIT CHIP?
│    ├ A1) Encoding & detection path: DISCRETE-VARIABLE (single photons)?
│    │    ├ A1.i) Are superconducting detectors (SNSPD/TES) ON-CHIP or CO-PACKAGED?
│    │    │    ├ YES → Plan CRYOGENICS (≈0.1–4 K). Also avoid thermo-optic tuning; use Pockels/magneto-optic/phase-change.
│    │    │    └ NO  → Go to A1.ii.
│    │    ├ A1.ii) Are you using near-deterministic QD single-photon SOURCES on-chip/co-packaged?
│    │    │    ├ YES → Plan CRYOGENICS (≈4–10 K). Processor often rides in same cryostat.
│    │    │    └ NO  → Go to A1.iii.
│    │    ├ A1.iii) Are DETECTORS external and warm-compatible (Si/GeSi SPADs; InGaAs SPADs with TEC)?
│    │    │    ├ YES → Processor CAN stay ROOM TEMPERATURE (stabilize with small TEC if needed).
│    │    │    └ NO  → If external detectors are SNSPDs, only the detector rack is cold; processor can still be ROOM TEMPERATURE.
│    │
│    └ A2) Encoding & detection path: CONTINUOUS-VARIABLE (squeezed states + homodyne)?
│         ├ Sources and balanced-homodyne detectors are ROOM TEMPERATURE by default.
│         └ Only plan CRYOGENICS if co-integrating cold peripherals (e.g., rare-earth memories) or if your system choice is to
│           co-locate everything to cut fiber coupling loss into a cryostat.
│
└ B) Are you talking about a NON-QUBIT QUANTUM INTEGRATED CIRCUIT?
     ├ B1) Quantum communications TRANSMITTERS, linear-optics processors, quantum sensors (no on-chip cryo parts)?
     │    └ ROOM TEMPERATURE (standard hermetic/TEC packages).
     ├ B2) Photonic READOUT for superconducting electronics (e.g., 4 K data links) or on-chip SNSPD arrays for sensing?
     │    └ Plan CRYOGENICS; use cryo-compatible EO modulators (LN/BTO), not thermo-optic heaters.
     └ B3) Memories/interfaces:
          ├ Rare-earth-doped solid-state memories → CRYOGENICS (few kelvin).
          └ Warm-vapor (alkali) memories → ROOM TEMPERATURE, with bandwidth/noise trade-offs.
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