Magnetic Random Access Memory (MRAM) for Embedded Quantum Computing Hardware

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***Abstract*—In the current era of noisy intermediate-scale quantum computing, classical memory is an optional buffer between the quantum and classical domains. Intermediate computation results that do not require quantum operations, as well as data processing and communication throughout the quantum stack, can benefit from the closer proximity of classical memory to the quantum processor. For the coming era of practical, fault-tolerant quantum computing, having high-density, near or in-processor memory functions could allow quantum error correction schemes on larger physical qubit counts of high fidelity that reach into the millions. Our findings have demonstrated the use of nanoscale spin-transfer torque magnetic tunnel junctions as memory cells at low temperature. Other results from our work show successful implementation of voltage control exchange coupling in spin-orbit torque magnetic tunnel junctions, which could be more energy-efficient than previously reported works on spin-transfer torque devices. We propose a hybrid-compatible cryogenic magnetic random-access memory architecture containing nanoscale spin-orbit torque magnetic tunnel junctions for quantum computing hardware architectures.**

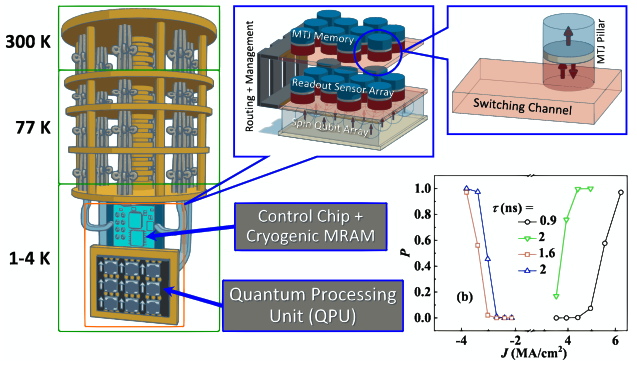
Keywords—cryogenic memory; spin-orbit torque; quantum computing; quantum hardware; MRAM

I. Introduction

Classical computer memory is a ubiquitous technology found in a variety of consumer applications. It can be found in some current forms of noisy intermediate-scale quantum (NISQ) computers and superconducting computers. Towards the progress of useful, fault-tolerant quantum computing (FTQC), it is worth exploring compatible, enabling, near or on-quantum-processor classical memory devices for such a quantum system expected to contain quantum error correction, a high qubit count, and lower error rates or high-fidelity. These can be divided into topics of exploration in and of themselves, however they are also challenges that must and can be addressed through the use of a robust memory.

A range of memory approaches on the market are implemented using complementary metal oxide semiconductor (CMOS) platforms, as well as magnetic-based platforms, such as magnetoresistive random-access memory (MRAM) [1, 2]. Generally, cryogenic-compatible platforms of classical memory can be applied to both classical and quantum computing configurations at low temperatures [3, 4, 6, 8, 10]. In lab scale quantum computers, the physical qubits are placed inside a dilution-refrigerator that can maintain a temperature in the milli-Kelvin range, while the qubit control components are kept at ambient temperature (300 K). This means that a large number of wires connecting the control components and qubits are a bottleneck because of the large thermal gradient along the control wires. However, this issue can be solved by integrating the control components, memory, and qubits onto the same level of the dilution refrigerator.

Notably, static random-access memory (SRAM) has been successfully implemented, so far, into the cryogenic CMOS qubit control architecture for purposes of storing and reusing qubit control pulse sequences and shapes [5]. Typically, the idea



	Mainstream Memories			Emerging Memories	
	SRAM	DRAM	FLASH	STT-MRAM	RRAM
Major Advantages	Fast read/write	Fast read/write High density	Multi-bit Non-volatility	High density Non-volatility	High density Non-volatility
Critical Drawbacks	High leakage power Large cell area	Short retention time	Low durability	Patterning complexities	Large process variation
Cryogenic Effects	Faster speed Near-zero leakage	Faster speed Improved retention time	Increased endurance Improved retention	Higher write overhead Shorter read latency Better TMR	Higher operational voltage Narrow switching window

Fig.1 (a) Model of our proposed hybrid-compatible near-quantum-processor MRAM for a quantum processor unit (QPU) in a crystat. The QPU mentioned here can be swapped out with superconducting qubits. (b) Idea for our MRAM integration with spin-based, magnetic qubits, plus a close-up of the MTJ memory cell. (c) Benchmarking results from our sub-ns, ultrafast, current-driven, Mo-based STT-pMTJs. P represents the switching probabilty as a function of pulse width (τ) and current density (J) [7]. (d) Comparison of various cryogenic memories, including STT-MRAM, adapted from reference [9].

regarding the use of quantum error correction involves the employment of a technique called syndrome measurement. This process performs multi-qubit measurements that do not disturb quantum information in the encoded state, however it retrieves information about the error. Occurrence, type, and location of errors can then be determined and addressed according to the type of quantum error correction code being used.

The CMOS-based cryogenic quantum control platform here takes digital commands for its input and then generates many parallel qubit control pulses, which are stored in the memory. It is important to acknowledge that as the number of high-fidelity qubits on a chip increases, a high-density, reliable memory is needed. For both superconducting quantum and spin-based quantum computing systems, cryogenic memory architectures are considered to be compatible [5, 6]. This is an example of where the benefits of MRAM in quantum computing hardware can begin to be considered.

Although magnetic memory cells and MRAM architectures primarily exist in ambient temperature applications, they can be used in cryogenic conditions with a noticeable increase in overall performance such as a shorter read latency, sub-ns switching, and higher tunnel magnetoresistance (TMR) [3, 7, 9]. Our previous work shows that devices on memory chips are aimed at providing an enhancement of overall computing efficiency based on the advantages of material performance in cryogenic conditions and its ability to store reusable qubit control pulse sequences for larger quantum processors [5, 7, 13].

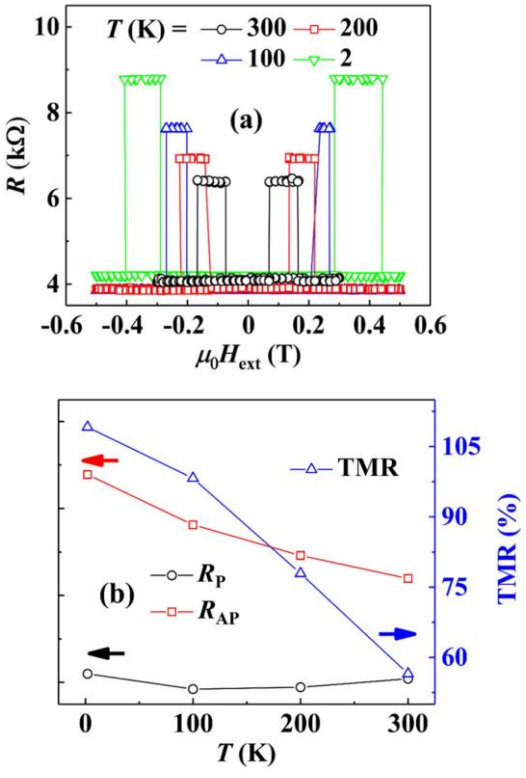


Fig. 2 (a) Results of major R vs. $\mu_0 H_{ext}$ loops showing increased magnetoresistance of our Mo-based STT-MTJ memory cell exposed to low temperatures down to 2 K. (b) Parallel, antiparallel resistances (R_P, R_{AP}), and TMR vs. T [7].

Although experimental quantum memory devices exist for quantum computing, they will not be discussed here [2].

The main building block of MRAM is the magnetic tunnel junction (MTJ), which uses the TMR effect in a ferromagnet-insulator-ferromagnet junction as a way to store classical bits of information in a cell. Each memory cell contains a magnetic anisotropy in the in-plane or out-of-plane (perpendicular) direction. For the purposes of this work, we will focus mostly on the use of MTJs with perpendicular magnetic anisotropy (PMA) otherwise known as perpendicular magnetic tunnel junctions (pMTJs). We will report our efforts to develop MRAM and its integration with qubits. Although superconducting quantum and spin-based quantum computing systems are both mentioned, it would be worth exploring the use of MRAM in hybrid quantum computing as well.

II. Results and Discussion

A. STT-MTJs at Low Temperatures

Studying the temperature (T)-dependence of magneto-transport properties and switching of pMTJs at low temperatures allows for the validation of use in cryogenic memory. In the quest to achieve sub-ns switching of pMTJs, spin-transfer torque (STT)-driven MTJs were fabricated and studied based on their confirmed cryogenic-temperature functionality in our lab [7]. The importance of such an ultrahigh switching speed comes from the motivation to compete with or replace SRAM or dynamic random-access memory (DRAM), especially at low temperatures [16]. Mo-based pMTJs were found to outperform mainstream Ta-based pMTJs in terms of thermal tolerance and PMA. Since the cryogenic-temperature functionality of nanoscale Mo-pMTJs had not previously been tested, we prepared nanoscale Mo-pMTJs, demonstrated their ultrafast switching to the sub-ns timescale, and verified their cryogenic functionality down to 2 K. To confirm the strong PMA of the Mo-pMTJs, vibrating sample magnetometry (VSM) measurements were conducted.

The texture and structure of the devices, characterized by scanning transmission electron microscopy (STEM), showed good structure integrity and a diameter of $\approx$ 100 nm. For various time constants or pulse widths (τ) and current densities (J), ultrafast switching was observed well within the precessional regime. The optimal energy (E) is 0.64 pJ/bit (P→AP) and 0.71 pJ/bit (AP→P). The TMR ratio, based on AP state resistance (R_{AP}), nearly doubled when the devices were cooled down to 2 K. As T decreases, switching current density (J_{SW}) generally increases except for extremely low T. Our study on Mo-pMTJs advances them toward promising cryogenic memory.

B. Energy-Efficient VCEC-MTJs

In nanoscale pMTJs of 100 nm diameter, with a synthetic antiferromagnetic (SAF) free layer, we were able to experimentally demonstrate and theoretically confirm bipolar electric-field switching [15, 17]. Compared to best reported STT-switched MTJs, pMTJs switched by VCEC showed a one

order of magnitude lower J_{SW} of ~1.1×10^5A/cm^2. This ultra-low-energy switching mechanism is based on the voltage-controlled exchange coupling (VCEC) effect, which can modulate the sign of the interlayer exchange coupling (IEC) in the SAF structure while inducing a linear IEC torque. The field-like interlayer exchange coupling torque generated by the ferromagnetic-antiferromagnetic exchange coupling transition of the SAF free layer were suggested according to the theoretical results. Although VCEC-MTJs can be applied to both logic and memory at room temperature, the compatibility with cryogenic devices can be derived by simply characterizing the material stack at low temperatures (down to 2 K for consistency).

C. Ultra-Fast SOT-MTJs with VCEC-MTJs

The combination of VCEC and SOT switching can effectively be merged within a SAF pMTJ to exploit the energy efficiencies of each. This means that ultrafast switching speeds that have been reported in SOT-pMTJs at ≈ 0.27 ns can therefore roughly be maintained with ultralow-energy-switching as opposed to its typical, negatively-impacting, large switching current densities [18]. In our studies, we demonstrated bidirectional switching of such a SAF pMTJ with a 150 nm diameter and ultralow switching current densities, J_C, $_{VCEC}$ = 2.8×10^3 A cm^{-2} and J_{SOT} = 6.8×10^7 A cm^{-2} [14]. We designed and fabricated our devices with a SAF free layer and bilayered spin Hall channel.

The above-mentioned bidirectional switching current densities were found to be two orders of magnitude lower than the best reported values for VCEC-only switched devices as well. It was found that SOT plays a critical role in the bidirectional VCEC switching of magnetization based on ultralow-switching current density. By selecting advanced SOT or quantum materials to replace the heavy-metal (Ta, W, Pt)-based spin Hall channel, such as a topological insulator, a lower switching current density can be achieved.

Consequently, Joule heating can be diminished by such an approach, further reducing noise overall, within a compatible quantum computing system. This is especially important when considering a configuration where cryogenic memory components, near to a low-temperature quantum processor, might indirectly affect the performance of the physical qubits [6]. Although we expect to see a more immediate integration of our cryogenic MRAM approach with superconducting and magnetic-based spin qubits, its compatibility with both CMOS and beyond-CMOS architectures indicates further compatibility with semiconductor spin qubit arrays in advanced manufacturing [19].

Given the research strength of the magnetics and quantum computing community, there is a tremendous opportunity to combine quantum and classical architectures at the device level, especially for, but not exclusive to, spin-based circuits. Exploiting spin transport mechanisms between devices on the hardware level of the so-called quantum stack may help deliver a much-needed boost to current and future physical quantum systems. In our case, cryogenic, energy-efficient MRAM could potentially enable research on larger, scalable quantum computers for both academia and industry. The approach lies in the ability to not only swap out limited ability cryogenic RAM with reliable, energy-efficient, cryogenic MRAM, but also the ability to use it with multiple physical qubit platforms and some of the latest quantum materials available.

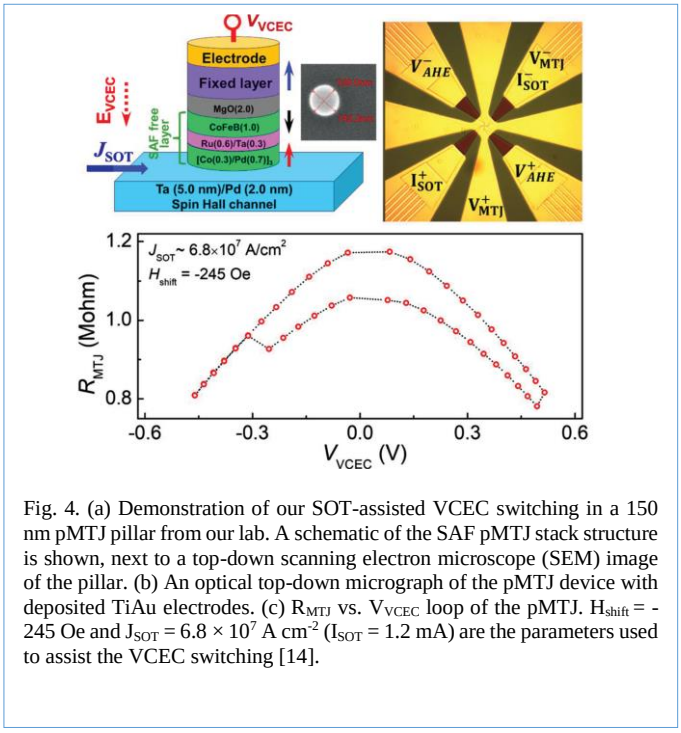


Fig. 4. (a) Demonstration of our SOT-assisted VCEC switching in a 150 nm pMTJ pillar from our lab. A schematic of the SAF pMTJ stack structure is shown, next to a top-down scanning electron microscope (SEM) image of the pillar. (b) An optical top-down micrograph of the pMTJ device with deposited TiAu electrodes. (c) R_{MTJ} vs. V_{VCEC} loop of the pMTJ. H_{shift} = -245 Oe and J_{SOT} = 6.8×10^7 A cm^{-2} (I_{SOT} = 1.2 mA) are the parameters used to assist the VCEC switching [14].

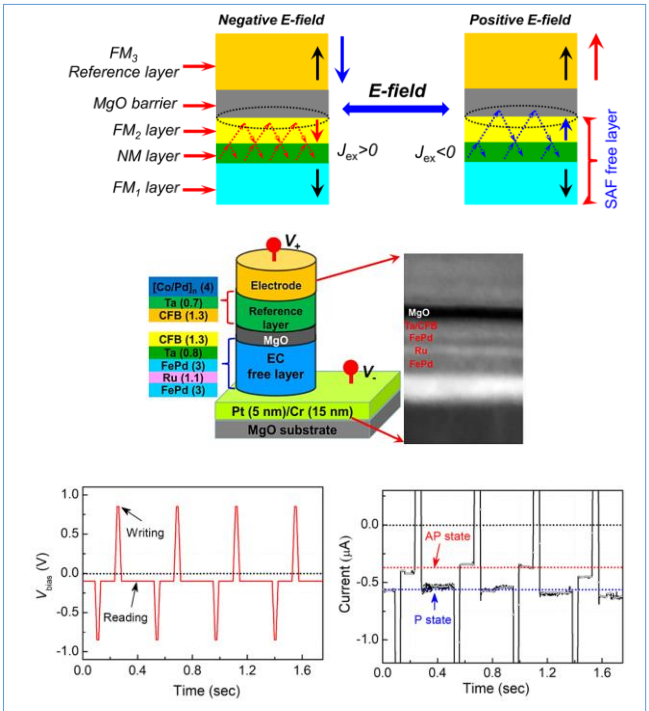


Fig. 3. (a) Schematic of our VCEC-MTJs, with a switching current density of ~1.1×10^5A/cm^2, an order of magnitude lower than the best-reported STT-based devices. (b) Schematic of the SAF pMTJ stack with a scanning tunneling electron microscope (STEM) image cross-section of the stack. (c) Voltage pulses for write and read operation showing the device state (parallel or anti-parallel) followed by (d) the measured curent vs. time without H_{ext} [17].

CONCLUSIONS

The next step, as we slowly pass through the current noisy intermediate-scale quantum computing era into the fault-tolerant quantum era, requires consideration for robust memory implementations. Our work has demonstrated the use of STT-MTJs as memory cells at low temperature, giving immense potential as cryogenic memory for related applications. Other findings from our lab demonstrate successful implementation of VCEC + SOT in energy efficient pMTJs, which could be advantageous in that regard than previously reported works. By using MRAM as a classical memory function closer to the quantum processor, we can exploit the cryogenic performance of MTJs for both immediate and future use cases of quantum computing hardware.

ACKNOWLEDGMENT

This work is currently supported by ASCENT, one of six centers of JUMP, a Semiconductor Research Corporation program that is sponsored by MARCO and DARPA, and DARPA HR001117S0056-FP-042 "Advanced MTJs for computation in and near random access memory." Portions of this work were conducted in the Minnesota Nano Center, which is supported by the National Science Foundation through the National Nano Coordinated Infrastructure Network (NNCI) under Award Number ECCS-1542202.

REFERENCES

[1] A. Hirohata, K. Yamada, Y. Nakatani, I. L. Prejbeanu, B. Diény, P. Pirro, B. Hillebrands, "Review on spintronics: Principles and device applications," J. Magn. Magn. Mater. 509, 166711, March 2020.

[2] F. Giustino, J. H. Lee, F. Trier, M. Bibes, S. M. Winter, R. Valentí, Y. W. Son, L. Taillefer, C. Heil, A. I. Figueroa, B. Plaçais, Q. S. Wu, O. V. Yazyev, E. P. A. M. Bakkers, J. Nygård, P. Forn-Díaz, S. D. Franceschi, J. W. McIver, L. E. F. F. Torres, T. Low, A. Kumar, R. Galceran, S. O. Valenzuela, M. V. Costache, A. Manchon, E. A. Kim, G. R. Schleder, A. Fazzio, and S. Roche, "The 2021 quantum materials roadmap," J. Phys. Mater., 3, 042006, January 2020.

[3] S. Alam, M. S. Hossain, S. R. Srinivasa, and A. Aziz, "Cryogenic Memory Technologies," Nat. Electron., 6, pp. 185-198, March 2023.

[4] J. Preskill, "Quantum Computing in the NISQ era and beyond," Quantum, 2, p. 79, August 2018.

[5] F. Sebastiano, J. P. G. Van Dijk, B. Patra, J. van Staveren, X. Xue, C.G. Almudever, G. Scappucci, M. Veldhorst, L. M. K. Vandersypen, A. Vladimirescu, and S. Pellerano, "Cryo-CMOS interfaces for large-scale quantum computers," IEEE International Electron Devices Meeting, (IEDM) pp. 25-2, December 2020.

[6] S. J. Pauka, K. Das, R. Kalra, A. Moini, Y. Yang, M. Trainer, A. Bousquet, C. Cantaloube, N. Dick, G. C. Gardner, M. J. Manfra, and D. J. Reilly, "A cryogenic CMOS chip for generating control signals for multiple qubits," Nat. Electron., 4, pp. 64-70, January 2021.

[7] D. Lyu, P. Khanal, Y. Lv, B. Zhou, H. Yun, Q. Jia, B. R. Zink, Y. Fan, K. A. Mkhoyan, W. Wang, and J. P. Wang, "Sub-ns Switching and Cryogenic-Temperature Performance of Mo-Based Perpendicular Magnetic Tunnel Junctions," IEEE Electron Device Lett., vol. 43, 8, pp. 1215-1218, August 2022.

[8] M. H. Nguyen, G. J. Ribeill, M. V. Gustafsson, S. Shi, S. V. Aradhya, A. P. Wagner, L. M. Ranzani, L. Zhu, R. Baghdadi, B. Butters, and E. Toomey, "Cryogenic Memory Architecture Integrating Spin Hall Effect based Magnetic Memory and Superconductive Cryotron Devices," Sci. Rep., 10, 248, January 2020.

[9] Y. Hou, W. Ge, Y. Guo, L. Naviner, Y. Wang, B. Liu, J. Yang, and H. Cai, "Cryogenic In-MRAM Computing," IEEE/ACM International Symposium on Nanoscale Architectures (NANOARCH), pp. 1-6, November 2021.

[10] J. B. Yau, Y. K. K. Fung, and G. W. Gibson, "Hybrid cryogenic memory cells for superconducting computing applications," IEEE International Conference on Rebooting Computing (ICRC), pp. 1-3, November 2017.

[11] E. Garzón, L. Yavits, A. Teman, and M. Lanuzza, "STT-MRAM Technology For Energy-Efficient Cryogenic Memory Applications," IEEE 14th Latin America Symposium on Circuits and Systems (LASCAS), pp. 1-4, February 2023.

[12] M. H. Nguyen, G. E. Rowlands, and T. A. Ohki, "Cryogenic MRAMS for Superconducting Computers," In 2021 IEEE 32nd Magnetic Recording Conference (TMRC), pp. 1-2, August 2021.

[13] P. W. Swatek, X. Hang, Y. Fan, W. Jiang, H. Yun, D. Lyu, D. Zhang, T. J. Peterson, P. Sahu, O. J. Benally, Z. Cresswell, J. Liu, R. Pahari, D. Kukla, T. Low, K. A. Mkhoyan, and J. P. Wang, "Room temperature spin-orbit torque efficiency in sputtered low-temperature superconductor δ-TaN," Physical Review Materials, vol. 6, 7, p. 074206. July 2022.

[14] B. R. Zink, D. Zhang, H. Li, O. J. Benally, Y. Lv, D. Lyu, and J. P. Wang, "Ultralow current switching of synthetic‐antiferromagnetic magnetic tunnel junctions via electric‐field assisted by spin‐orbit torque," Advanced Electronic Materials, 8, 10, p. 2200382, July 2022.

[15] T. J. Peterson, A. Hurben, W. Jiang, D. Zhang, B. Zink, Y. C. Chen, Y. Fan, T. Low, and J. P. Wang, "Enhancement of voltage controlled magnetic anisotropy (VCMA) through electron depletion," Journal of Applied Physics, 131, vol. 15, 153904, April 2022.

[16] Y. Huai, H. Gan, Z. Wang, P. Xu, X. Hao, B. K. Yen, R. Malmhall, N. Pakala, C. Wang, J. Zhang, Y. Zhou, D. Jung, K. Satoh, R. Wang, L. Xue, and M. Pakala, "High performance perpendicular magnetic tunnel junction with Co/Ir interfacial anisotropy for embedded and standalone STT-MRAM applications," Appl. Phys. Lett., vol. 112, no. 9, February 2018.

[17] D. Zhang, M. Bapna, W. Jiang, D. Sousa, Y. C. Liao, Z. Zhao, Y. Lv, P. Sahu, D. Lyu, A. Naeemi, T. Low, and J. P. Wang, "Bipolar Electric-Field Switching of Perpendicular Magnetic Tunnel Junctions through Voltage-Controlled Exchange Coupling," Nano Lett., 22, pp. 622-629, January 2022.

[18] E. Grimaldi, V. Krizkova, G. Sala, F. Yasin, S. Couet, G. S. Kar, K. Garello, and P. Gambardella, "Single-shot dynamics of spin–orbit torque and spin transfer torque switching in three-terminal magnetic tunnel junctions" Nat. Nanotechnol., 15, 111-117, January 2020.

[19] A. M. J. Zwerver, T. Krähenmann, T. F. Watson, L. Lampert, H. C. George, R. Pillarisetty, S. A. Bojarski, P. Amin, S. V. Amitonov, J. M. Boter, R. Caudillo, D. Correas-Serrano, J. P. Dehollain, G. Droulers, E. M. Henry, R. Kotlyar, M. Lodari, F. Lüthi, D. J. Michalak, B. K. Mueller, S. Neyens, J. Roberts, N. Samkharadze, G. Zheng, O. K. Zietz, G. Scappucci, M. Veldhorst, L. M. K. Vandersypen and J. S. Clarke, "Qubits made by advanced semiconductor manufacturing" Nat. Electron., 5, 184-190, March 2022.