

Quantum Hardware Overview

Onri Jay Benally

Quantum Hardware Engineer

NSF Graduate Research Fellow

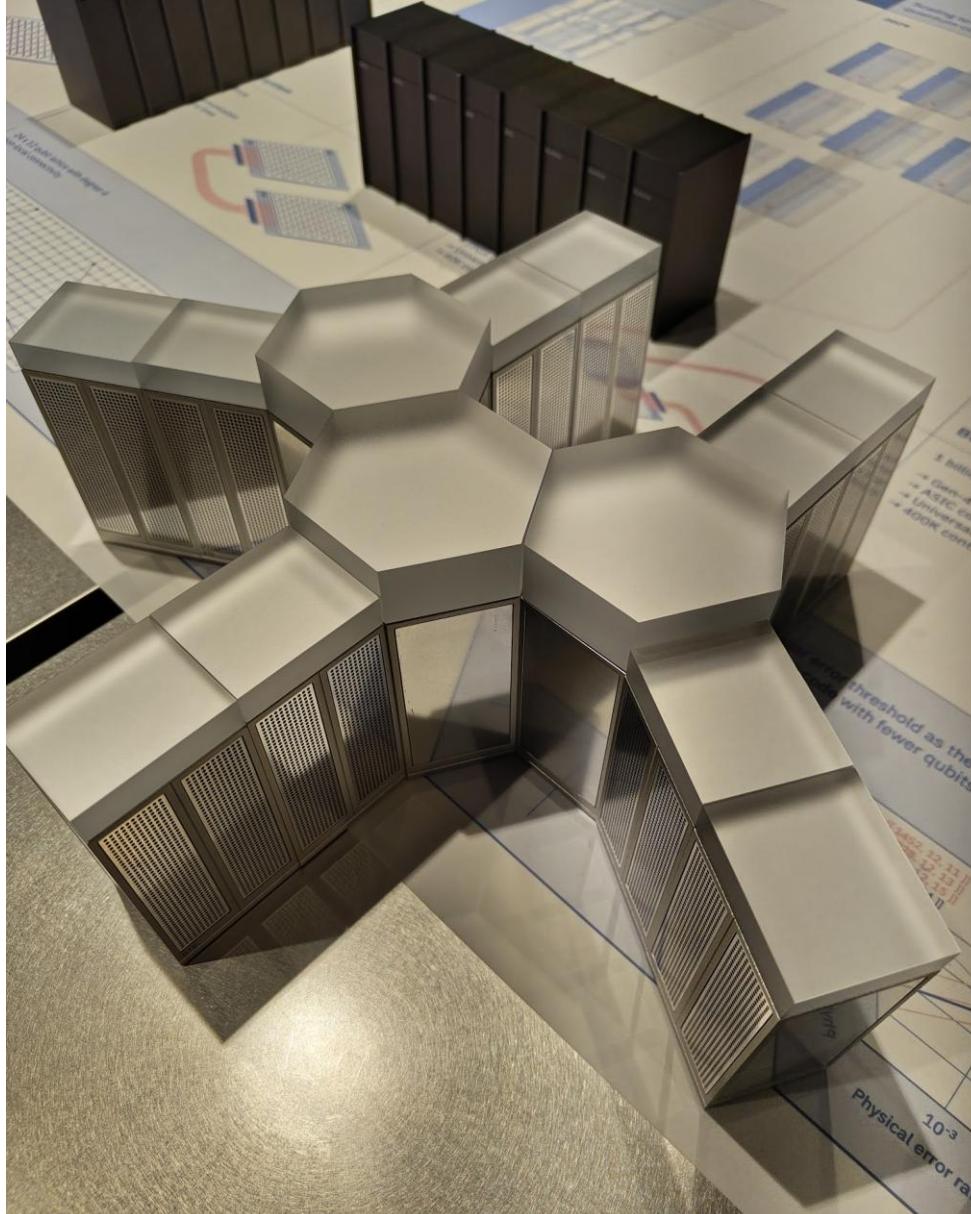


UNIVERSITY OF MINNESOTA
Driven to Discover®

Background & Motivation



Background & Motivation



Background & Motivation (Related Repositories)

 **OJB-Quantum/QC-Hardware-How-To**

Everything you need for quantum **hardware** engineering in the field. Curated by Onri Jay Benally.

[Unstar](#)

sustainability quantum quantum-mechanics quantum-computing qed

Jupyter Notebook · ⭐ 65 · Updated 6 hours ago

 **OJB-Quantum/Qiskit-Metal-to-Litho**

From **Qiskit Metal** to pattern generation to real nanofabrication demo. Here, quantum devices on a chip are patterned via direct-write elec...

[Unstar](#)

quantum quantum-computing manufacturing hardware-designs quantum-information

Jupyter Notebook · ⭐ 45 · Updated 24 days ago

 **OJB-Quantum/Generative-Layout-Notebooks**

GDSII/OASIS layouts, including fractals, generated in working Google Colab notebooks. Layout previews are plotted as 2D graphics before e...

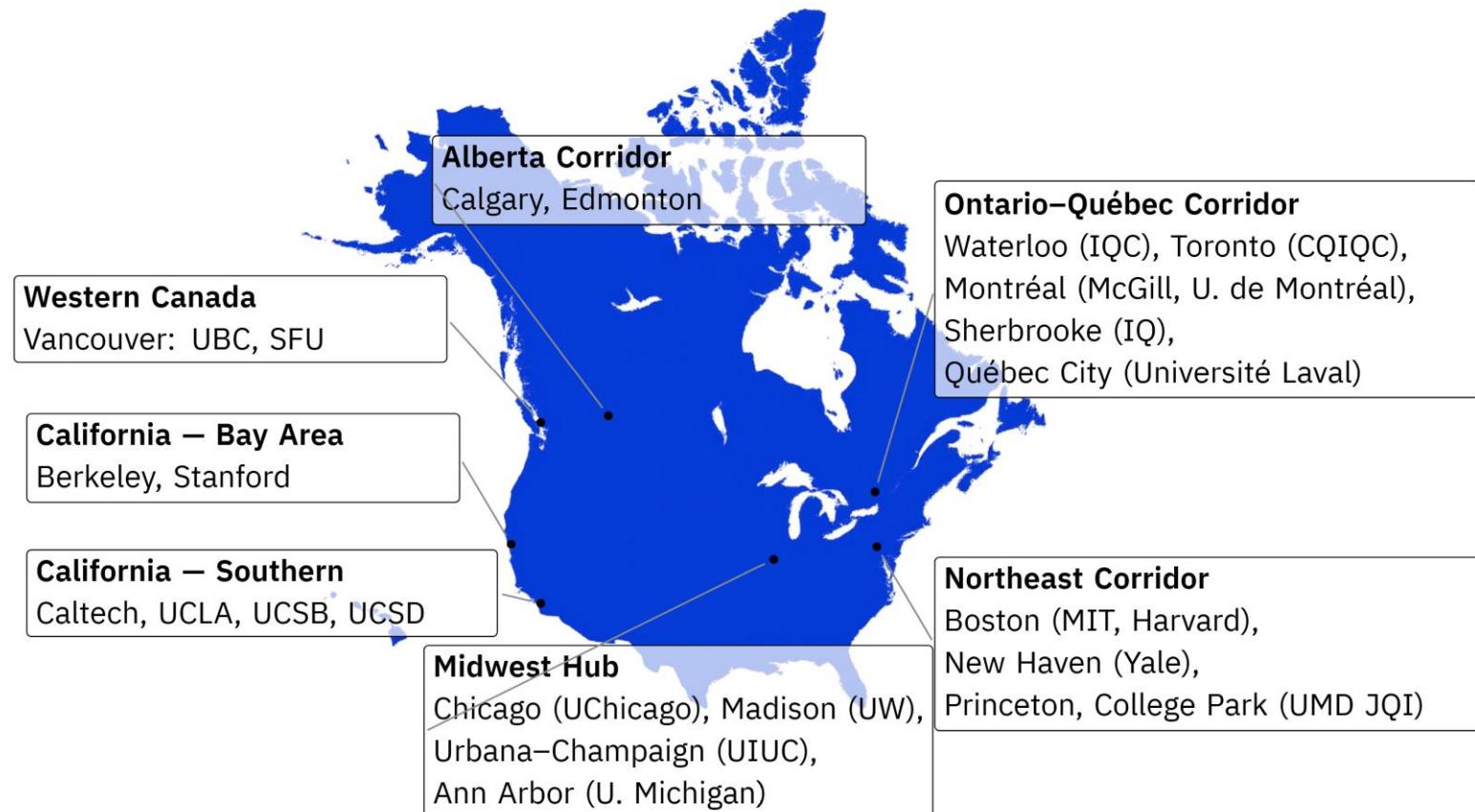
[Unstar](#)

open-source automation google layout quantum

Jupyter Notebook · ⭐ 6 · Updated on Aug 14

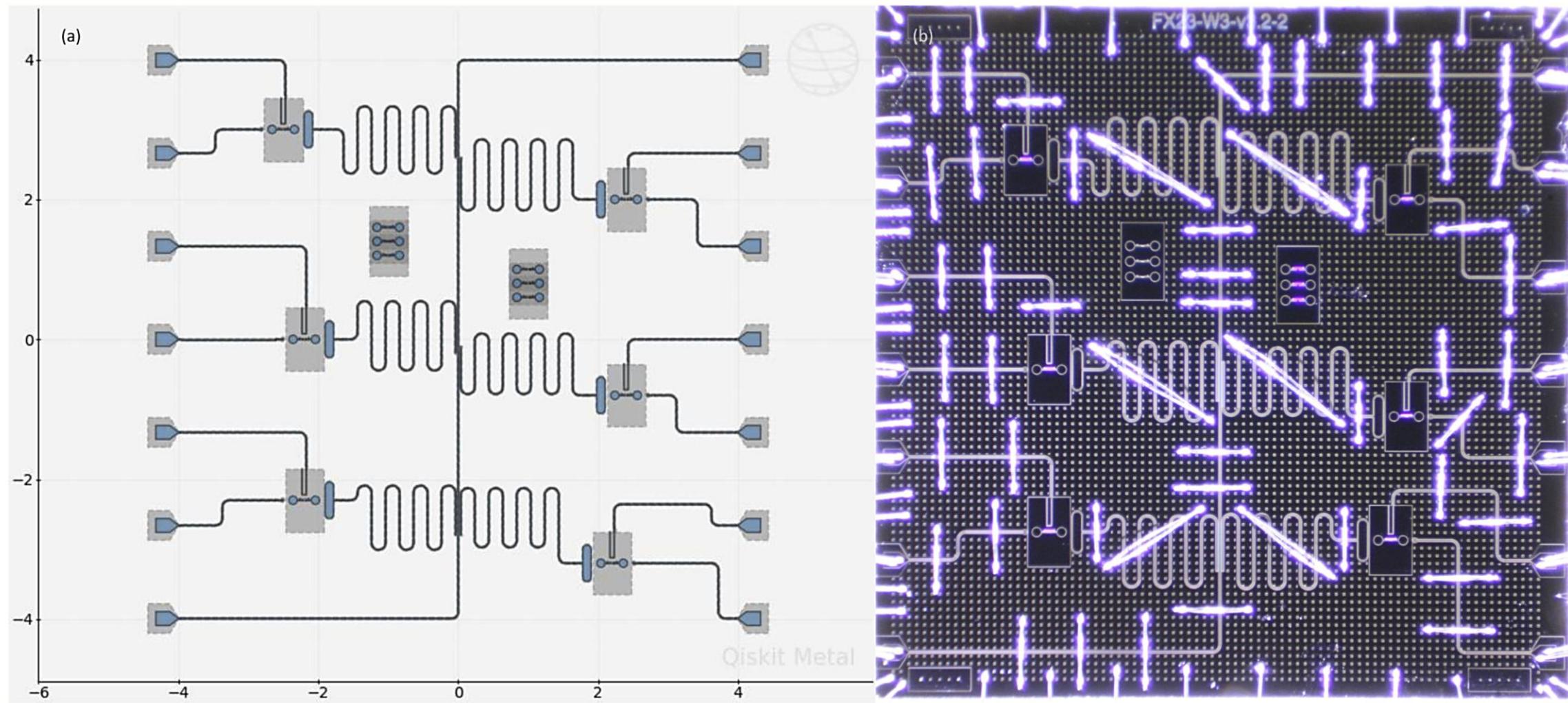
Background & Motivation

Geographic View: Major U.S. Hubs and the Canadian Corridor

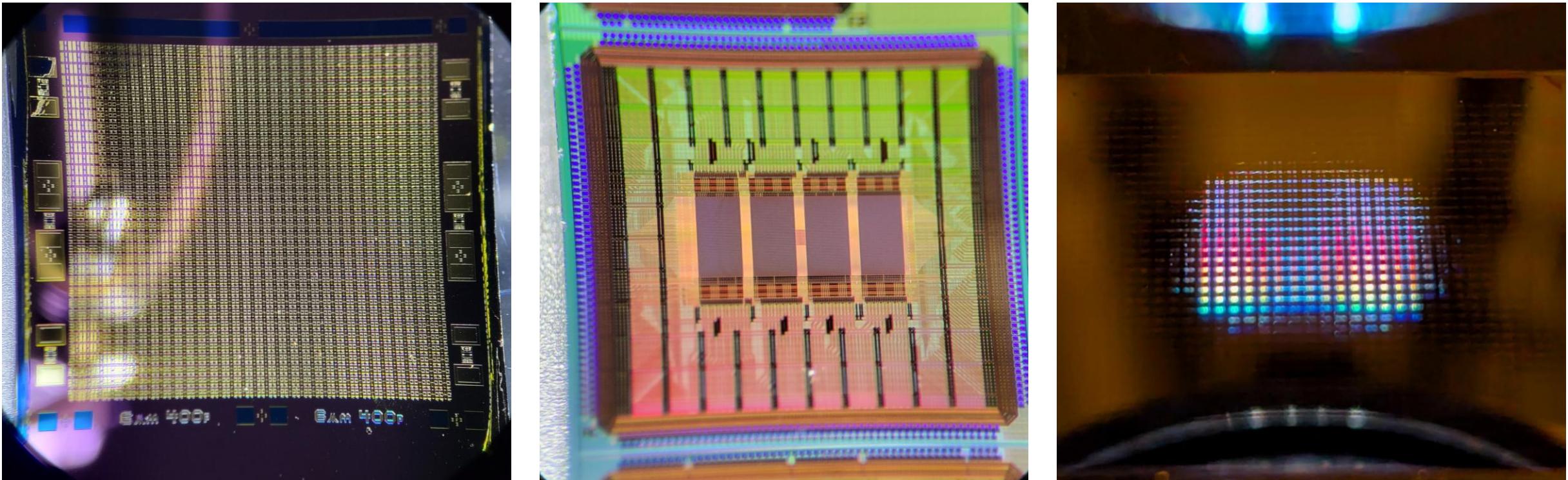


As quantum hardware training infrastructure and programs develop, more major hubs will show up on the map. Eventually, UMN may join the Midwest Hub as well.

Background & Motivation

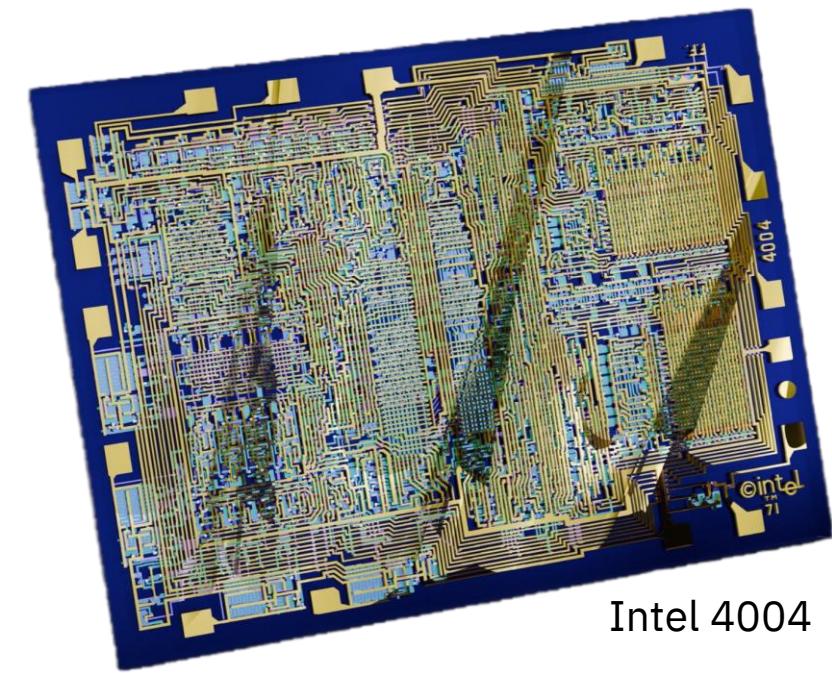


Background & Motivation

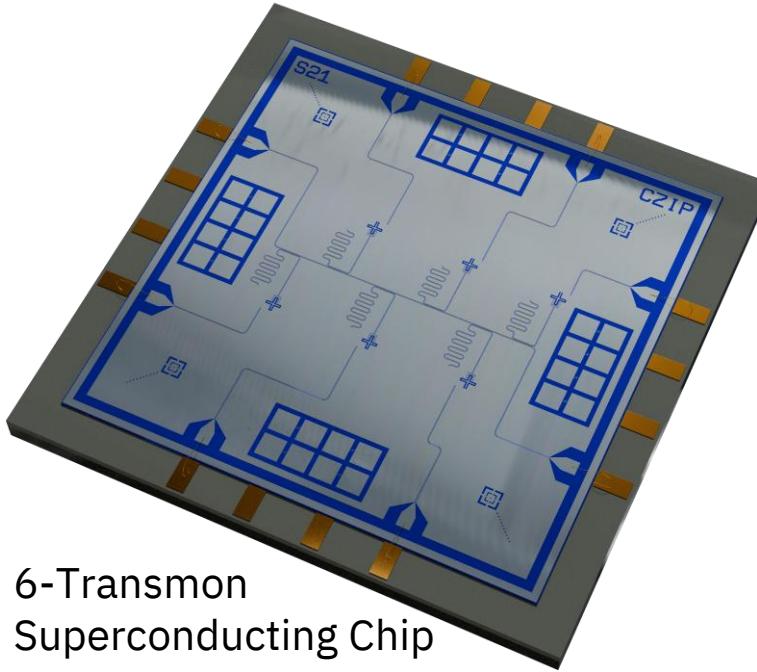


Some images of cryogenically compatible memory chips fabricated by me
(taken through an optical microscope + phone camera).

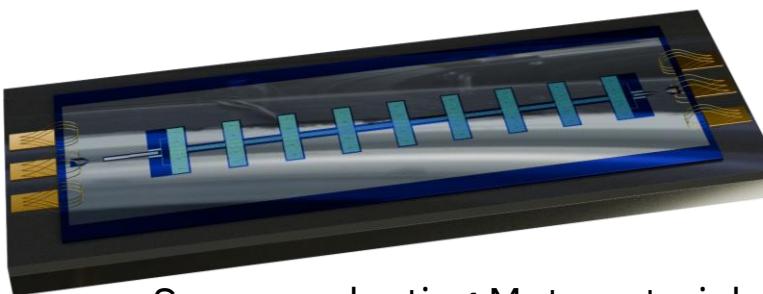
Examples at the Chip Level (Rendered with Blender)



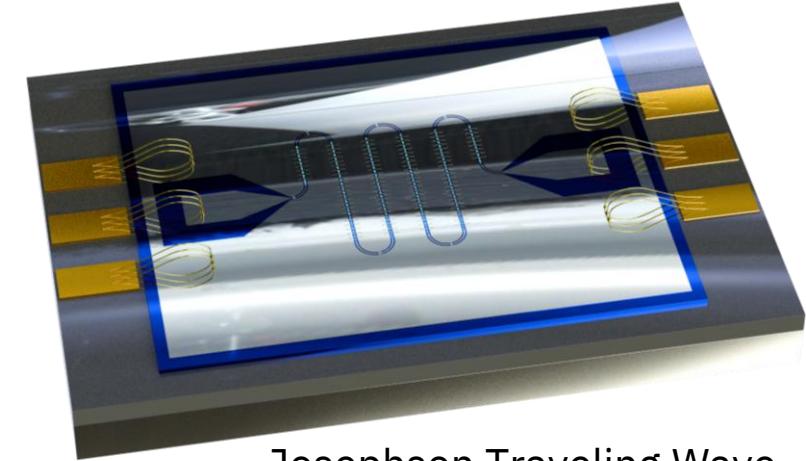
Classical Chips



6-Transmon
Superconducting Chip



Superconducting Metamaterial
Waveguide Resonator Chip

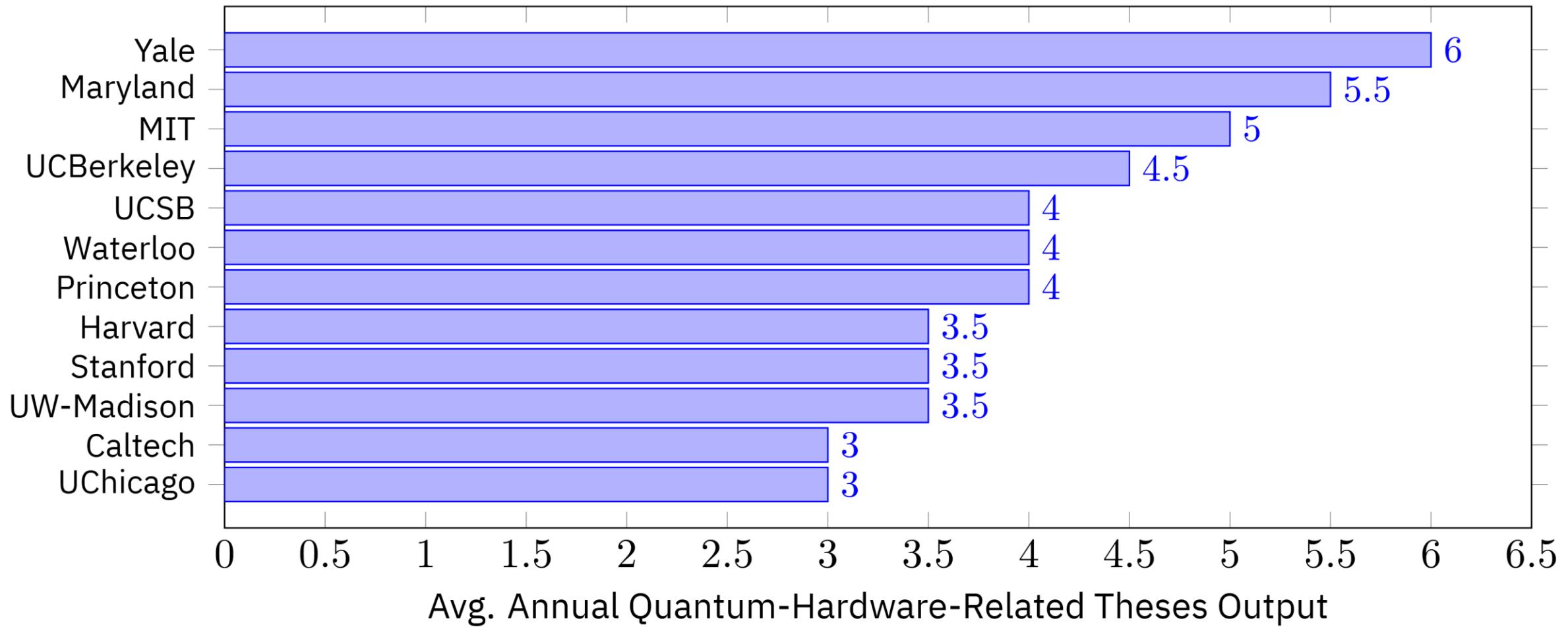


Josephson Traveling Wave
Parametric Amplifier Chip



Coplanar Waveguide
Single Resonator Chip

Quantum Hardware Related Graduate Research in the US & Canada



Extensive List of Quantum Hardware Categories

+-- I. Quantum-Core Hardware

- | +-+ A. Qubit Technologies
 - | | +-+ 1. Superconducting Qubits
 - | | | - Transmon, Fluxonium, Flux qubit
 - | | | - Cavity-protected (cat, binomial, GKP-encoded)
 - | | +-+ 2. Spin-Based Qubits
 - | | | +-+ a. Semiconductor Spins (Si/SiGe, GaAs, donors, NV)
 - | | | +-+ b. Magnetic and Molecular Spins
 - | | | | - Magnetic clusters (Fe8, Mn12, heterometallic rings, other candidates)
 - | | | | - Magnetic nanodisks (meron/skyrmion qubits)
 - | | +-+ 3. Bosons (microwave photons, phonons, magnons)
 - | | +-+ 4. Topological/Majorana Candidates
- | +-+ B. Quantum Interconnects ("Buses")
 - | | +-+ 1. Planar Resonators (CPW lambda/4, lambda/2, lumped, stripline)
 - | | +-+ 2. 3-D Superconducting Cavities
 - | | +-+ 3. Metamaterial Waveguides & Resonators
 - | | +-+ 4. Photonic Waveguides & Ring-resonator PICs
 - | | +-+ 5. Hybrid Quantum Transducers (electro-optic, electro-acoustic, magnonic)
- | +-+ C. Quantum-Limited & Quantum-Enhanced Detectors
 - | | +-+ 1. SNSPD
 - | | +-+ 2. KID/MKID
 - | | +-+ 3. Josephson Photomultipliers (JPM) & Photonics
 - | | +-+ 4. Quantum-optimized Bolometers/Calorimeters
- | +-+ D. Quantum Memories
 - | | +-+ 1. Rare-earth AFC crystals
 - | | +-+ 2. Magnon memories
 - | | +-+ 3. 3-D Cat-code cavities
 - | | +-+ 4. Nuclear-spin ensembles
- | +-+ E. Quantum Photonic Integrated Circuits (QPICs)
 - | | +-+ 1. SiN/Si/SiO2 wafer-scale
 - | | +-+ 2. III-V hybrids (GaAs, InP)
 - | | +-+ 3. Diamond & LiNbO3

+-- II. Quantum-Adjacent Hardware

- | +-+ A. Cryogenic Digital Control Logic
 - | | +-+ 1. Single-Flux-Quantum families (RSFQ, RQL, AQFP, eSFQ)
 - | | +-+ 2. Deep-Cryo CMOS (4 K)
 - | | +-+ 3. Milli-Kelvin CMOS (<= 100 mK)
- | +-+ B. Cryogenic Mixed-Signal & RF ICs
 - | | +-+ 1. Time-interleaved DAC/ADC
 - | | +-+ 2. RF Transceiver SoCs (2-18 GHz I/Q)
 - | | +-+ 3. Cryo Class-D Drivers/Piezo
- | +-+ C. Cryogenic Amplifiers, Filters, & Passive Components
 - | | +-+ 1. mK Parametric Pre-Amplifiers
 - | | | a. Flux-pumped Josephson Parametric Amplifier/Converter (JPA/JPC)
 - | | | b. Josephson Traveling-Wave Parametric Amplifier (JTWPA)
 - | | | c. Kinetic-Inductance Traveling-Wave Parametric Amplifier (KI-TWPA)
 - | | | d. Nanobridge Kinetic Parametric Amplifier (NKPA)
 - | | | e. Quantum Capacitance Parametric Amplifier (QCPA)
 - | | | f. SNAIL-based Parametric Amplifier (SPA/SNAIL-TWPA)
 - | | +-+ 2. 4 K HEMT LNAs (octave-wide, high dynamic range)
 - | | +-+ 3. RF Isolators/Circulators (ferrite or on-chip)
 - | | +-+ 4. Superconducting & SAW Filters
- | +-+ D. Cryogenic Packaging & Interconnects
 - | | +-+ 1. Flex-print & interposer tiles
 - | | +-+ 2. 3-D cavities w/ cryogenic bump-bonds/ interconnects
 - | | +-+ 3. Coax/waveguide/stripline wiring (NbTi, Nb, CuNi)
 - | | +-+ 4. Optical fiber feedthroughs (1-4 K)
 - | | +-+ 5. Magnetic & vibration shielding, radiation hardeners
- | +-+ E. Cryogenic Memory & Storage
 - | | +-+ 1. SRAM (FinFET 14-nm & 5-nm cryo-SRAM)
 - | | +-+ 2. Floating-Body RAM (FBRAM) at 77 K
 - | | +-+ 3. Capacitor-less eDRAM/DRAM benchmarks (2T0C, 4 K)
 - | | +-+ 4. JJ-based RAM (JJ-RAM, JMRAM)
 - | | +-+ 5. Spin-orbit-torque (SOT) MRAM at 4 K

Some Portmanteaus

- Portmanteaus
 - Transistor
 - transconductance + varistor
 - transconductance + variable + resistor
 - transfer + resistor (widely accepted)
 - Spintronics
 - spin + transport + electronics
 - spin + electronics
 - Qubits
 - quantum + bit
 - quantum + binary + digit
 - Qudits
 - quantum + digit

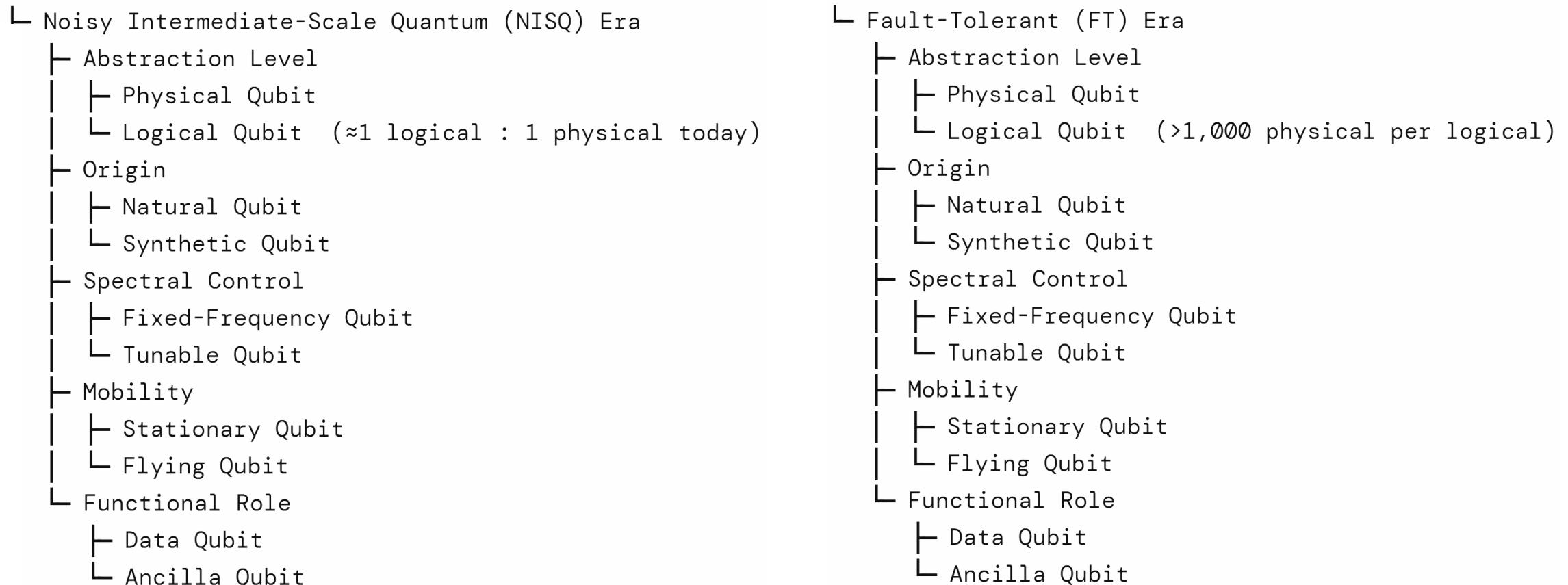
Qubit Classification Trees

Qudit-Related Relationships of Quantum Information Carriers

- └ Terminology

- └ Qubit = dimension-2 qudit
- └ Qutrit = dimension-3 qudit
- └ Ququart = dimension-4 qudit
- └ Qudit = quantum digit (general dimension)

Qubit Classification Trees



Quantum Stack



Quantum
Algorithms

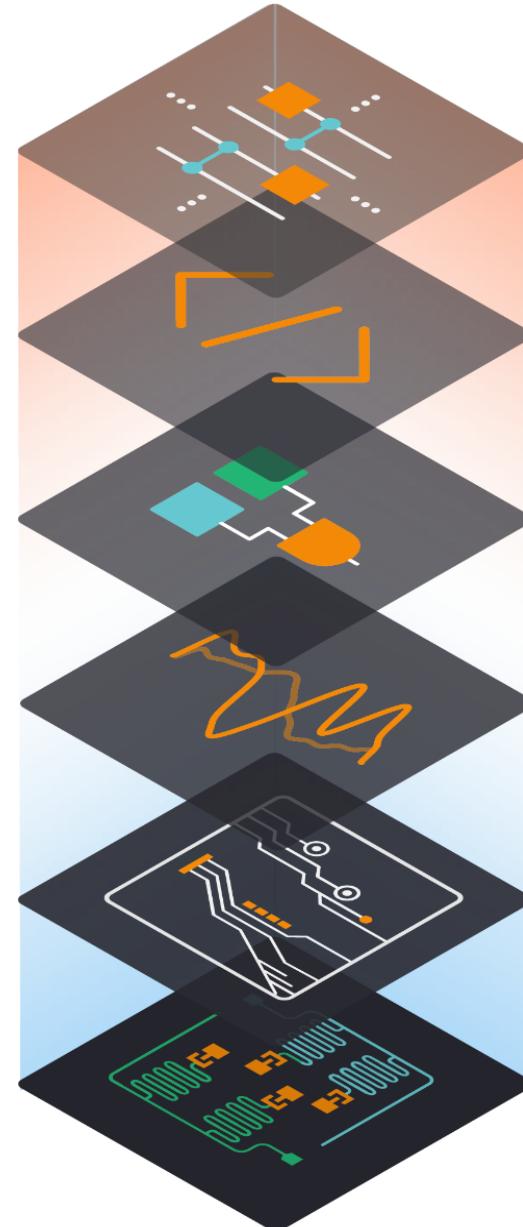
Control
Software

Control
Electronics

μ wave signal
processing

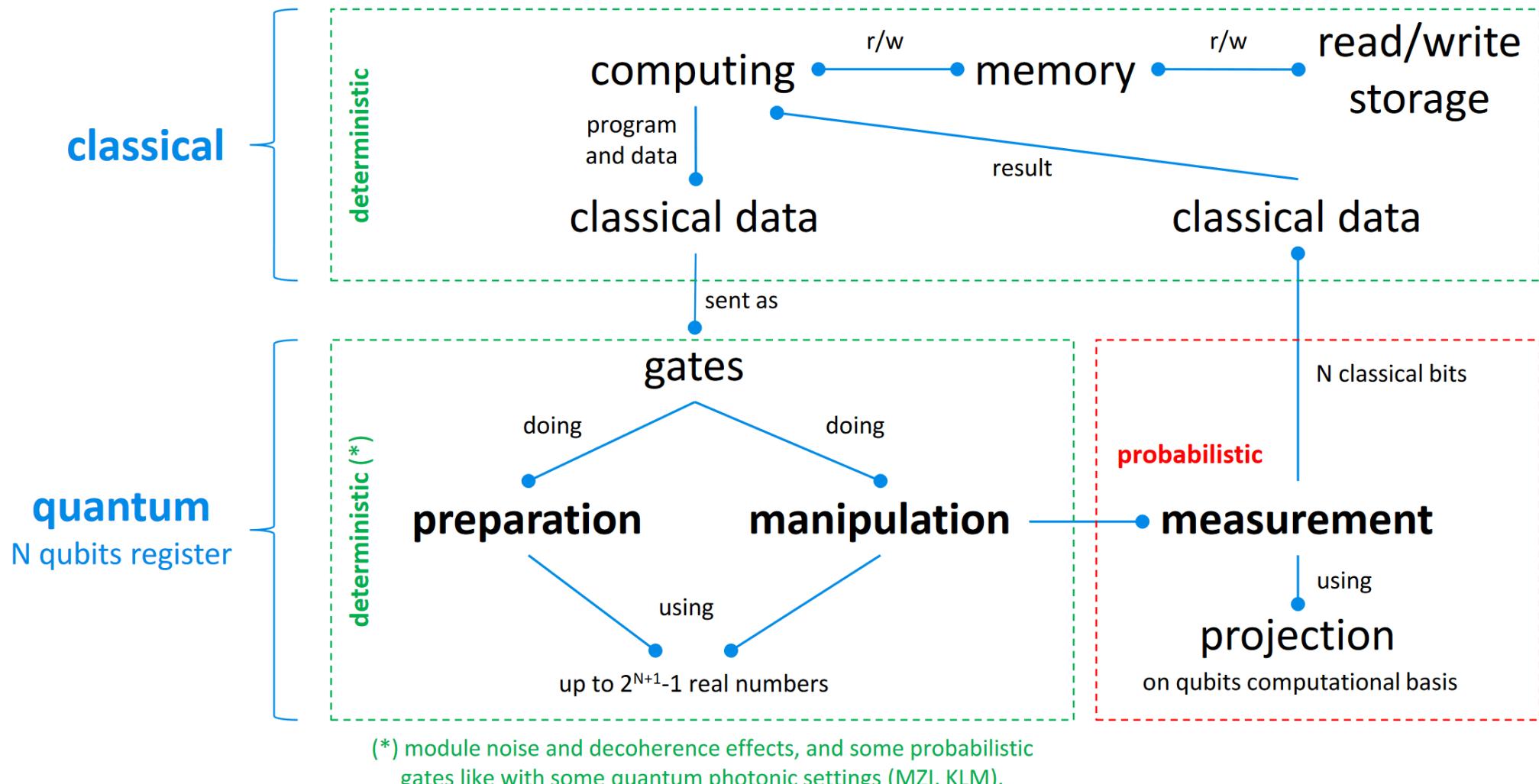
Cryogenics &
interconnects

Device

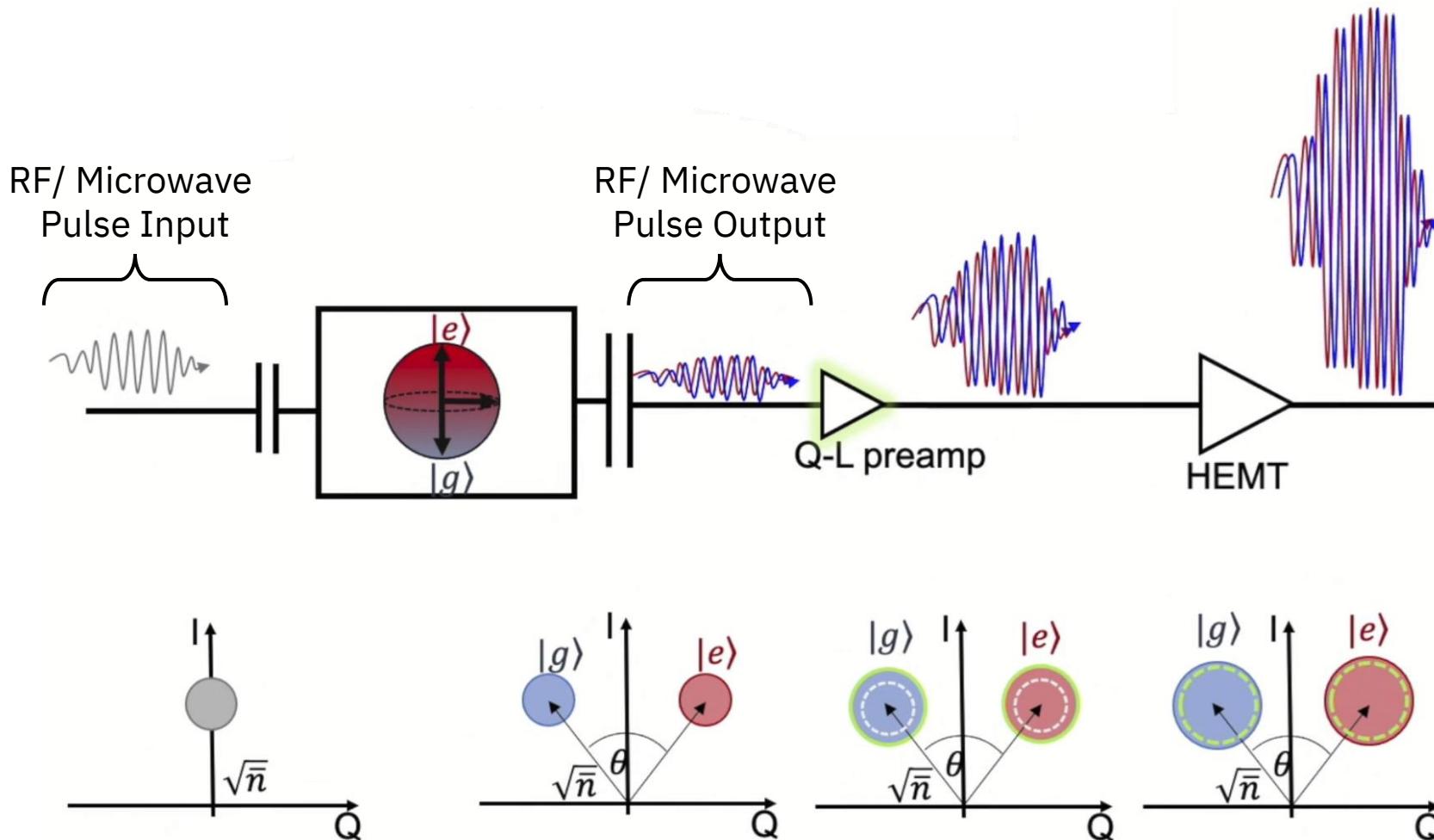


Workflow for Gate-Based Quantum Computing

- Every quantum gate has a unique waveform for every physical gate supported by the system.



Context: A Conventional Quantum System Workflow (w/ Quantum-Limited Amplification)



Note: this workflow is generally applicable for quantum computing hardware, although the output signal may differ (RF/MW vs. charge steps)

HEMT = High Electron Mobility Transistor [Amp.]

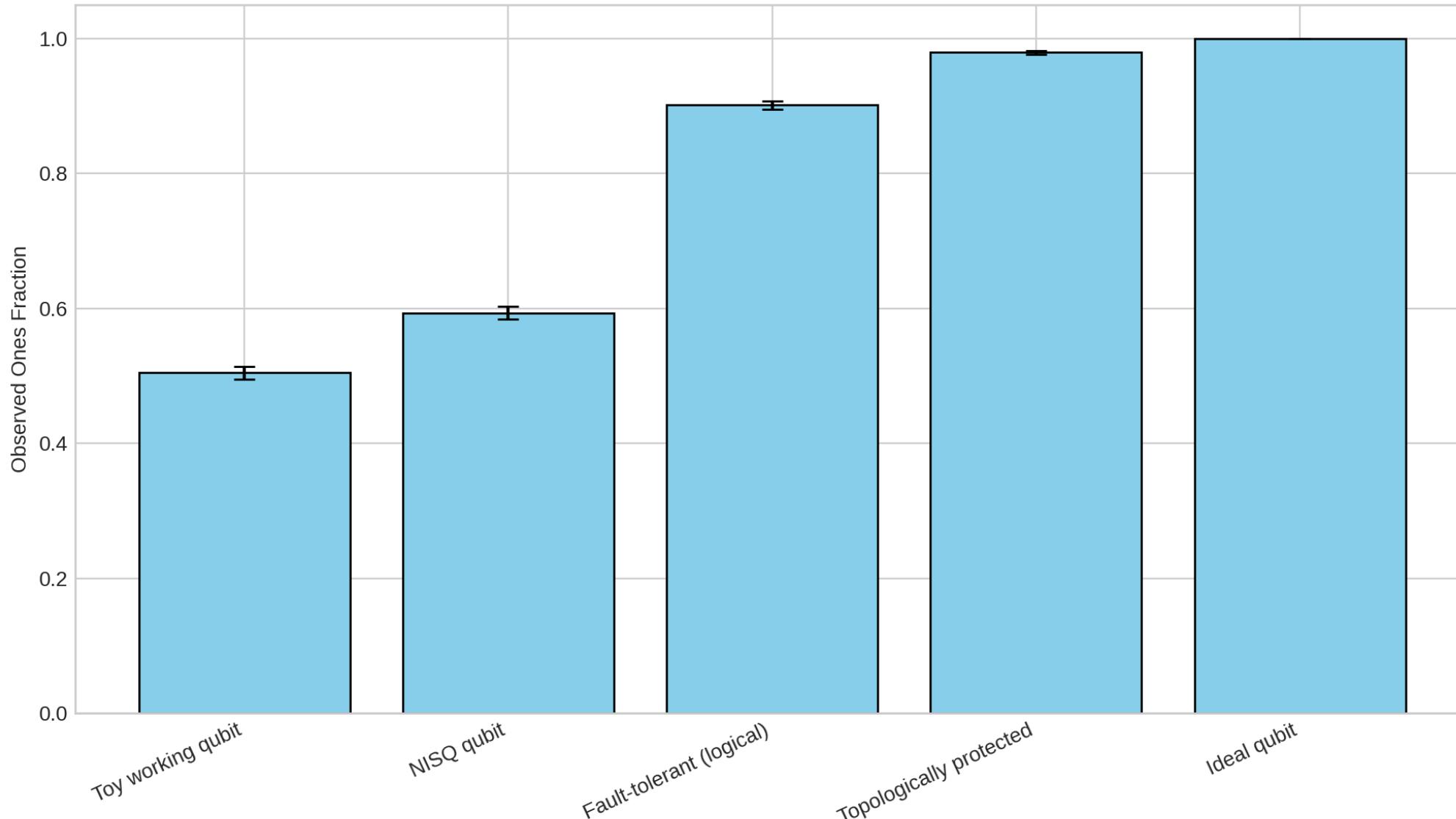
How to Think About The Outcome of Qubits Based on Their Classification

Model	Target p	Shots	(Successes)	(Failures)	Successes Fraction (Observed p)	Wilson CI 95% Low	Wilson CI 95% High	CI Width (95%)	Required Shots for ±2%	Required Shots for ±1%	Required Shots for ±0.5%
Toy working qubit	0.50	10,000	5,025	4,975	0.5025	0.4927	0.5123	0.0196	2,401	9,604	38,415
NISQ qubit	0.60	10,000	6,010	3,990	0.6010	0.5914	0.6105	0.0191	2,305	9,220	36,878
Fault-tolerant (logical)	0.90	10,000	9,013	987	0.9013	0.8956	0.9067	0.0111	865	3,458	13,830
Topologically protected	0.98	10,000	9,797	203	0.9797	0.9769	0.9822	0.0053	189	753	3,011
Ideal qubit	1.00	10,000	10,000	0	1.0000	0.9996	1.0000	0.0004	1	1	1

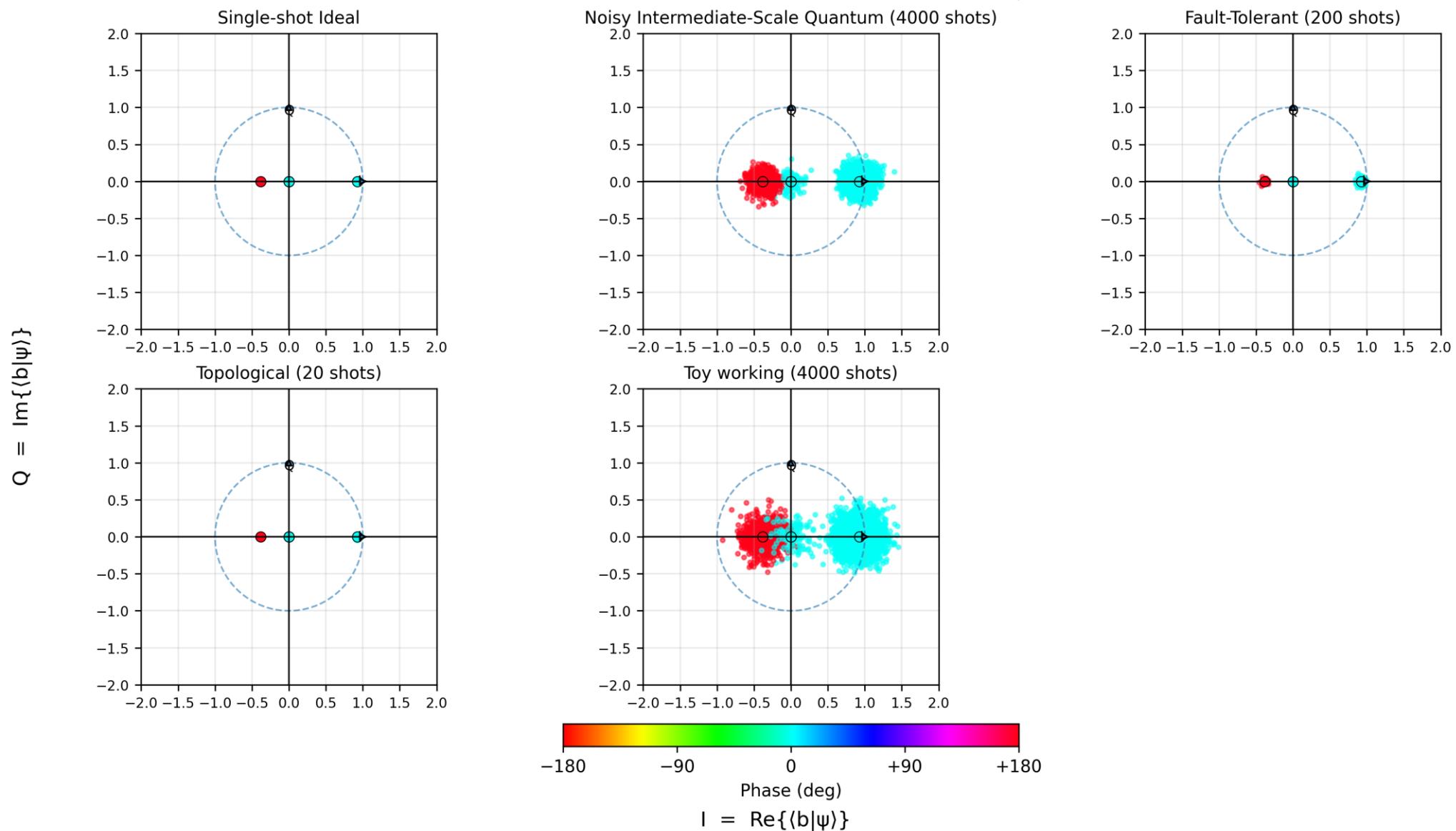
- **Toy working qubit** — Simple demonstrator; about half shots meet the criterion.
- **NISQ qubit** — Noisy Intermediate-Scale Quantum device; modest success rate above chance.
- **Fault-tolerant (logical)** — Error-corrected logical qubit; high single-shot success probability.
- **Topologically protected** — Intrinsic protection; very high single-shot success probability.
- **Ideal qubit** — Theoretical perfect qubit; always successful in a single shot.

Illustrative Single-Shot Success Rates for Qubit Types

Observed Single-Shot Success Rates with 95% Wilson CI

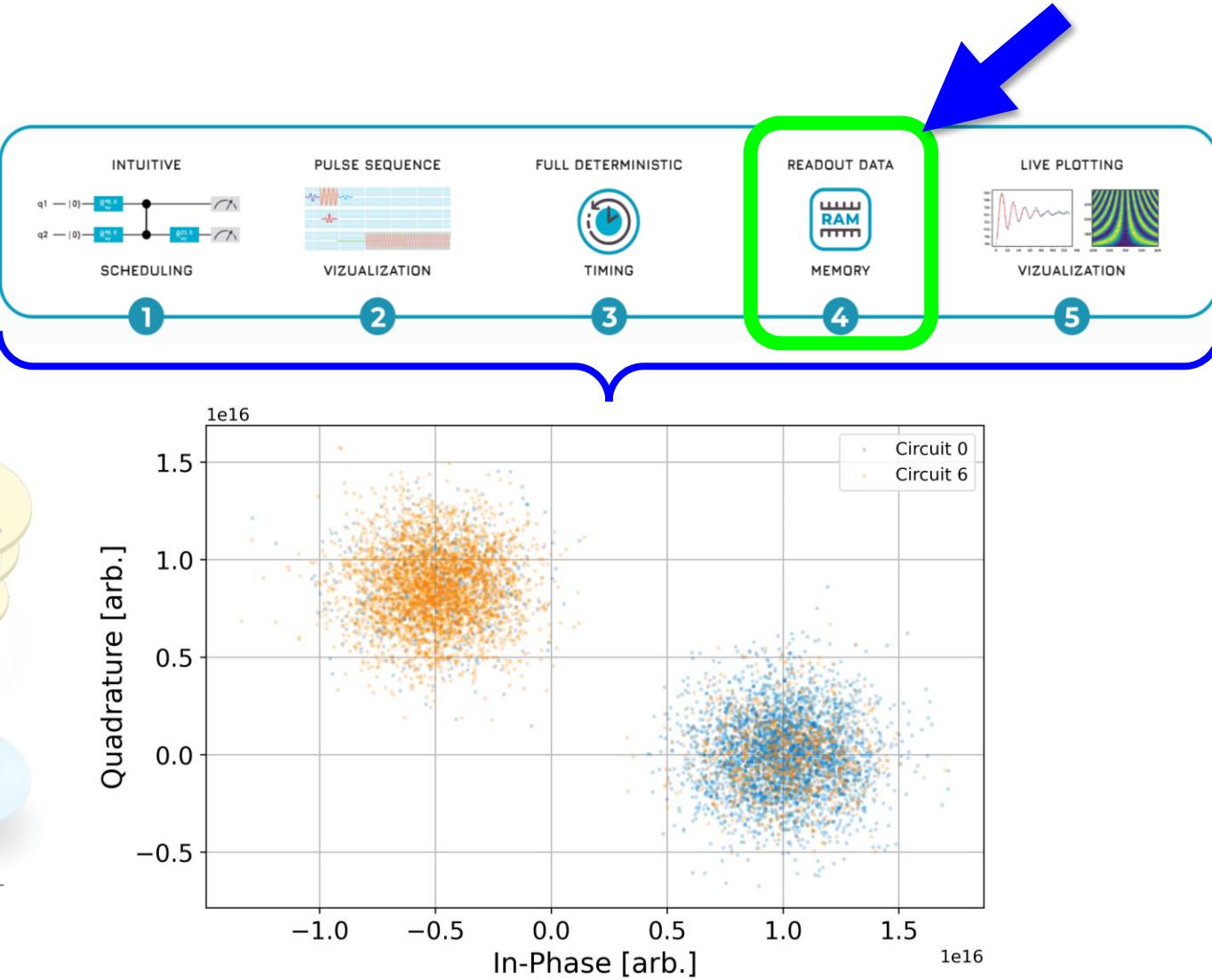
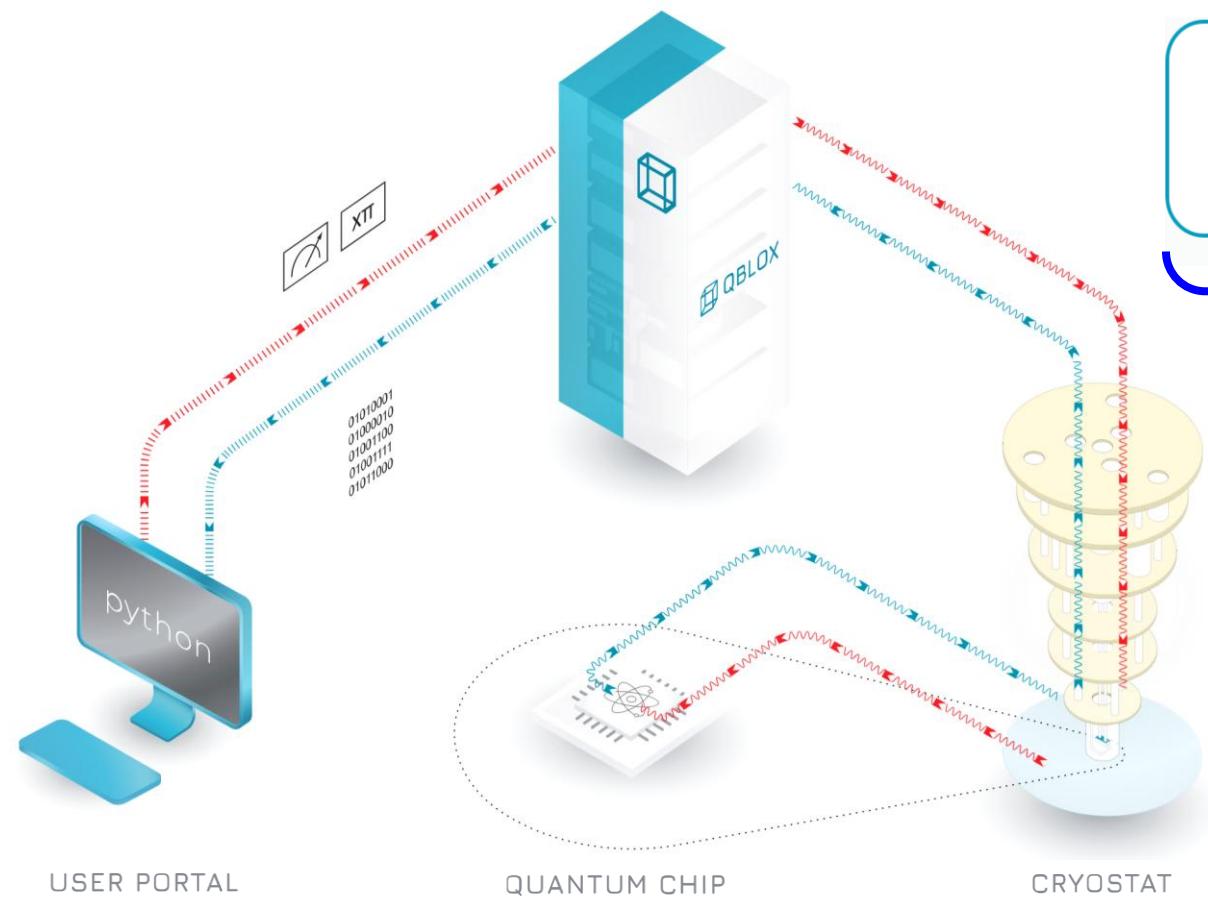


Illustrative Single-to-Multi-Shot Success Rates for Qubits

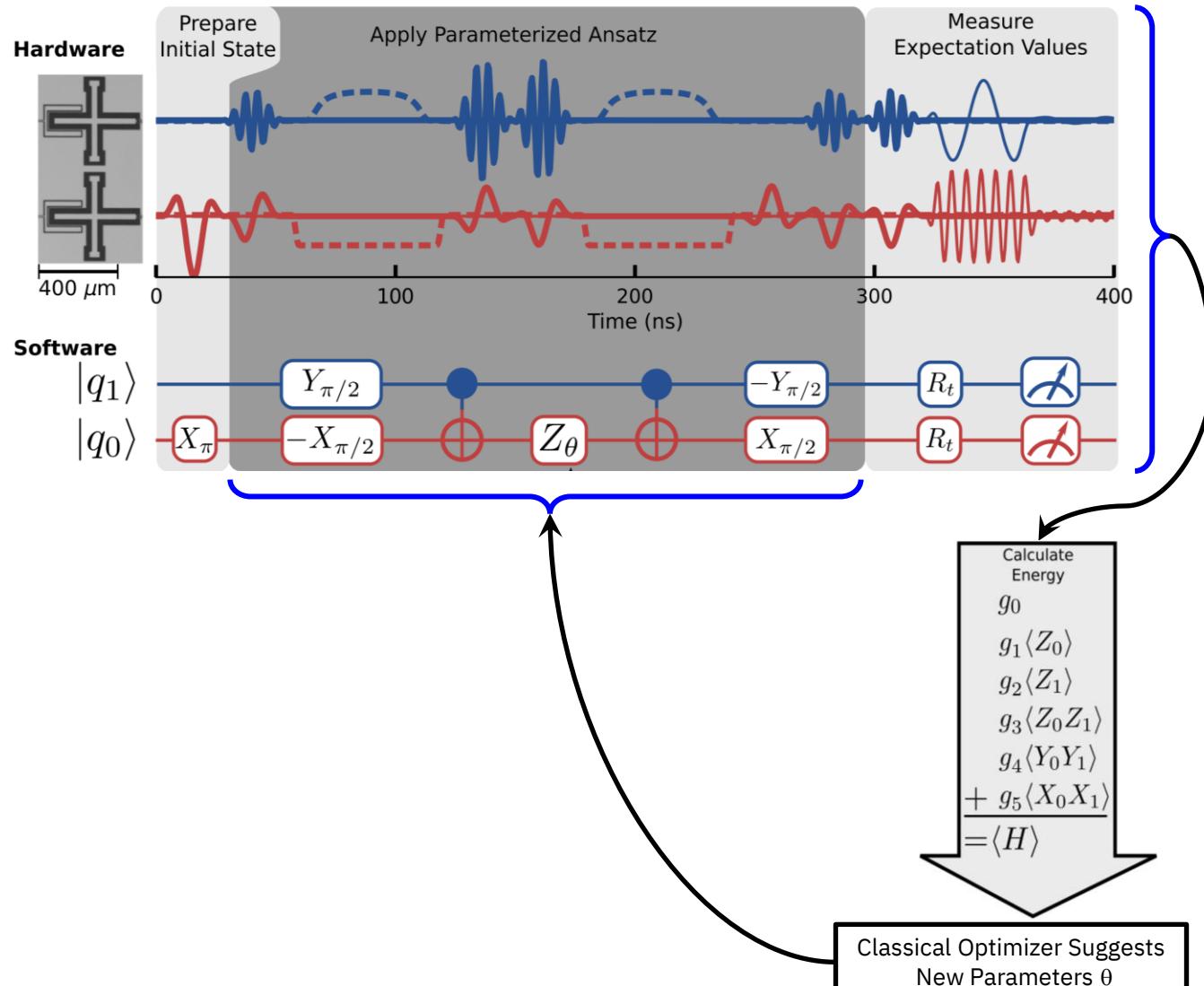
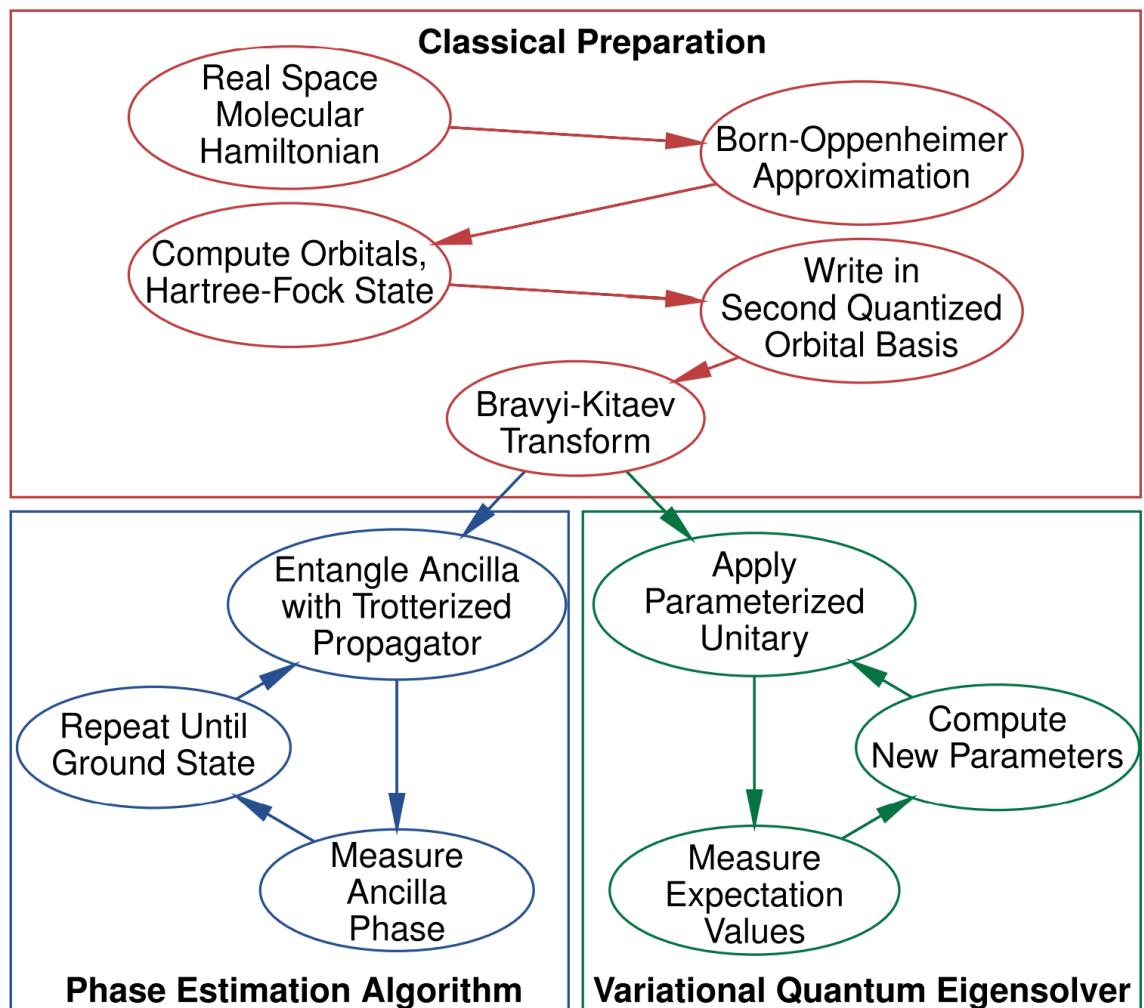


Available at: github.com/OJB-Quantum/QC-Hardware-How-To

Generic Qubit Drive & Readout Workflow w/ Example



Example of Required Steps to Compute Molecular Energies



1. van Dijk et al., *Microprocessors and Microsystems* 6, 2019.02.004 (2019)
2. Adapted from: O'Malley et al., *Phys. Rev. X*, 6 031007 (2016)

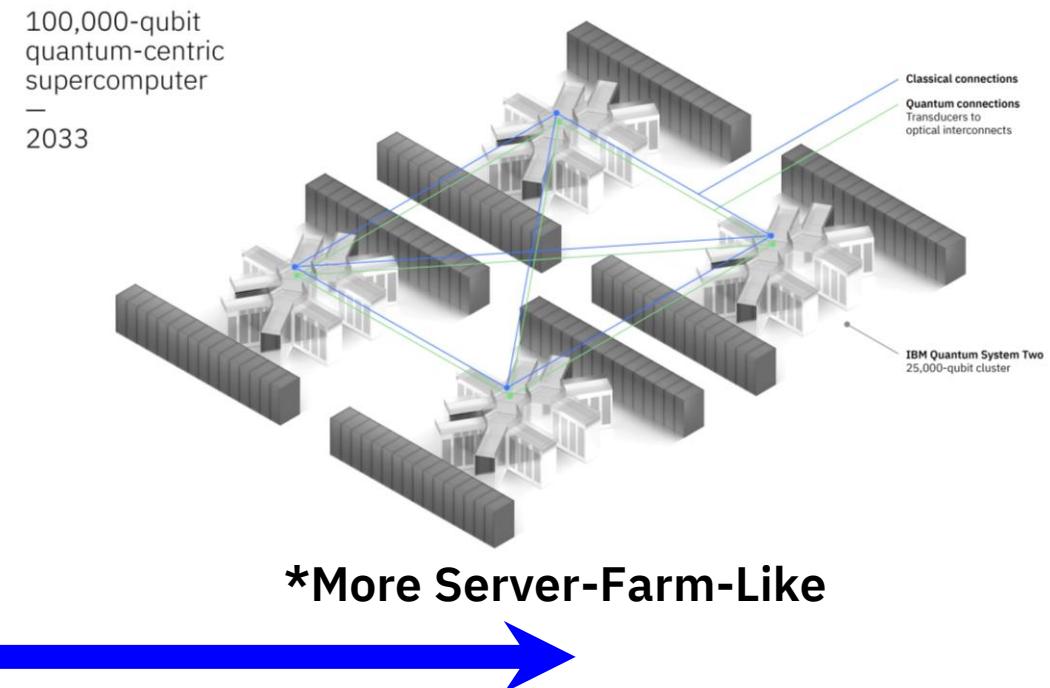
Quantum Systems Range in Size

- In configuring quantum machines, it is useful to know that **control components** have been made available in various sizes and formfactors.
- Control components for qubits can take up a **lot of hardware space/ footprint**.
 - However, an effort has been made to miniaturize them using cryo-compatible:
 - Complementary Metal Oxide Semiconductor (CMOS) chips.
 - Application Specific Integrated Circuit (ASIC) or Field-Programmable Gate Array (FPGA) chips.



More Desktop-Like

Up to 3-qubit desktop quantum PC (novelty).
Price ≈ \$5,000
FPGA-controlled NMR



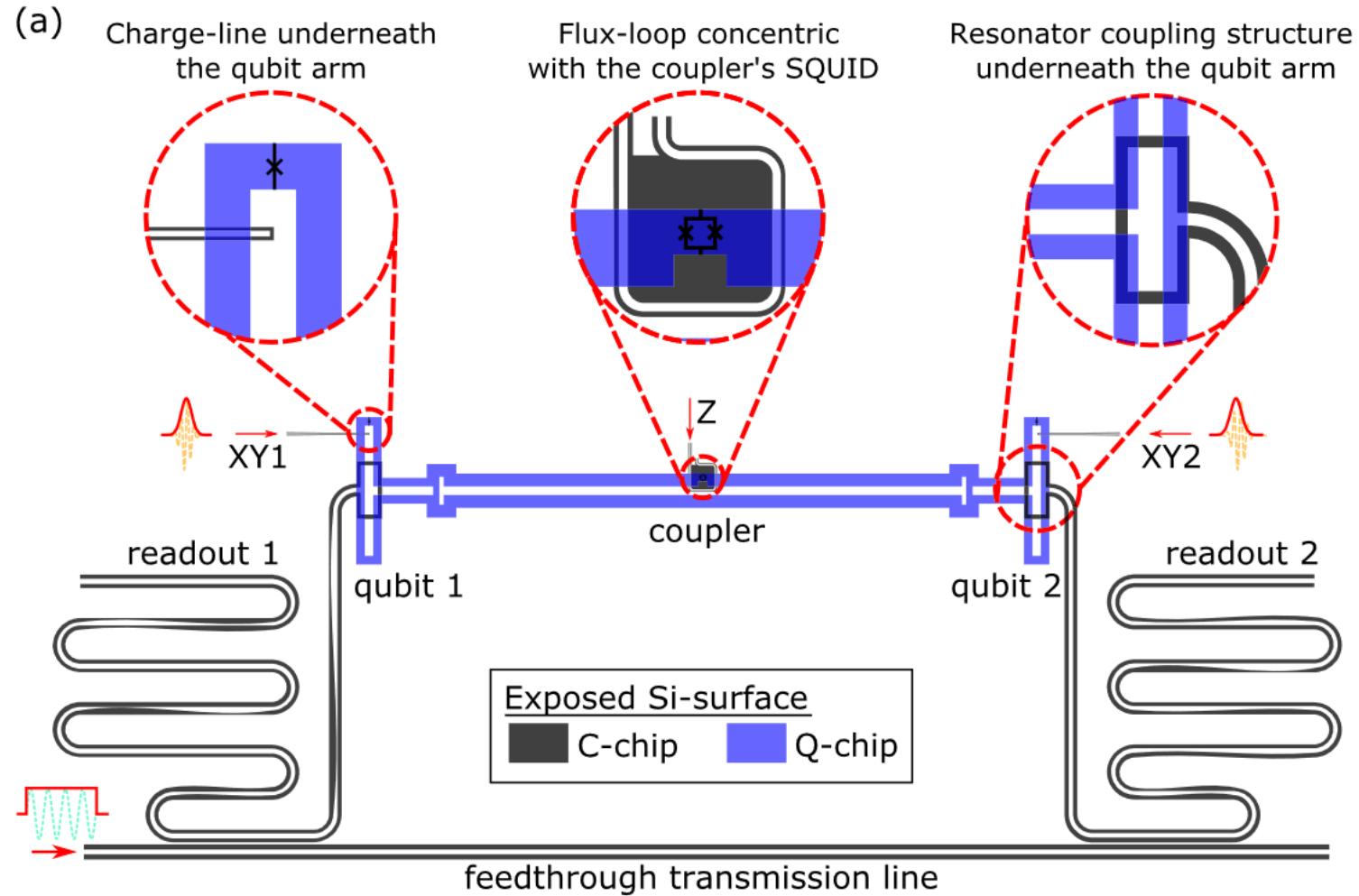
1. SpinQ, Gemini 2 [2-Qubit System] (2022)
2. IBM Research

*Also called server-clusters

Advanced Quantum Computers Are Controlled Using 2 Approaches

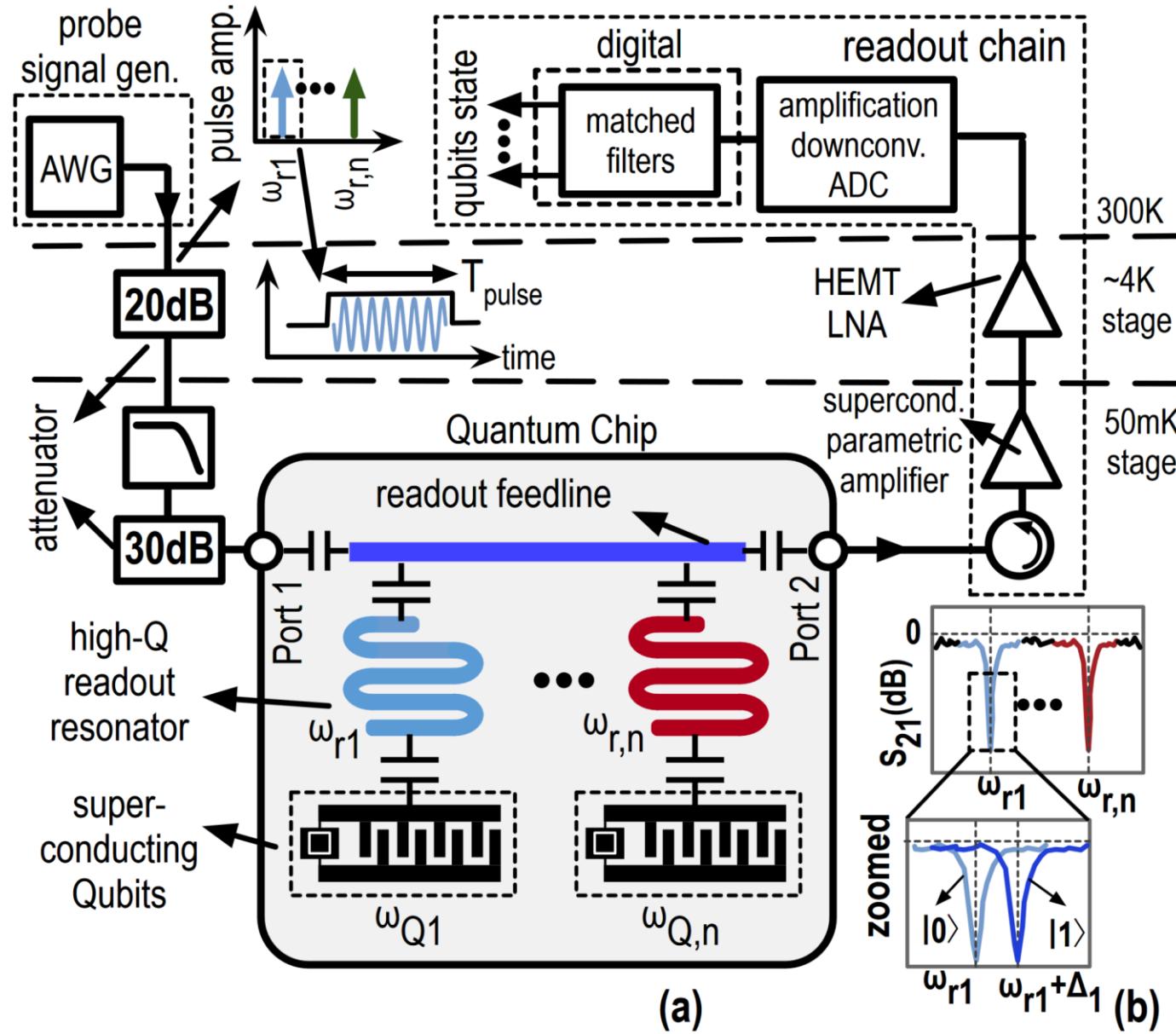
Controller Type	Full Name	Description
Cryo-FPGA	Cryogenic Field Programmable Gate Array	A reconfigurable logic device designed to operate at cryogenic temperatures, used for flexible signal processing and control of qubits.
Cryo-ASIC	Cryogenic Application Specific Integrated Circuit	A custom-designed integrated circuit optimized for cryogenic operation, tailored for efficient and low-power qubit control and readout.

Linkable Quantum Computing Systems



Momentary flux tuning of the coupler temporarily turns on an entangling two-qubit interaction, then returns to idle to minimize ZZ. Here, ZZ is an undesired static two-qubit interaction (cross-Kerr).

Linkable Quantum Computing Systems



1. [Mehrpoor et al., IEEE ISCAS 8702452 \(2019\)](#)

Other Entangling Mediators Per Qubit Platform Based on Hardware Scaling Requirements

- |- Superconducting
 - | Cross-Resonance → ZX (drive-induced dispersive) → CNOT/eCR
 - | Tunable Coupler → exchange/ZZ (flux or parametric) → CZ, iSWAP, fSim
 - | Bus-RIP → dispersive ZZ (driven resonator) → CZ, multi-qubit phase
 - | MAP/CCR → engineered higher-levels/ exchange → CPHASE, iSWAP
- |- Trapped Ions
 - | Mølmer-Sørensen → XX/YY (spin-dep. force via phonons) → CNOT-equiv.
 - | Cirac-Zoller → sideband-mediated (phonon bus) → CNOT
- |- Neutral Atoms
 - | Rydberg blockade → Ising-like ZZ (vdW shift) → CZ/CNOT
- |- Semiconductor Spins
 - | Exchange J(V) → Heisenberg/Ising-like → CZ/CNOT/(\sqrt{V})iSWAP
 - | Capacitive → dipole-dipole (charge-assisted) → CZ/iSWAP-like
 - | cQED resonator → exchange via virtual photons → iSWAP/fSim
- |- NV Centers
 - | Spin-photon link → heralded entanglement → Bell/parity ops
 - | Dipolar (local) → secular dipole terms → CZ/SWAP-like
- |- Photonics
 - | Linear optics → measurement-induced nonlinearity → CZ/CNOT (prob.)
 - | CV squeezing → Gaussian entanglers → MBQC two-mode ops

Current Memory & Waveform Use Flowchart for Quantum

- Leading to the comparison between specialized waveform memory and the use of RAM for wave encoding.
- Every quantum gate has a unique waveform for every physical gate supported by the system. The data points along the envelope are something that can be stored in classical memory.

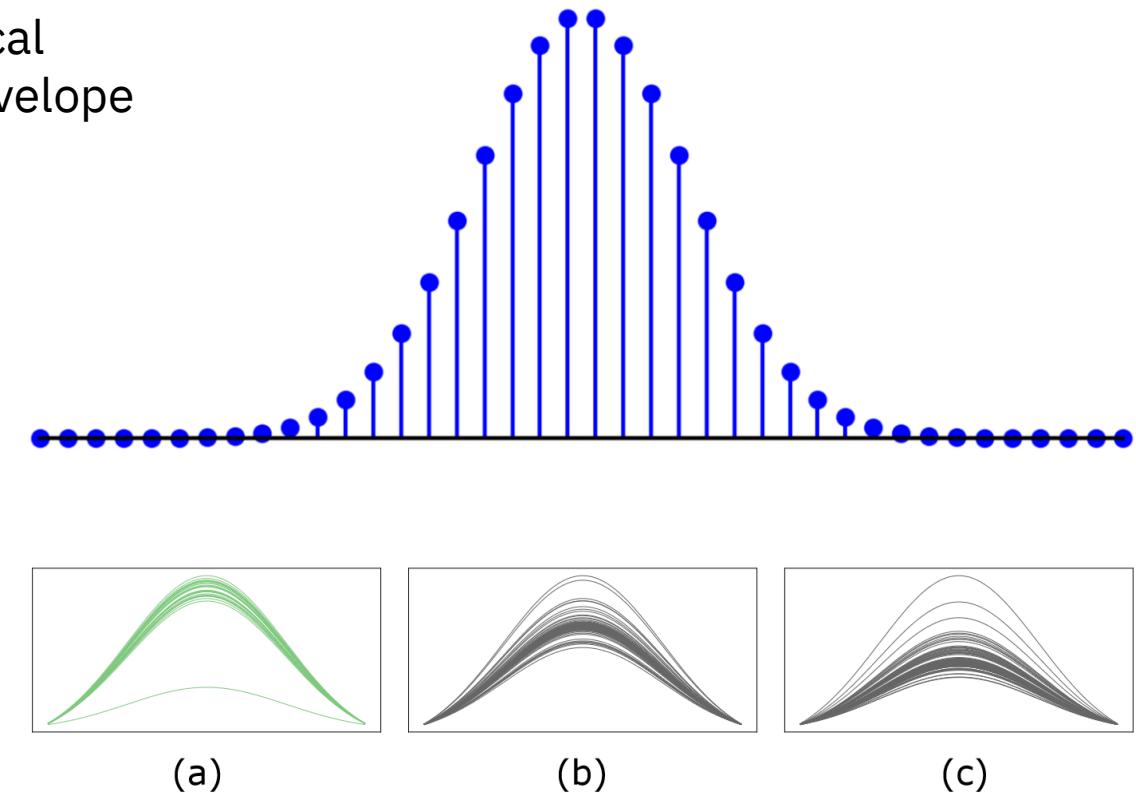
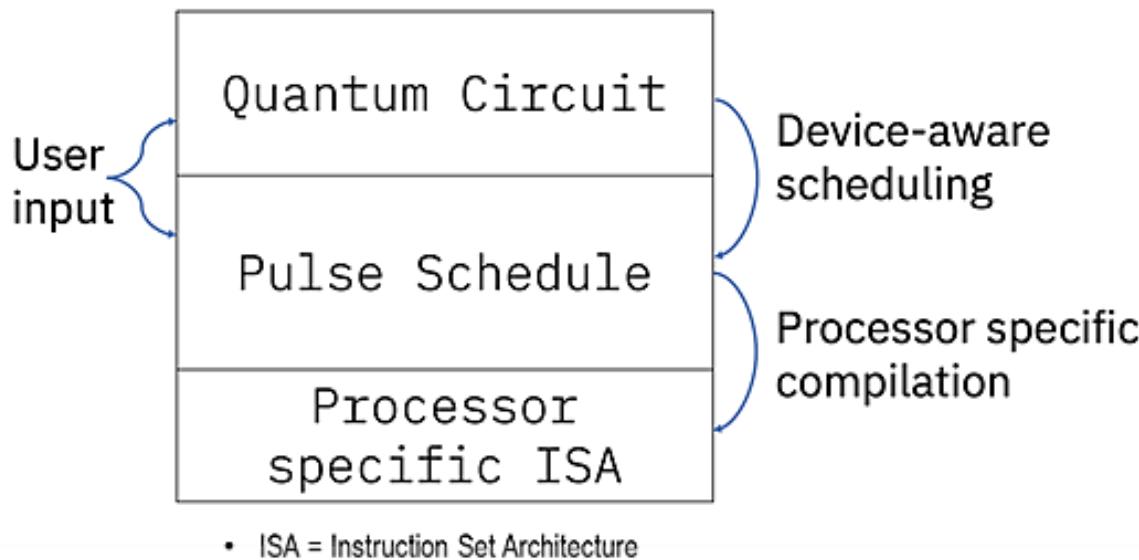
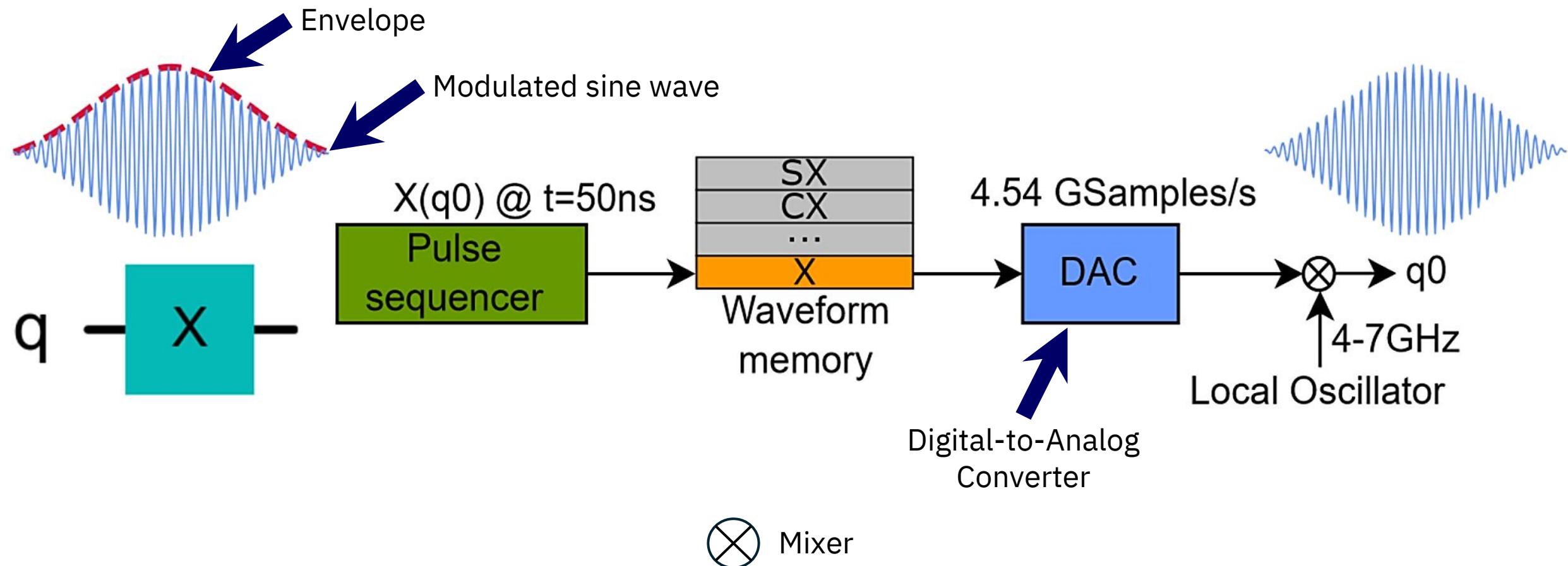


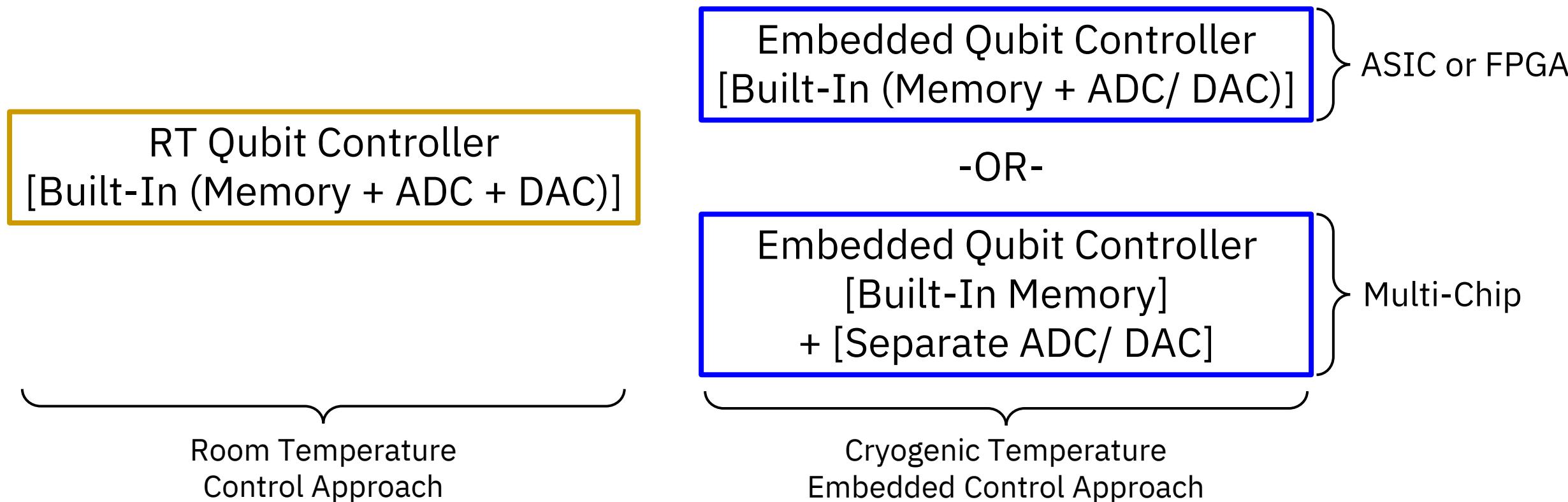
Figure 4. π -pulse shapes of all (a) 27 qubits on IBM Toronto (b) 65 qubits on IBM Brooklyn (c) 127 qubits on IBM Washington machines.

Qubit Control Pulse Generation Pipeline

- Every quantum gate has a unique waveform for every physical gate supported by the system.
- In this example, the mixer helps with up-conversion (from MHz tone to suitable GHz tones).



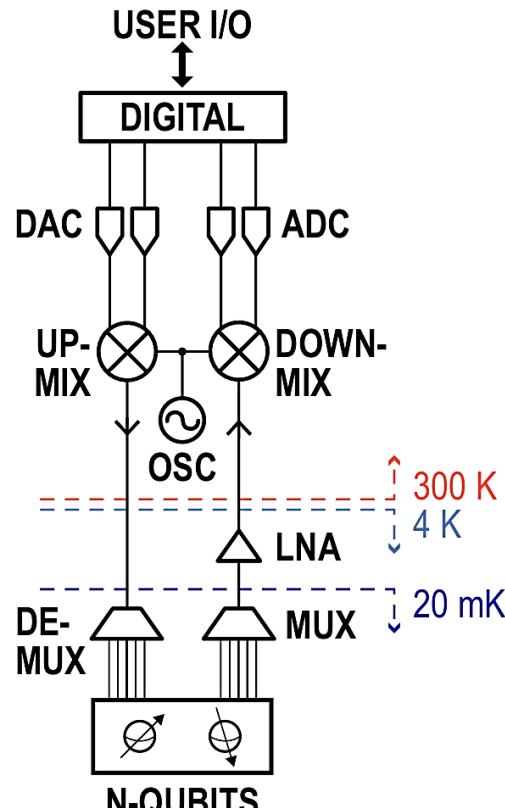
Room Temp. Control vs. Embedded Cryogenic Control of Qubits



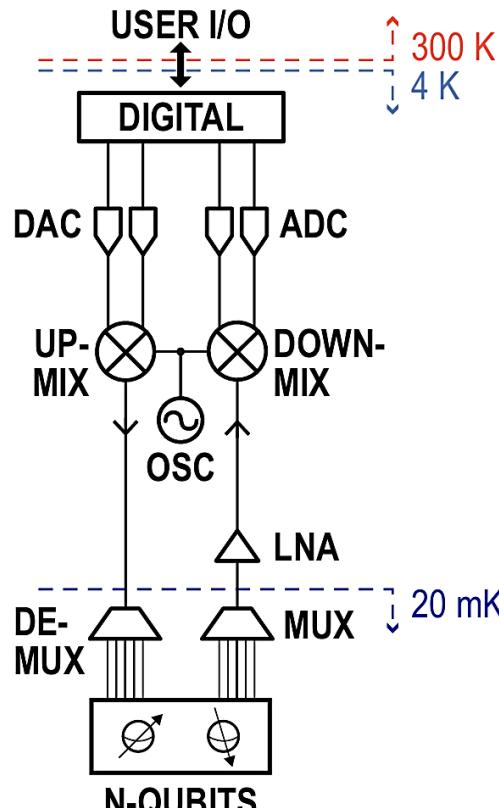
Note: Here, cryogenic is referred to as being below 123 K.
*SoC: System on a Chip

1. [Pobell, Matter and Methods at Low Temp. 3rd ed. Springer, 978-3-540-46360-3 \(2007\)](#)

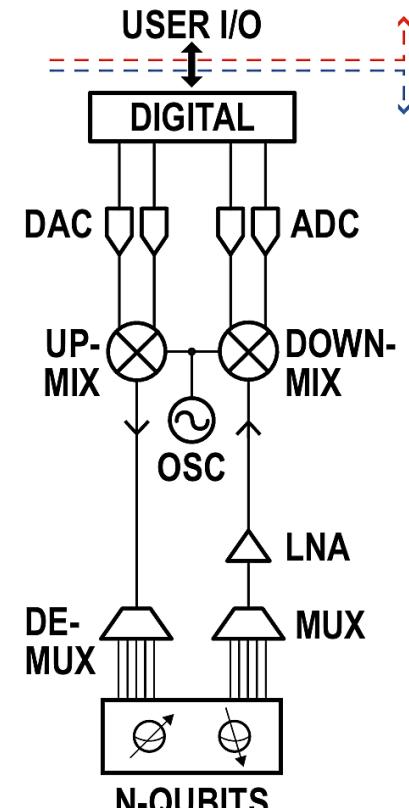
Linkable Quantum Computing Systems (Architecture Level)



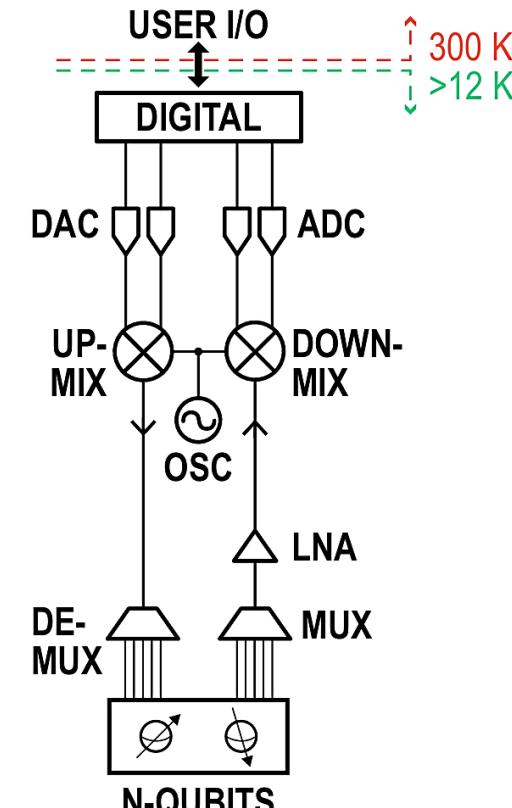
Currently Available



Short Term



Near Future



Distant Future

Common Cryostat Formfactors

Item	
Large-frame dilution refrigerator (DR).	
Floor standing cryostat (cryogen-free PPMS-type).	
Floor standing cryostat (liquid cryogen Dewar type).	

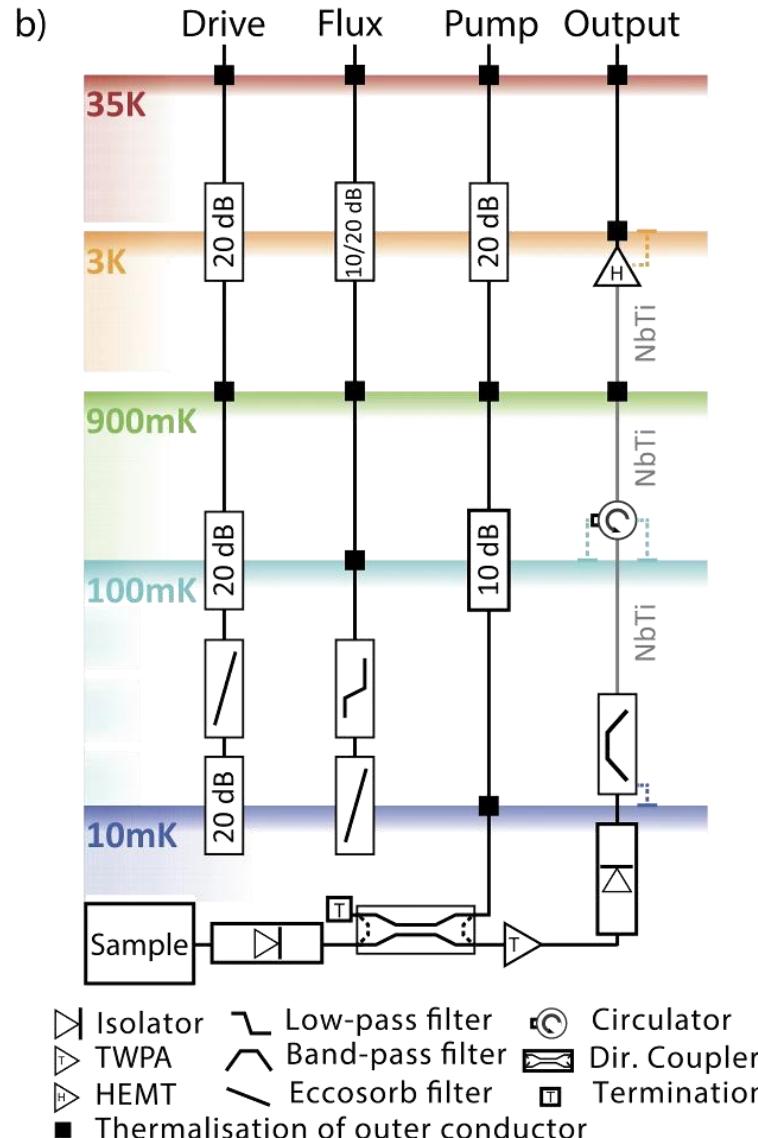
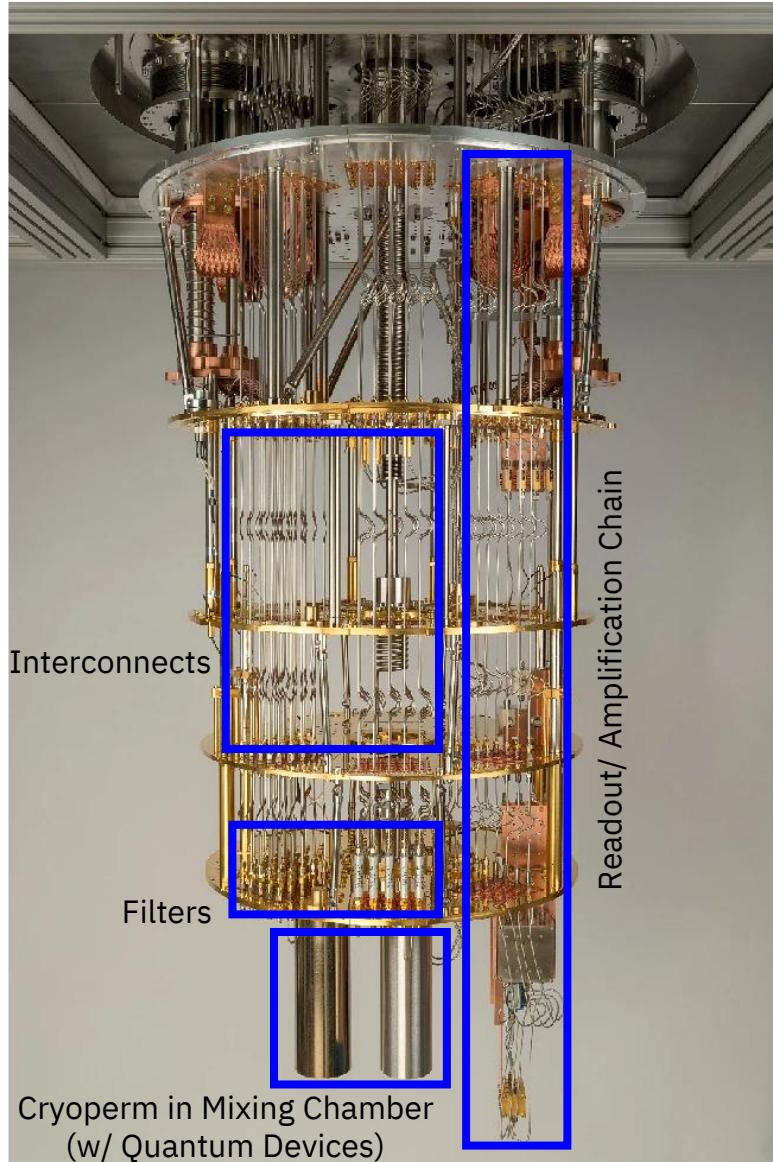
DR available
(Integrated or
insert attachment)

No DR available

Can be rendered in 3D and with ray tracing in **Blender** for educational purposes.

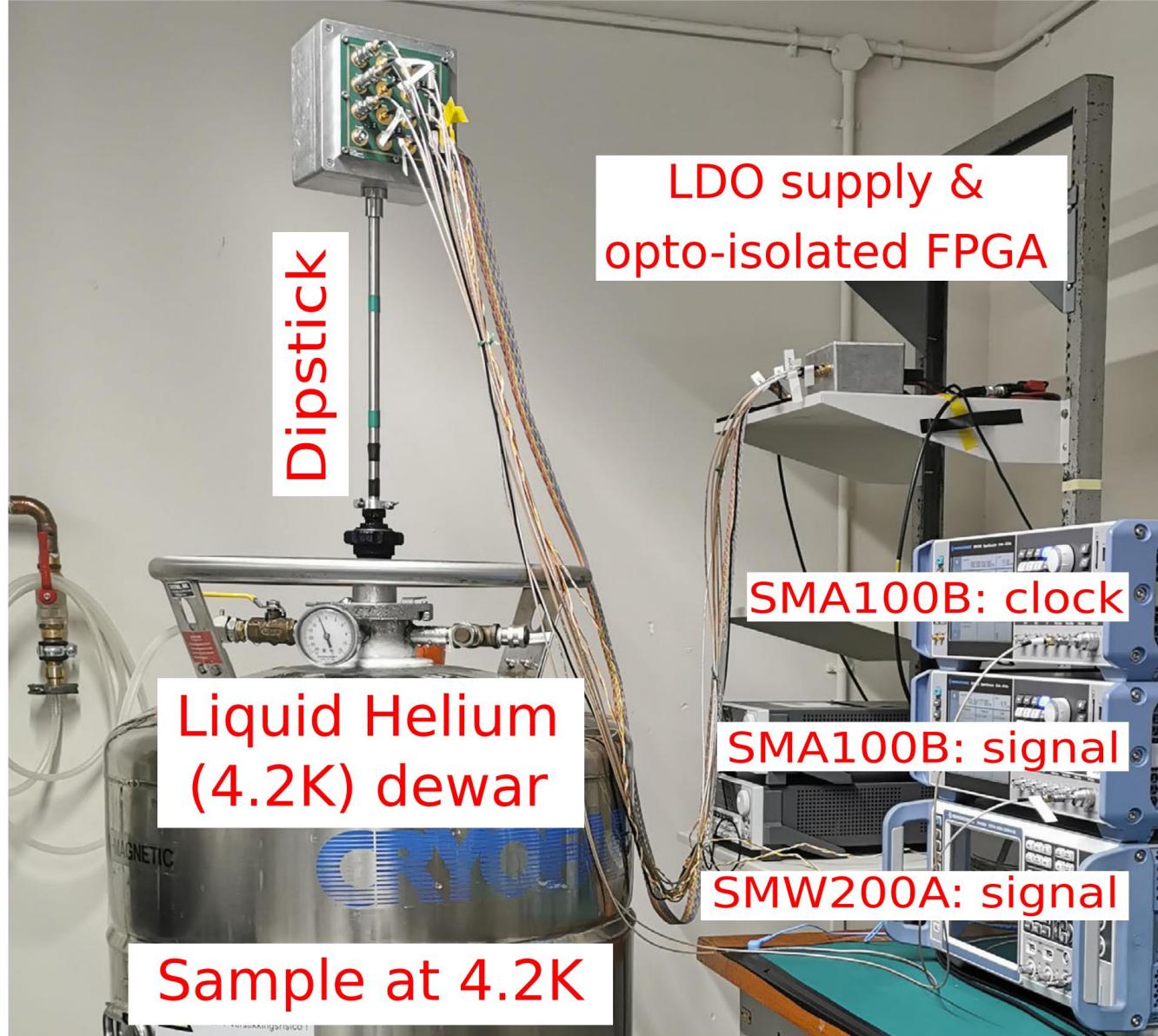
Dilution Fridge Measurement System

Mixing Chamber { Measurement System }

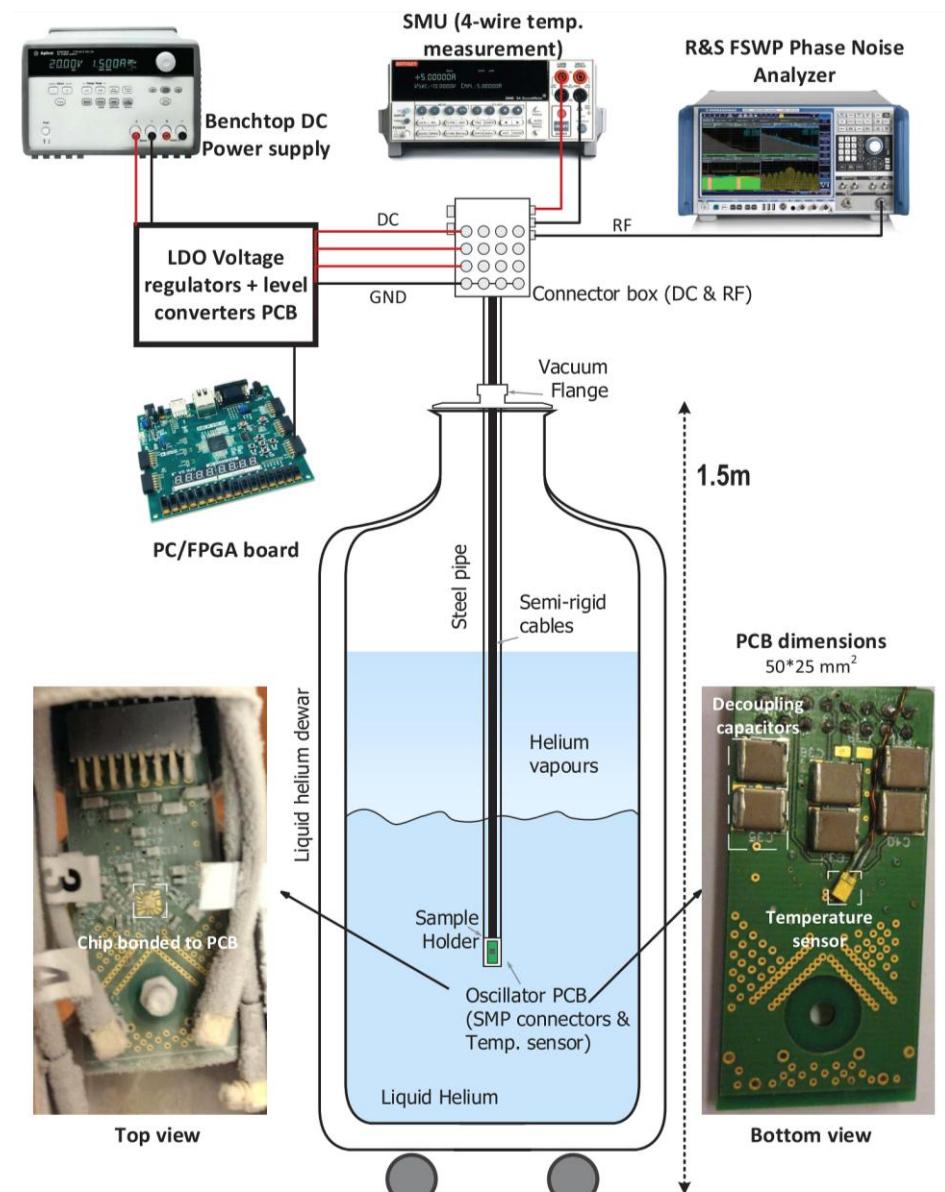


1. [Krinner et al., EPJ Quantum Technol. 6, 2 \(2019\)](#)
2. [Hollister, SQMS \(2023\)](#)

External FPGA & Cryo-CMOS Control/Readout



1. Patra et al., *IEEE J. Solid-State Circuits* (2018)
2. Kiene et al., *IEEE J. Solid-State Circuits* (2023)



*LNA: Low Noise Amplifier

Cabling Options (Depending on Signal Traffic/ Bandwidth Requirements)



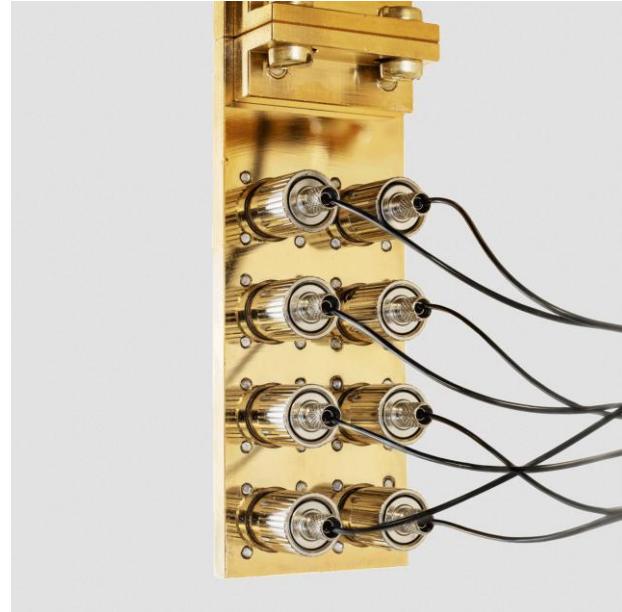
Standard Coaxial
Wiring



High-Density
Coaxial Wiring



High-Density
'Ribbon' Flex Wiring



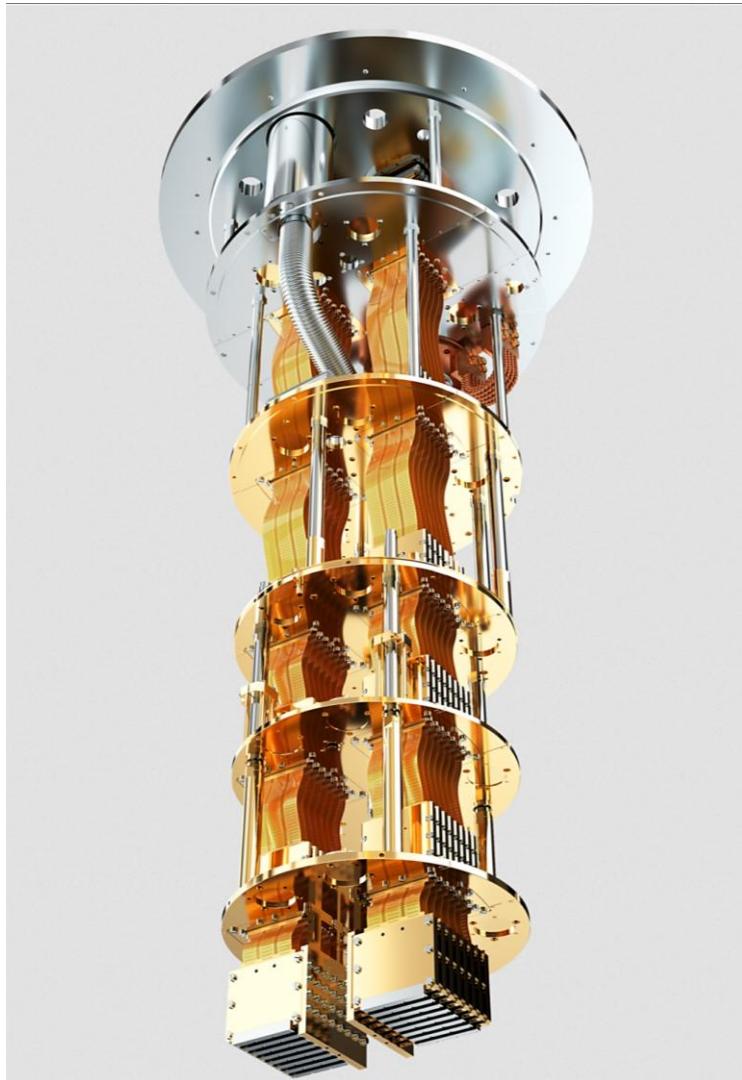
Cryogenic
Optical Fiber



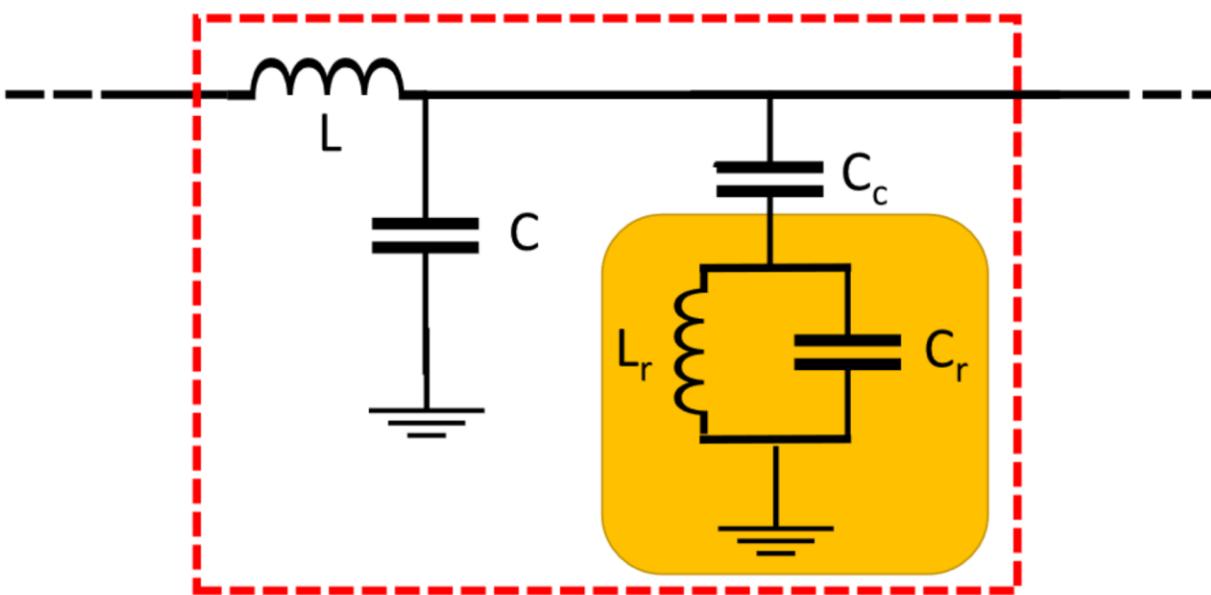
Increased Bandwidth Capability

1. Bluefors
2. Ardent Concepts

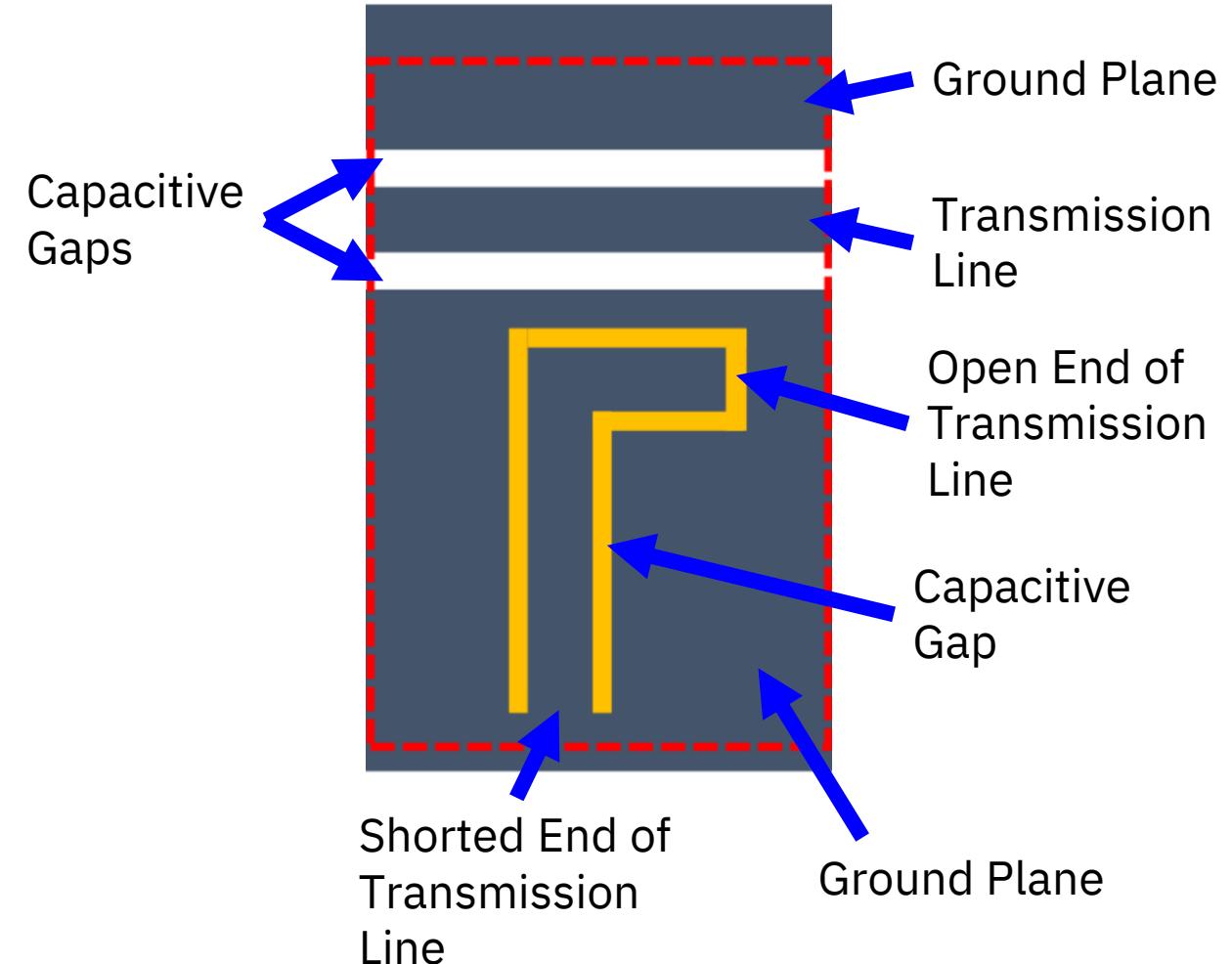
Closer Look at IBM & Bluefors High Bandwidth ‘Ribbon’ Flex Cables



Coupled Coplanar Waveguide Resonator (Elbow)

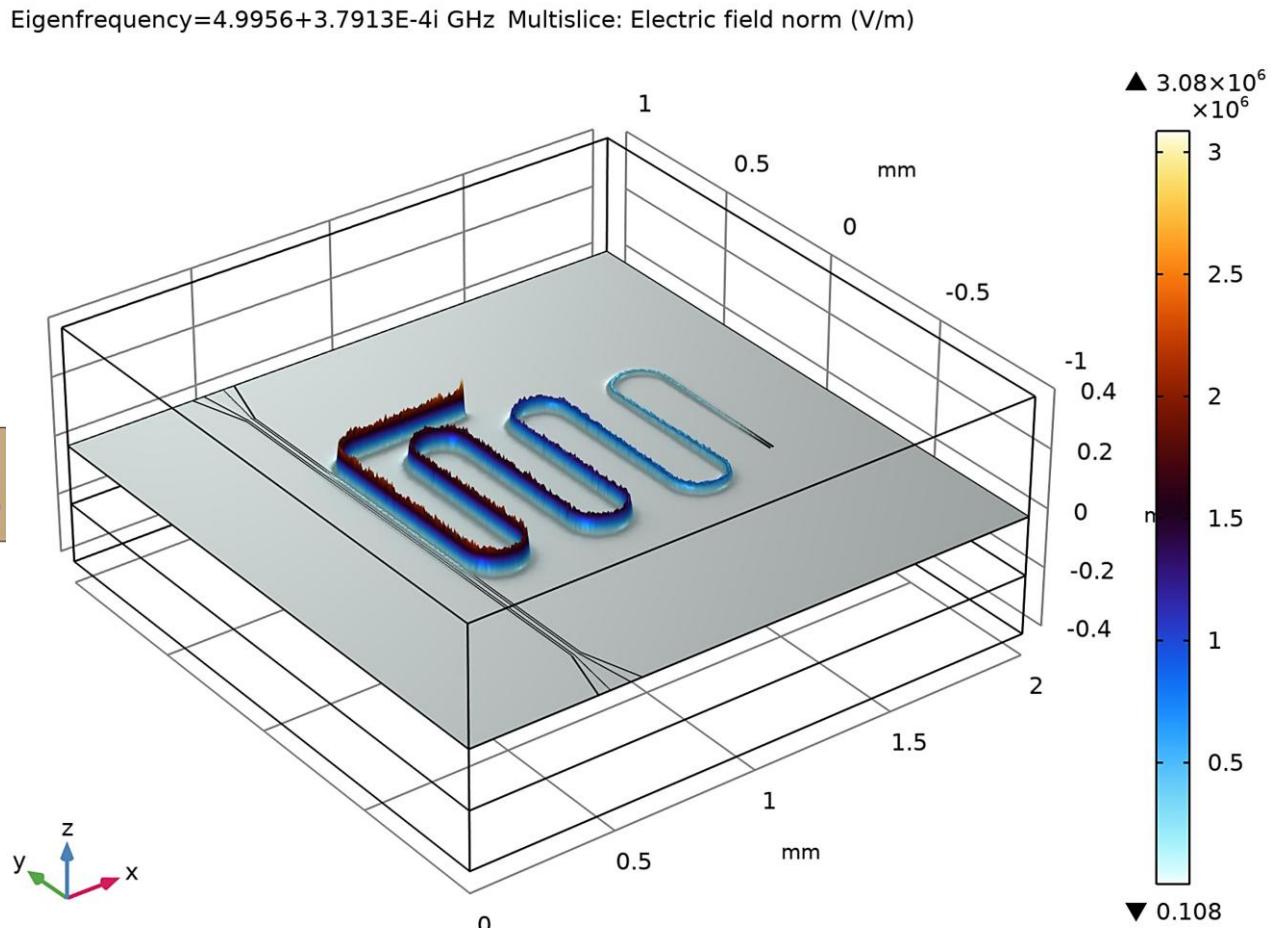
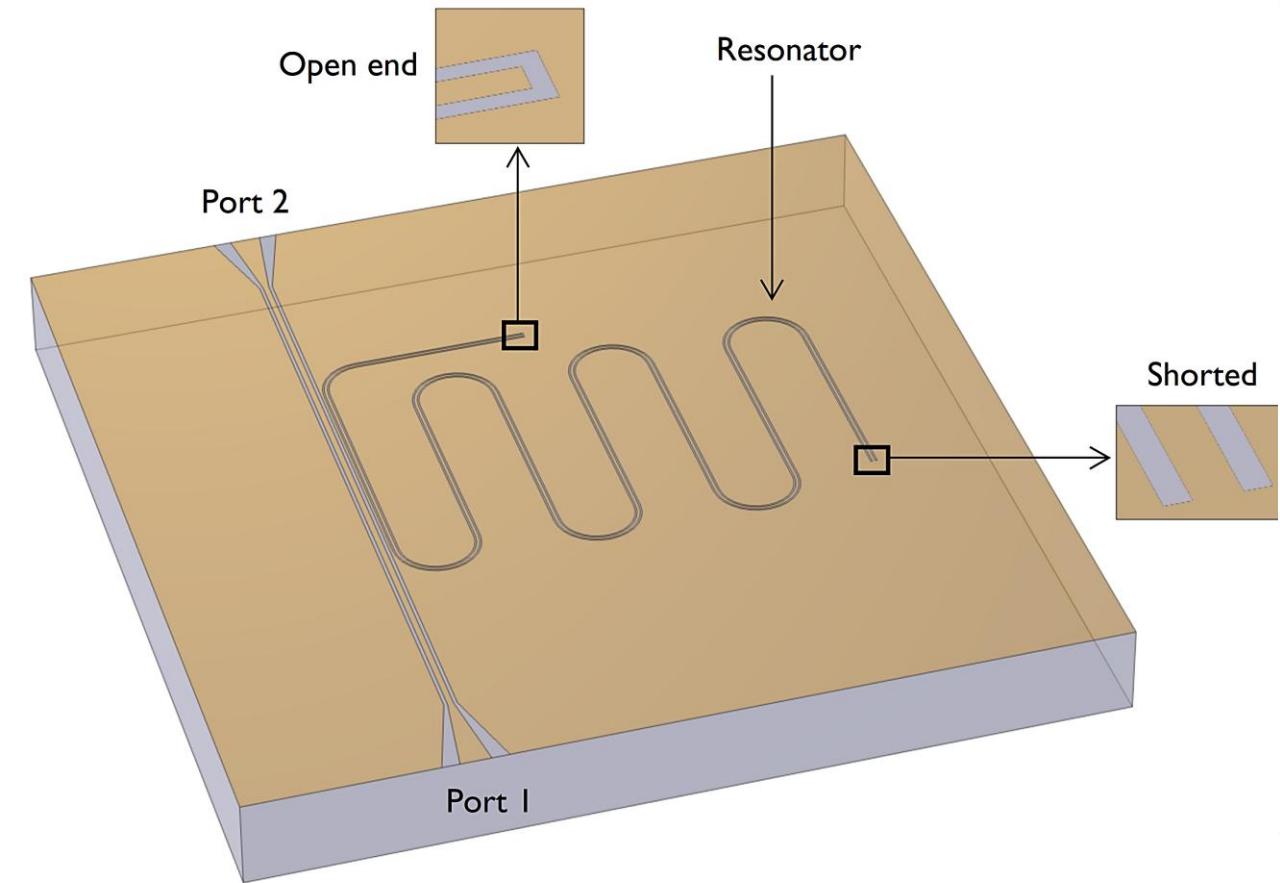


Lumped element equivalent circuit

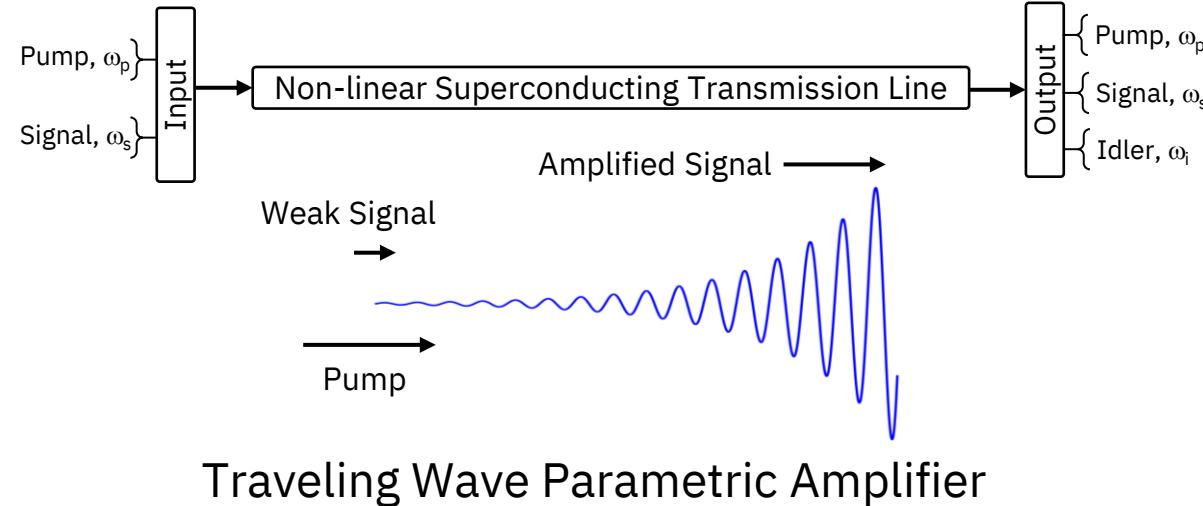


1. Adapted from [Sweetnam et al., Supercond. Sci. Technol. 35 095011 \(2022\)](#)

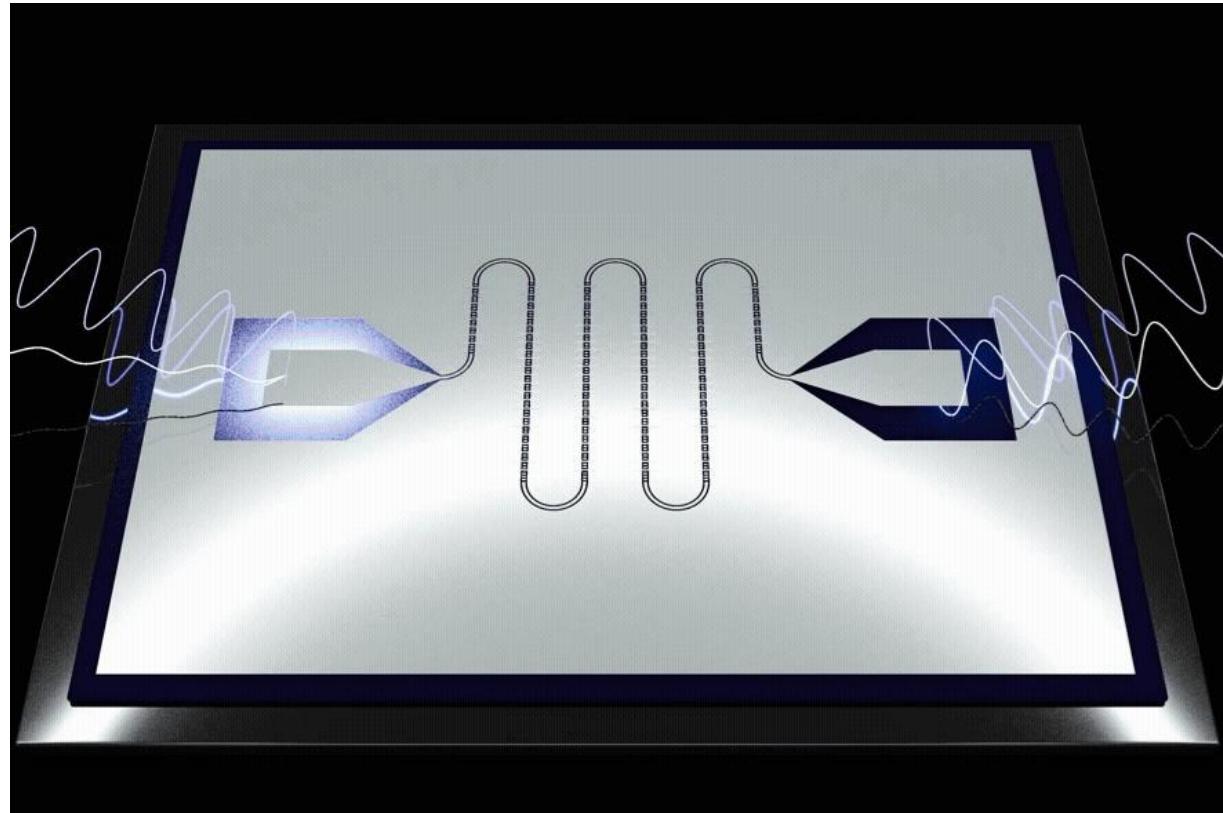
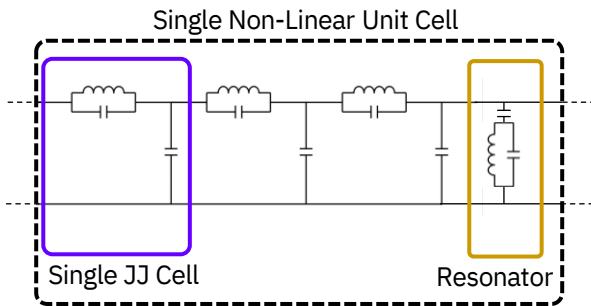
The Beauty of Abstractions in Superconducting Circuits



Josephson Traveling Wave Parametric Amplifiers (J-TWPAs)



Traveling Wave Parametric Amplifier

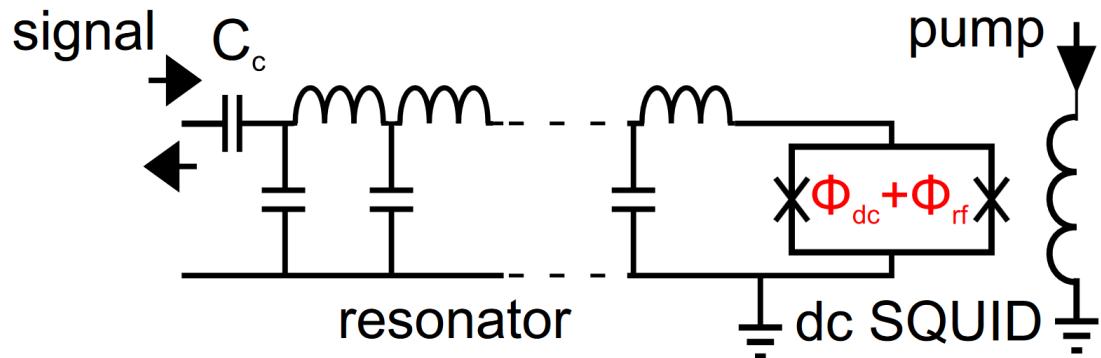
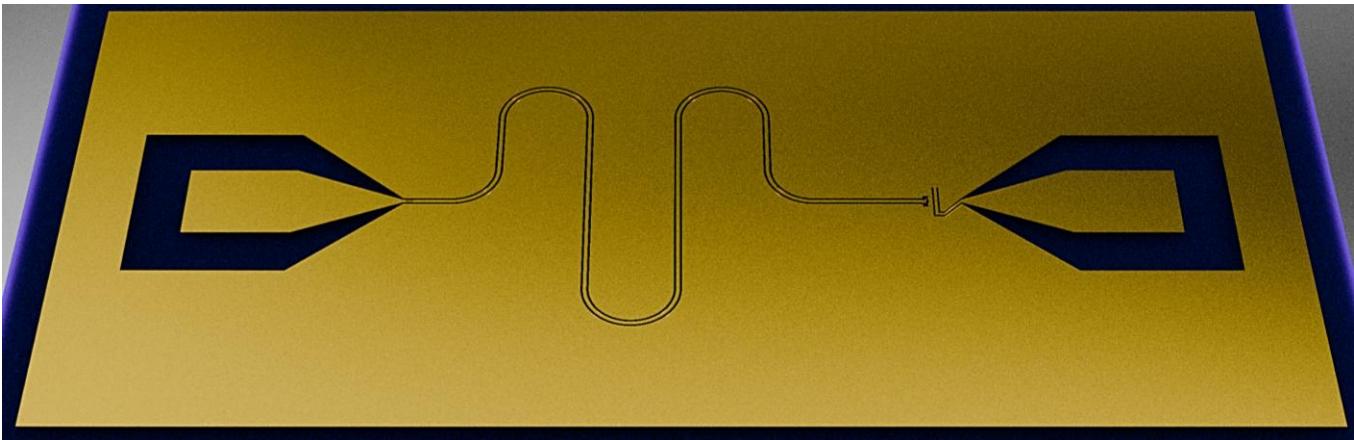
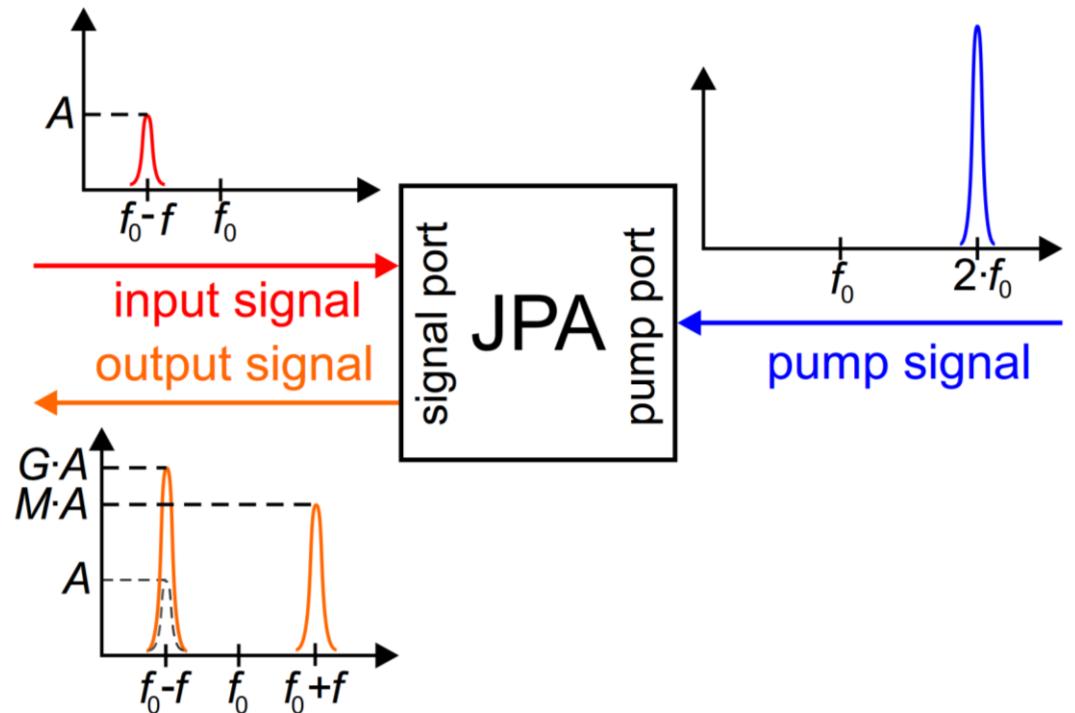


Blender Rendering of a J-TWPA
Performing 3-Wave Mixing

J-TWPA is transmissive mode device with high bandwidth.
It can perform 3 or 4 wave mixing (3WM or 4WM).

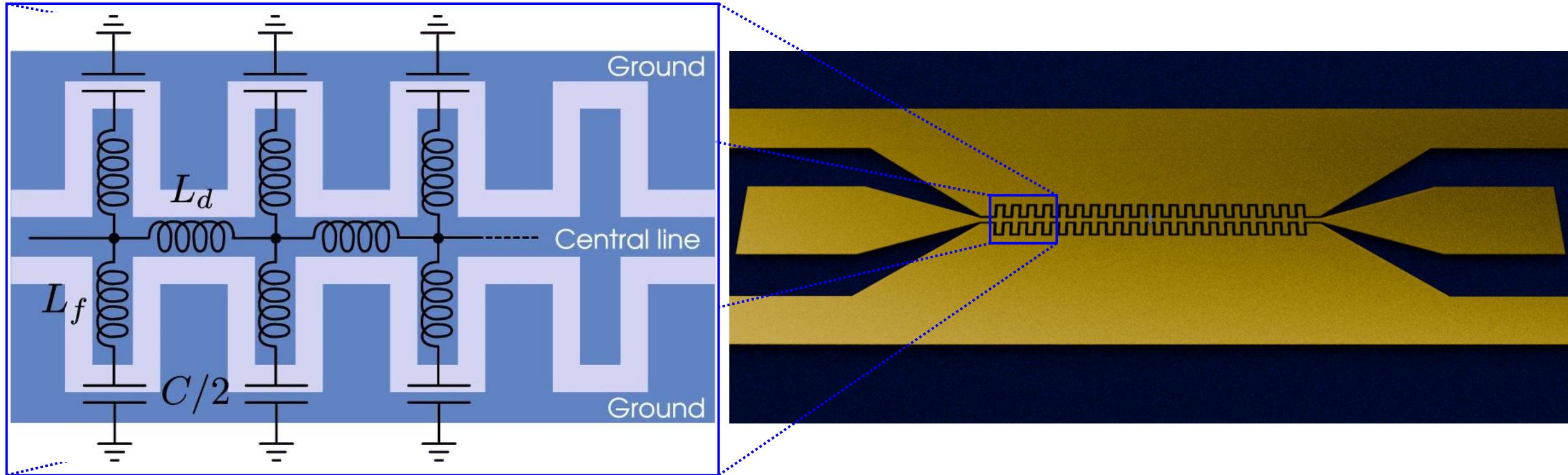
1. For more, check: [Tan et al., UCMMT 8068511 \(2017\)](#)

Josephson Parametric Amplifiers (JPAs)



JPA is reflective mode device with low to 'medium' bandwidth.
It can perform 3 or 4 wave mixing (3WM or 4WM).

Kinetic Inductance Traveling Wave Parametric Amplifiers (KI-TWPAs)



KI-TWPA is transmissive mode device with high bandwidth.
It can perform 3 or 4 wave mixing (3WM or 4WM).

1. Adapted from: [Giachero et al., J Low Temp Phys 209, 658–666 \(2022\)](#)

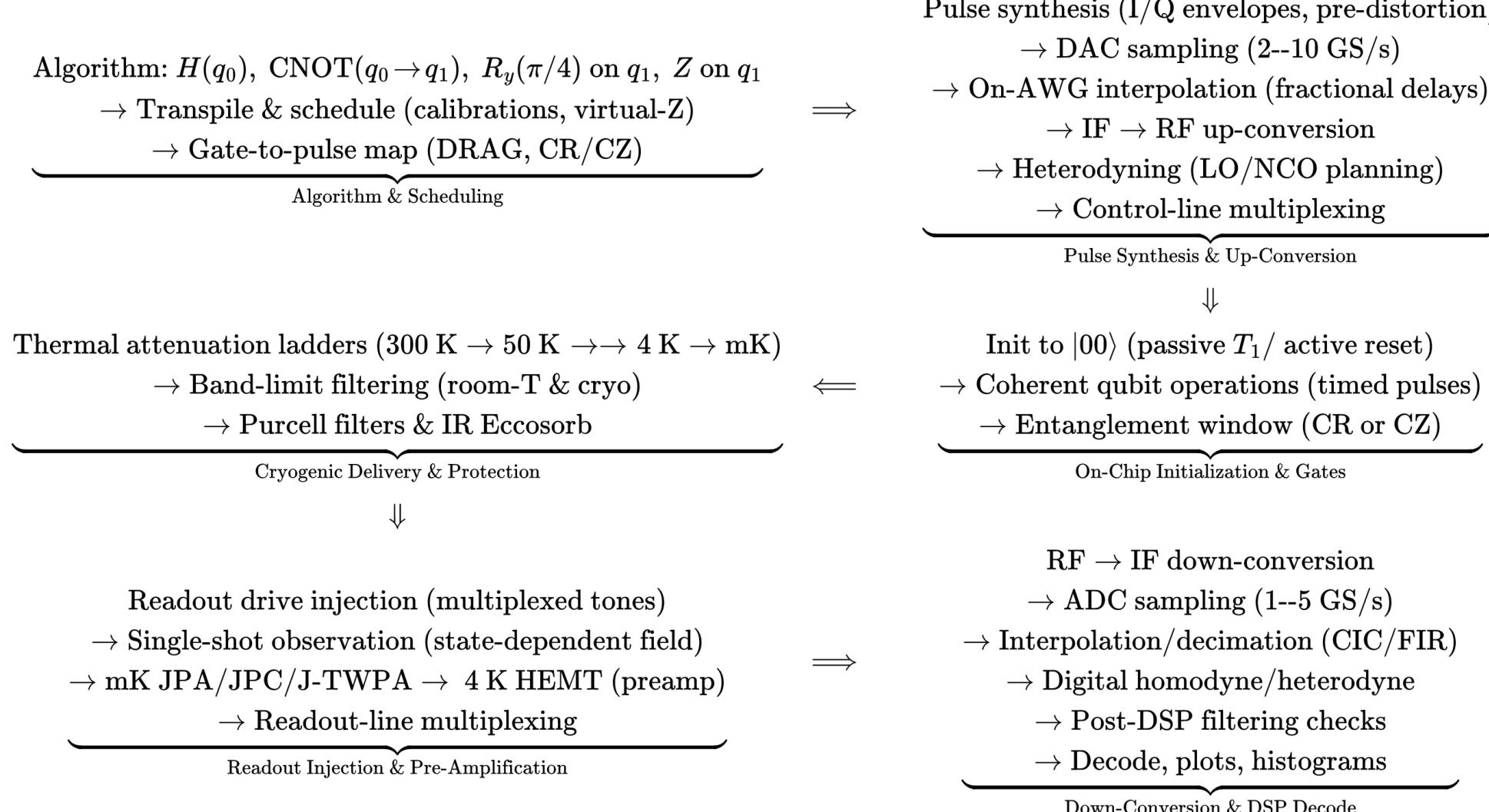
Deployment of Quantum Processors (Academic vs. Corporate)

- └ Small-scale/ Academic-lab chips (few traffic lanes)
 - ├ Fixed-frequency transmons on single dies
 - └ Cross-resonance & sideband gates, 2-to-10-qubit testbeds
 - ├ Fluxonium qubits
 - └ >100 μs coherence; microwave-only CZ studies
 - ├ NV-center diamond qubits
 - └ Two-qubit entanglement & sensor-LASER hybrids
 - ├ Semiconductor spin quantum dots
 - └ 2-to-4-qubit Si/SiGe or MOS devices (TU Delft, UNSW/ Dirac)
 - ├ Photonic linear-optics benches
 - └ Dual-rail photons, Hong-Ou-Mandel, teleportation demos
 - └ Superconducting flux qubits (annealing physics)
 - └ Non-stoquastic Hamiltonian & prime-factor test circuits

- └ Large-scale/ Data-center-oriented ($\approx 10^2\text{-}10^6$ physical qubits, many lanes)
 - ├ Superconducting transmon lattices
 - └ IBM "Heron-class" tunable-coupler tiles (modular roadmap)
 - ├ 133-qubit Heron r1/r2 chips (baseline fidelity node)
 - ├ Crossbill prototype: 3 Herons + on-package m-couplers
 - ├ 462-qubit Flamingo module: l-couplers for ~1 m links
 - └ 1,386-qubit Flamingo tri-module demonstration (2026)
 - └ Starling fault-tolerant block (≈ 200 logical qubits, 10^8 gates, 2029)
 - └ Blue Jay quantum-centric supercomputer ($\approx 2,000$ logical qubits, 10^9 gates, 2033)
 - └ IBM 127-qubit Eagle → 1,386-qubit Kookaburra (legacy multi-chip)
 - ├ Rigetti modular tiles
 - └ 84-qubit Ankaa-3 (99.5% CZ fidelity, 2024)
 - └ 36-qubit chiplet prototype (halved error, Jul 2025)
 - └ 336-qubit Lyra target (narrow quantum advantage, 2026)
 - ├ Google Quantum AI
 - └ 53-qubit Sycamore (2019)
 - └ 105-qubit Willow logical-scaling chip (2024)
 - └ Roadmap toward ~ 1 M physical qubits & fault-tolerance (~2033)
 - └ Fujitsu-RIKEN superconducting platform (hybrid AI-HPC)
 - └ 256-qubit RQC-Fujitsu machine, external access via hybrid platform (Q1 FY2025)
 - └ 1,000-qubit facility under construction (availability target: FY2026)
 - └ $\geq 10,000$ -qubit development program, system completion targeted around 2030, aligned with FugakuNEXT AI-HPC
 - ├ Superconducting bosonic/cat-code processors (oscillator-encoded)
 - └ AWS Center for Quantum Computing (Caltech)
 - └ Ocelot cat-qubit chip (Feb 2025)
 - └ Blueprint: concatenated cat codes + repetition/ surface code stack (2020-2022)
 - └ Neutral-atom arrays
 - └ QuEra Aquila 256-qubit Rydberg computer (2022 cloud)
 - └ Atom Computing "Phoenix" 1,225-qubit ytterbium array (2023)
 - └ Pasqal roadmap to 10,000-qubit array (2026)
 - └ Photonic cluster-state processors
 - └ PsiQuantum Omega silicon-photonics chiplets, mass-fab (2025)
 - └ Xanadu Borealis 216-mode Gaussian-boson-sampler (2022)
 - └ Trapped-ion modular racks
 - └ IonQ Forte (35 algorithmic qubits) + cryptographically relevant quantum computer roadmap (2028)
 - └ Silicon spin-qubit tiles
 - └ Intel "Tunnel Falls" 12-qubit chip, 300 mm CMOS fab (2023)
 - └ Horse Ridge II 4 K cryo-CMOS controller (wiring cutback)
 - └ Pando Tree mK cryo-CMOS fan-out (10-20 mK stage)
 - └ Flux-qubit quantum annealers
 - └ D-Wave Advantage2 ($\approx 7,000$ flux qubits, Zephyr topology, 2025 general availability)

Quantum Computing Signal Chain Example (w/ RT Control)

A × B Single-Shot Signal Chain – 2 Qubits, Room-Temperature Controllers



Quantum Computing Signal Chain Example (w/ Cryo-ASIC Control)

A × B Single-Shot Signal Chain – 2 Qubits, Cryogenic ASIC Controllers

Algorithm: $H(q_0)$, CNOT($q_0 \rightarrow q_1$), $R_y(\pi/4)$ on q_1 , Z on q_1

- Transpile & schedule (virtual-Z placement)
- Cryo-aware compilation (latency/power caps)
- Digital command packets to cryo-ASIC

⇒

On-ASIC DAC sampling (1–4 GS/s)

→ On-ASIC interpolation & pre-distortion

→ On-ASIC NCO/IQ up-conversion

→ Local heterodyning (shared cryo-LO/ digital SSB)

→ Near-chip fanout/multiplex

Cryo Up-Conversion & Fanout

↓

Initialize to $|00\rangle$ (passive T_1 or active reset)

→ Gate window ($H \approx R_z(\pi) R_y(\pi/2)$ with VZ)

→ Entanglement (CR or CZ)

On-Chip Execution

- Minimal thermal attenuation (short mK run)
→ Cryo filtering: band-limit, Purcell, IR Eccosorb

Delivery & Protection

⇐

- Readout pulse generated on ASIC
→ State-dependent imprint on resonator field
→ mK JPA/JPC/J-TWPA → 4 K HEMT

Readout Generation & Preamp

⇒

On-ASIC down-conversion

→ On-ASIC ADC & decimation

→ On-ASIC digital homodyne/heterodyne

→ Room-T validation & formatting

→ Final decode, storage, plots

Cryo Down-Conv, ADC, DSP, Host Decode

Quantum Computing Signal Chain Example + RAM Placement

A × B Single-Shot Signal Chain – 2 Qubits, Cryogenic ASIC Controllers (with Cryogenic RAM placement)

Algorithm: $H(q_0)$, CNOT($q_0 \rightarrow q_1$), $R_y(\pi/4)$ on q_1 , Z on q_1

- Transpile & schedule (virtual-Z placement)
- Cryo-aware compilation (latency/power caps)
- Digital command packets to cryo-ASIC

⇒

Algorithm→Cryo Packetization

On-ASIC DAC sampling (1–4 GS/s)

→ On-ASIC interpolation & pre-distortion

→ On-ASIC NCO/IQ up-conversion

→ Local heterodyning (shared cryo-LO/ digital SSB)

→ Near-chip fanout/multiplex

→ High-speed cryo-SRAM @ 4 K (on-ASIC): waveform/LUT buffers, sequencer microcode

→ Cryo eDRAM/ 2T-DRAM @ 4 K: extended pulse trains, cal tables

Cryo Up-Conversion & Fanout

↓

Initialize to $|00\rangle$ (passive T_1 or active reset)

→ Gate window ($H \approx R_z(\pi) R_y(\pi/2)$ with VZ)

→ Entanglement (CR or CZ)

→ mK: logic only; bulk RAM avoided due to heat budget

→ Any needed state for fast reset is fetched from 4 K cryo-SRAM

On-Chip Execution

↓

Readout pulse generated on ASIC

- State-dependent imprint on resonator field
- mK JPA/JPC/J-TWPA → 4 K HEMT

⇒

Readout Generation & Preamp

On-ASIC down-conversion

→ On-ASIC ADC & decimation

→ On-ASIC digital homodyne/heterodyne

→ High-speed cryo-SRAM @ 4 K: ADC capture buffers, accumulators

→ Cryo eDRAM/ 2T-DRAM @ 4 K: ring buffers, batch queues

→ Cold-DRAM @ 77 K: large logs/datasets (spillover)

→ Room-T validation & formatting

→ Final decode, storage, plots

Cryo Down-Conv, ADC, DSP, Host Decode

Bonus: Do I Need Cryogenic Equipment for My Quantum Photonic Chip (If I Have One)?

- ─ A) Are you talking about a QUANTUM PHOTONIC QUBIT CHIP?
 - ─ A1) Encoding & detection path: DISCRETE-VARIABLE (single photons)?
 - ─ A1.i) Are superconducting detectors (SNSPD/TES) ON-CHIP or CO-PACKAGED?
 - ─ YES → Plan CRYOGENICS ($\approx 0.1\text{-}4$ K). Also avoid thermo-optic tuning; use Pockels/magneto-optic/phase-change.
 - ─ NO → Go to A1.ii.
 - ─ A1.ii) Are you using near-deterministic QD single-photon SOURCES on-chip/co-packaged?
 - ─ YES → Plan CRYOGENICS ($\approx 4\text{-}10$ K). Processor often rides in same cryostat.
 - ─ NO → Go to A1.iii.
 - ─ A1.iii) Are DETECTORS external and warm-compatible (Si/GeSi SPADs; InGaAs SPADs with TEC)?
 - ─ YES → Processor CAN stay ROOM TEMPERATURE (stabilize with small TEC if needed).
 - ─ NO → If external detectors are SNSPDs, only the detector rack is cold; processor can still be ROOM TEMPERATURE.
 - ─ A2) Encoding & detection path: CONTINUOUS-VARIABLE (squeezed states + homodyne)?
 - ─ Sources and balanced-homodyne detectors are ROOM TEMPERATURE by default.
 - ─ Only plan CRYOGENICS if co-integrating cold peripherals (e.g., rare-earth memories) or if your system choice is to co-locate everything to cut fiber coupling loss into a cryostat.
- ─ B) Are you talking about a NON-QUBIT QUANTUM INTEGRATED CIRCUIT?
 - ─ B1) Quantum communications TRANSMITTERS, linear-optics processors, quantum sensors (no on-chip cryo parts)?
 - ─ ROOM TEMPERATURE (standard hermetic/TEC packages).
 - ─ B2) Photonic READOUT for superconducting electronics (e.g., 4 K data links) or on-chip SNSPD arrays for sensing?
 - ─ Plan CRYOGENICS; use cryo-compatible EO modulators (LN/BTO), not thermo-optic heaters.
 - ─ B3) Memories/interfaces:
 - ─ Rare-earth-doped solid-state memories → CRYOGENICS (few kelvin).
 - ─ Warm-vapor (alkali) memories → ROOM TEMPERATURE, with bandwidth/noise trade-offs.