*Digital System Design Lab*

# CEL-442



## Lab Journal: 5

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*Class: BCE-6(A).*

### Enrollment no: 01-132182-024

Task\_1:

Module task1(a,b,c,d,e);

input a,b,c;

output d,e;

wire w1;

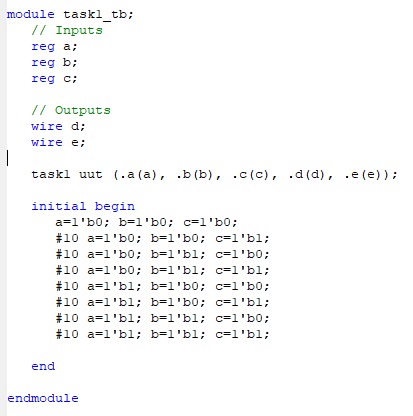
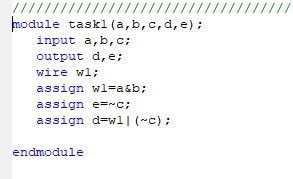
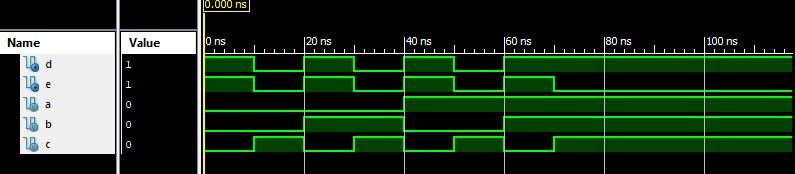
assign w1=a&b;

assign e=~c;

assign d=w1|(~c);

end module;

OUTPUT:



TASK\_2:

`timescale 1ns / 1ps

module HA(A,B,s,c);

input A,B;

output s;

output c;

assign {c,s}=A+B;

endmodule

module FA(A,B,cin,sum,cout);

input A,B;

input cin;

output sum;

output cout;

wire w1,w3;

wire w2;

HA n1(A,B,w2,w1);

HA n2(cin,w2,sum,w3);

assign cout=w1|w3;

endmodule

module RCA\_4(a,b,cin,sum,cout);

input[3:0] a,b;

input cin;

output[3:0] sum;

output cout;

wire c1,c2.c3;

FA fa0(a[0],b[0],cin,sum[0],c1);

FA fa1(a[1],b[1],c1,sum[1],c2);

FA fa2(a[2],b[2],c2,sum[2],c3);

FA fa3(a[3],b[3],c3,sum[3],cout);

endmodule;

//TEST\_BENCH

module RCATEST;

// Inputs

reg [3:0] a;

reg [3:0] b;

reg cin;

// Outputs

wire [3:0] sum;

wire cout;

// Instantiate the Unit Under Test (UUT)

RCA\_12bit uut (

.a(a),

.b(b),

.cin(cin),

.sum(sum),

.cout(cout)

);

initial begin

// Initialize Inputs

a = 4’b1101;

b = 4’0001;

cin = 0;

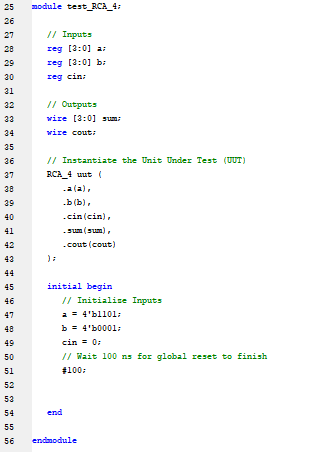
// Wait 100 ns for global reset to finish

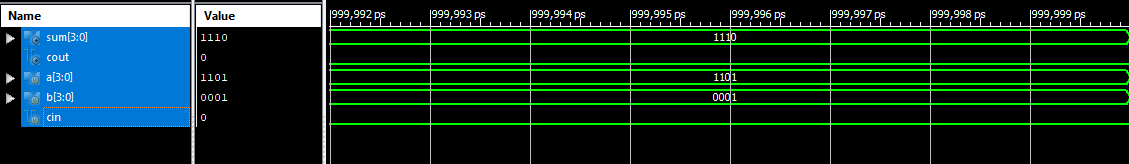
#100;

end

endmodule

**OUTPUT:**

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TASK\_3:

Module task3(a,b,sel,out);

input a,b,sel;

output out;

reg out;

always@(\*)

case(sel)

1’b0:out=b;

1’b1:out=a;

default: $display(“invalid”);

endcase

endmodule

|  |  |  |  |
| --- | --- | --- | --- |
| a | b | sel | out |
| 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 1 |
| 1 | 0 | 1 | 1 |
| 1 | 1 | 1 | 1 |

**OUTPUT:**

