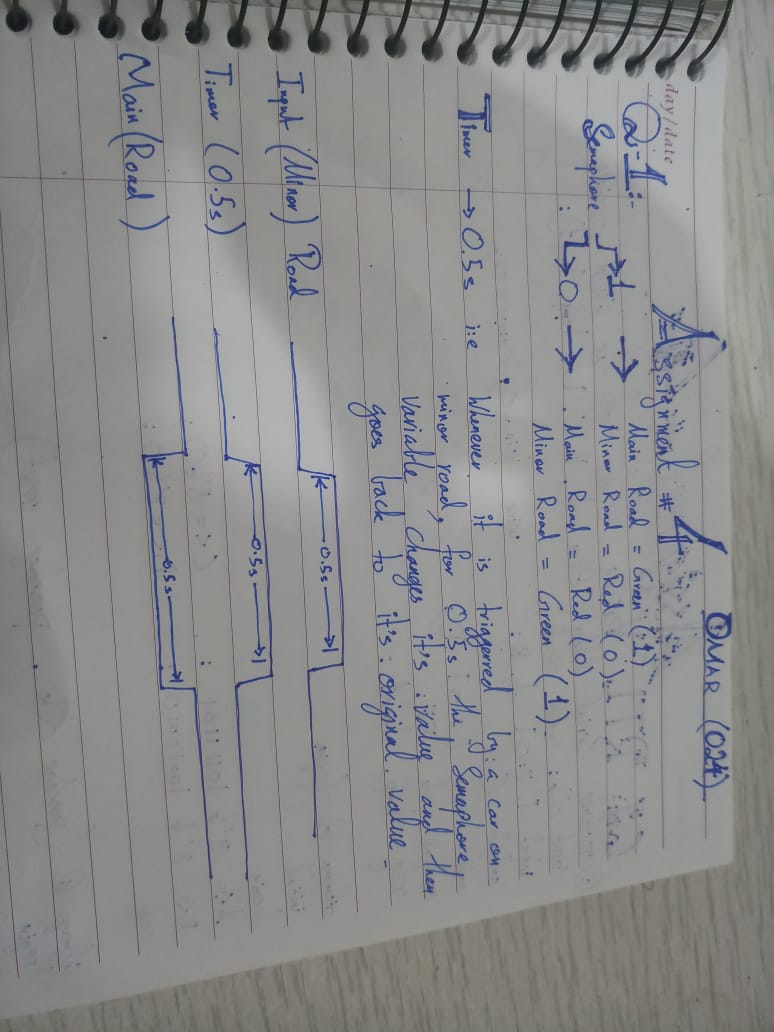
****

**Q2:**

**Code:**

`timescale 1ns / 1ps

module FA(

input a,

input b,

input cin,

output reg Sum,

output reg carry

);

always @ (\*)

begin

assign {carry,Sum} = a + b +cin;

end

endmodule

module Task\_1(

input clk,

input reset,

input [7:0]A,

input [7:0]B,

// output reg C,

output reg [7:0]D,

reg FF,

reg Sum,

reg Temp,

reg Temp1,

reg carry,

reg [7:0] A1,B1

);

wire [7:0]in1;

wire [7:0]in2;

assign in1=A;

assign in2=B;

initial

begin

A1 <= in1;

B1 <= in2;

//C <= 0;

D <= 8'b10000000;

end

always @(posedge clk,posedge reset)

begin

if (reset)

begin

A1 <= in1;

B1 <= in2;

//C <= 0;

//D <= 8'b10000000;

end

else

begin

Temp = A1[0];

A1= A1>>1;

Temp1 = B1[0];

B1 = B1>>1;

assign {carry,Sum} = Temp+Temp1+FF;

FF <= carry;

//C <= Sum;

D[7] <= Sum;

D <= D>>1;

end

end

endmodule

**Test Bench**

`timescale 1ns / 1ps

////////////////////////////////////////////////////////////////////////////////

// Company:

// Engineer:

//

// Create Date: 22:04:30 06/12/2021

// Design Name: Task\_1

// Module Name: E:/Semester 6/Assignments/DSD/Assignment\_4/Task\_1\_test.v

// Project Name: Assignment\_4

// Target Device:

// Tool versions:

// Description:

//

// Verilog Test Fixture created by ISE for module: Task\_1

//

// Dependencies:

//

// Revision:

// Revision 0.01 - File Created

// Additional Comments:

//

////////////////////////////////////////////////////////////////////////////////

module Task\_1\_test;

// Inputs

reg clk;

reg reset;

reg [7:0] A;

reg [7:0] B;

// Outputs

wire [7:0] D;

// Instantiate the Unit Under Test (UUT)

Task\_1 uut (

.clk(clk),

.reset(reset),

.A(A),

.B(B),

.D(D)

);

always

begin

#10;

clk = ~clk;

end

initial begin

// Initialize Inputs

clk = 0;

reset = 0;

A = 8'b11110000;

B = 8'b00001111;

#10;

clk = 1;

#10;

clk = 0;

#10;

clk = 1;

// Wait 100 ns for global reset to finish

#50;

end

endmodule

**OUTPUT:**

