

Cadence
Full-Custom IC Design

One chip Design

Minho Eom

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2. Digital Circuits & Analog Circuits

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3. Team Project

4. One Chip

PROGRAM & TOOL

PROGRAM & TOOL

Cadence Virtuoso Schematic Editor/Layout Editor

Cadence Virtuoso Spectre/ADE

Assura(LVS & DRC)

GPKD090

DIGITAL CIRCUITS

&

ANALOG CIRCUITS

DIGITAL CIRCUITS & ANALOG CIRCUITS

Digital Logic Gates

- NOT / SWITCH
- 2NAND / 3NAND / 4NAND
- 2NOR / 3NOR / 4NOR
- XOR

Digital Circuits

- 2x1 MUX / 4x1 MUX / 8x1 MUX / 16x1 MUX (Difference Logic & Switch)
- HALF_ADDER / FULL_ADDER / 4BIT_ADDER / 4BIT_SUBTRACTOR

Analog Circuits

- Common Source Amp / Differential Amp (Single-ended Output)

Team Project

- Asynchronous Counter / Synchronous Counter
- PIPO Shift Register
- Synchronous Counter + PIPO Shift Register

One Chip

DIGITAL LOGIC GATE

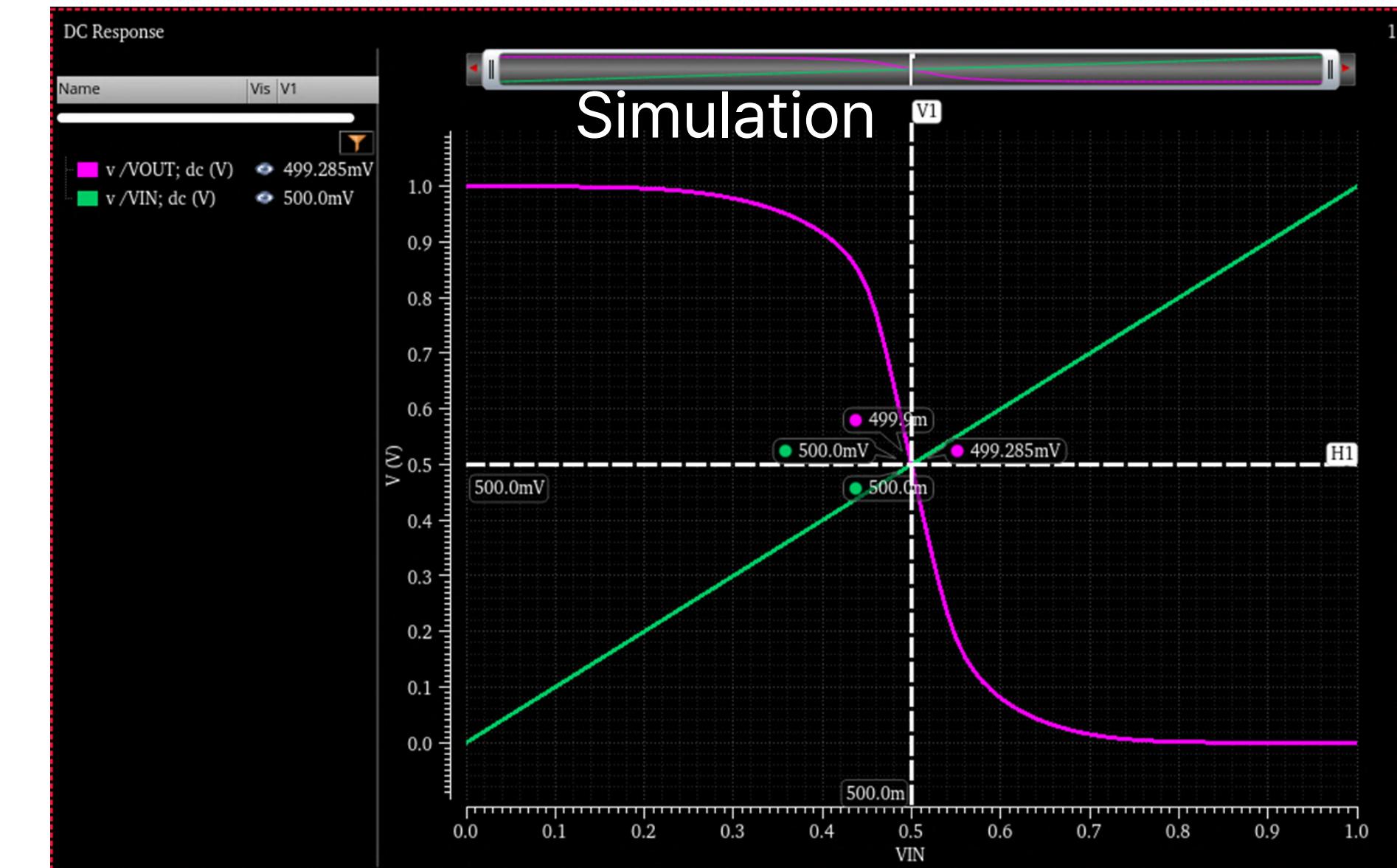
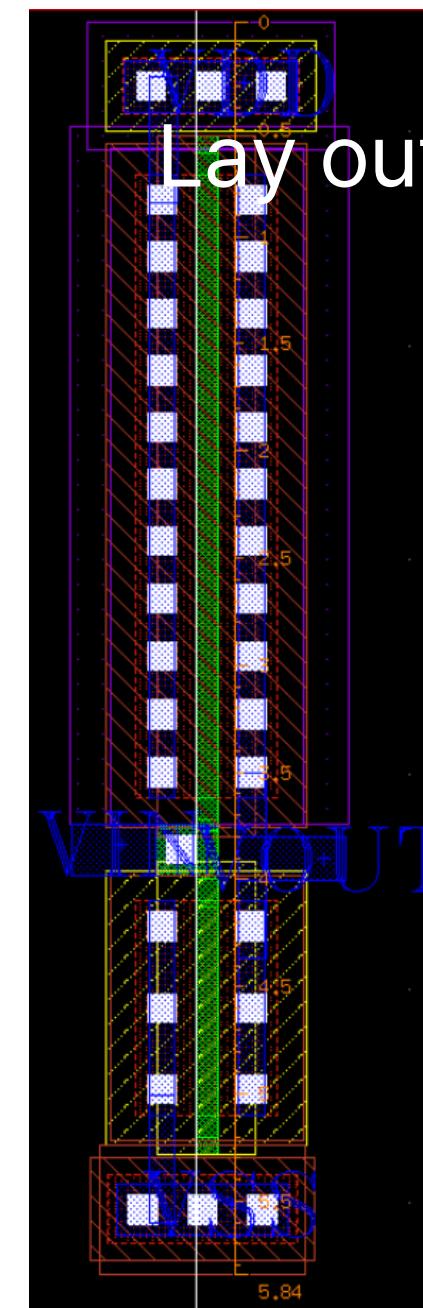
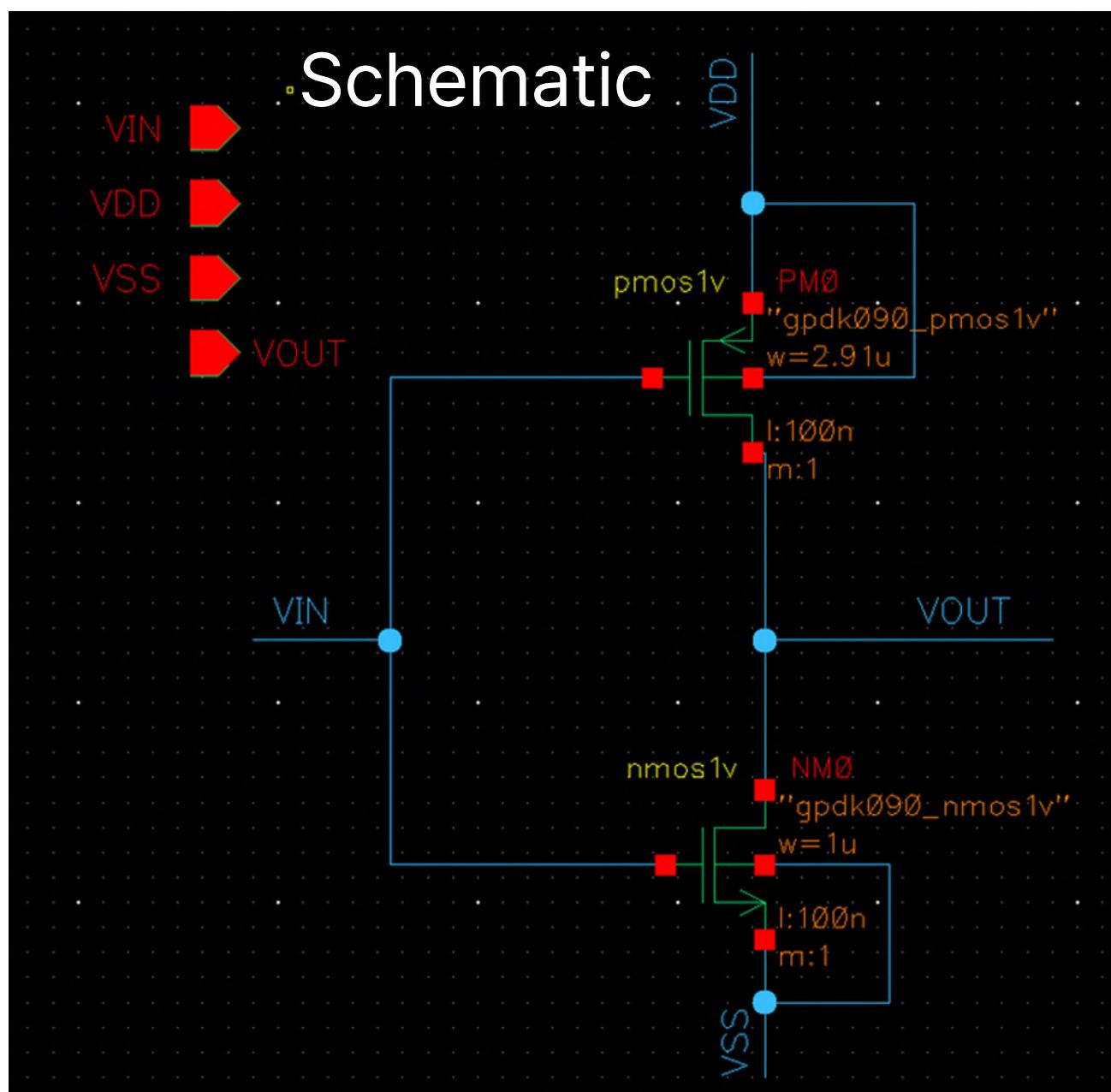
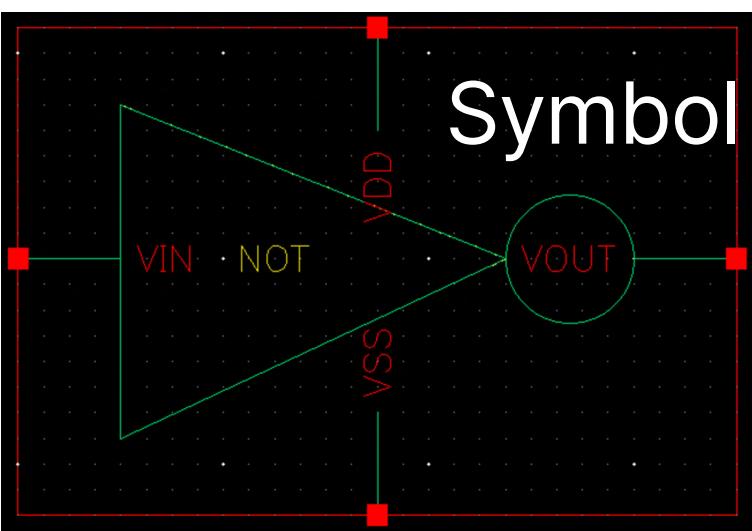
-NOT / SWITCH

-2NAND / 3NAND / 4NAND

-2NOR / 3NOR / 4NOR

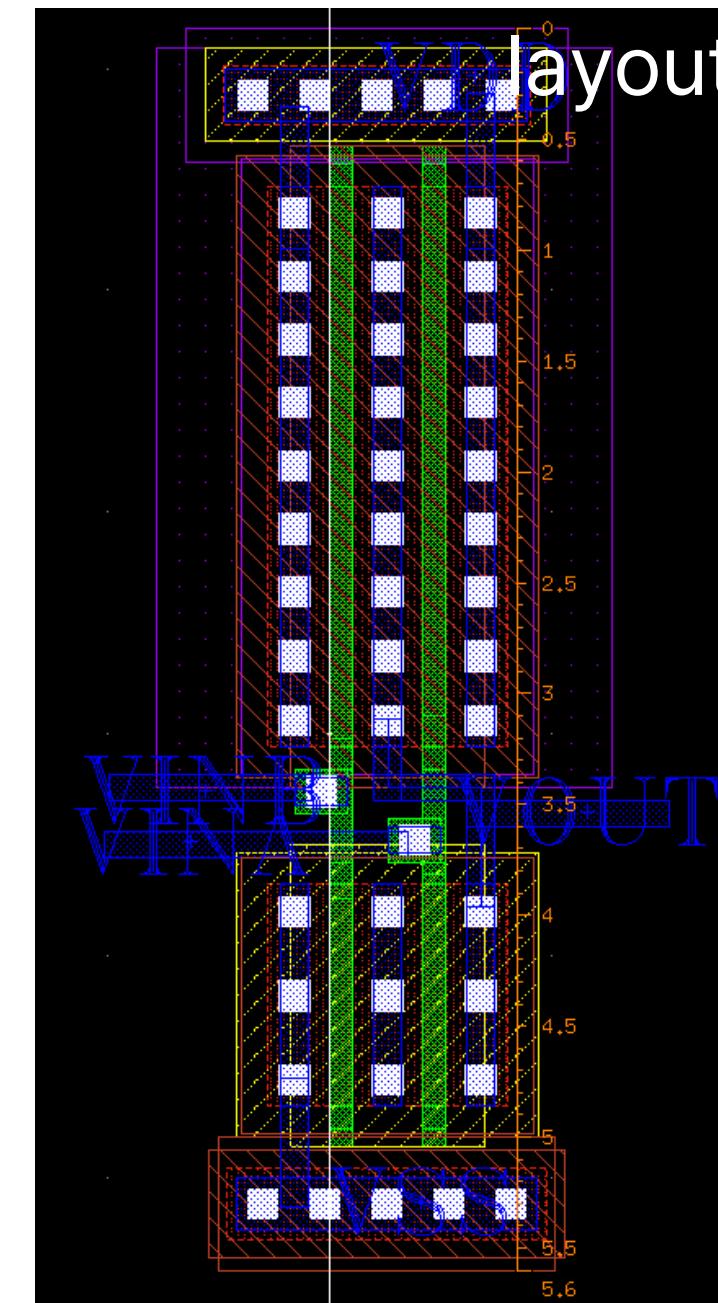
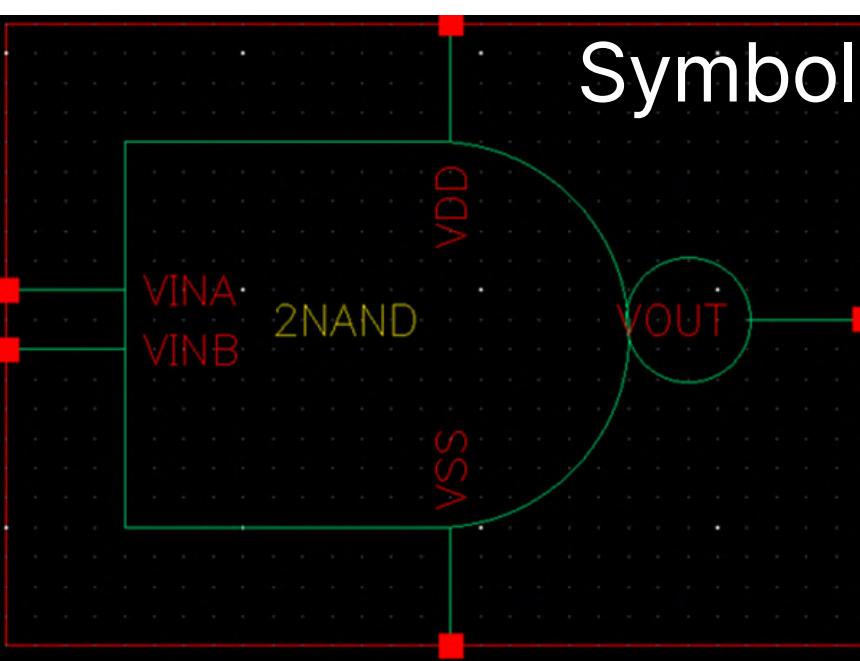
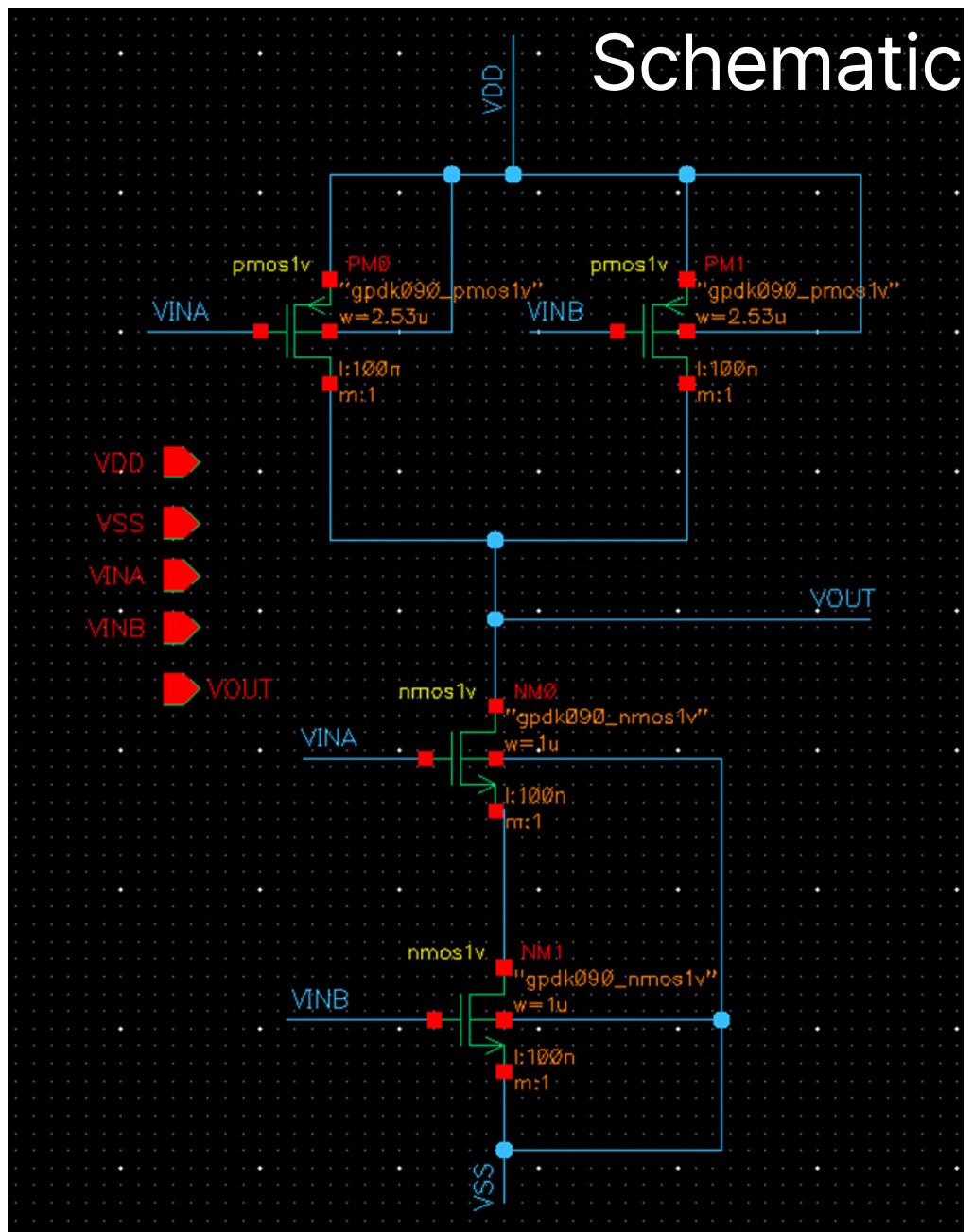
-XOR

NOT



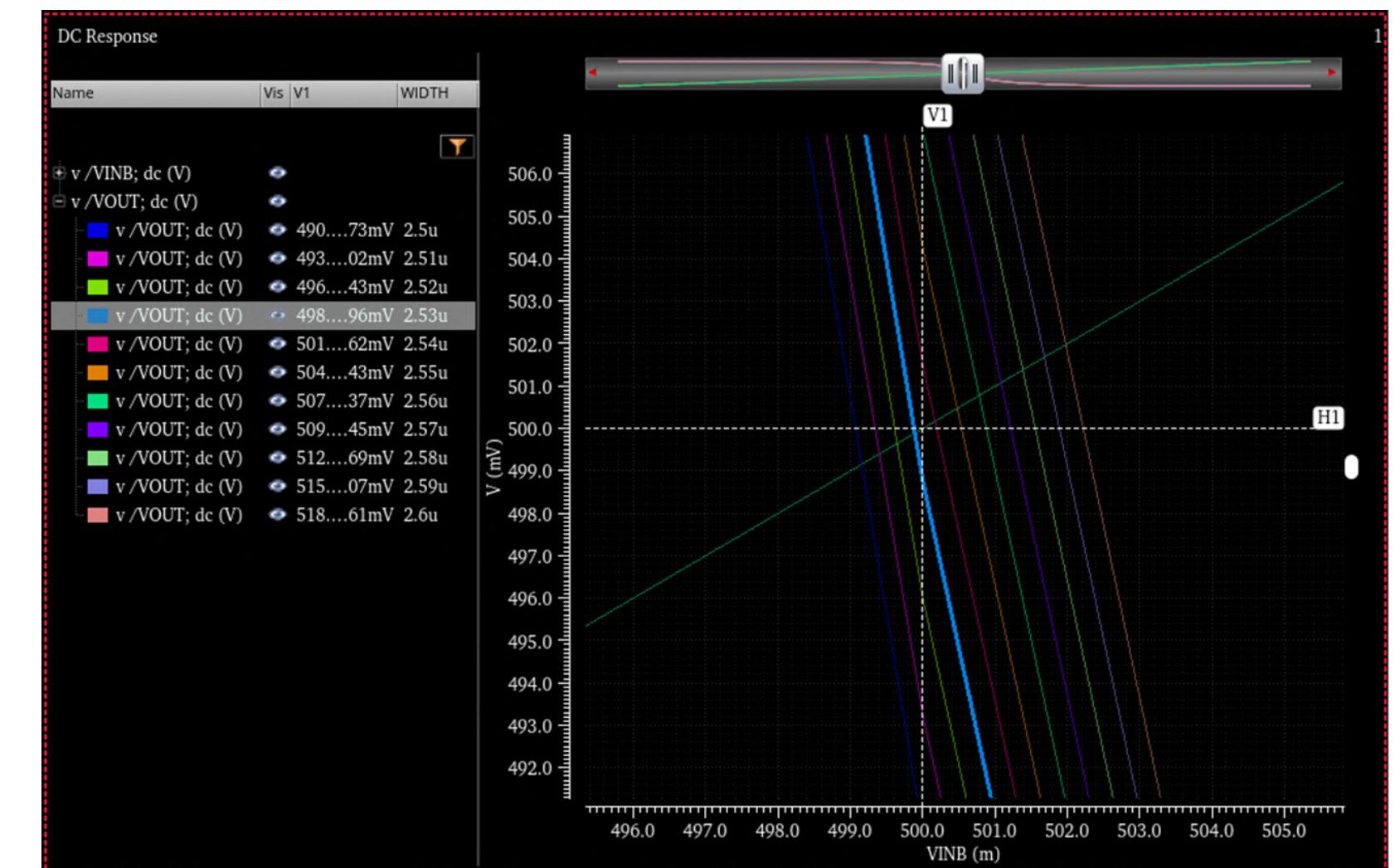
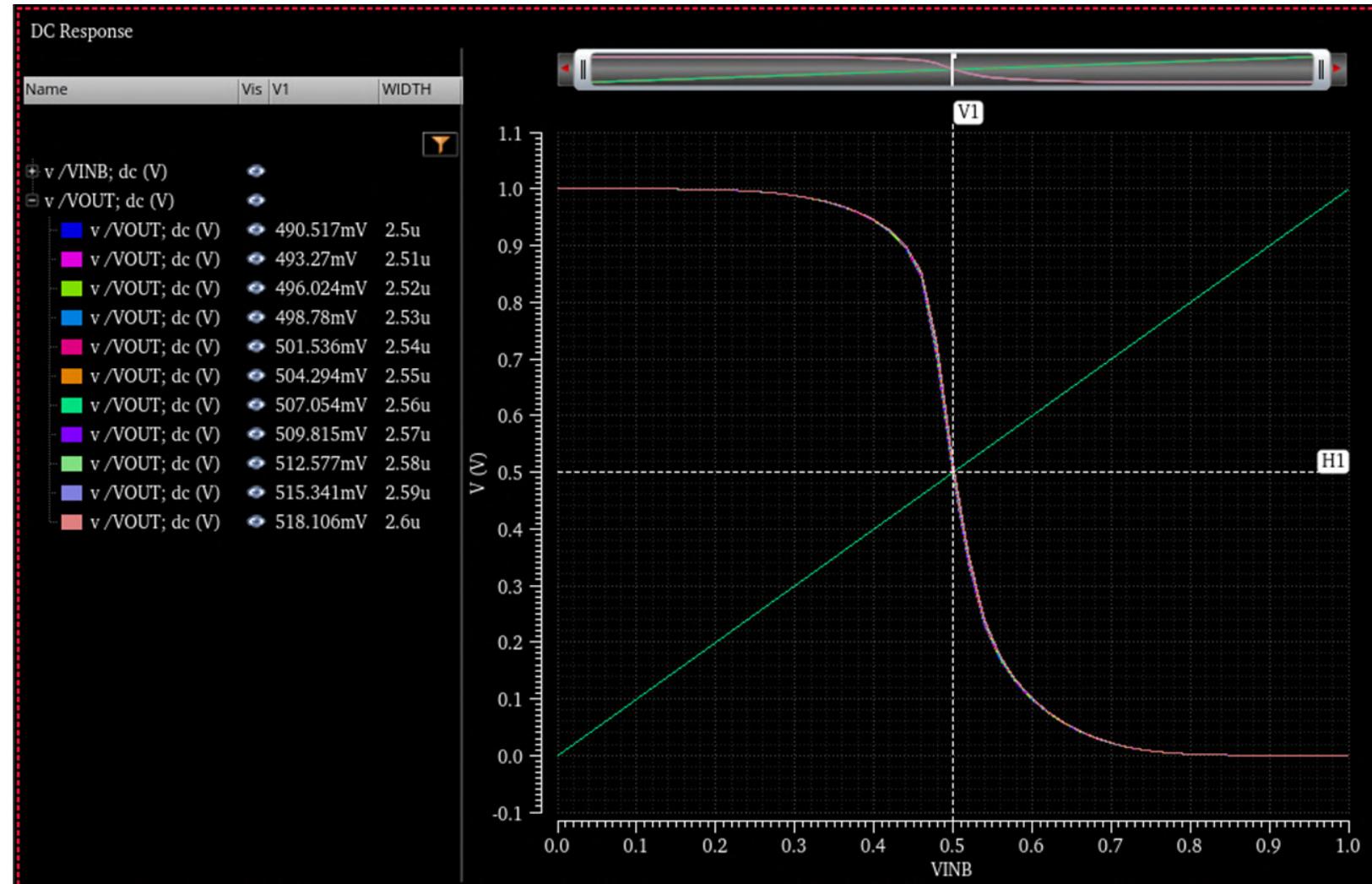
2NAND

length : 5.6u
width : 1.36u

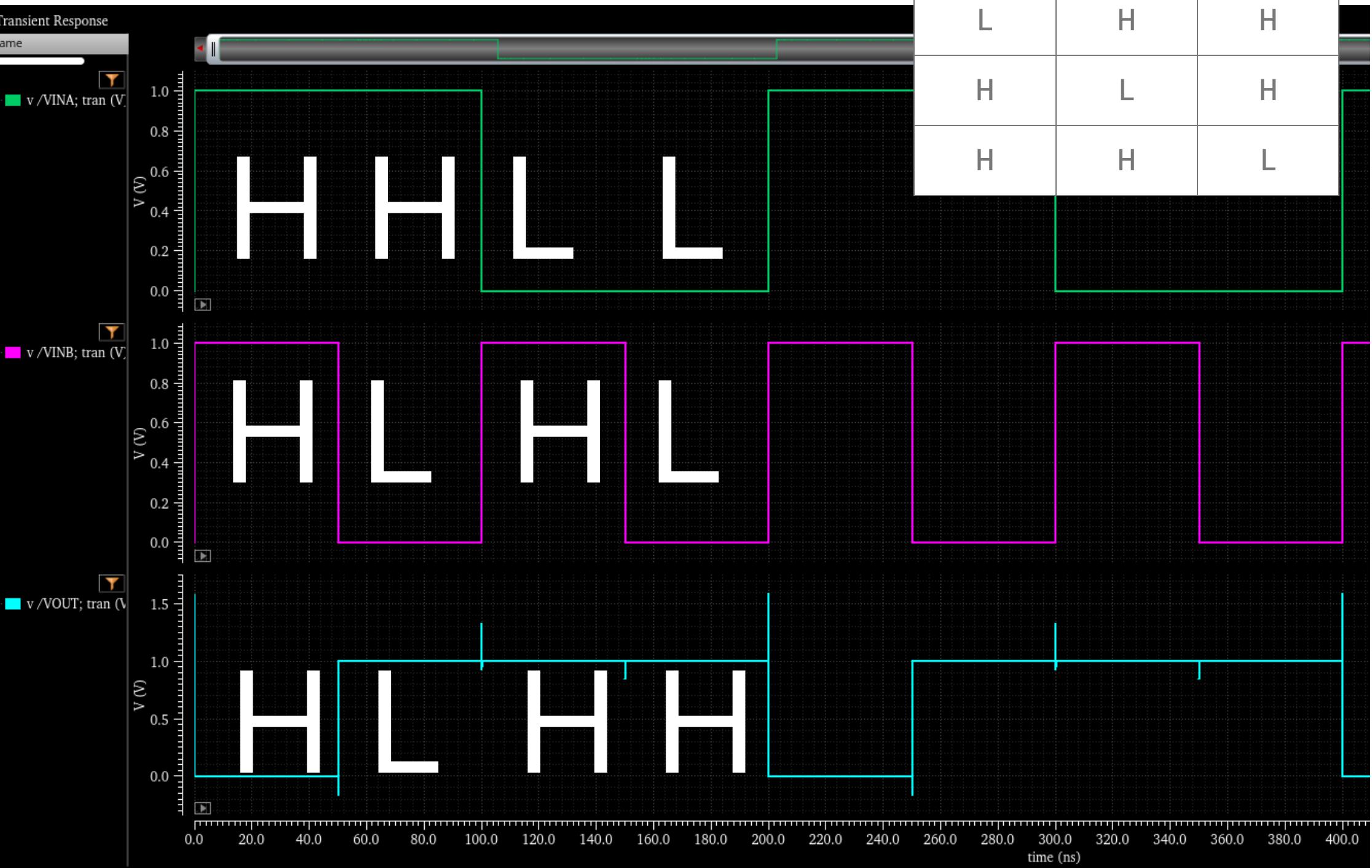
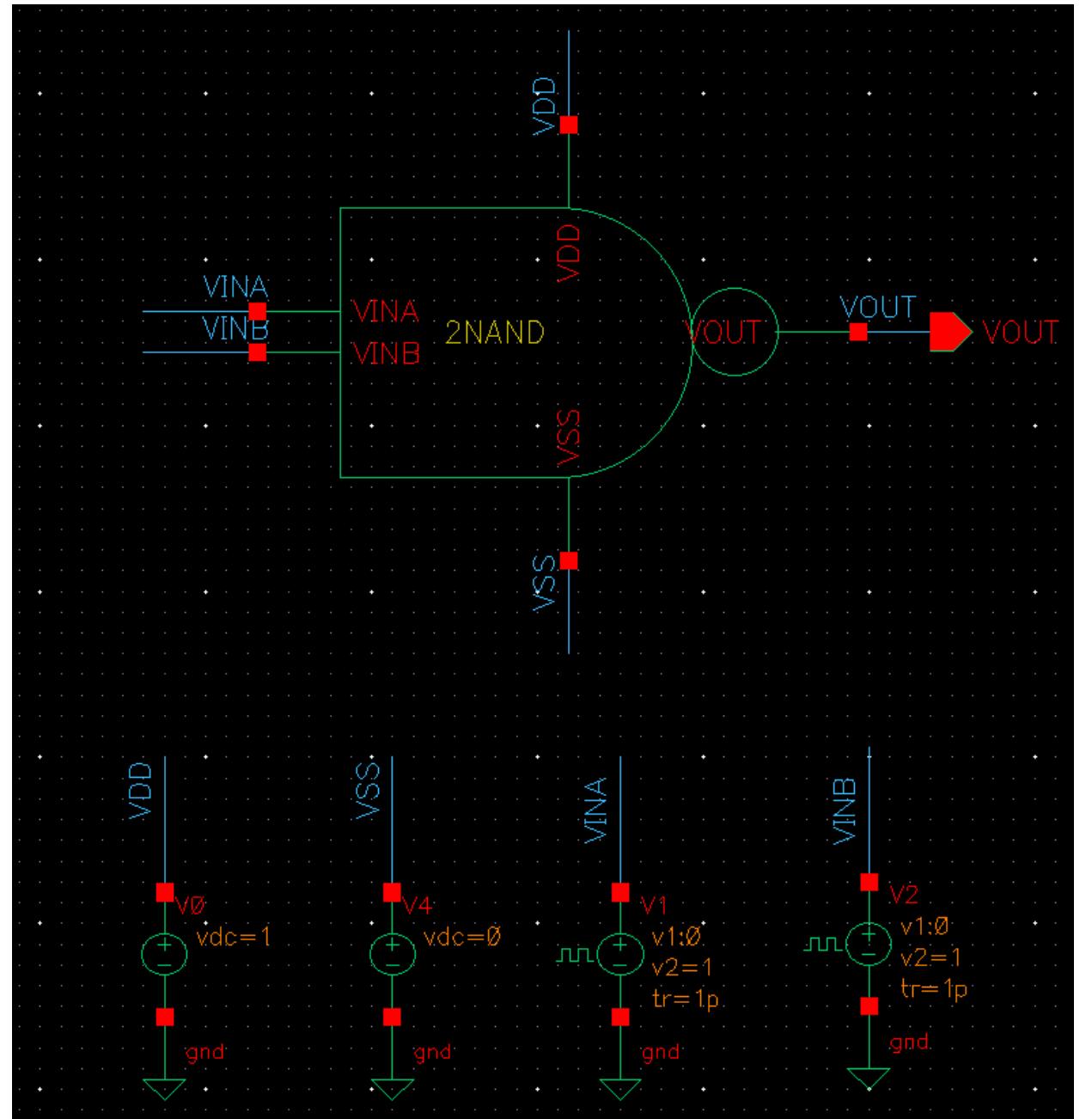


2NAND Simulation

PMOS WIDTH : 2.53u



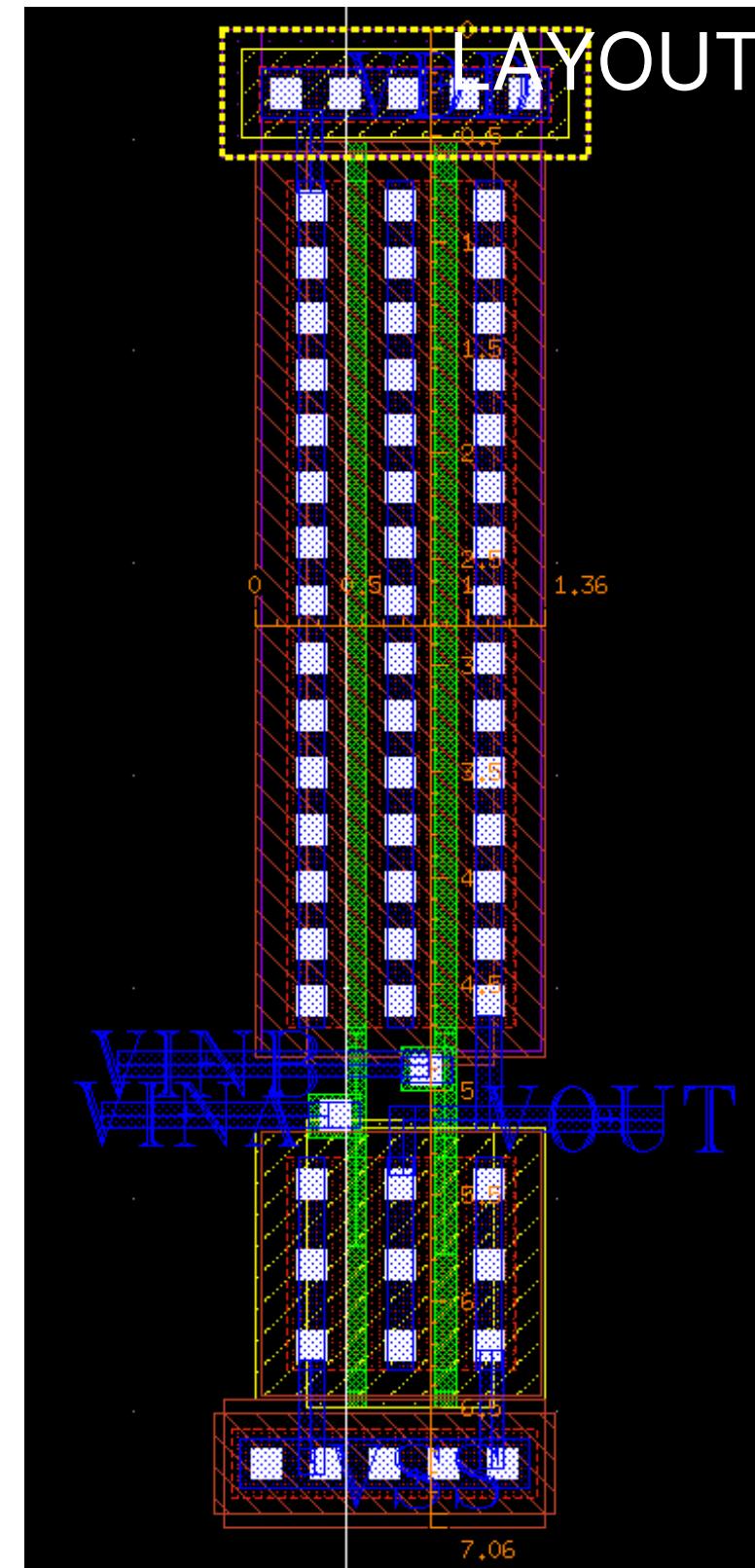
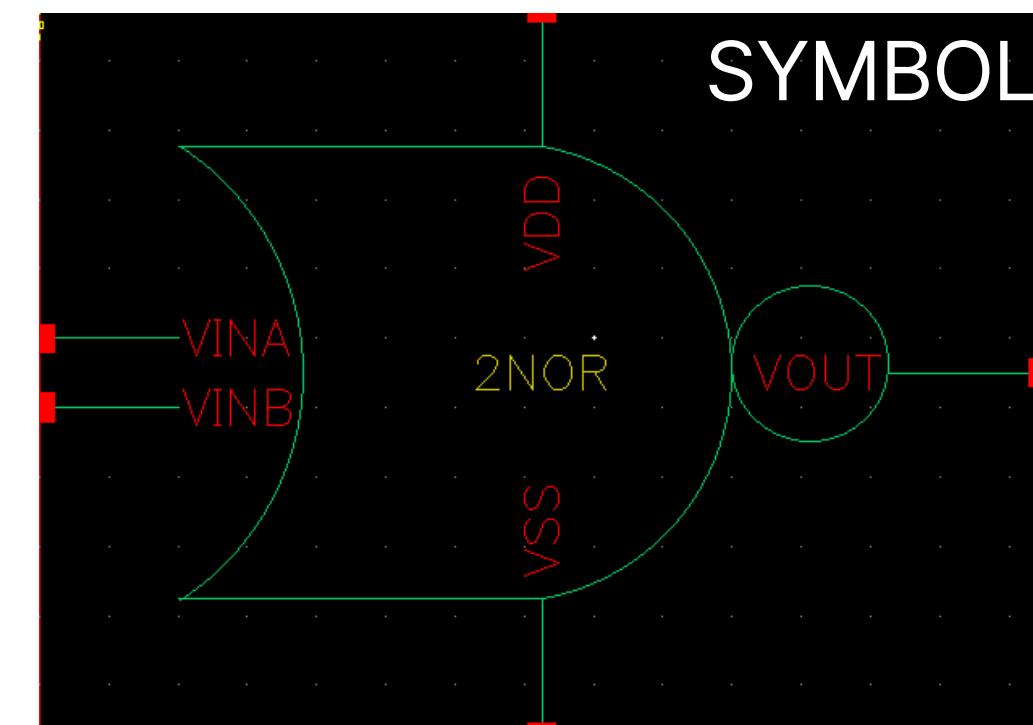
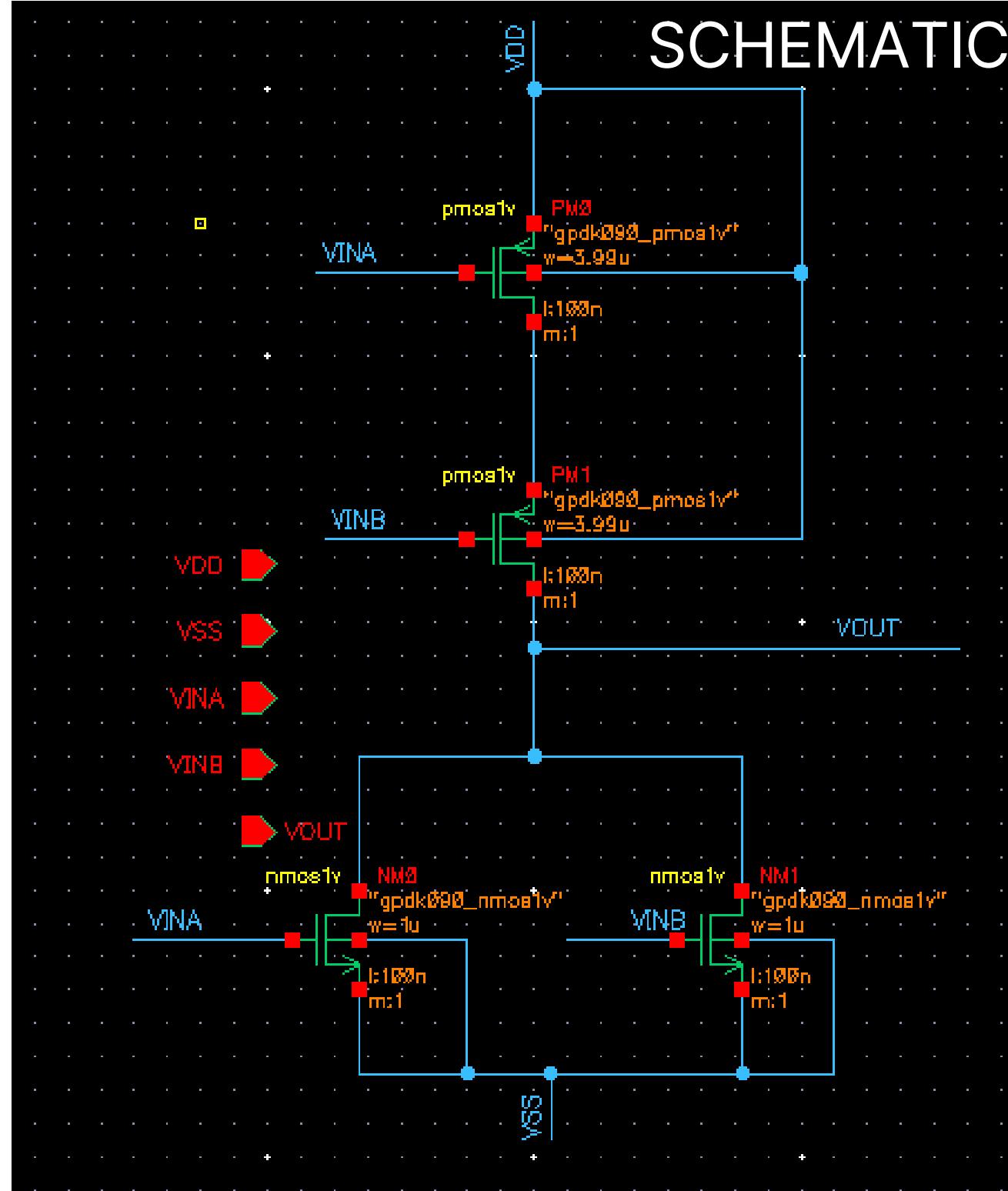
2NAND Simulation



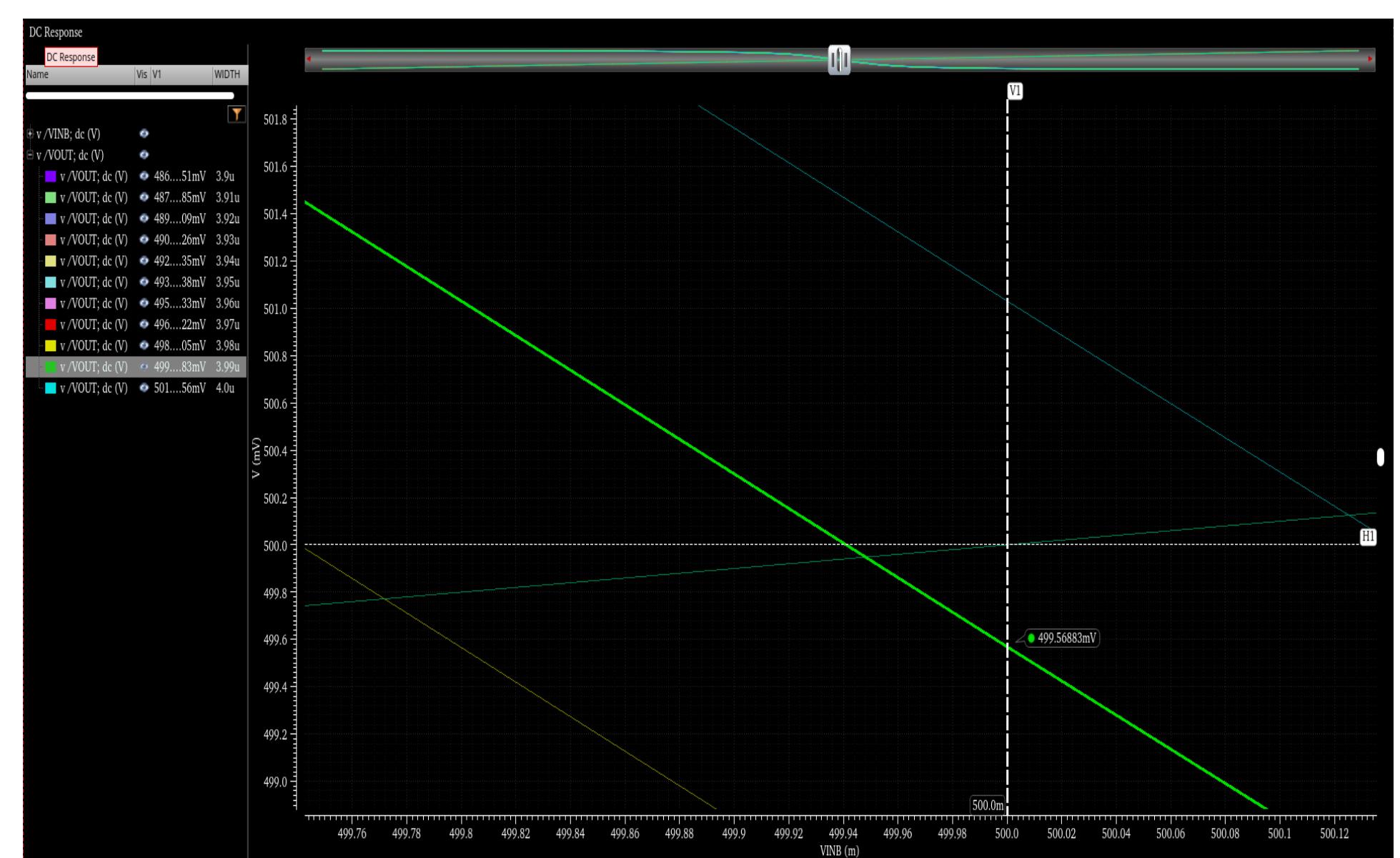
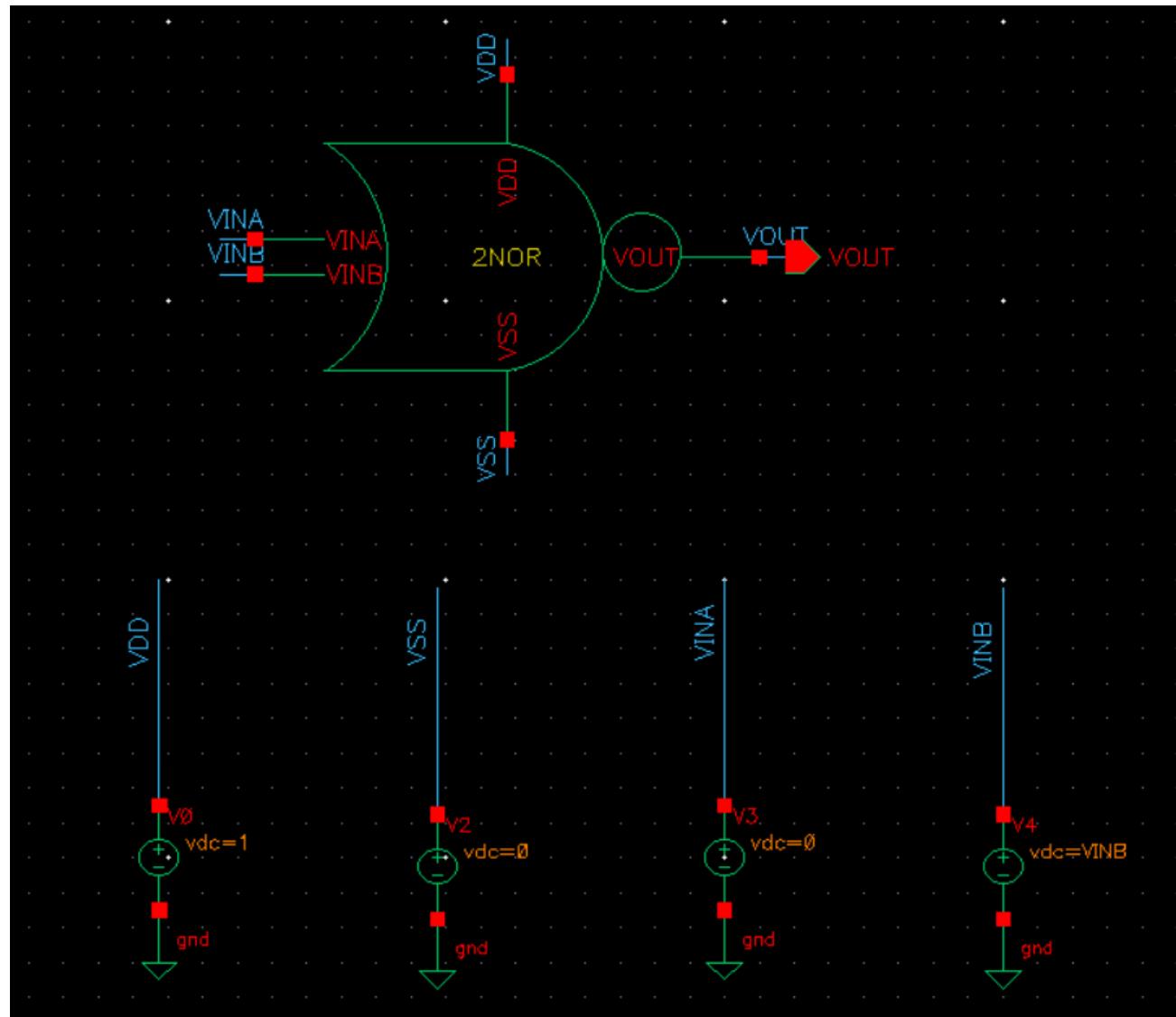
2NAND Truth Table

2NOR

length : 7.06u
width : 1.36u



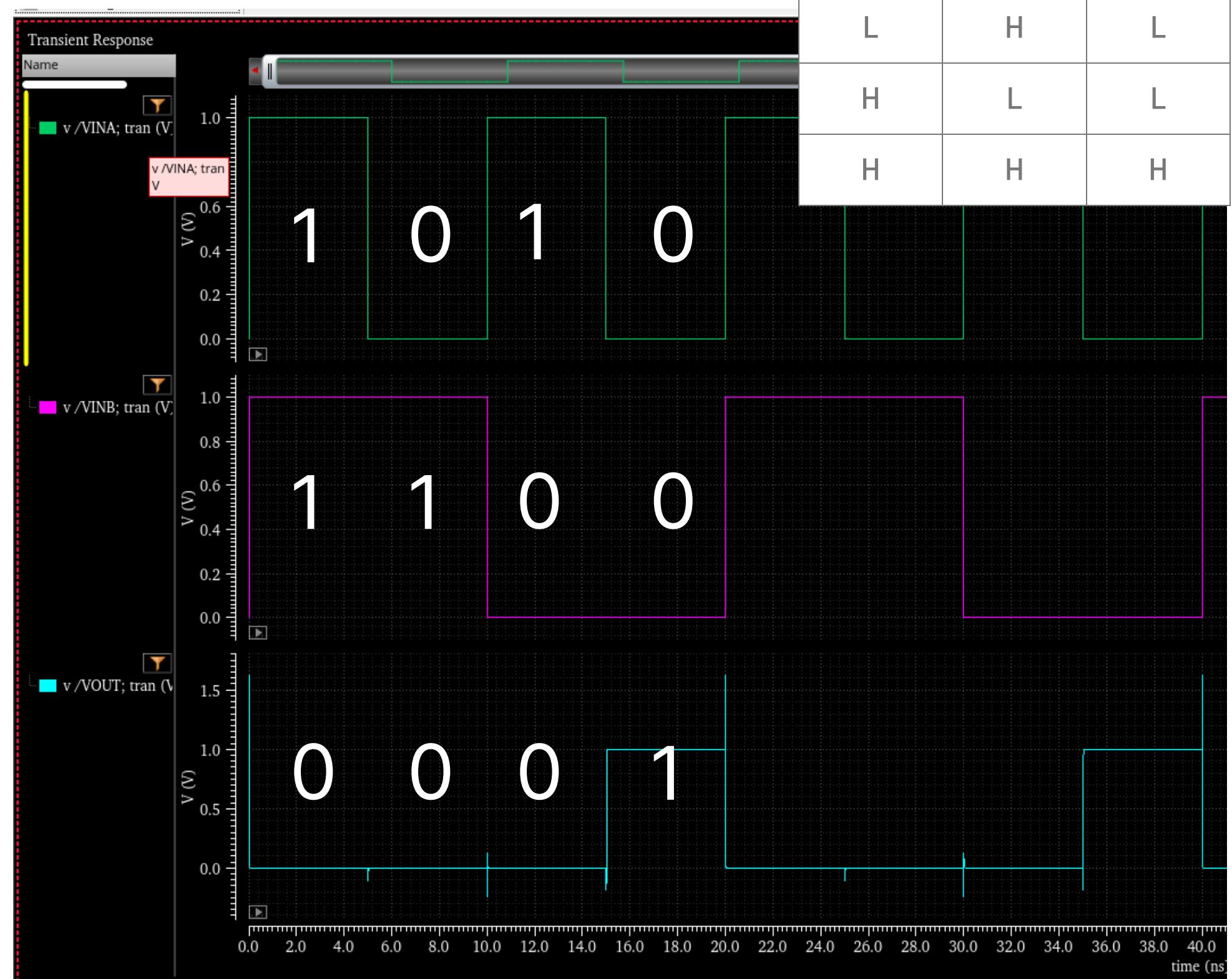
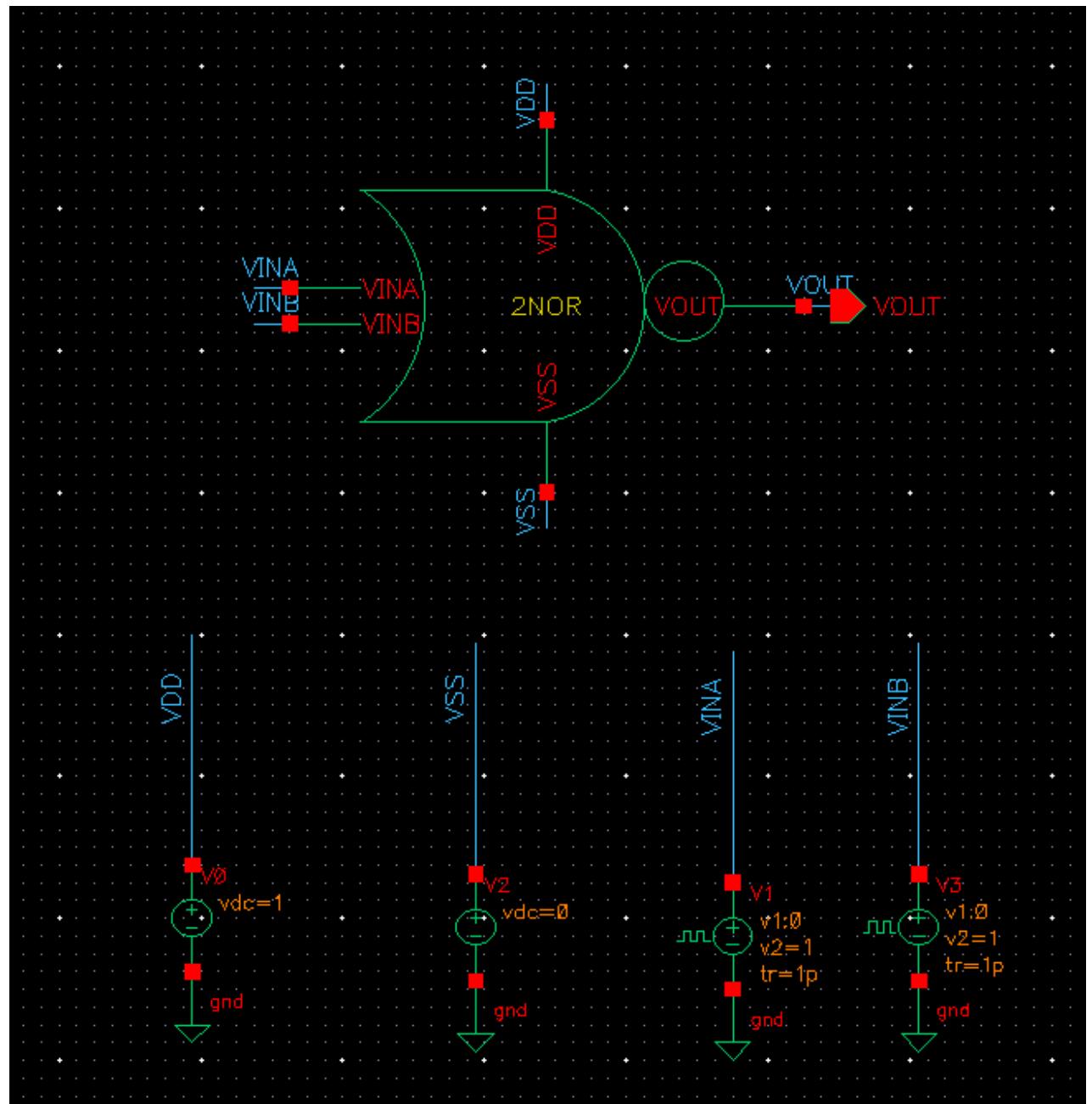
2NOR Simulation



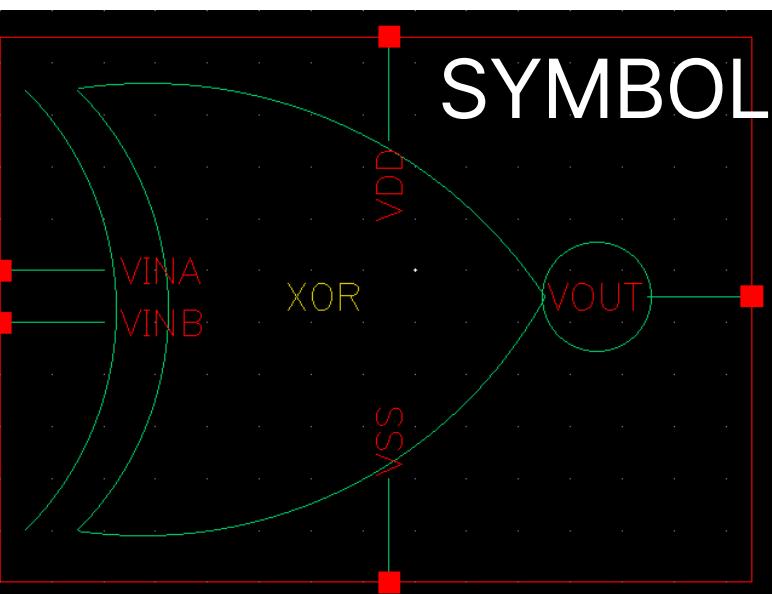
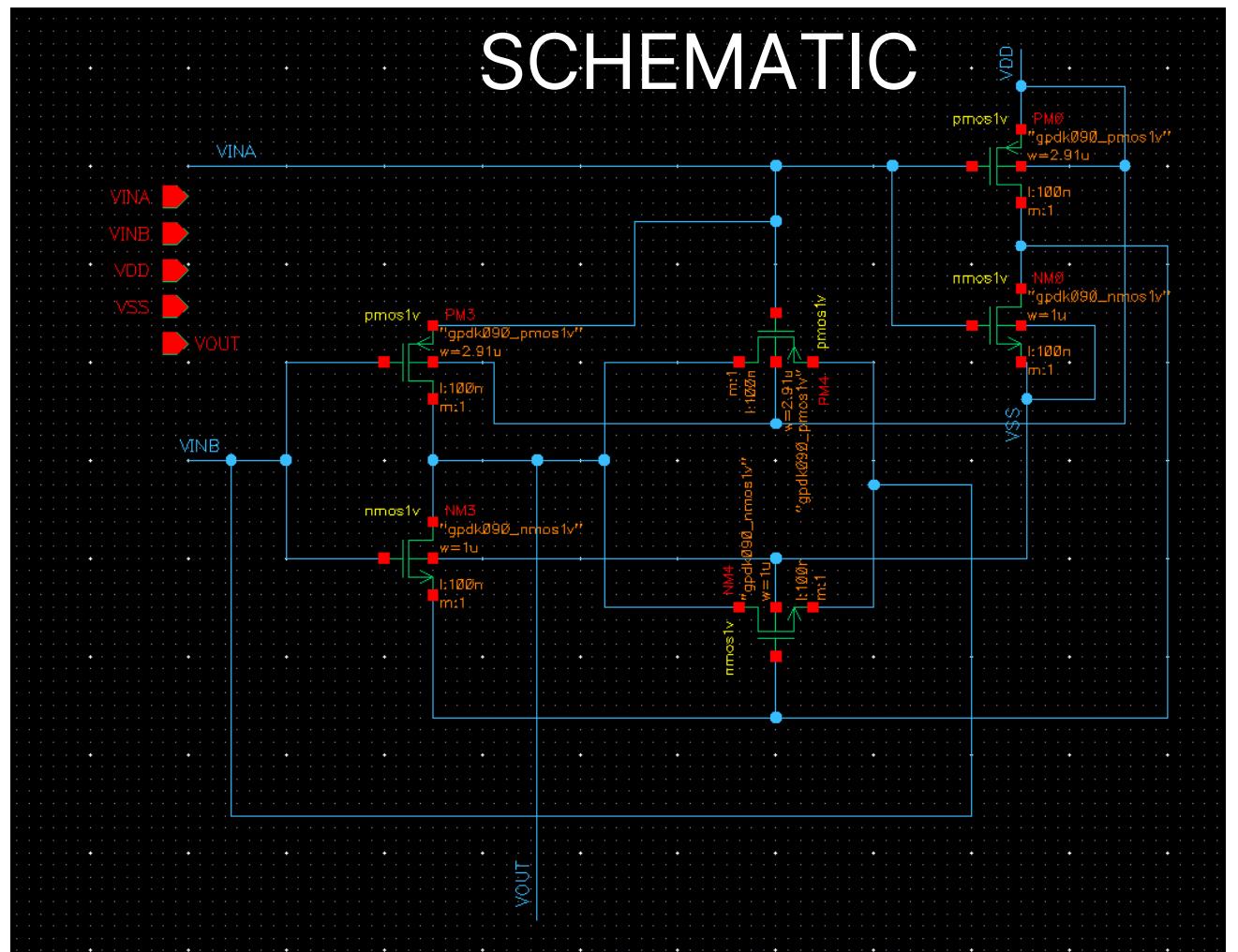
2NOR Truth Table

| VA | VB | VOUT |
|----|----|------|
| L | L | L |
| L | H | L |
| H | L | L |
| H | H | H |

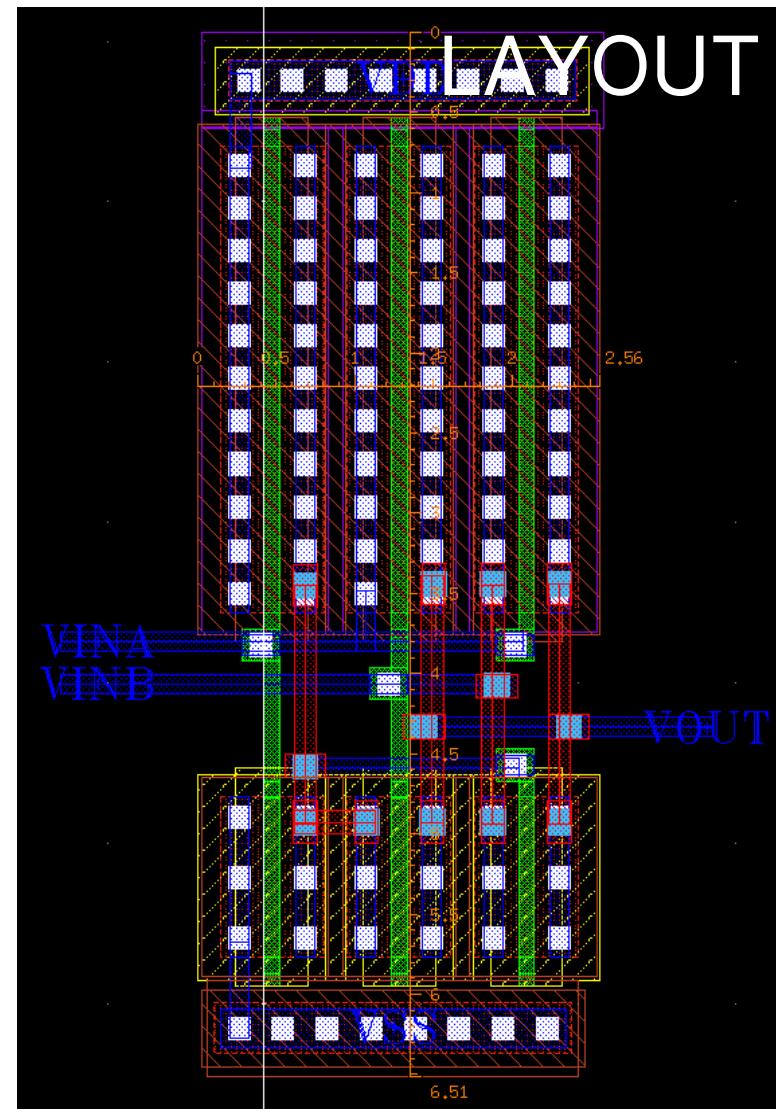
2NOR Simulation



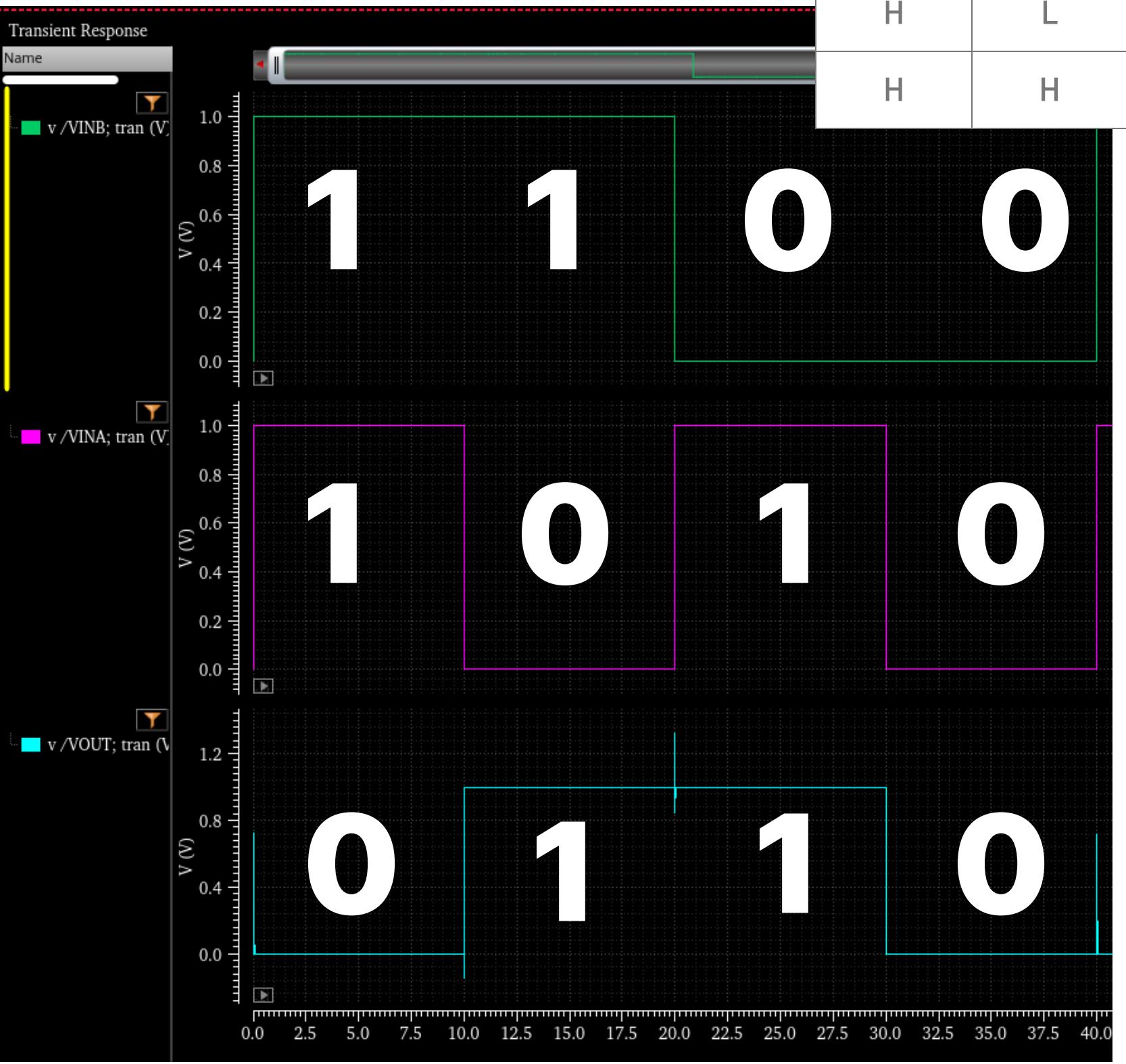
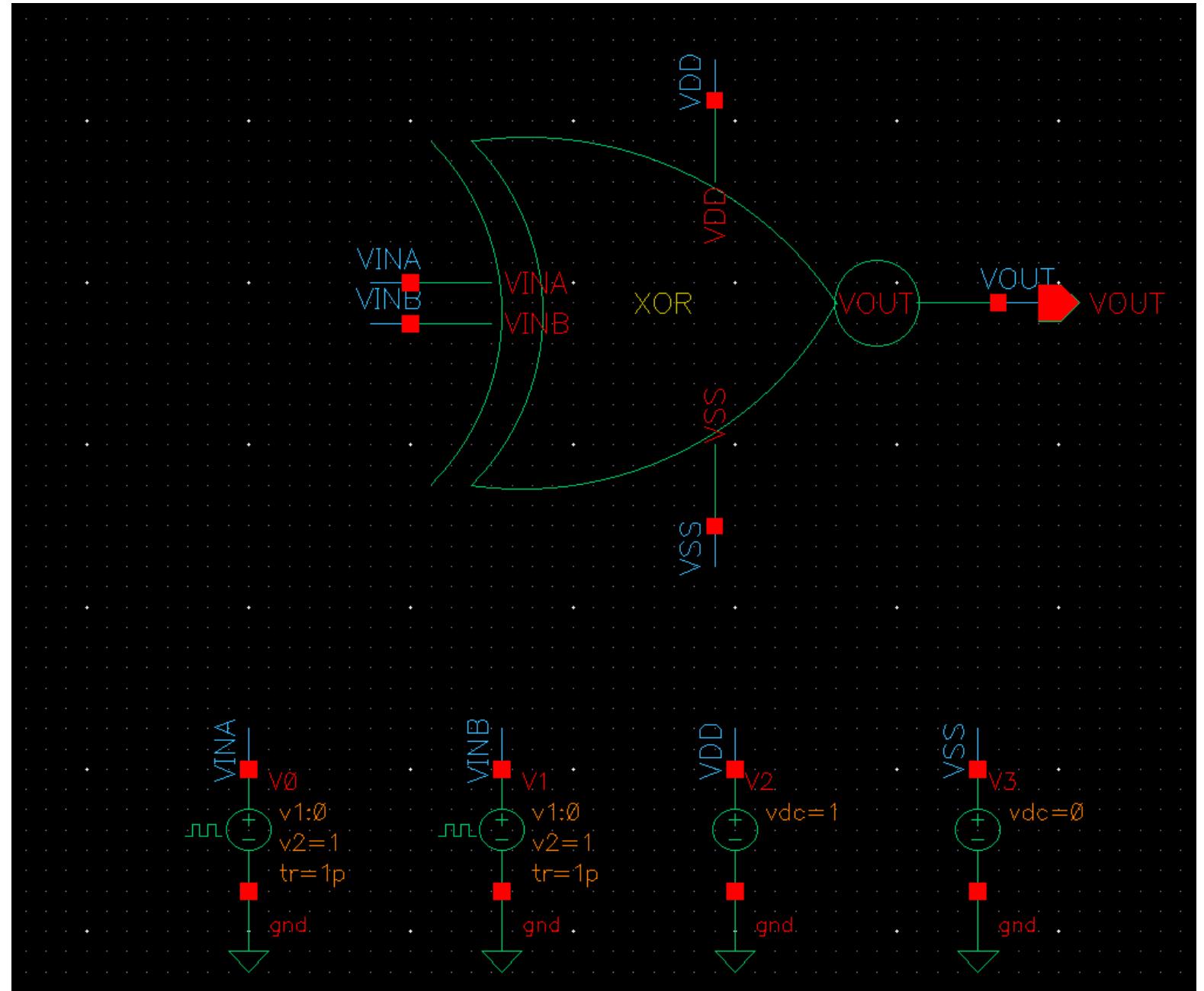
XOR



length : 6.51u
width : 2.56u

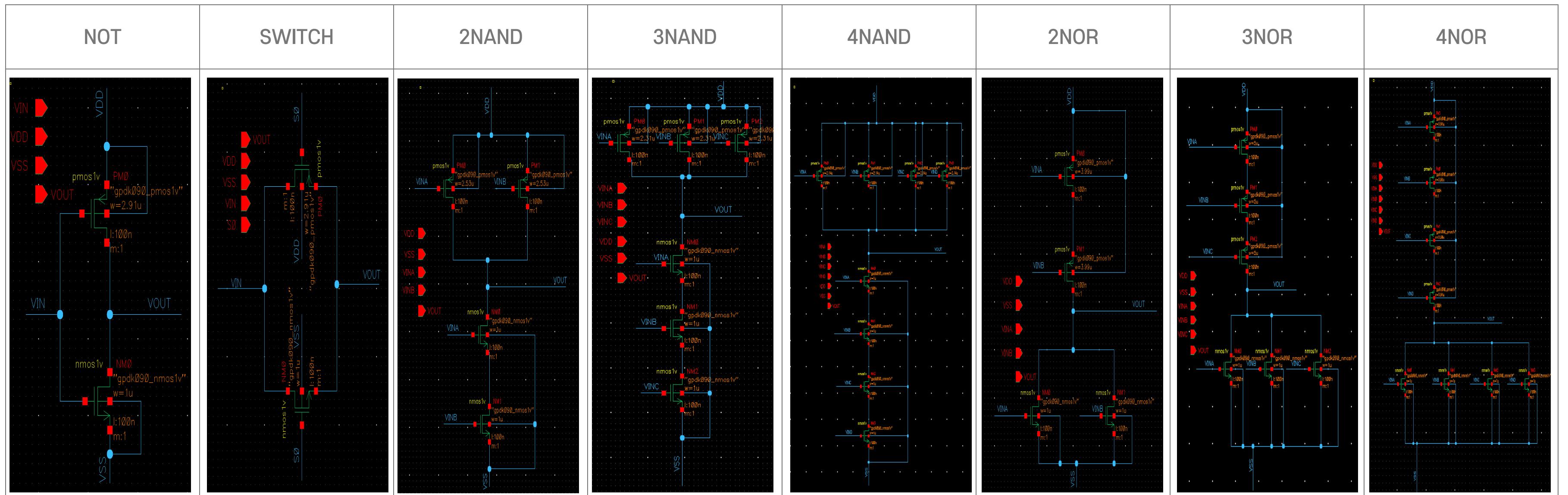


XOR Simulation



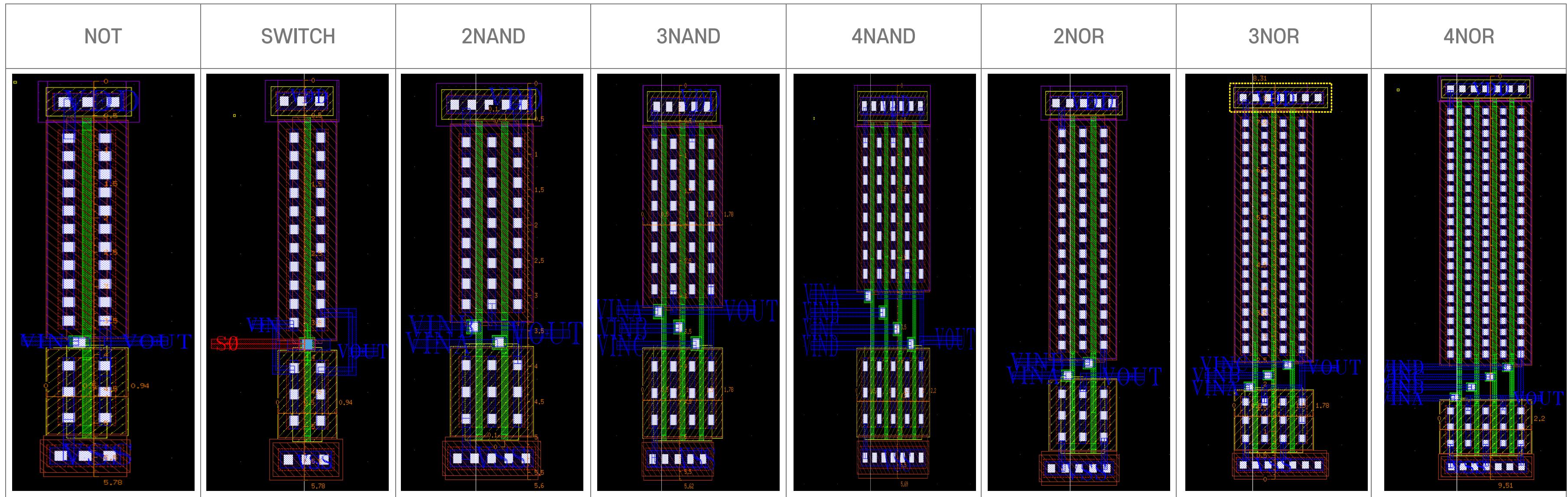
Digital Logic Gate schematic

| | NOT | SWITCH | 2NAND | 3NAND | 4NAND | 2NOR | 3NOR | 4NOR |
|-------------------|--------|--------|--------|--------|--------|--------|------|--------|
| NMOS L = 100nm | 1um | 1um | 1um | 1um | 1um | 1um | 1um | 1um |
| PMOS L = 100nm | 2.91um | 2.91um | 2.53um | 2.31um | 2.14um | 3.99um | 5um | 5.96um |

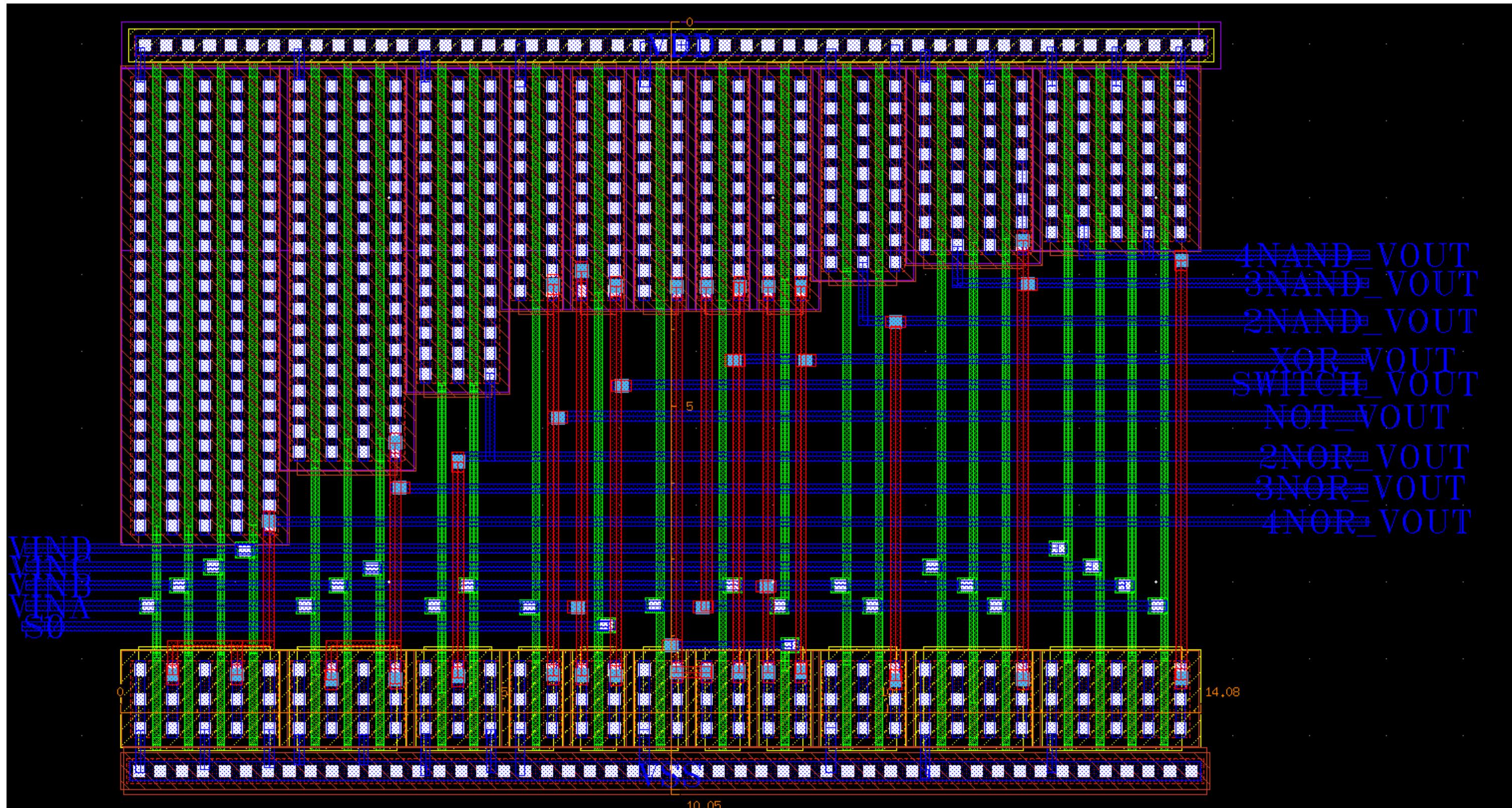


Digital Logic Gate Layout

| | NOT | SWITCH | 2NAND | 3NAND | 4NAND | 2NOR | 3NOR | 4NOR |
|-------------------------|------|--------|-------|-------|-------|------|-------|-------|
| Area(μm^2) | 5.43 | 5.43 | 7.61 | 10.00 | 12.52 | 9.60 | 14.77 | 20.92 |



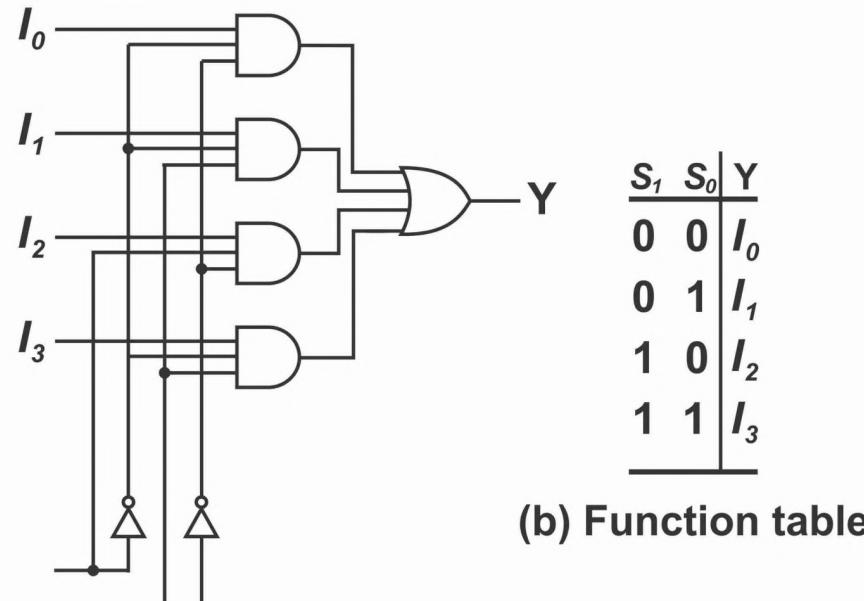
Digital Logic Gate Layout



DIGITAL CIRCUIT

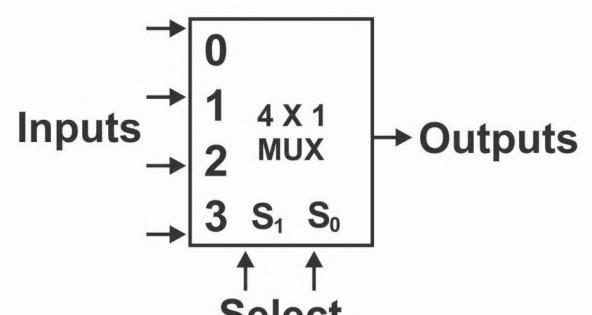
- 2×1 MUX / 4×1 MUX / 8×1 MUX / 16×1 MUX (Logic & Switch)
- HALF_ADDER / FULL_ADDER / 4BIT_ADDER / 4BIT_SUBTRACTOR

MUX(Multiplexer)



(b) Function table

(a) Logic diagram



(c) Blockdiagram

MUX

→ “Many-to-one” data selector.

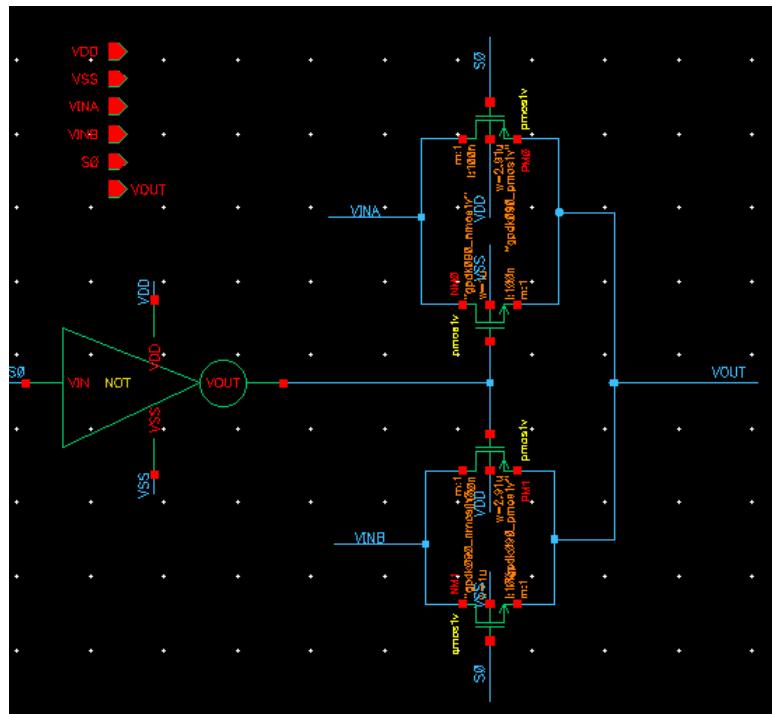
Routes 1 of 2^n inputs to a single output via n binary select lines.

Fig 4.4 A 4-to-1-line multiplexer

2X1 MUX (LOGIC & SWITCH)

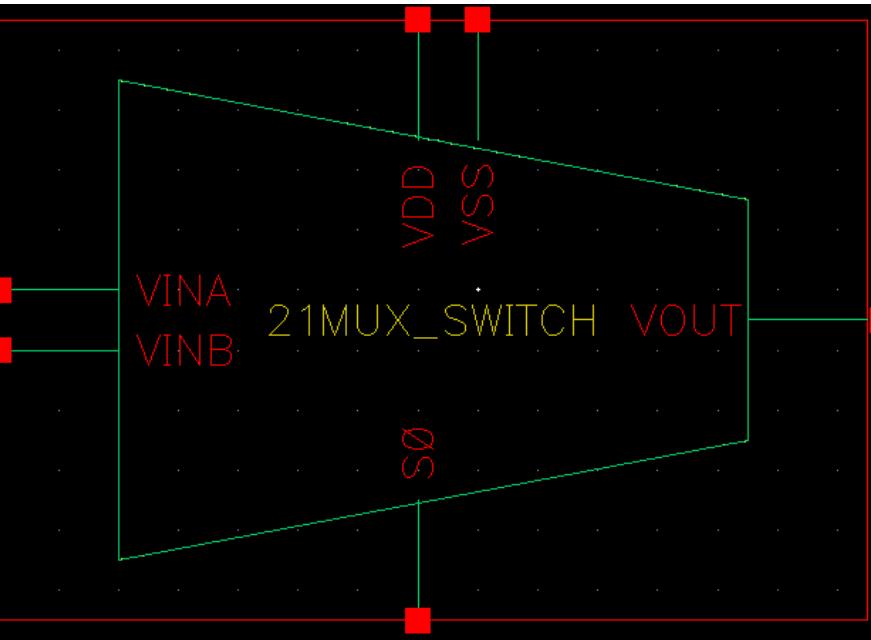
Layout

Schematic

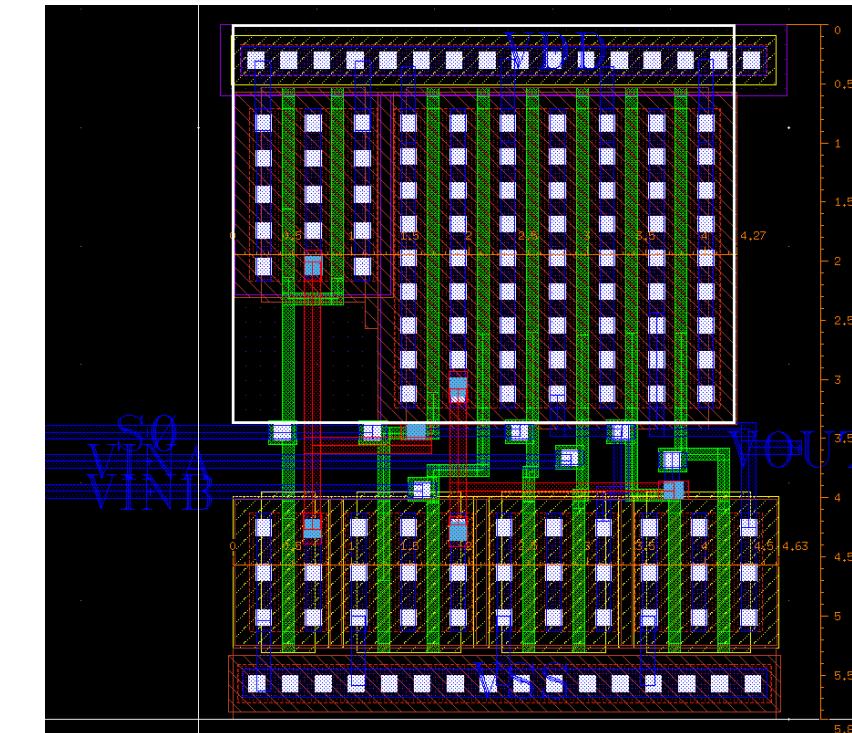
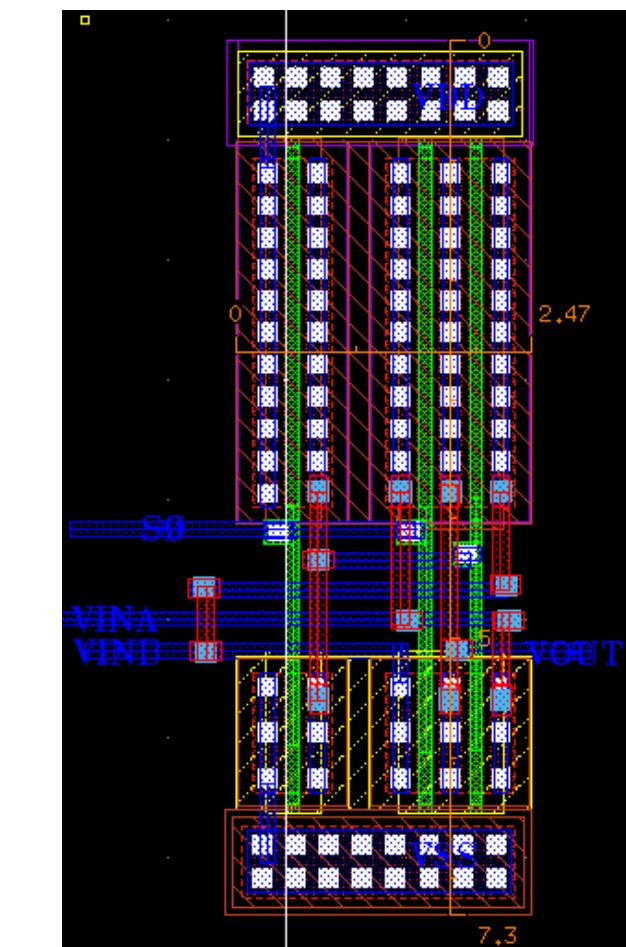
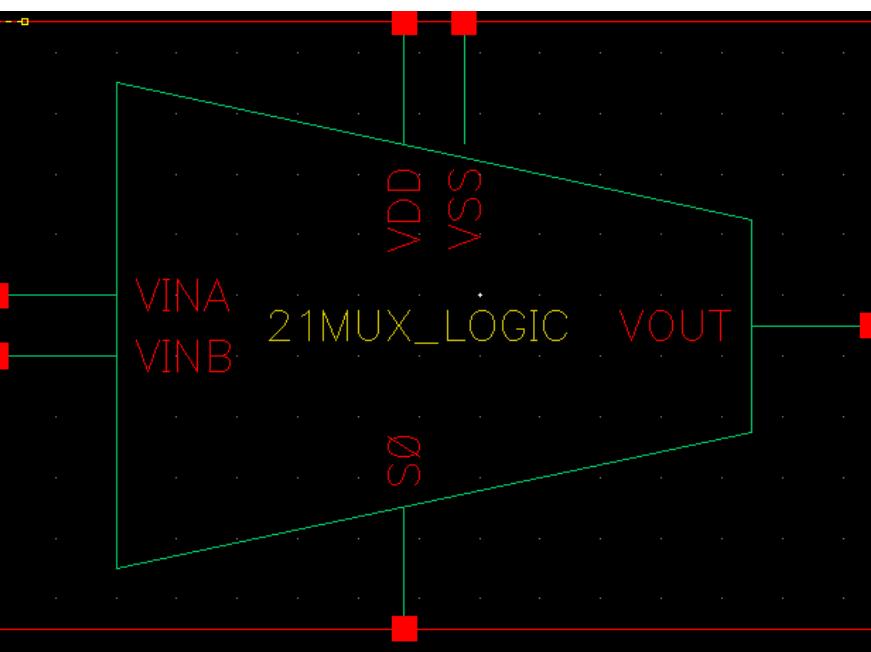
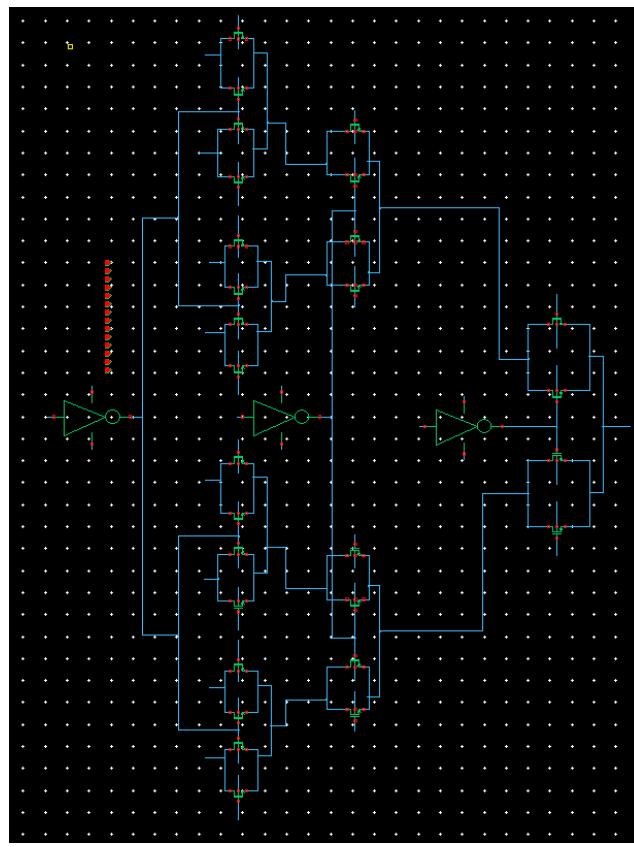


SWITCH

Symbol

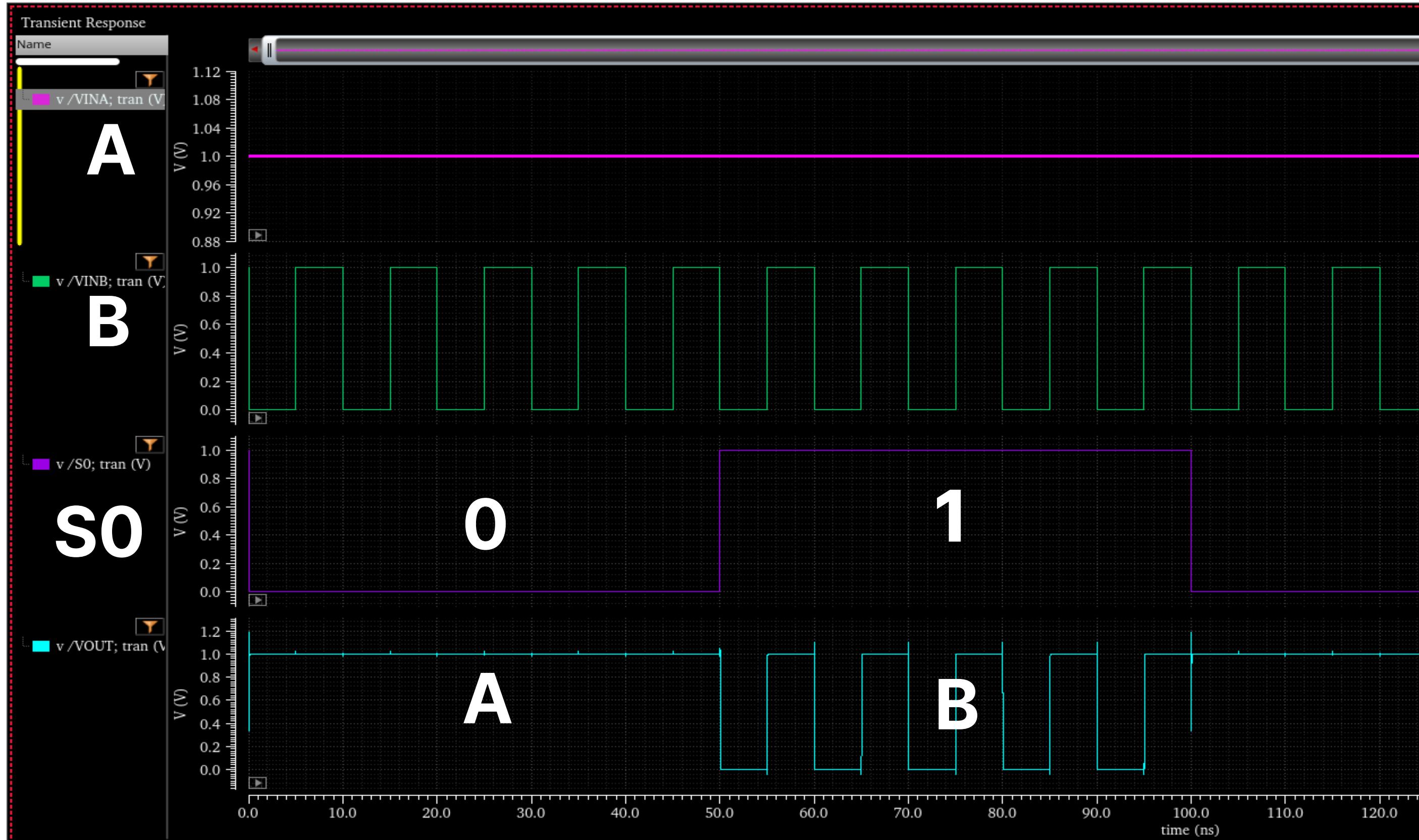


LOGIC



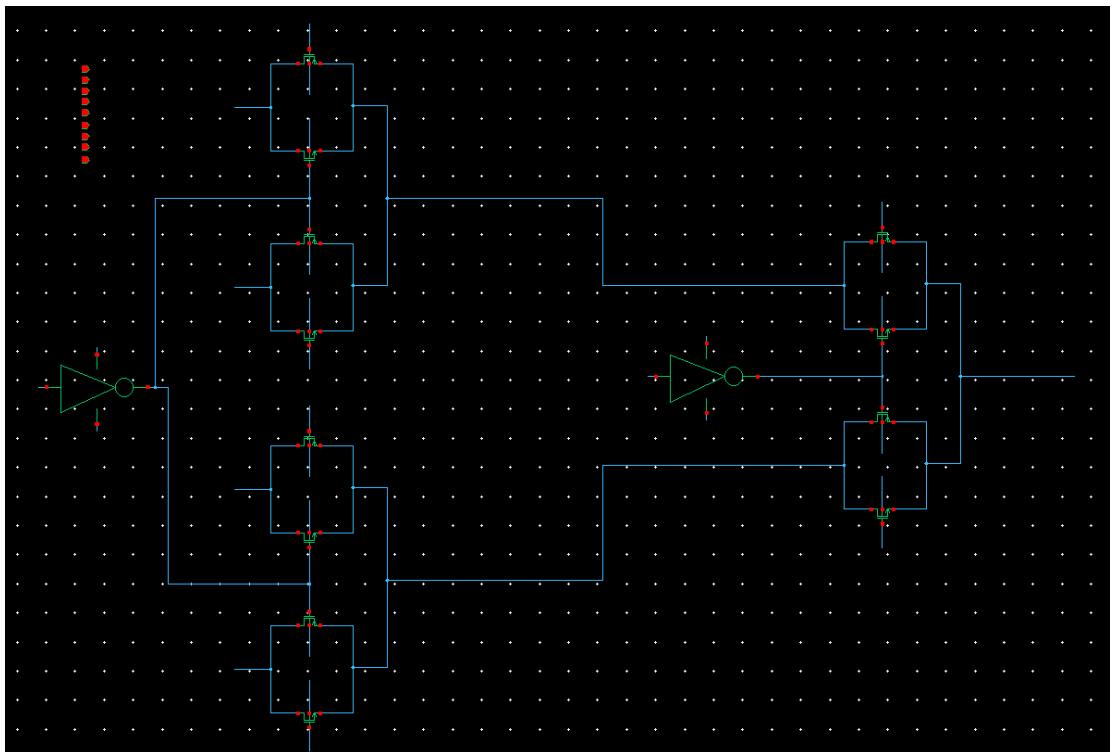
2X1 MUX (LOGIC & SWITCH)

Logic
&
Switch



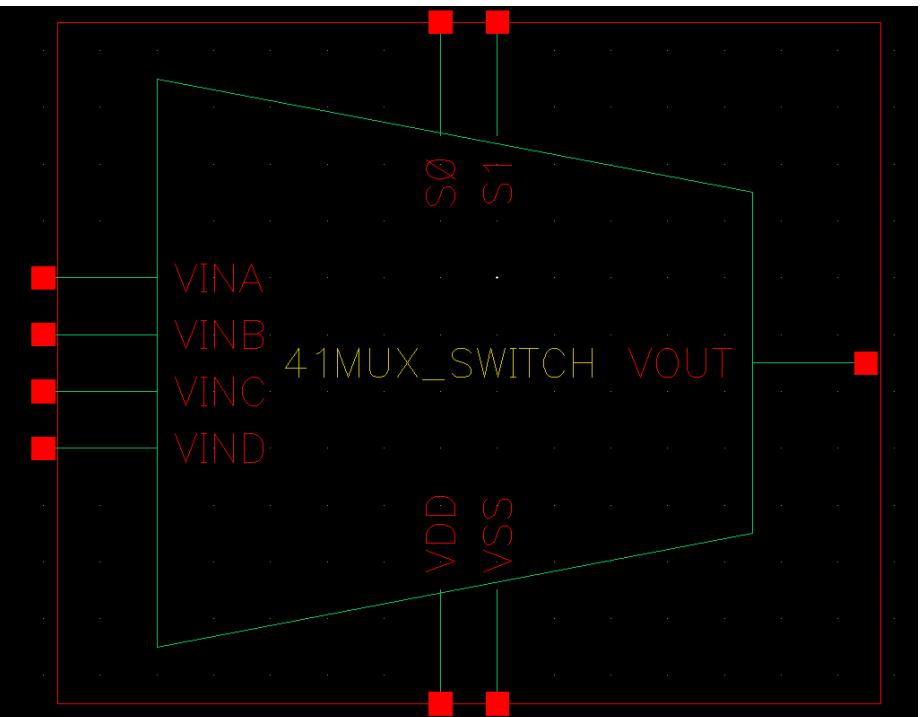
4X1 MUX (LOGIC & SWITCH)

Schematic

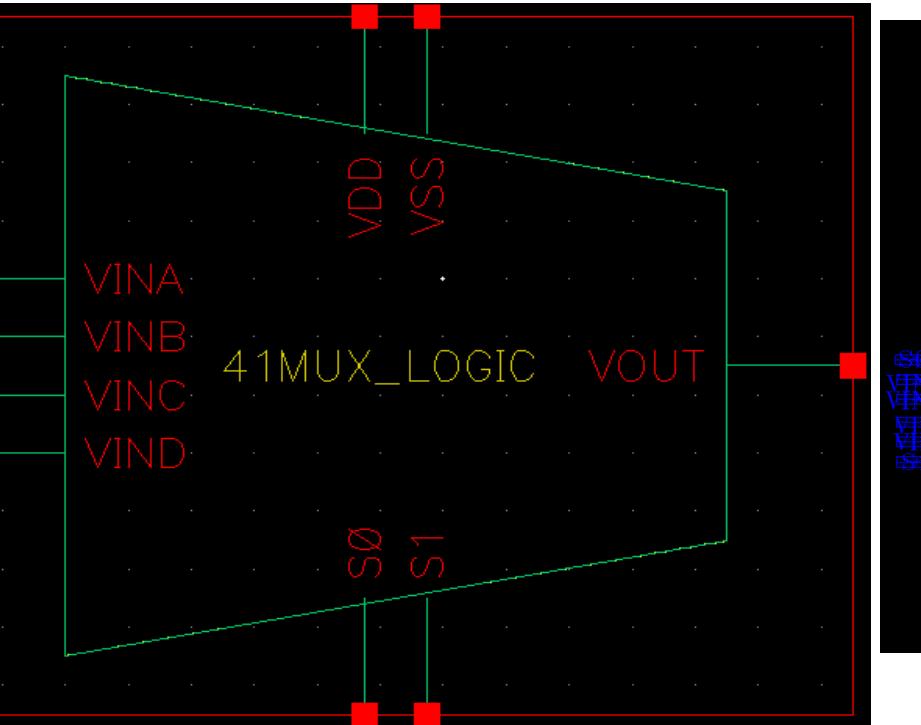
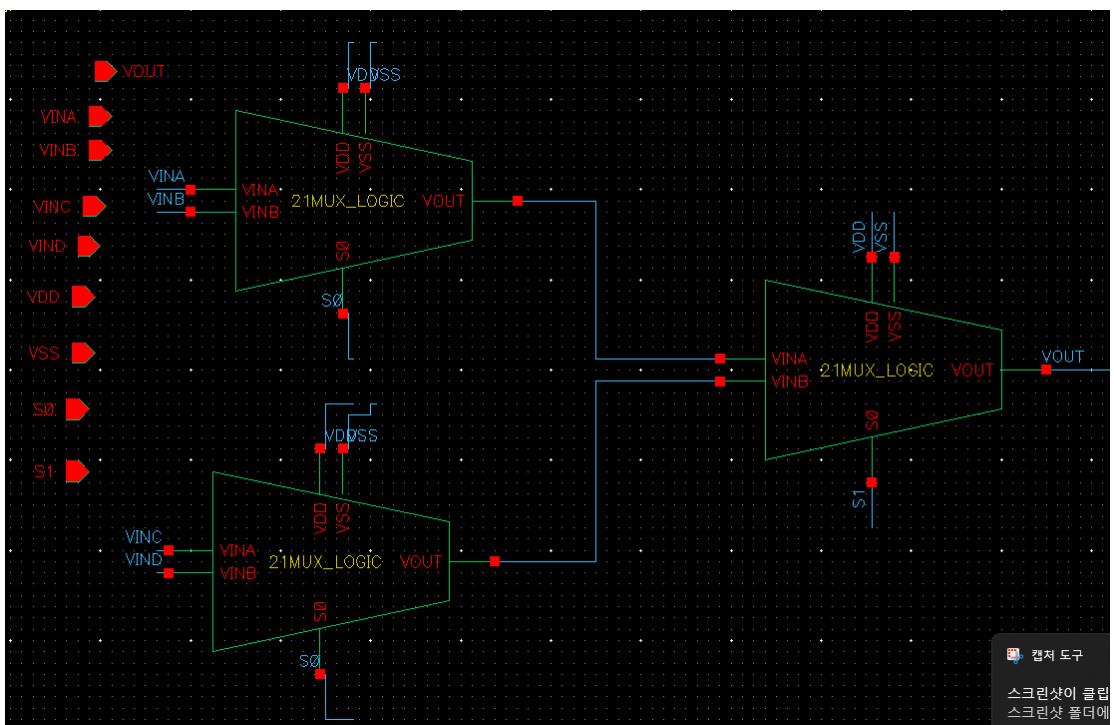


SWITCH

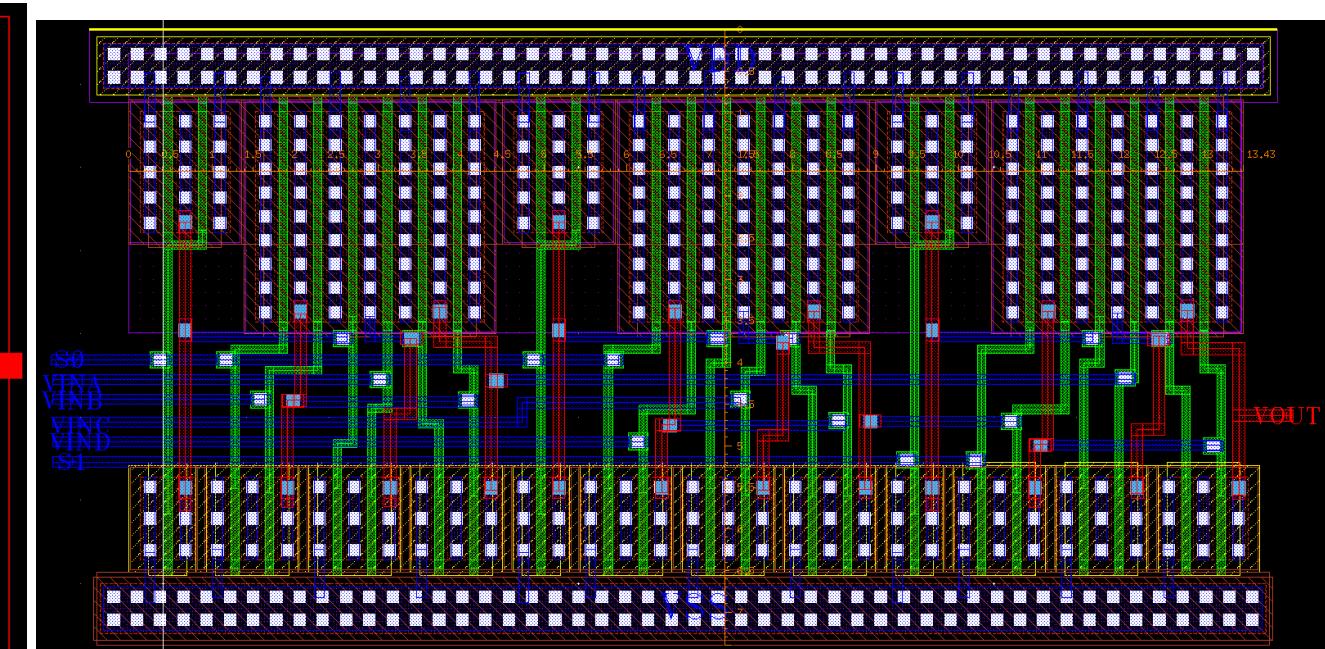
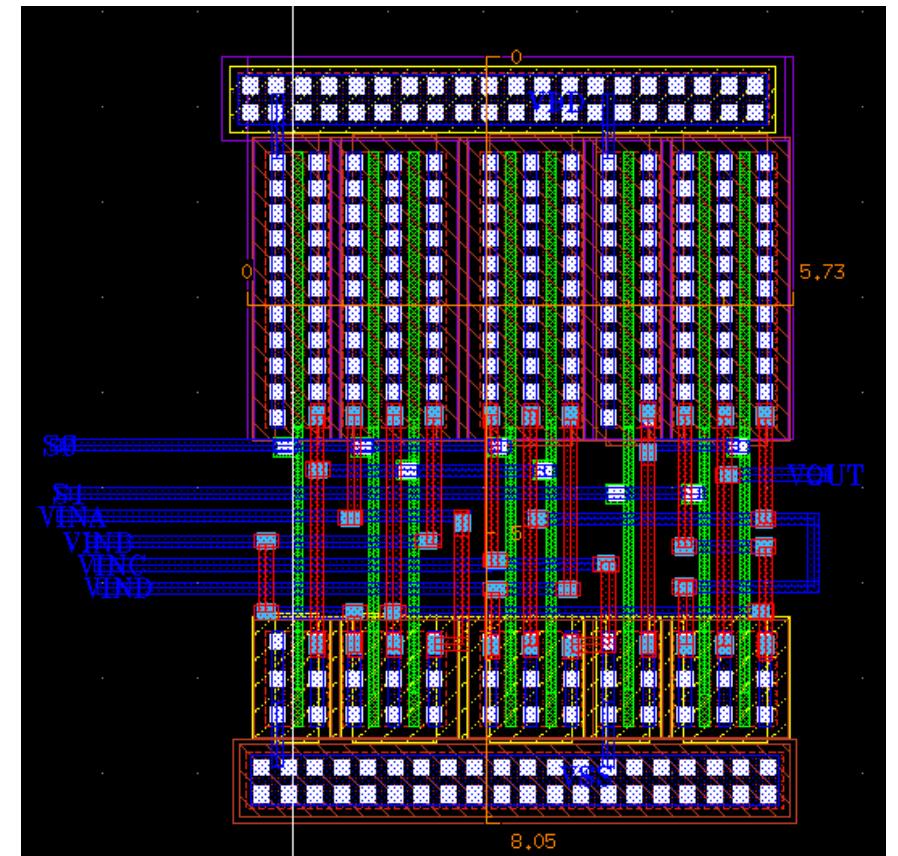
Symbol



LOGIC

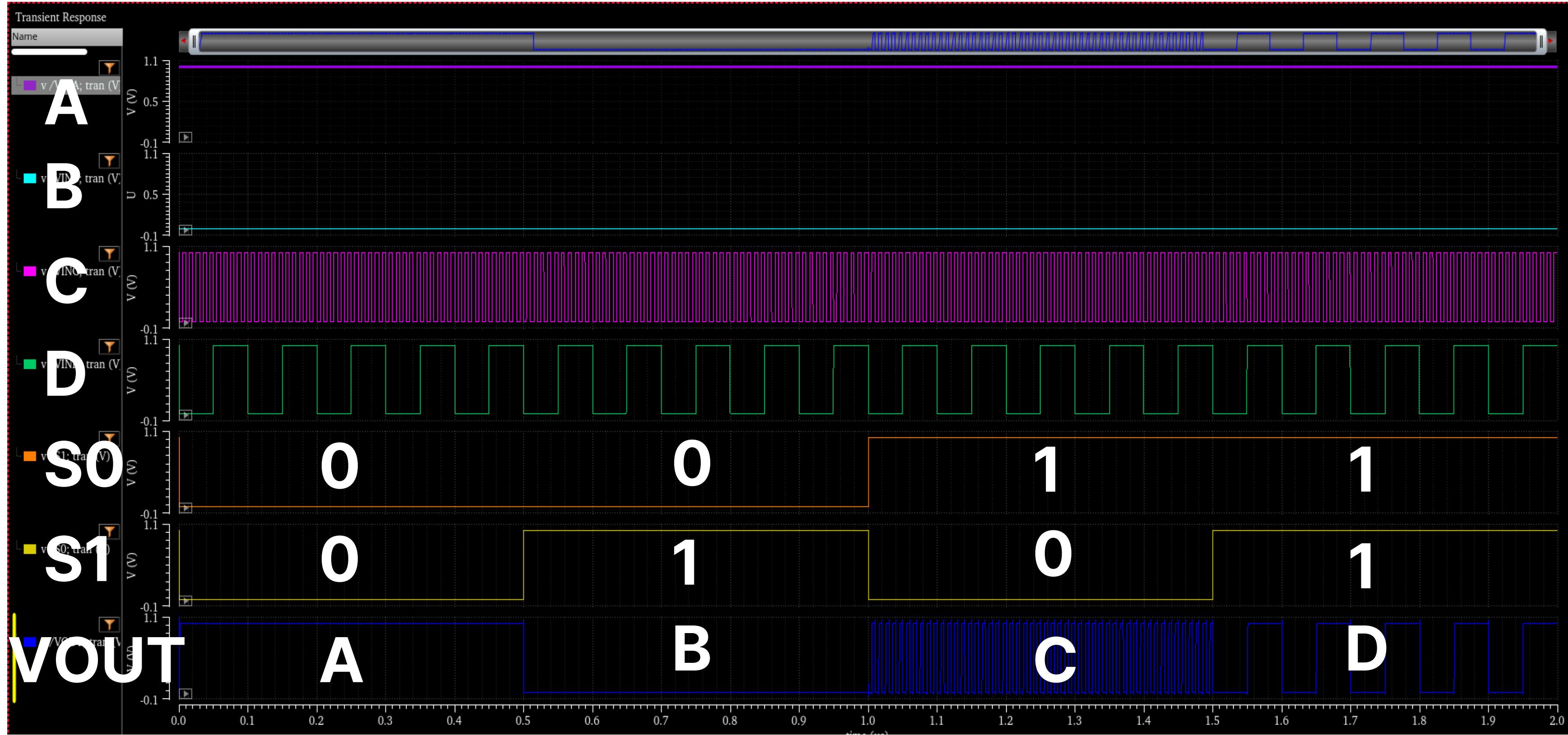


Layout



4X1 MUX (LOGIC & SWITCH)

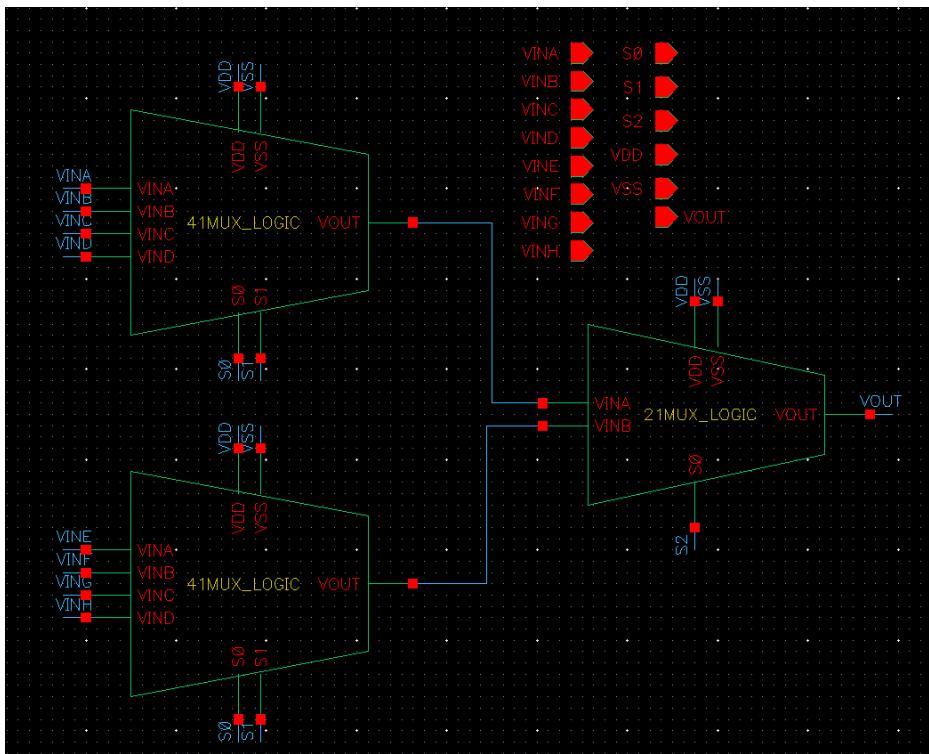
Logic
&
Switch



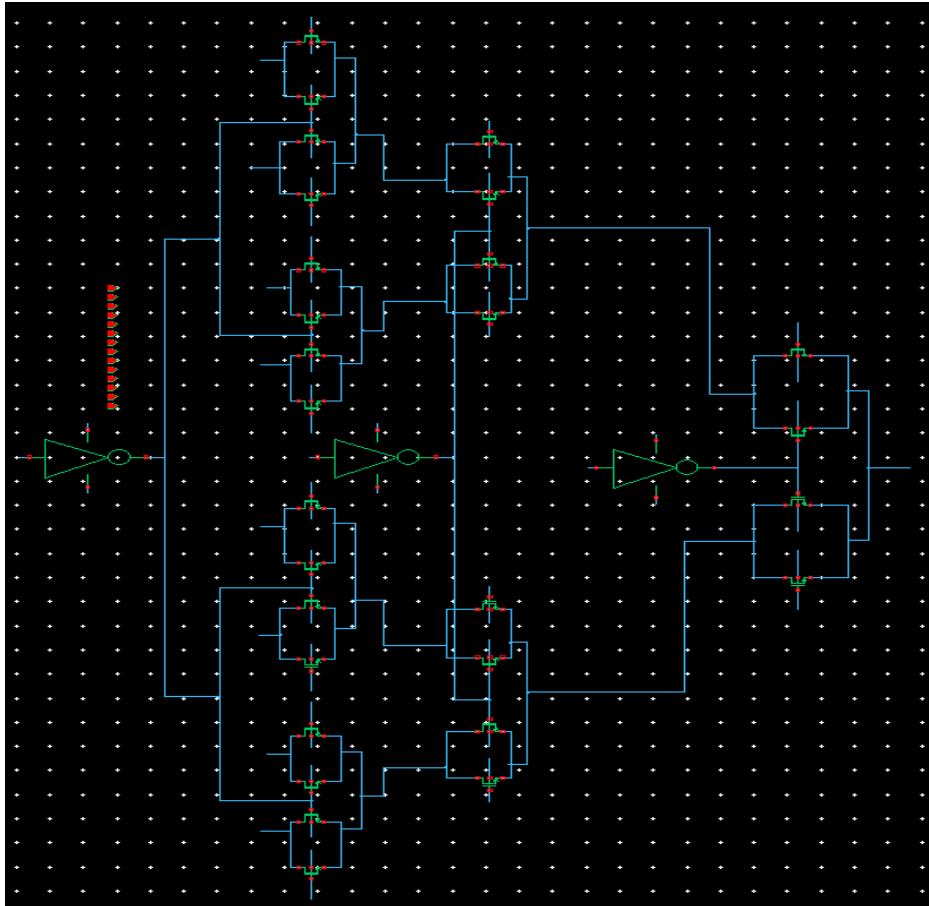
8X1 MUX (LOGIC & SWITCH)

Schematic

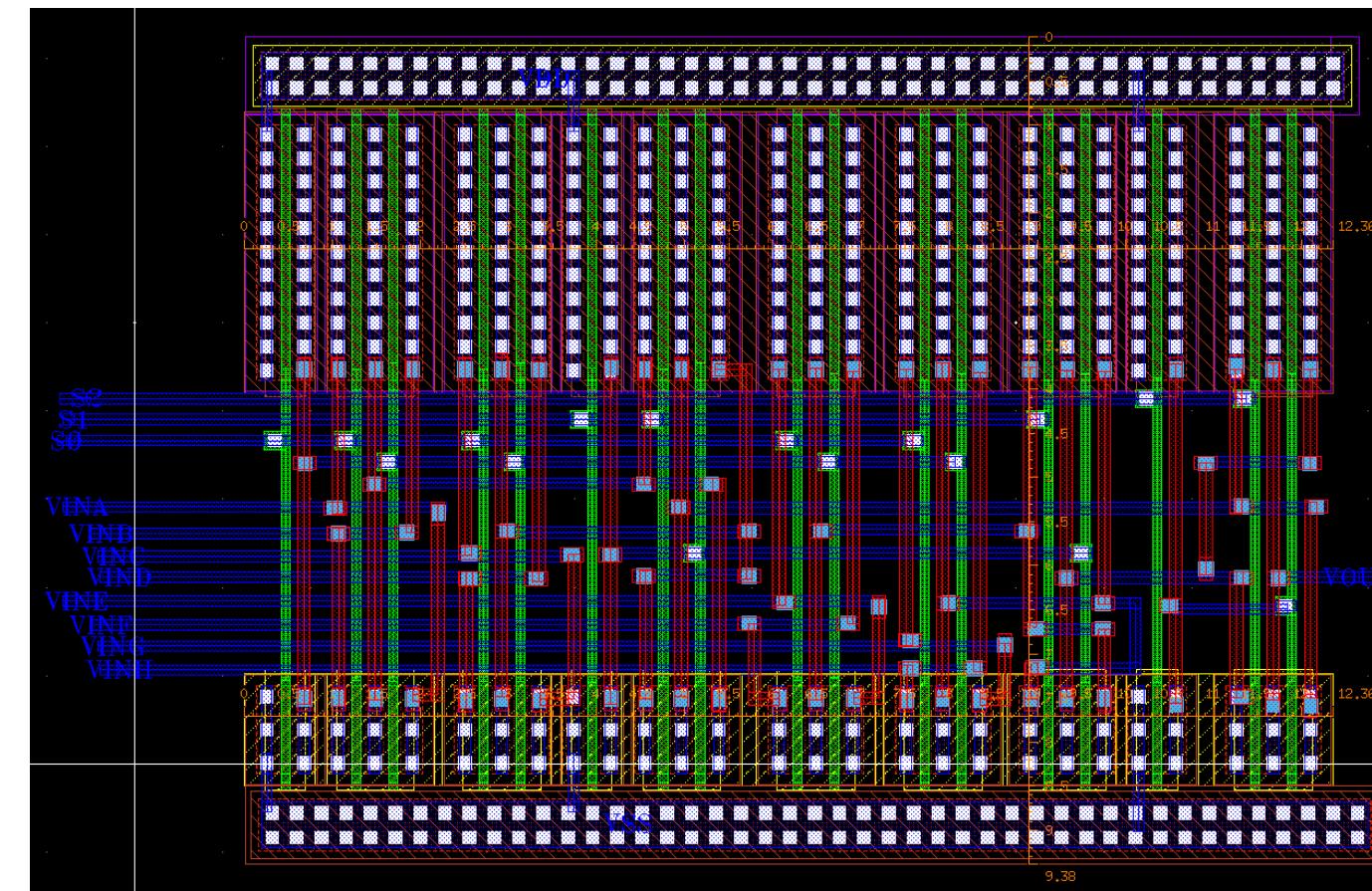
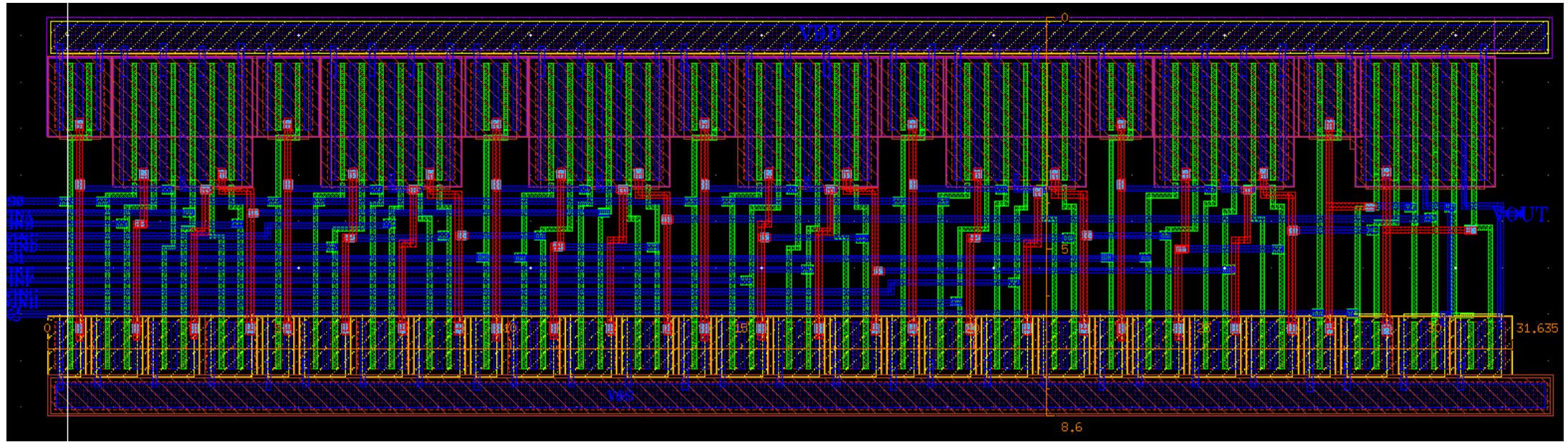
LOGIC



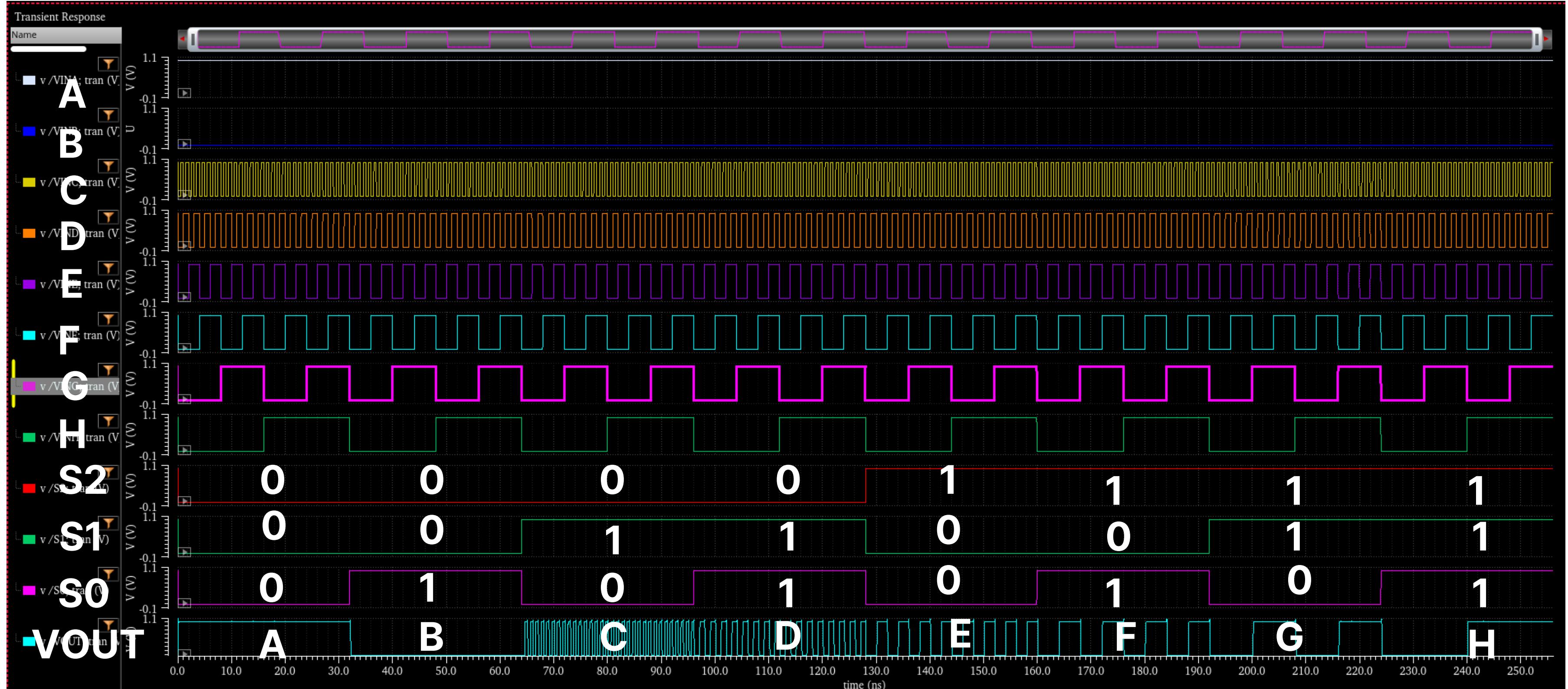
SWITCH



Layout



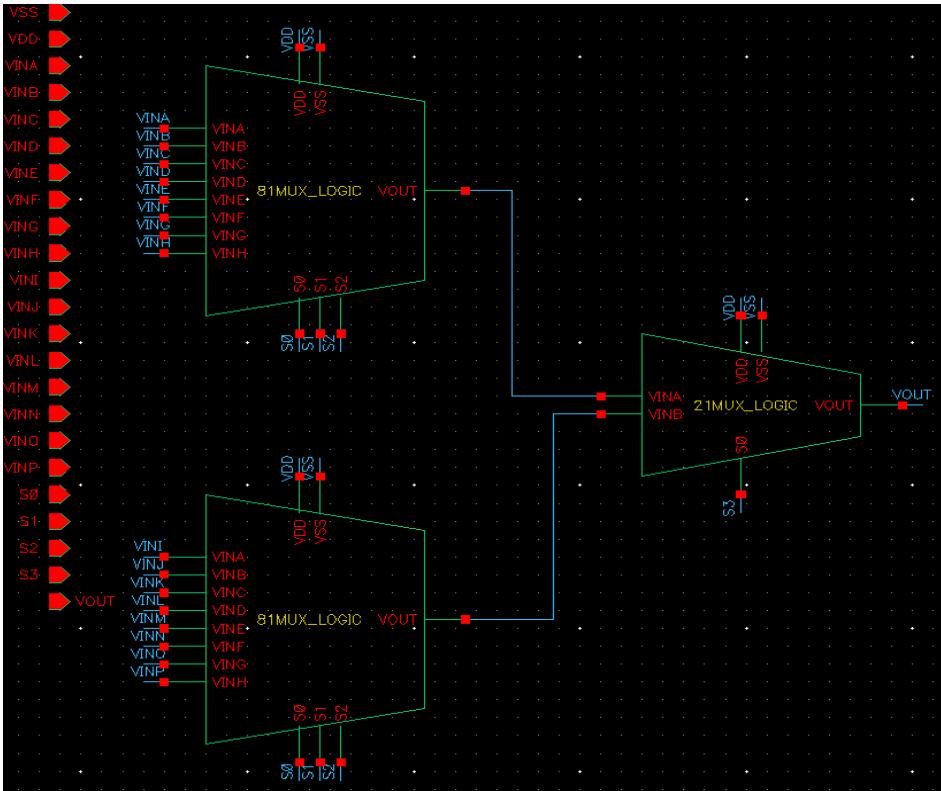
8X1 MUX (LOGIC & SWITCH)



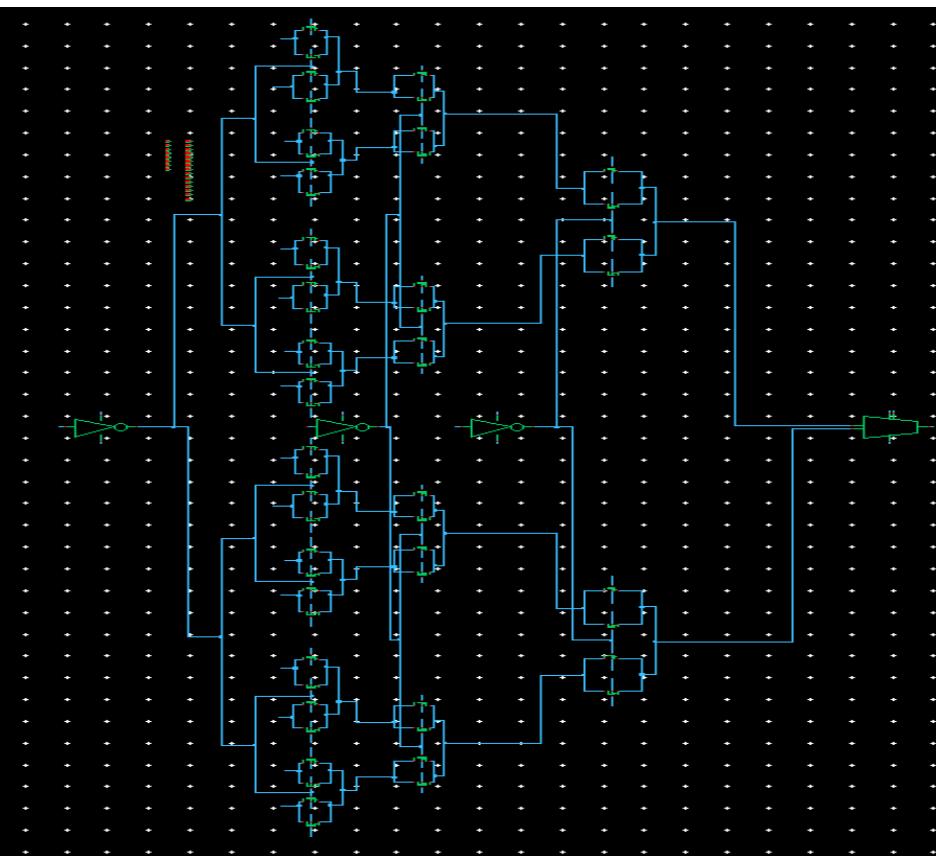
16X1 MUX (LOGIC & SWITCH)

Schematic

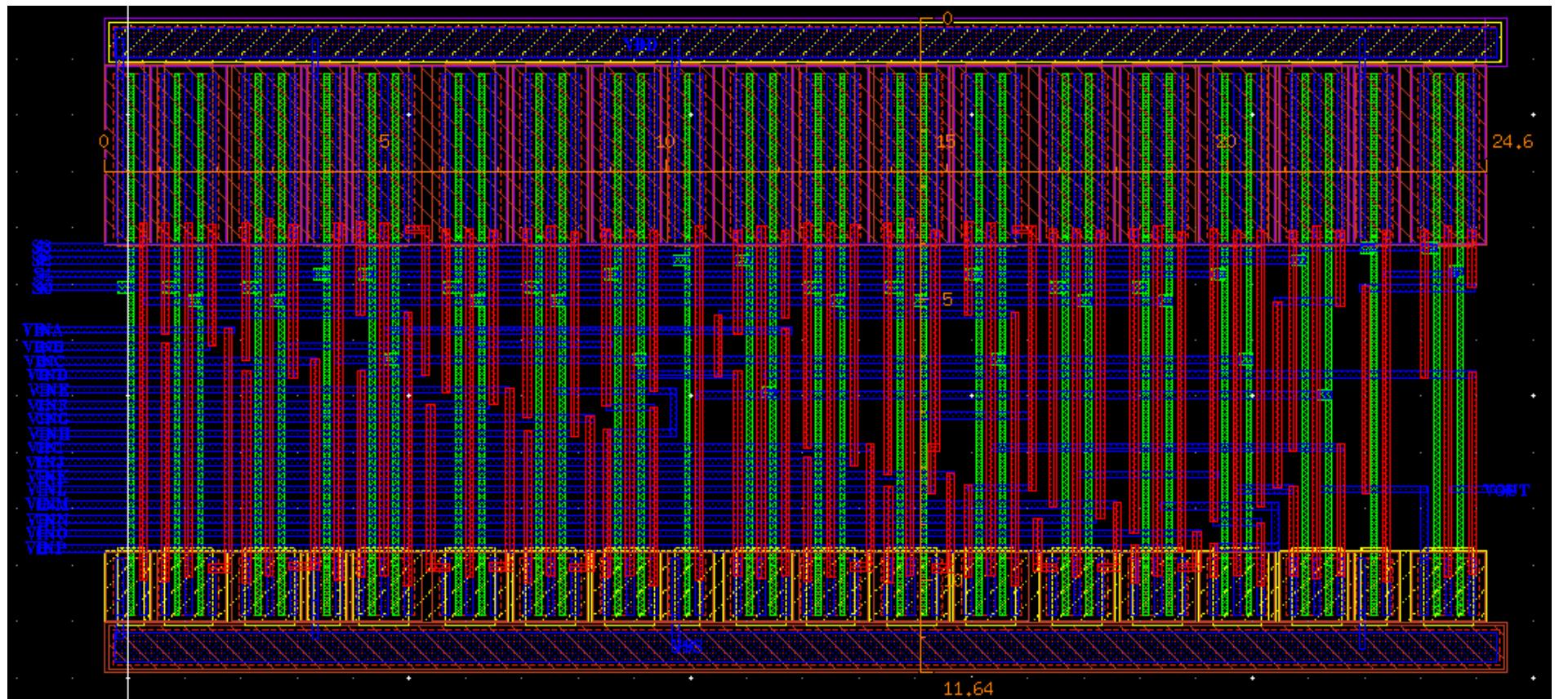
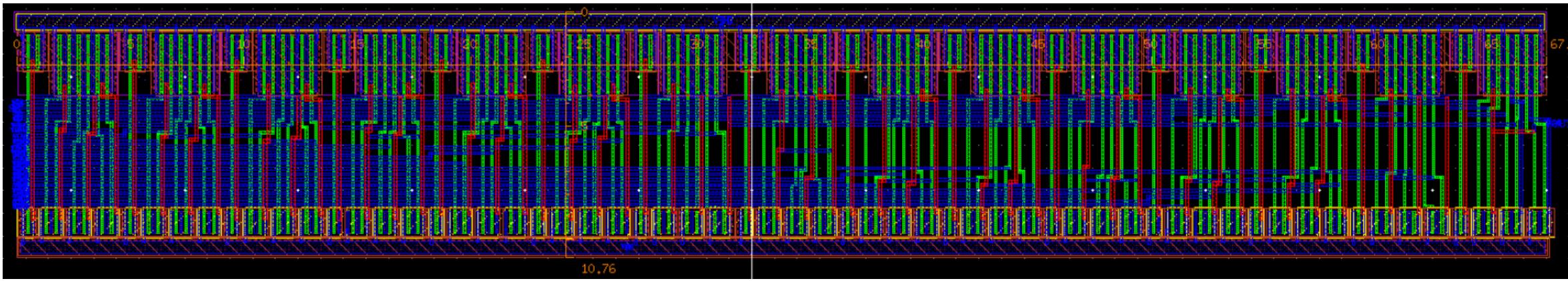
LOGIC



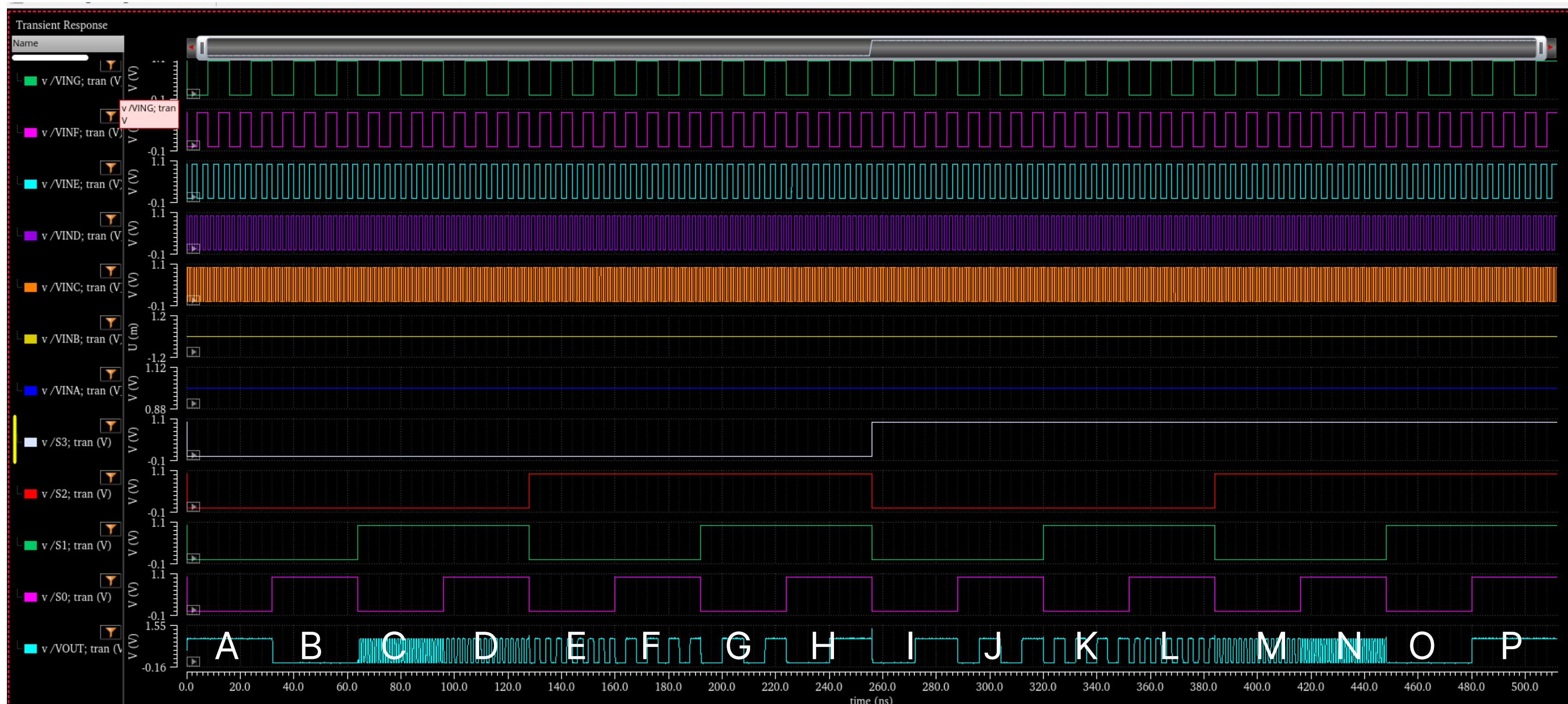
SWITCH



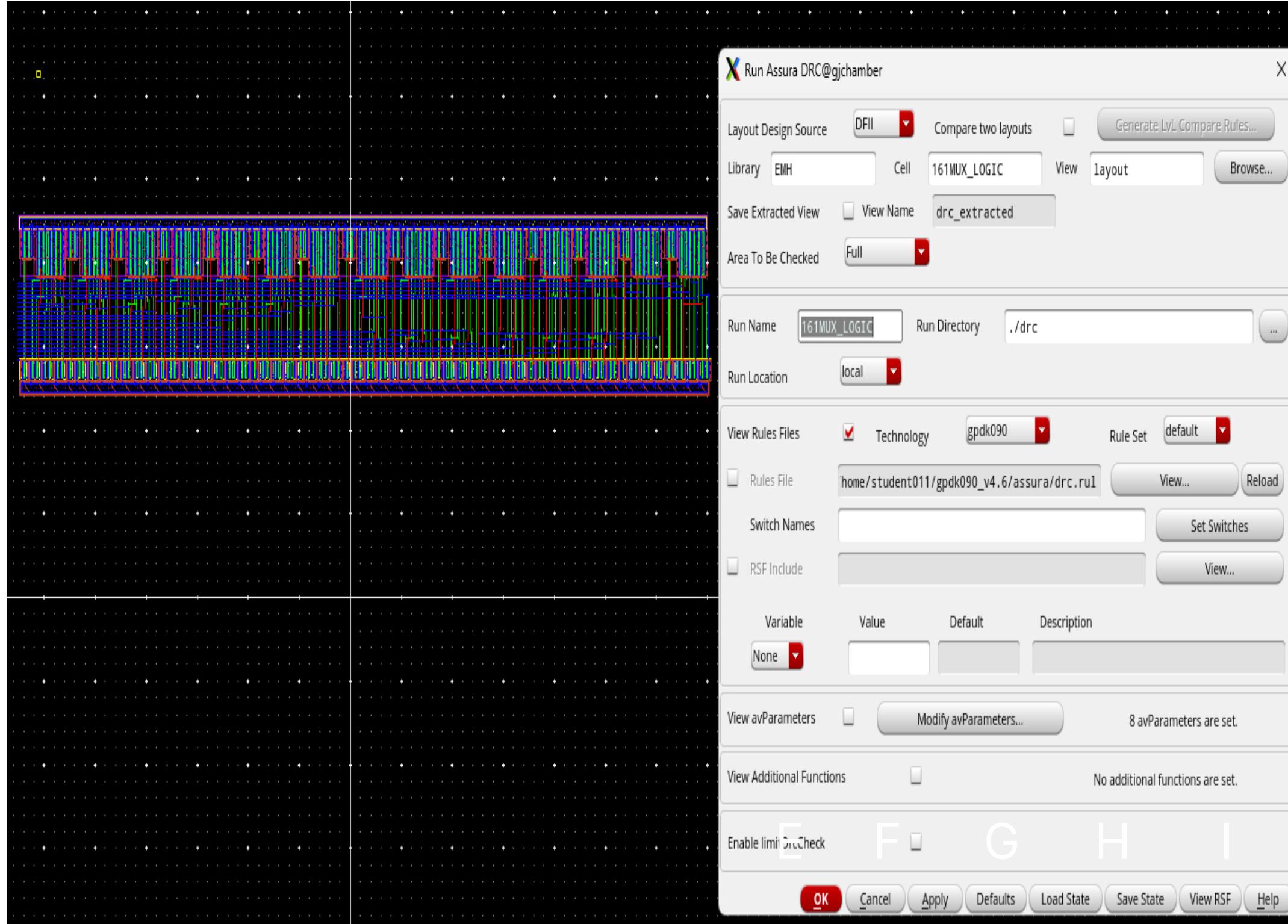
Layout



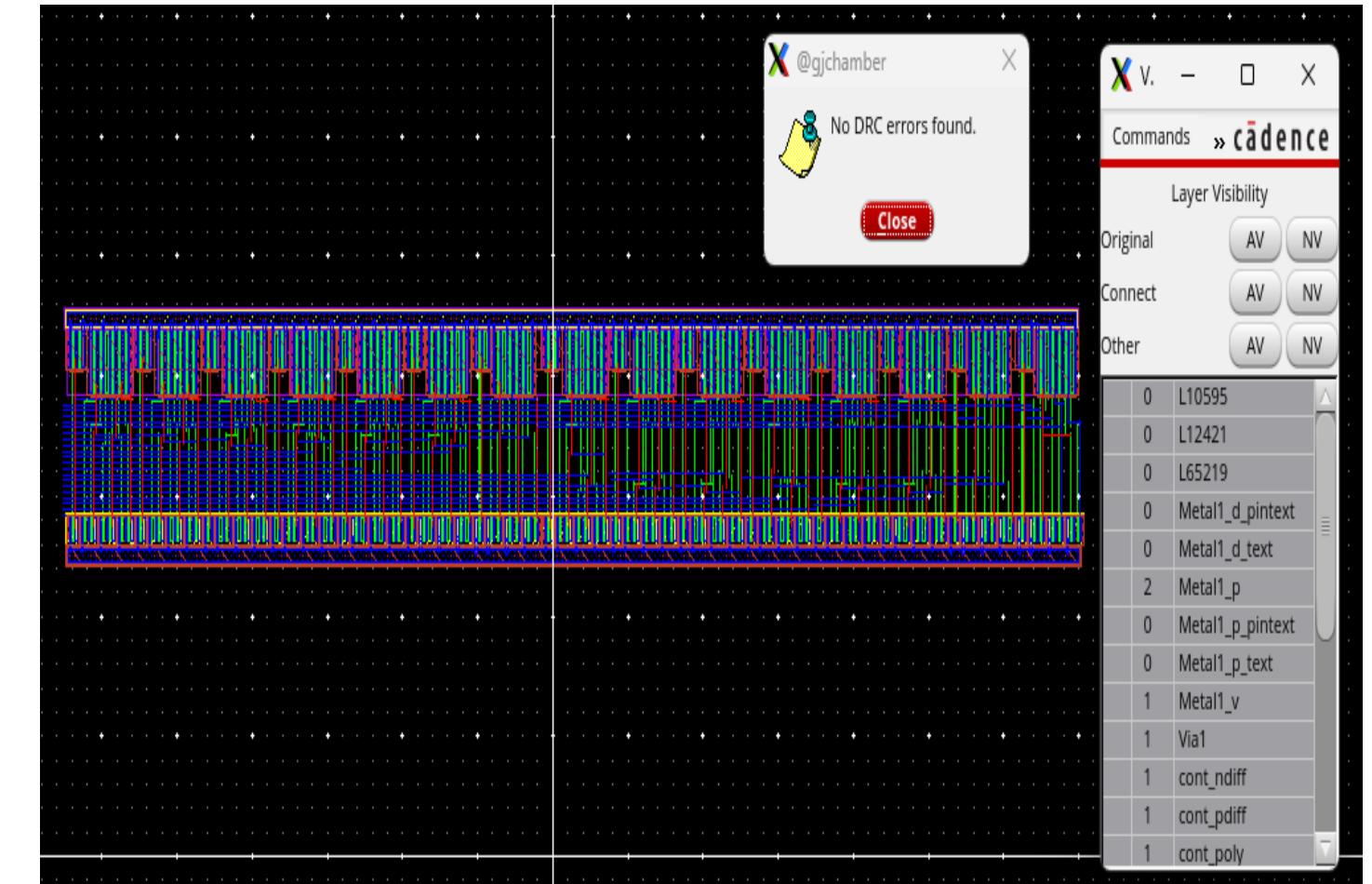
16x1 MUX (LOGIC & SWITCH)



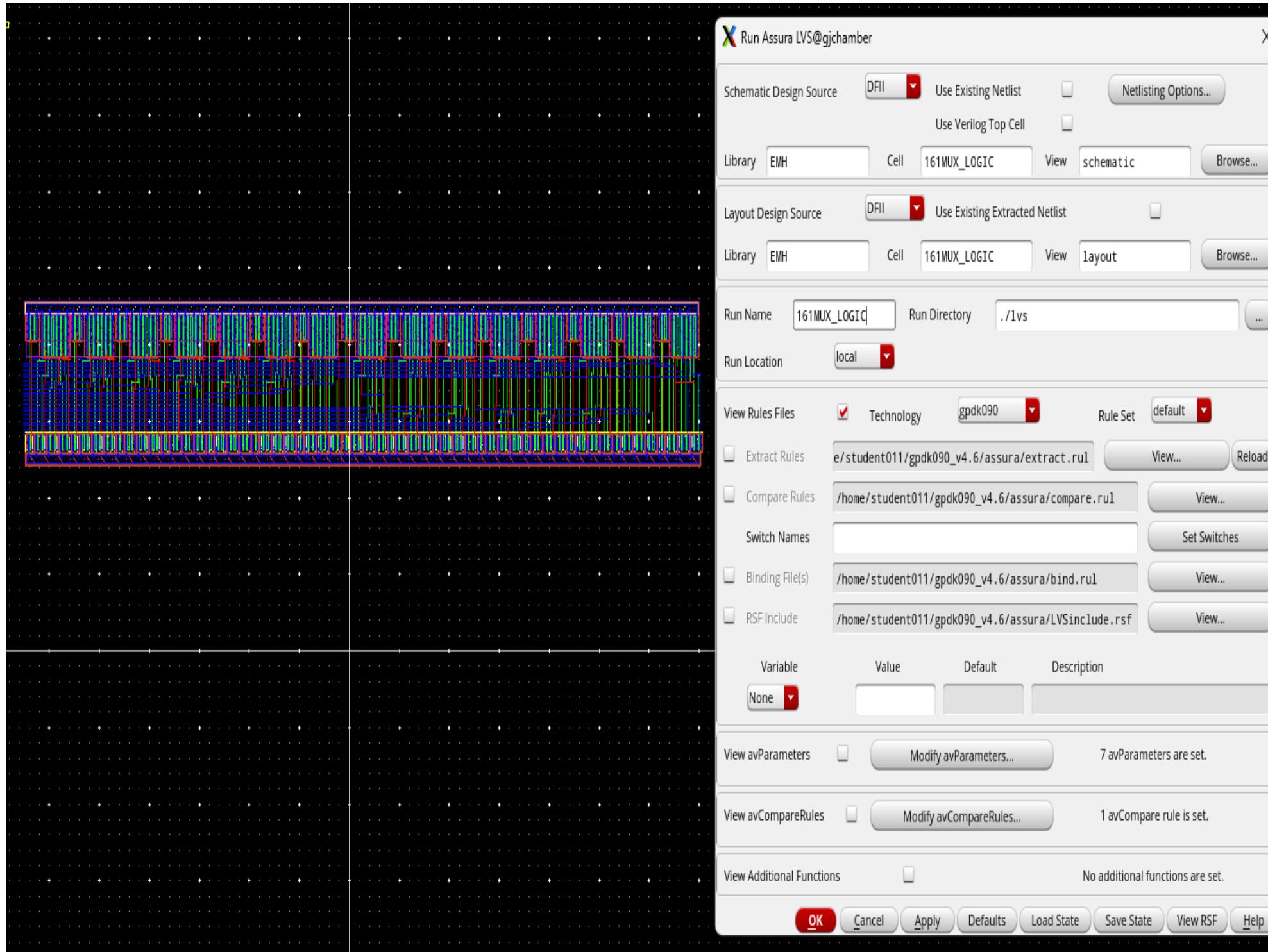
16X1 MUX (LOGIC & SWITCH)



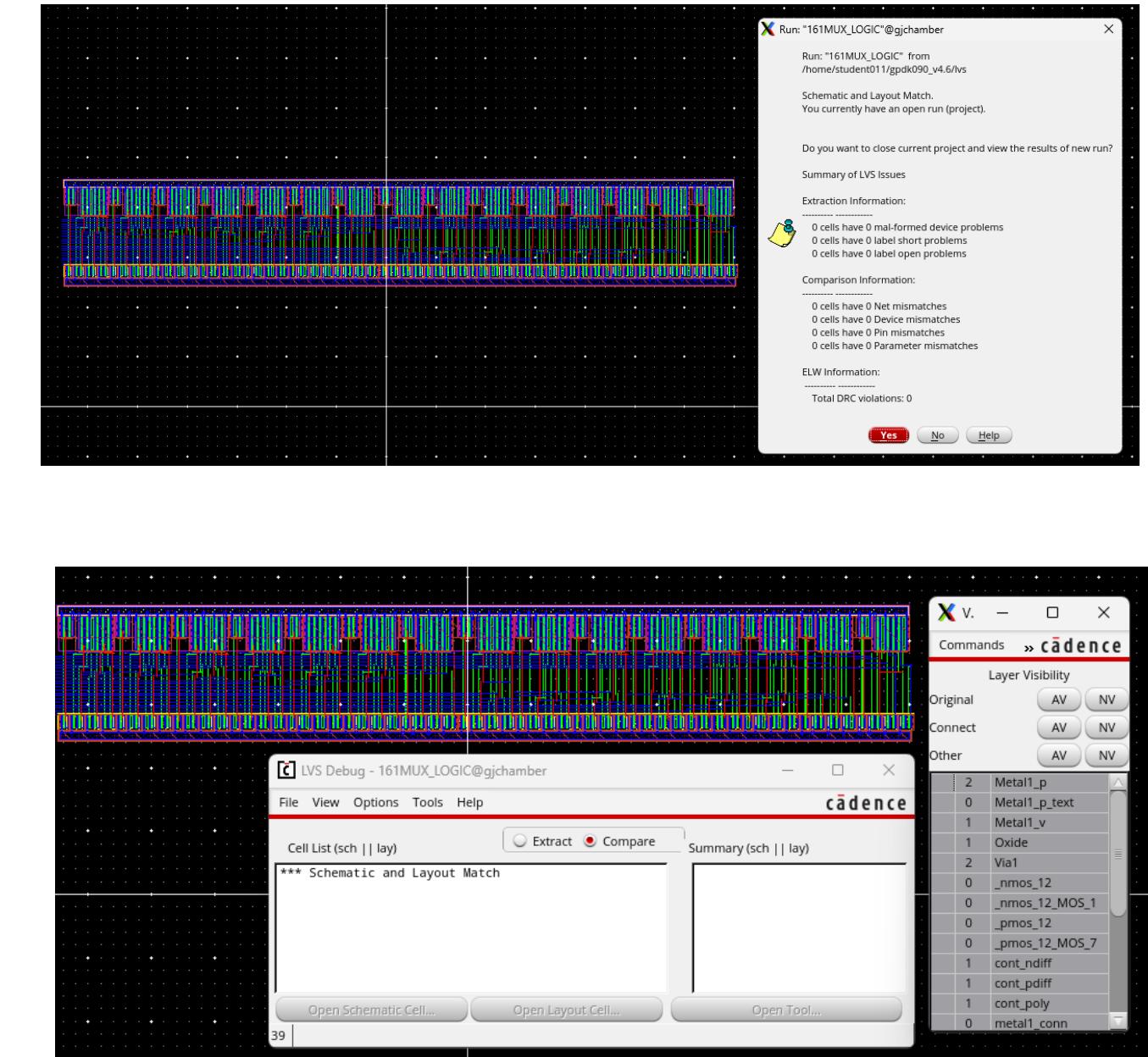
LOGIC DRC PASS



16X1 MUX (LOGIC & SWITCH)



LOGIC LVS PASS



LOGIC_MUX VS SWITCH_MUX

| Area | 2X1 MUX | 4X1 MUX | 8X1 MUX | 16X1 MUX |
|----------------------------|---------|---------|---------|----------|
| LOGIC (μm^2) | 25.06 | 99.38 | 272.10 | 725.22 |
| SWITCH (μm^2) | 18.03 | 46.13 | 116.77 | 286.34 |
| Ratio | 1.3999 | 2.15 | 2.33 | 2.53 |

| TR | 2X1 MUX | 4X1 MUX | 8X1 MUX | 16X1 MUX |
|--------|---------|---------|---------|----------|
| LOGIC | 14 | 42 | 98 | 210 |
| SWITCH | 6 | 16 | 34 | 68 |

Compared to logic-based MUX designs, transmission gate-based switch MUXes are more efficient due to their smaller area and lower transistor count.

ADDER

HALF_ADDER

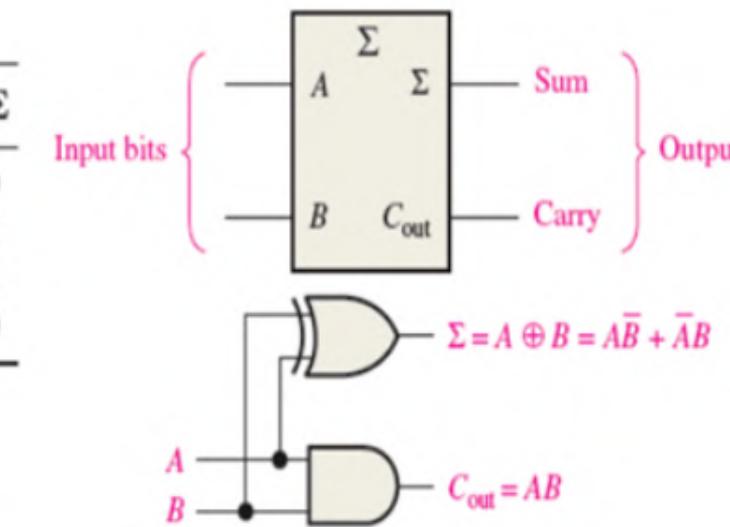
Half-adder truth table.

| A | B | C_{out} | Σ |
|---|---|-----------|----------|
| 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 0 |

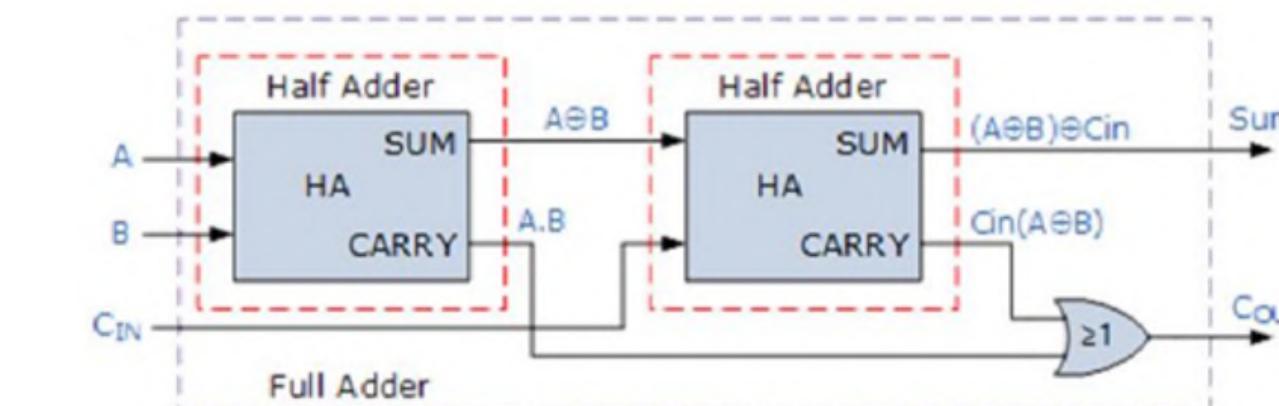
Σ = sum

C_{out} = output carry

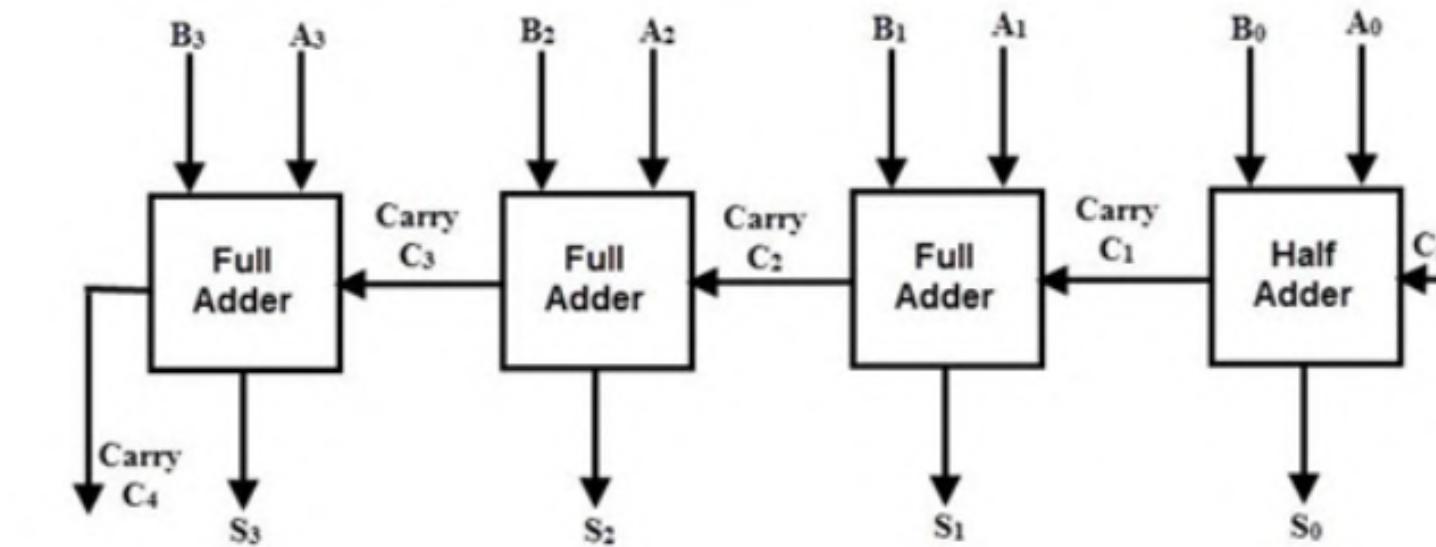
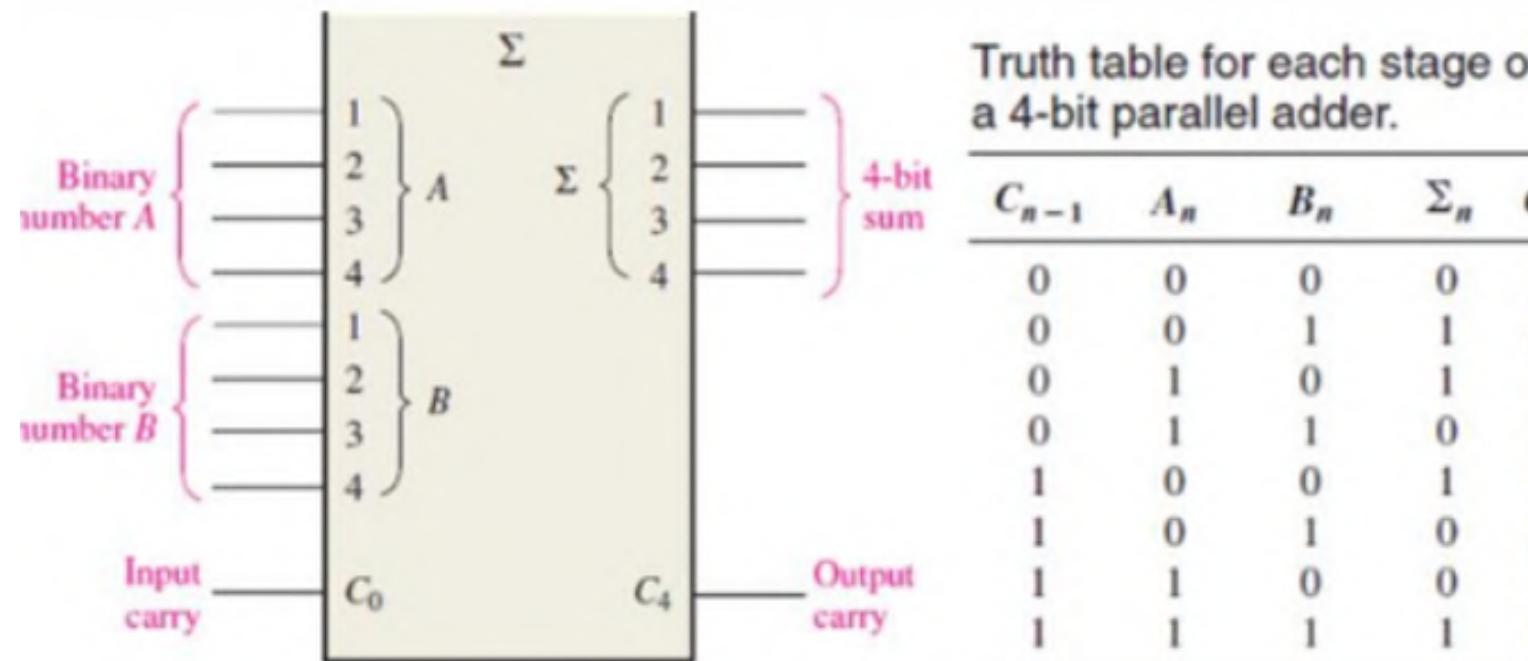
A and B = input variables (operands)



FULL_ADDER

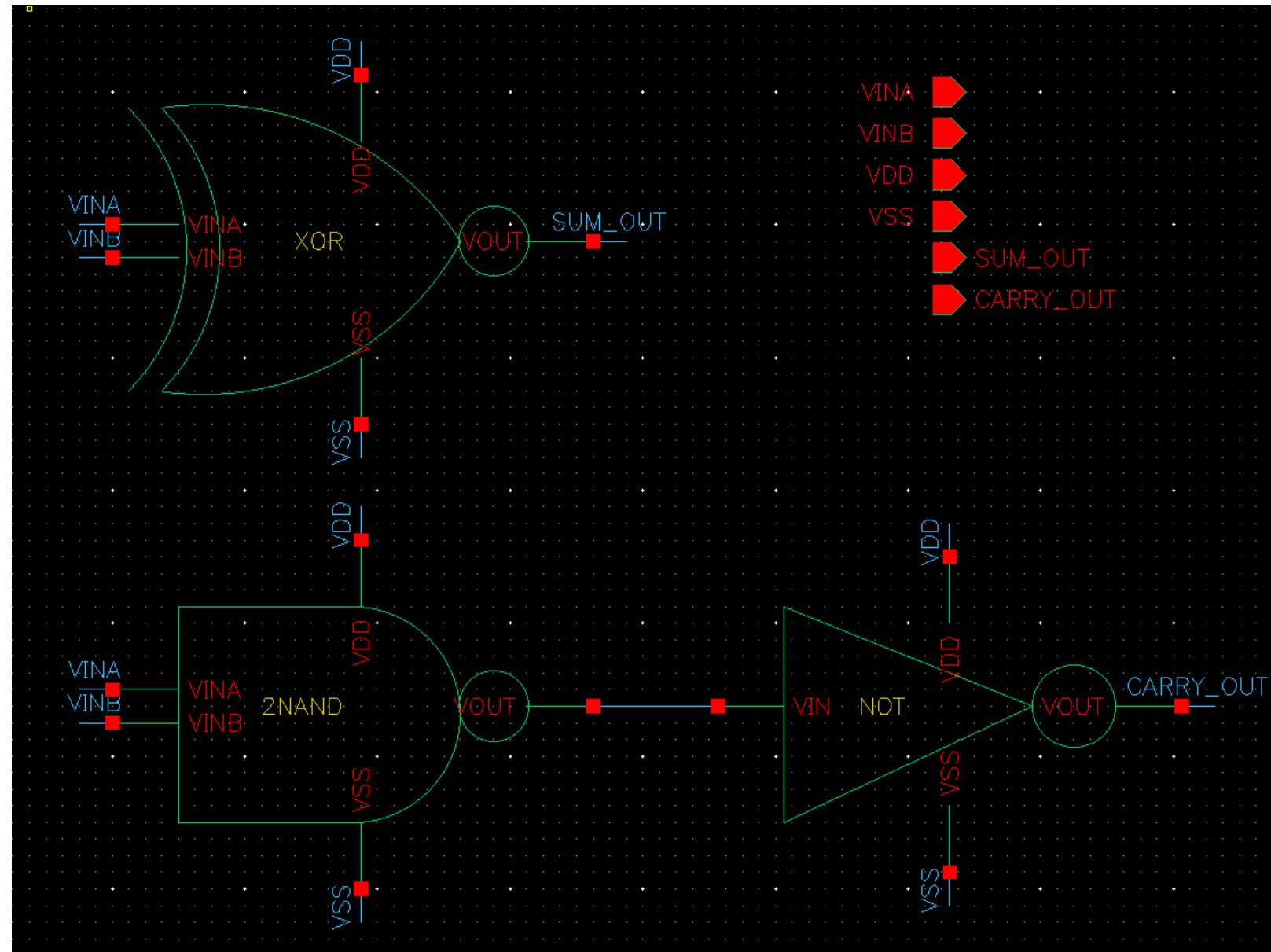


4BIT_ADDER

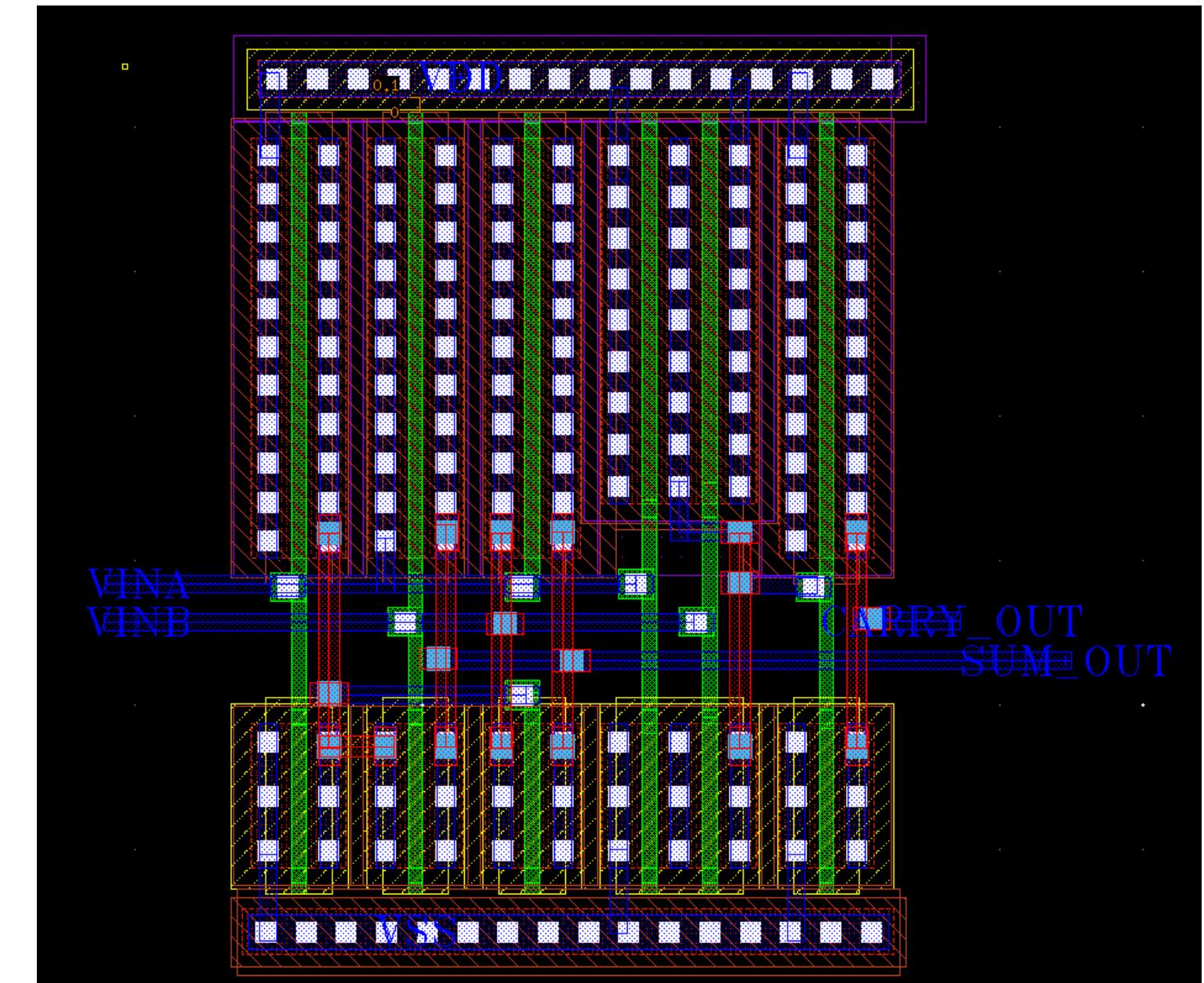


HALF_ADDER

Schematic



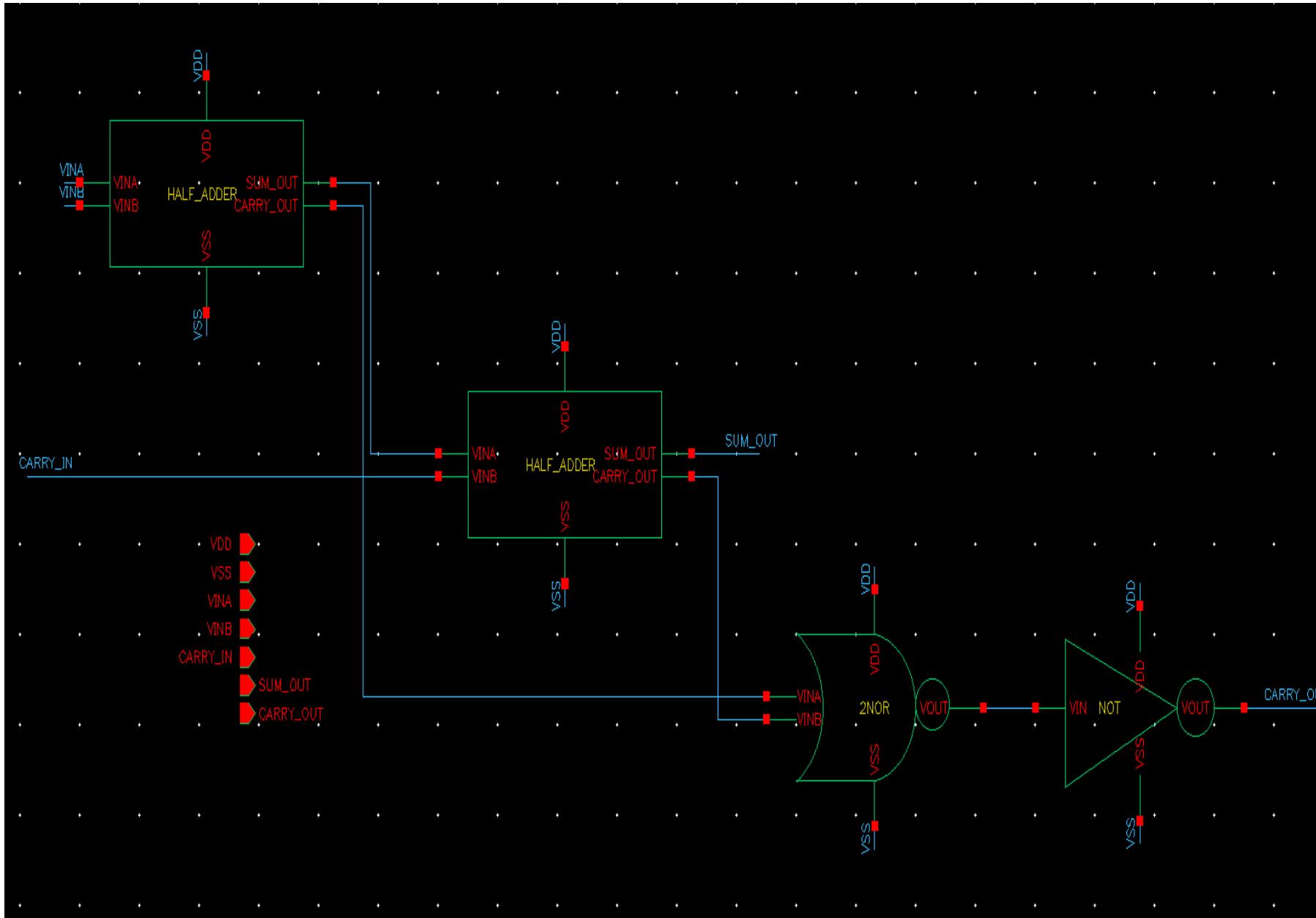
Layout



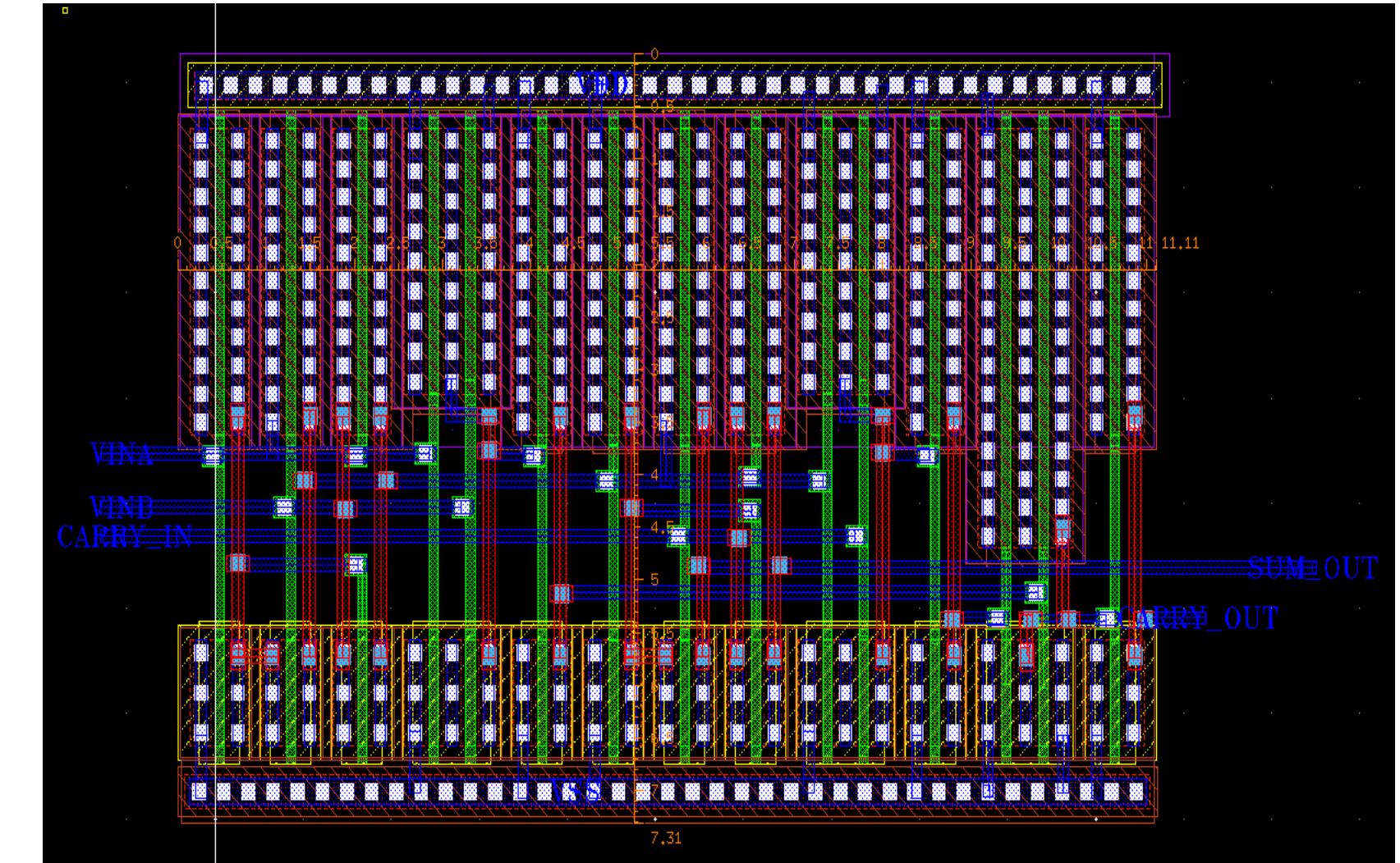
$$\text{AREA} : 4.6 * 6.51 = 29.95 \mu\text{m}^2$$

FULL_ADDER

Schematic

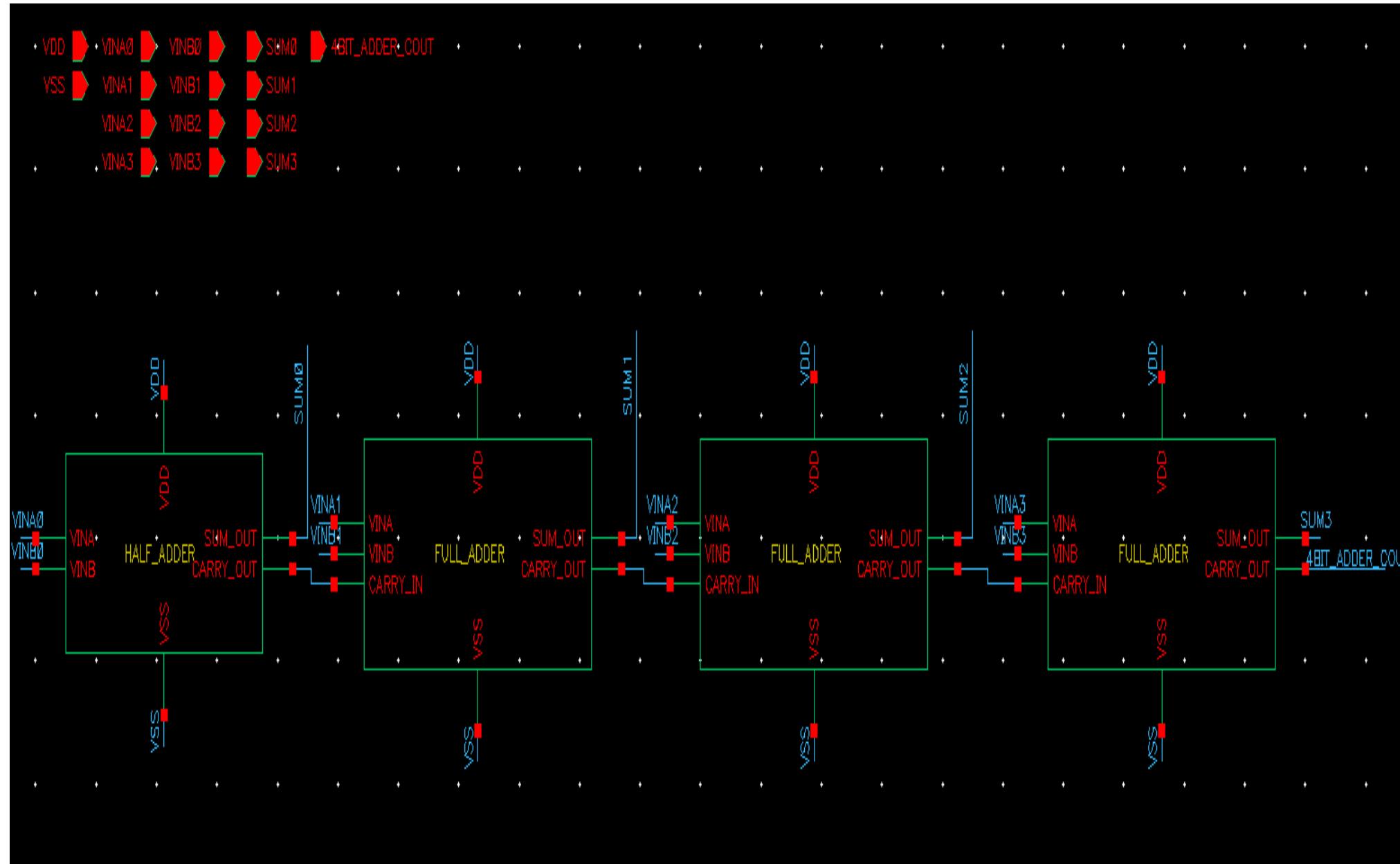


Layout



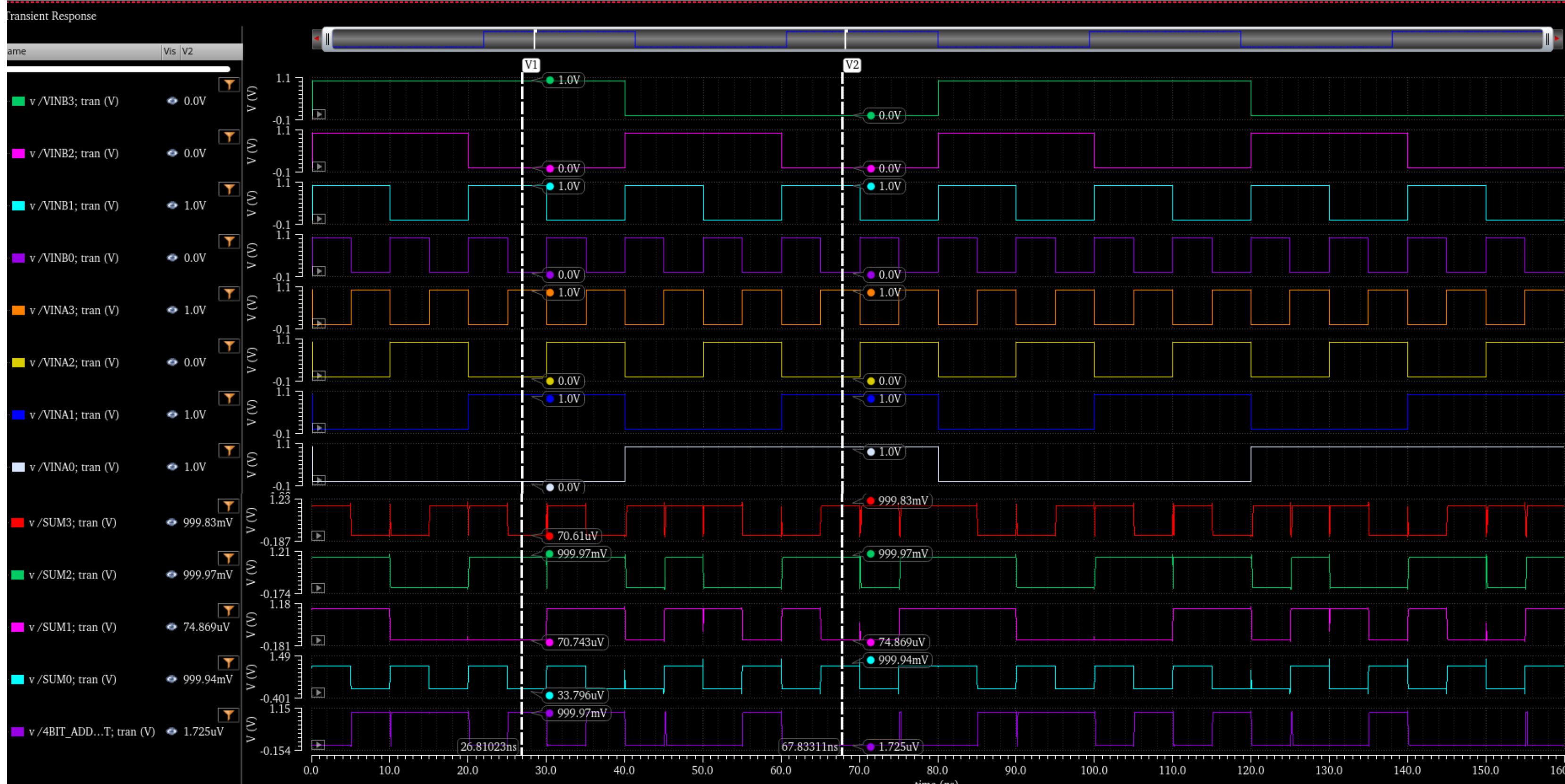
$$\text{AREA} : 11.11 * 6.31 = 82.21 \mu\text{m}^2$$

4BIT_ADDER

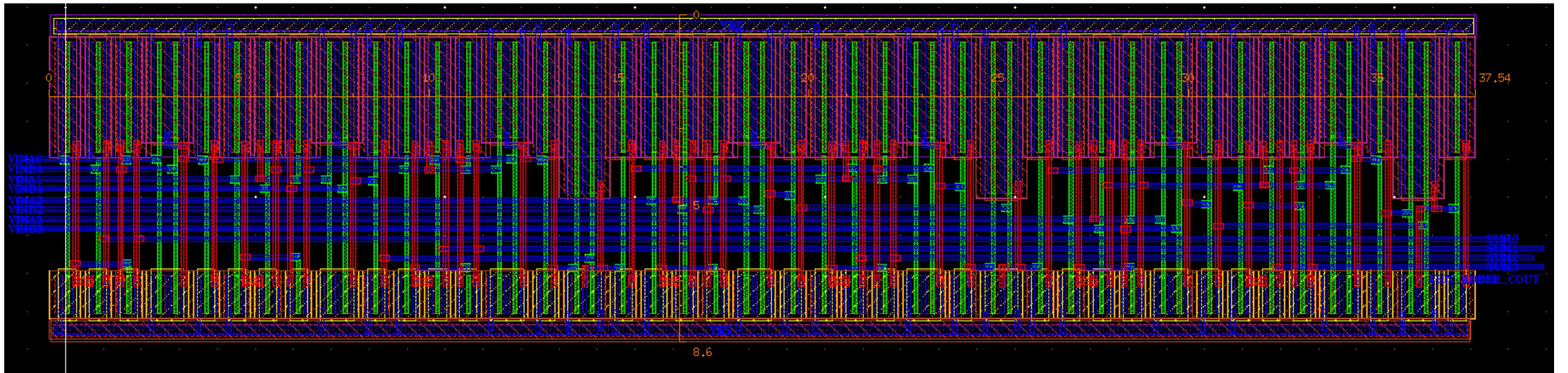


| A | | | | B | | | | Sum | | | | Carry |
|----|----|----|----|----|----|----|----|-----|----|----|----|-------|
| A3 | A2 | A1 | A0 | B3 | B2 | B1 | B0 | S3 | S2 | S1 | S0 | Cout |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 |
| 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 0 |
| 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 0 | 0 |
| 0 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 |
| 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 1 |
| 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 1 |
| 1 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 1 |
| 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 1 |
| 1 | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 |
| 1 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 |

4BIT_ADDER_Simulation

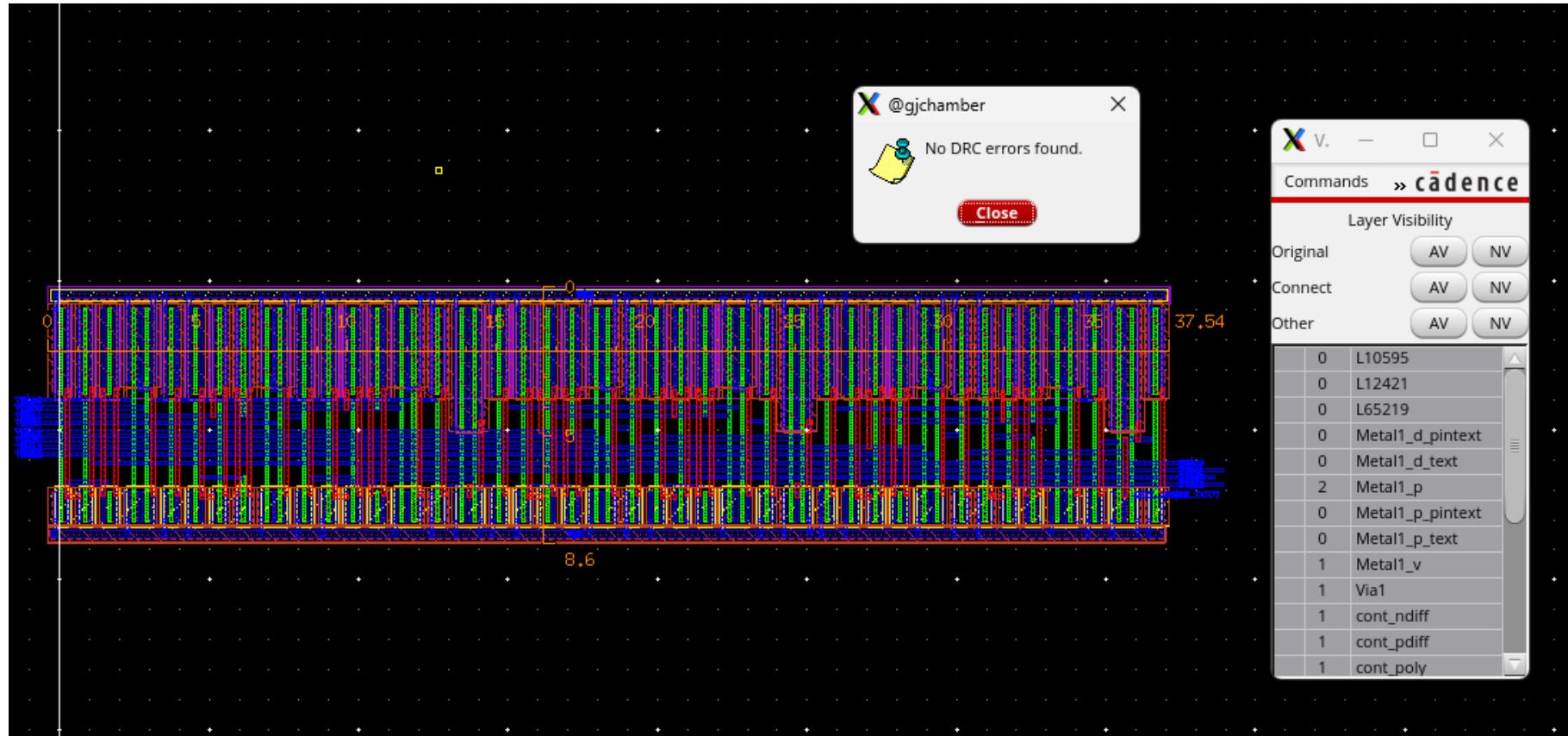


4BIT_ADDER LAYOUT

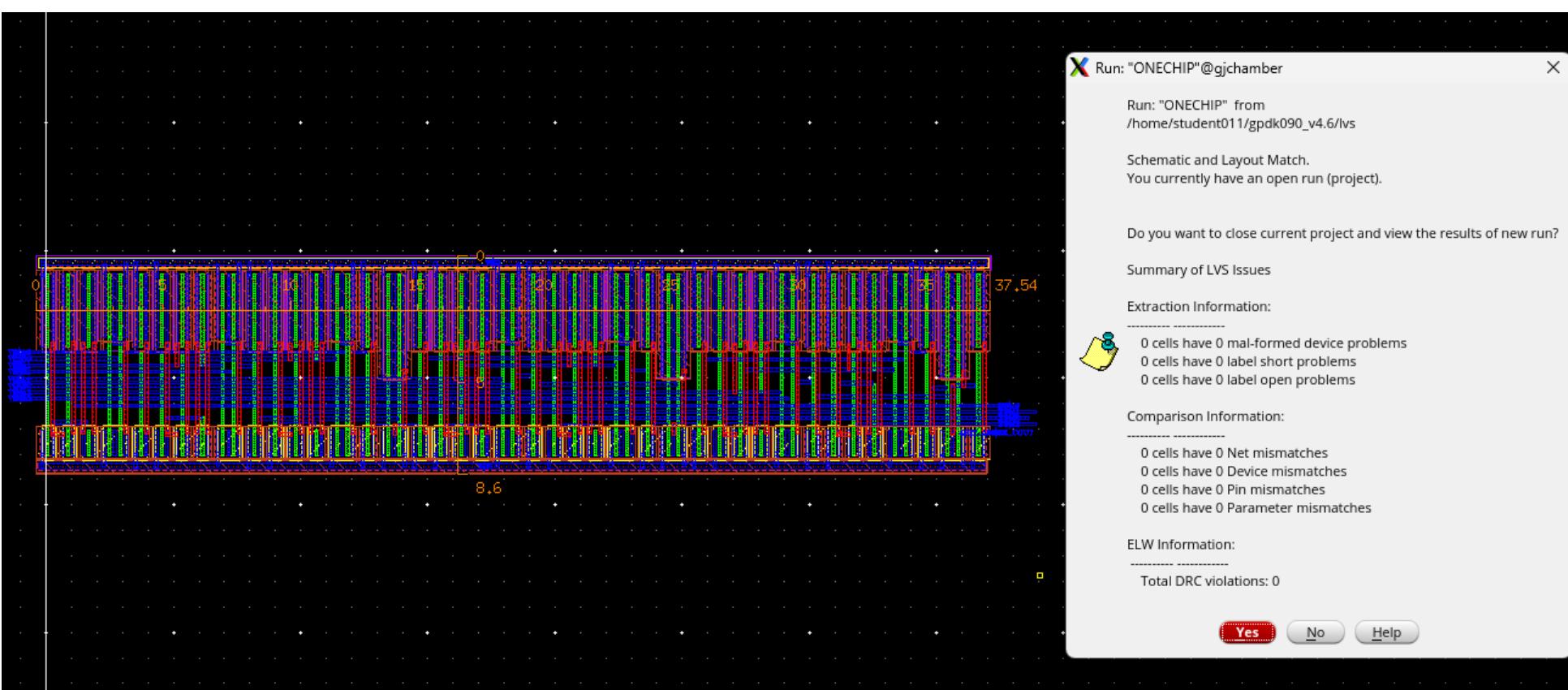


AREA : $37.54 * 8.6 = 322.84 \mu\text{m}^2$

4BIT_ADDER

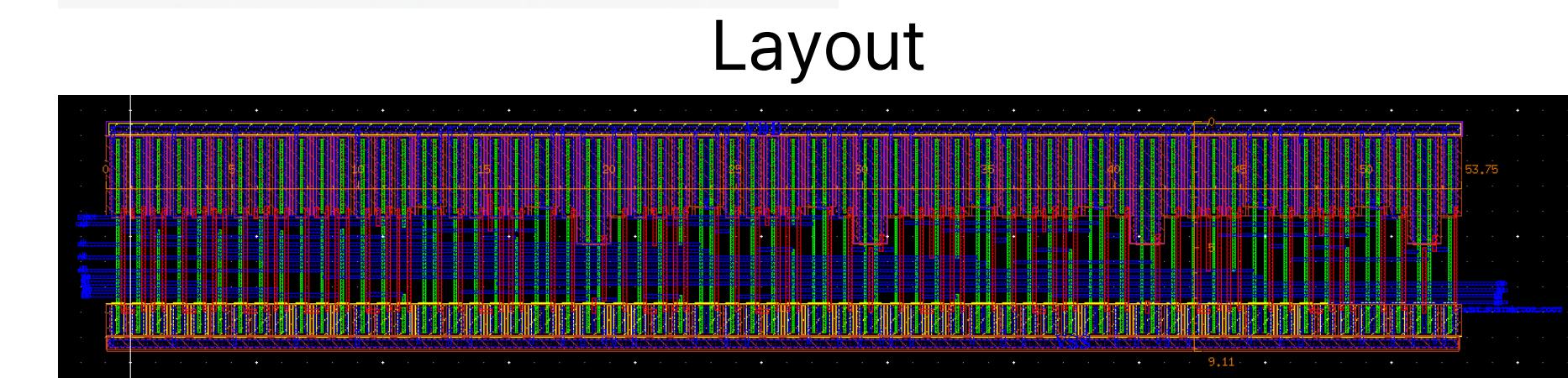
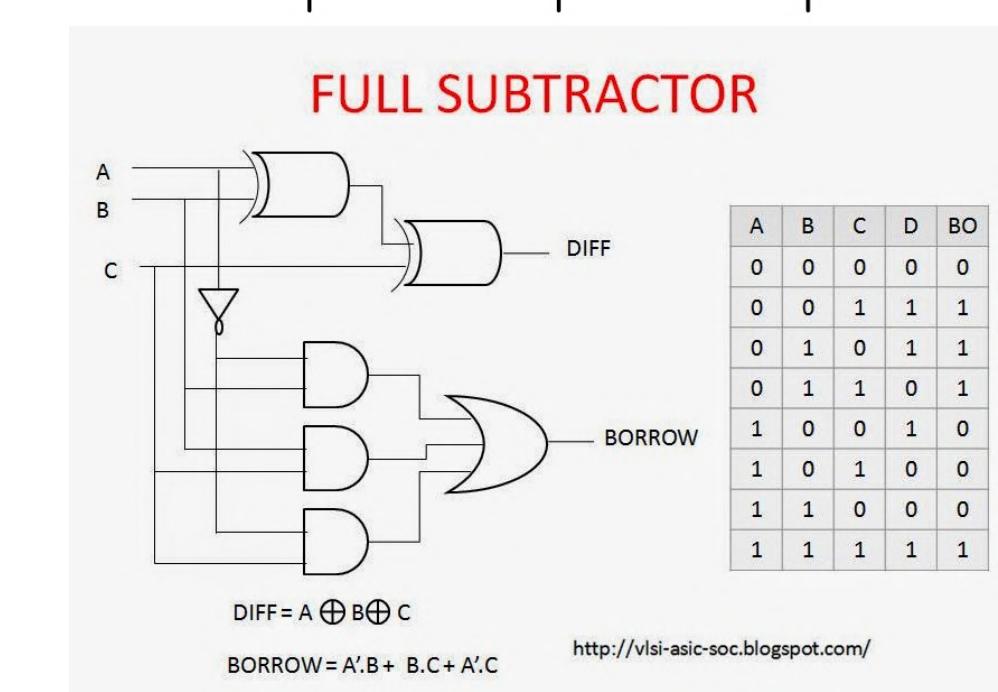
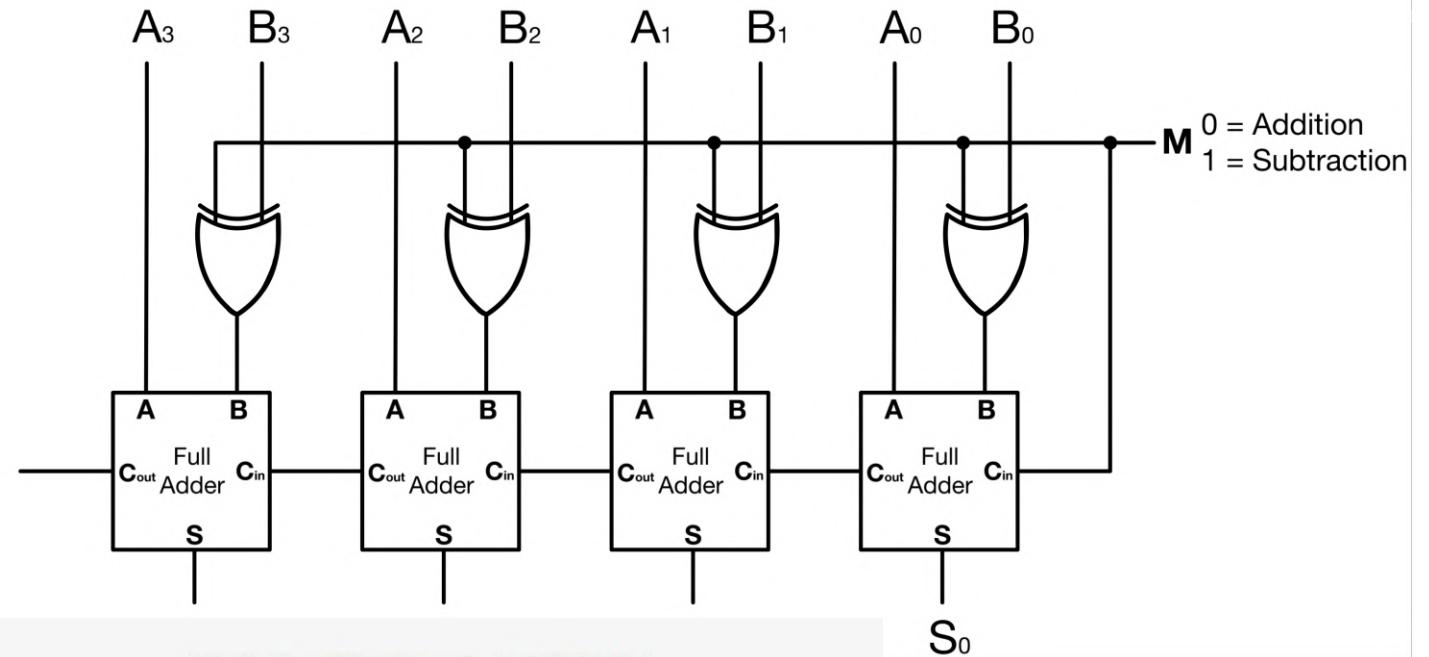
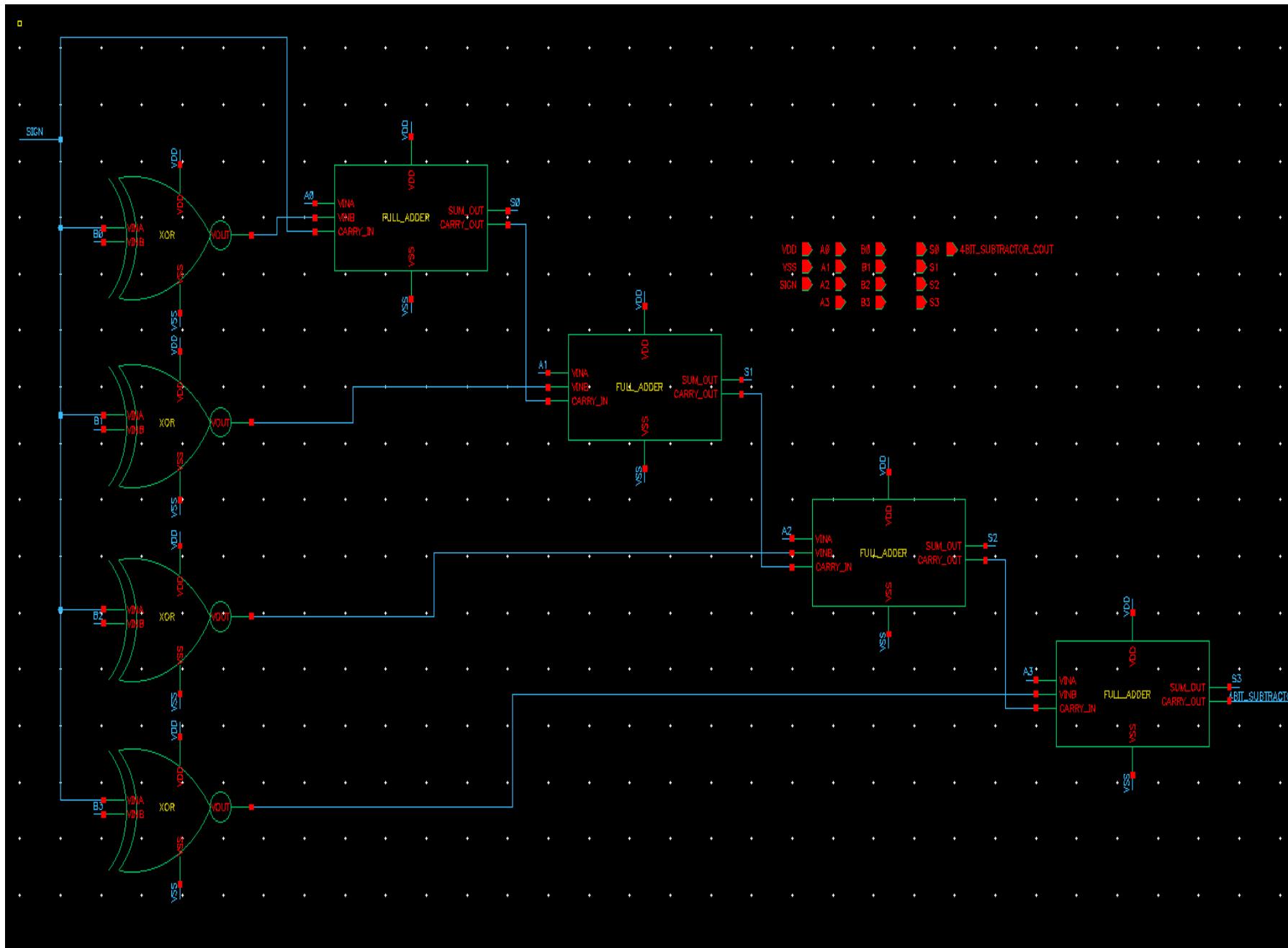


DRC / LVS
PASS



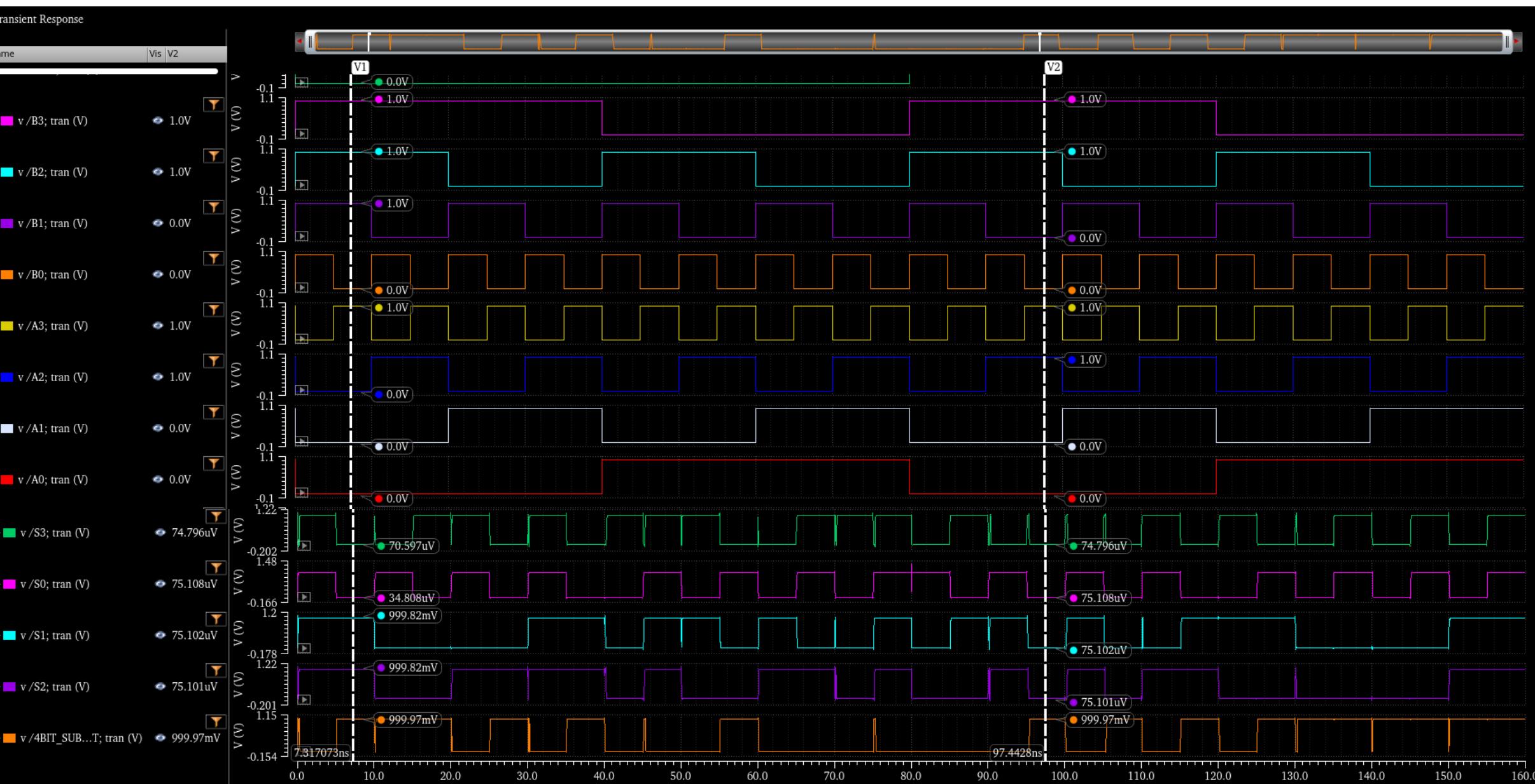
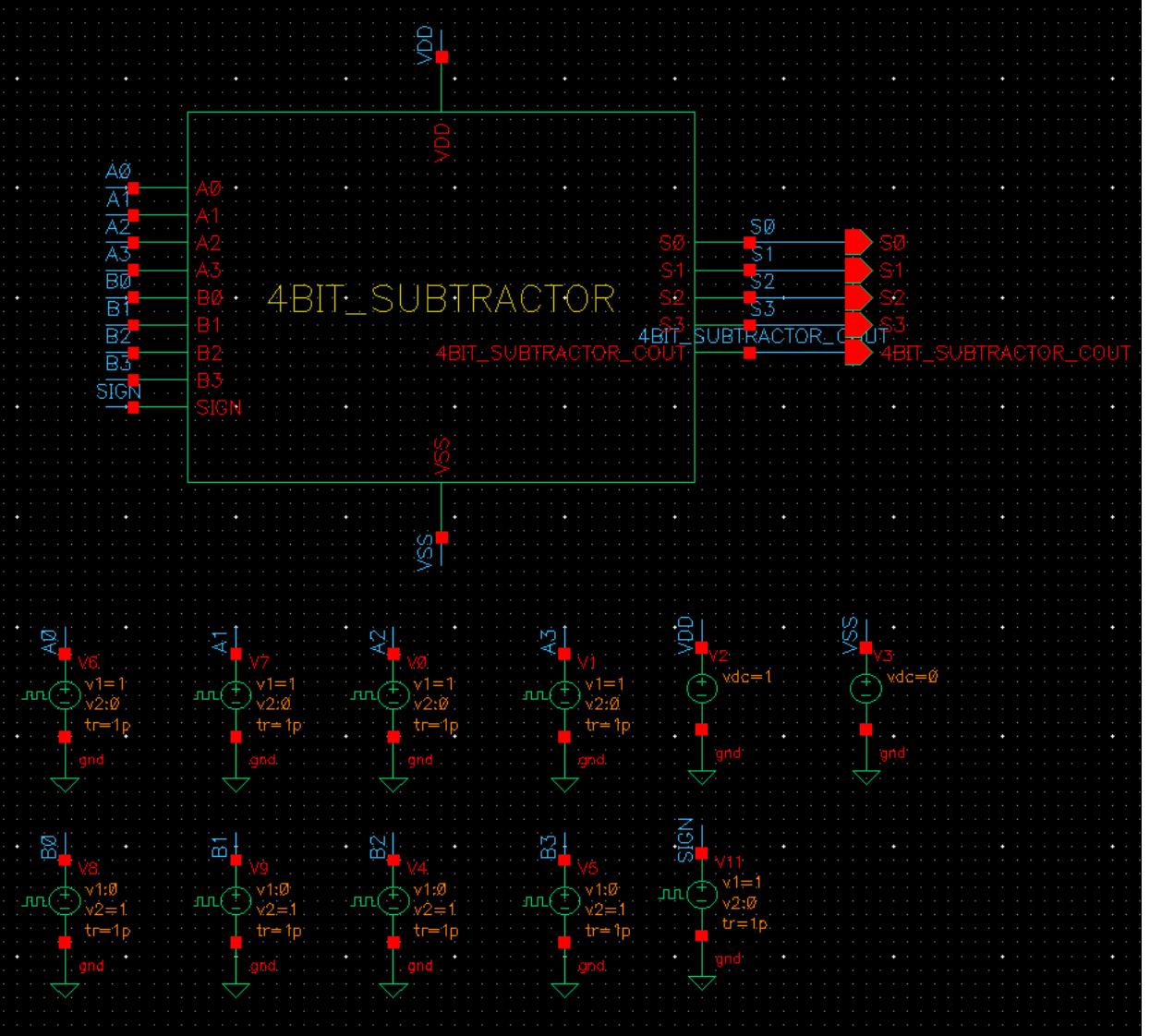
4BIT_SUBTRACTOR

Schematic



AREA : $53.75 * 9.11 = 489.11 \mu\text{m}^2$

4BIT_SUBTRACTOR



ANALOG CIRCUIT

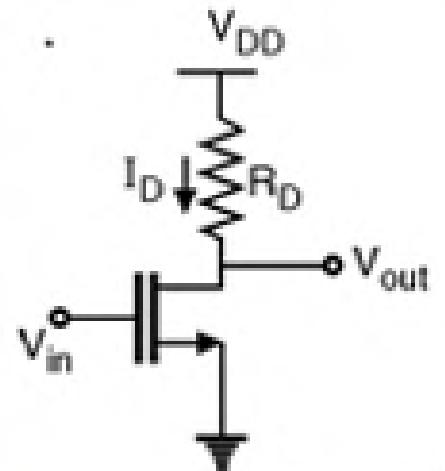
- Common Source Amp / Differential Amp (Single-ended Output)

ANALOG CIRCUIT SPEC

| | Res | Nmos0 | Nmos1 | Nmos2 | Nmos3 | Pmos0 | Pmos1 |
|----------|-----|-------|-------|-------|-------|-------|-------|
| CS_A,p | 4k | 1um | X | X | X | X | X |
| Diff_Amp | 25k | 2um | 2um | 800nm | 800nm | 250nm | 250nm |

| | gm | Gain (Av) | Bandwidth | Power Consumption |
|----------|-----------------|------------|--------------|-------------------|
| CS_Amp | ~754.59[uA/V] | 6.334[dB] | 3.04[GHz] | 123.153[uW] |
| Diff_Amp | ~189.955[uA/ V] | 13.448[dB] | 262.271[MHz] | 43.469[uW] |

COMMON SOURCE AMP



CS stage with resistive load

$$I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{TH})^2$$

$$\text{i.e. } I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{in} - V_{TH})^2$$

But by KVL,

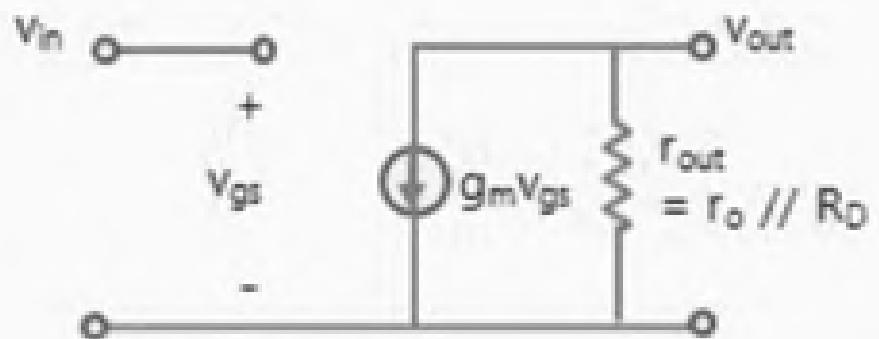
$$V_{DD} - I_D R_D = V_{out}$$

$$\therefore V_{out} = V_{DD} - \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{in} - V_{TH})^2 R_D$$

Differentiating this equation with respect to V_{in}

$$\frac{dV_{out}}{dV_{in}} = -\mu_n C_{ox} \frac{W}{L} (V_{in} - V_{TH}) R_D$$

$$\text{Hence, The voltage gain } A_v = -g_m R_D \quad \left[\because g_m = \mu_n C_{ox} \frac{W}{L} (V_{in} - V_{TH}) \right]$$



$$V_{in} = V_{gs}$$

$$V_{out} = -g_m V_{gs} r_{out}$$

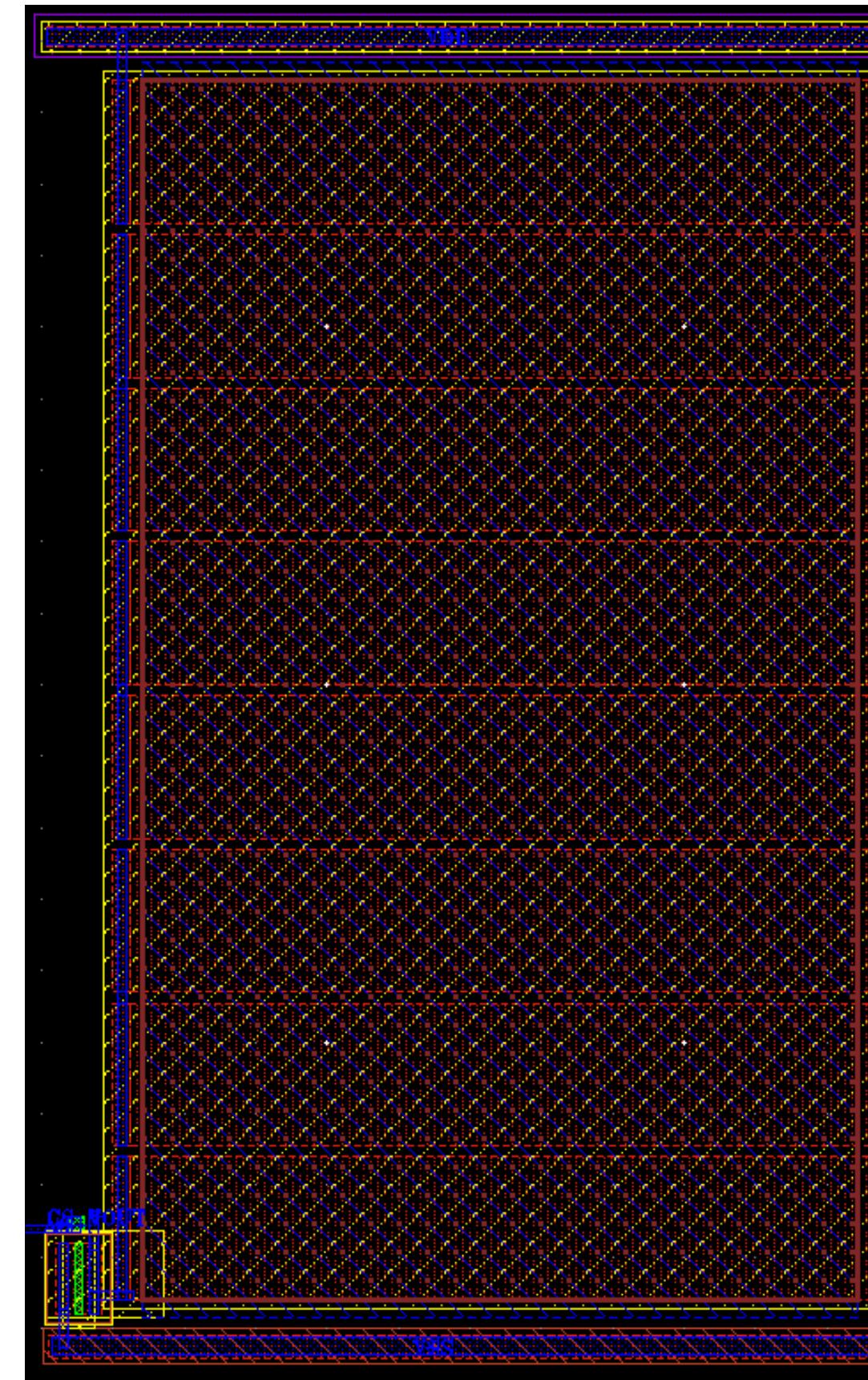
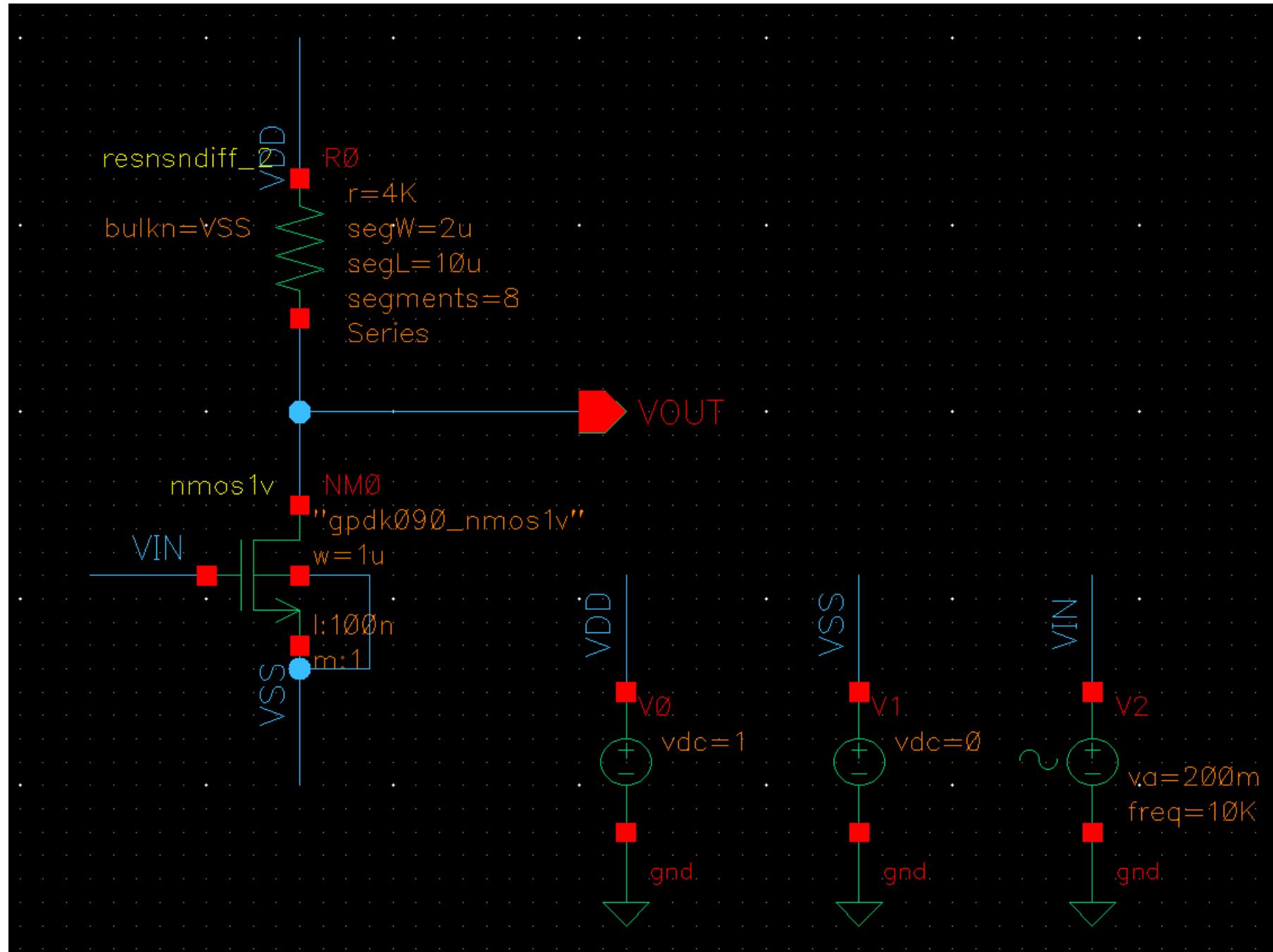
$$\frac{V_{out}}{V_{in}} = -g_m r_{out} \quad \text{Gain}$$

common-source amplifier is one of three basic single-stage field-effect transistor (FET) amplifier topologies, typically used as a voltage or transconductance amplifier.

COMMON SOURCE AMP

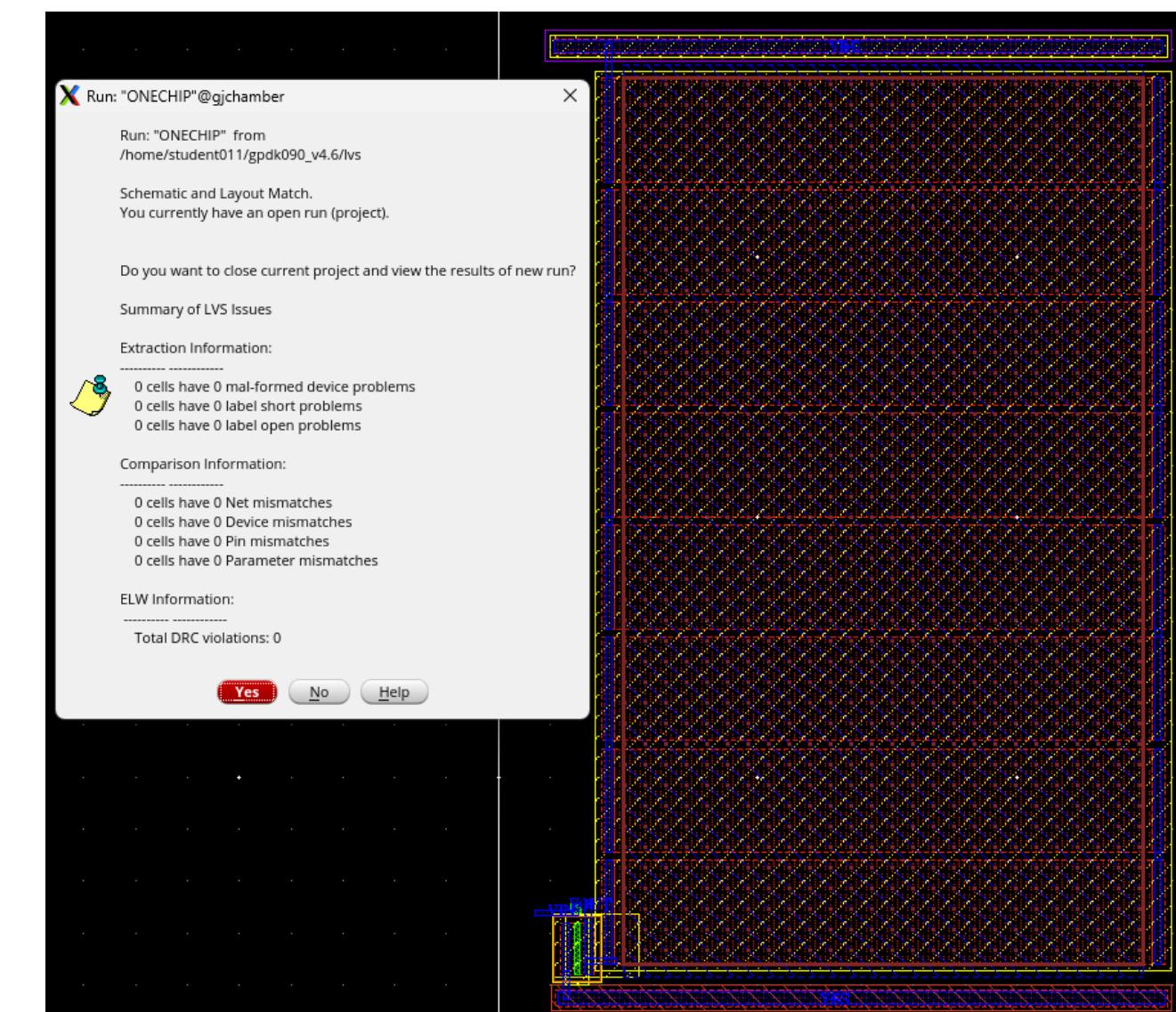
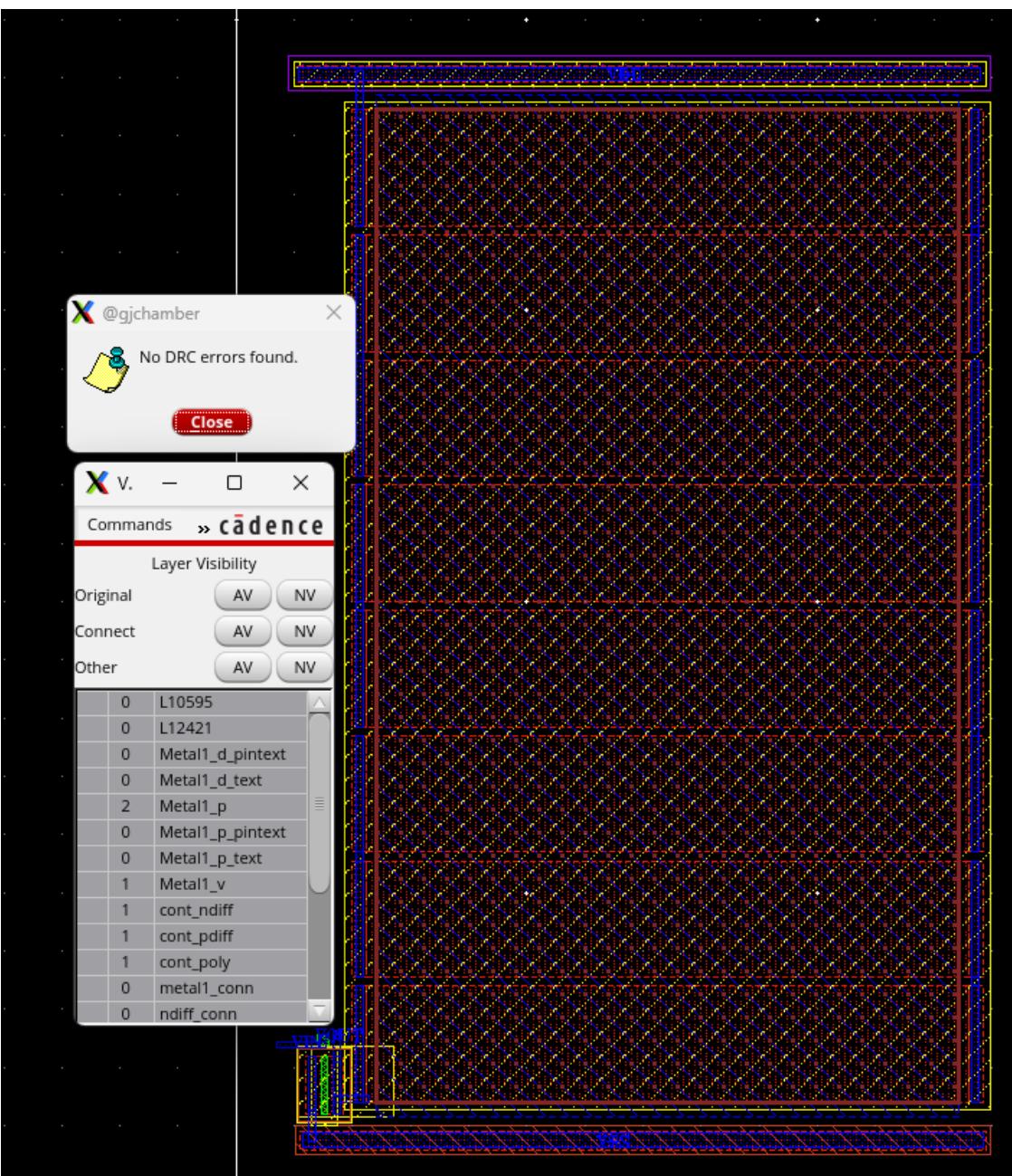
Layout

Schematic

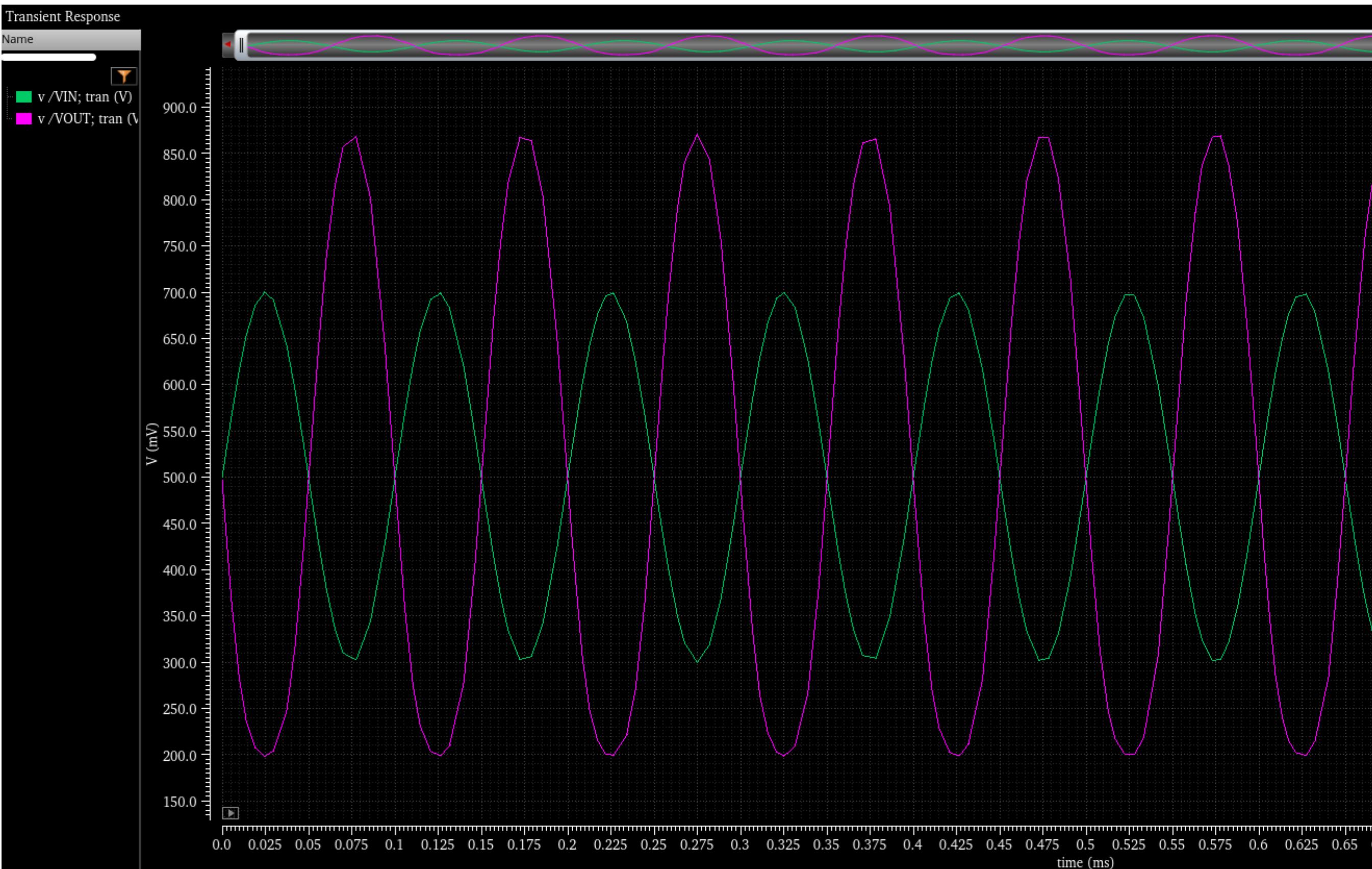


COMMON SOURCE AMP

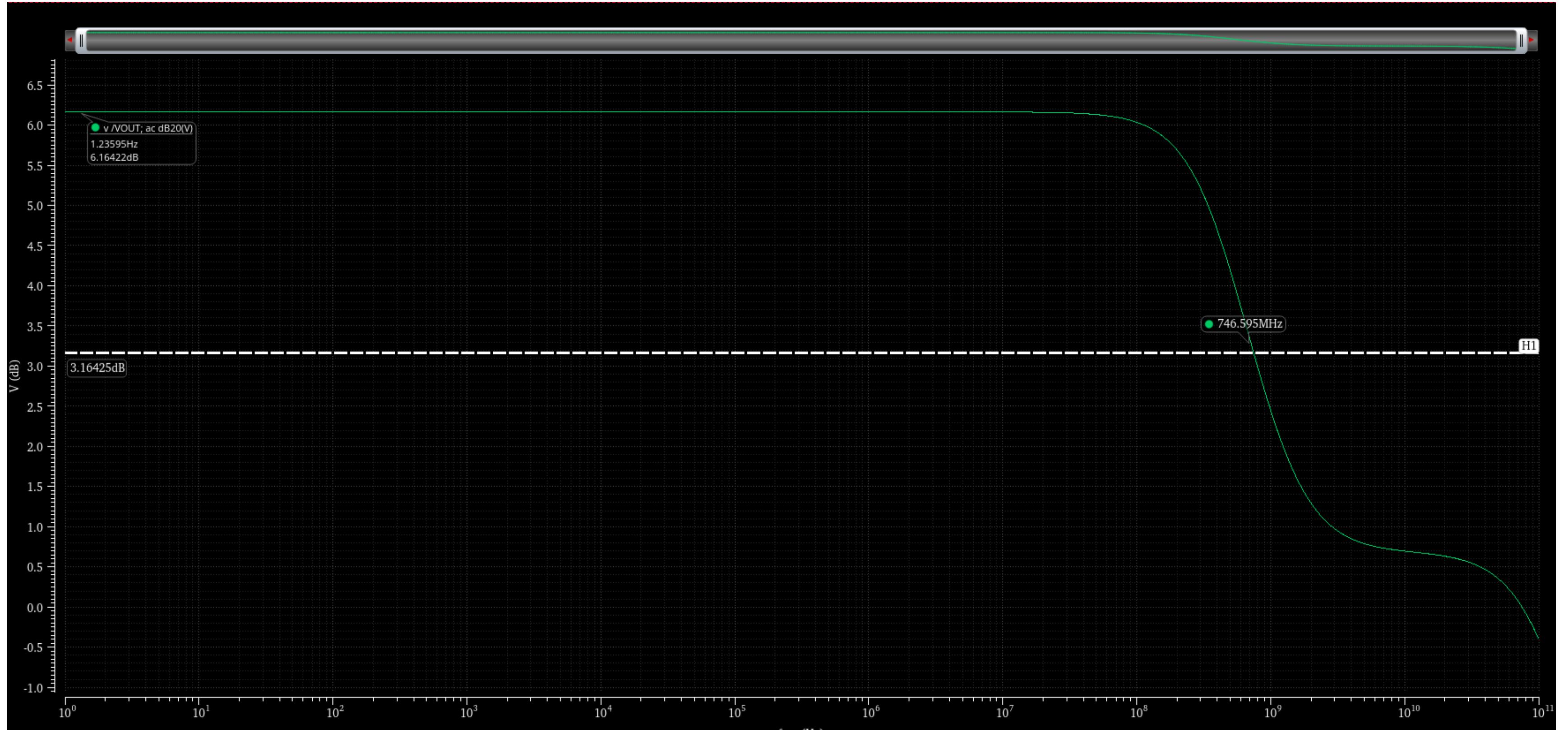
DRC / LVS PASS



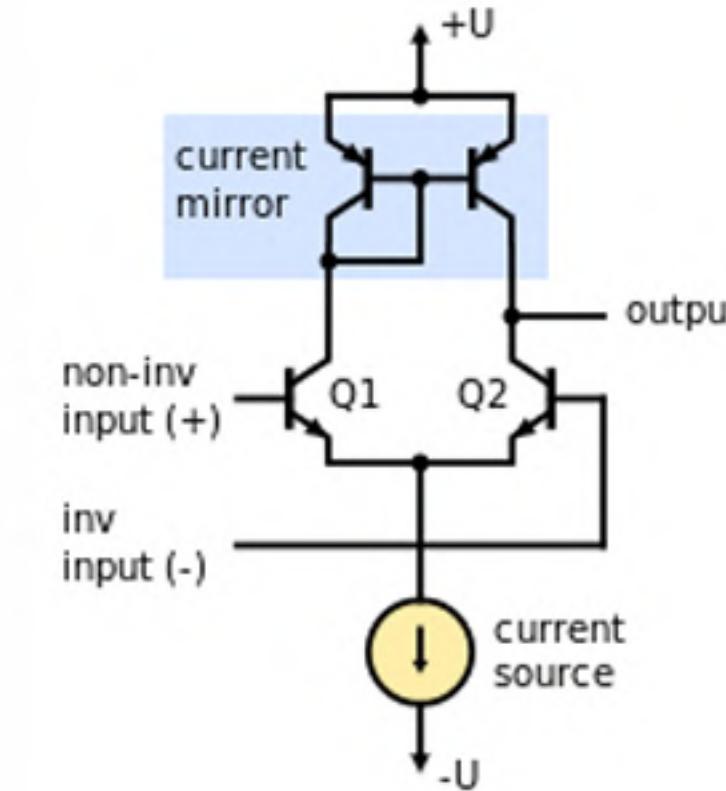
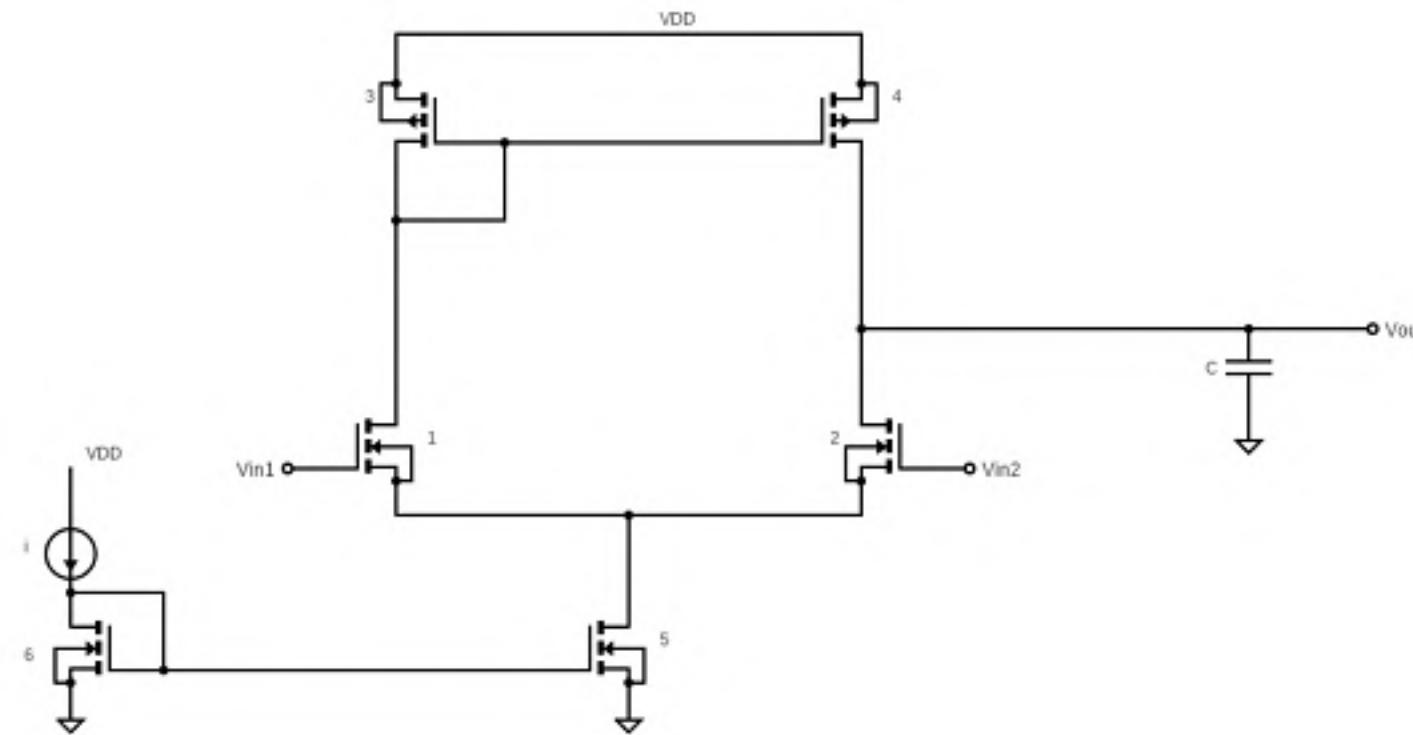
COMMON SOURCE AMP _ Simulation



COMMON SOURCE AMP_ Simulation



DIFFERENTIAL AMP

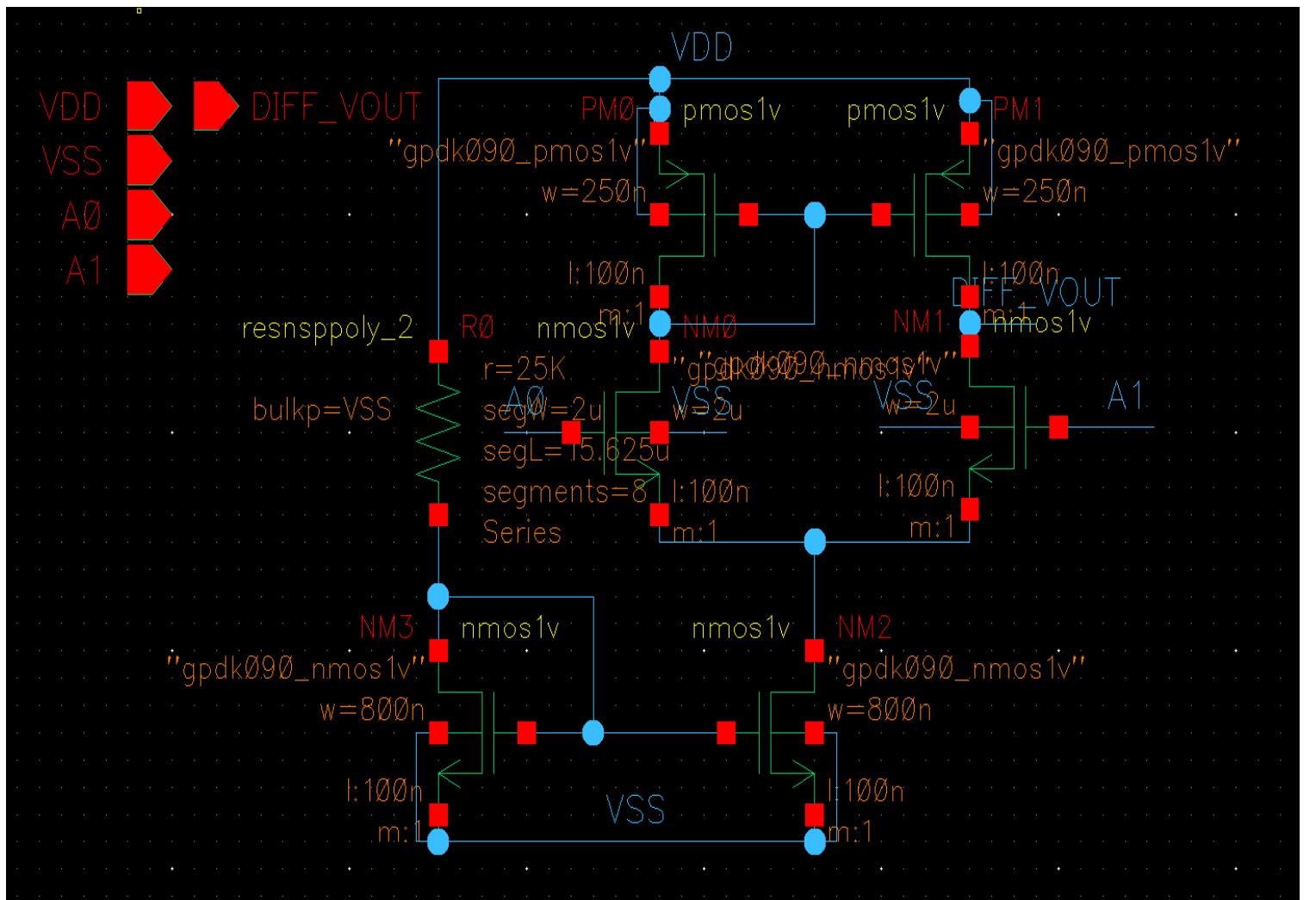


If the differential output is not desired, then only one output can be used (taken from just one of the collectors (or anodes or drains), disregarding the other output; this configuration is referred to as *single-ended output*.

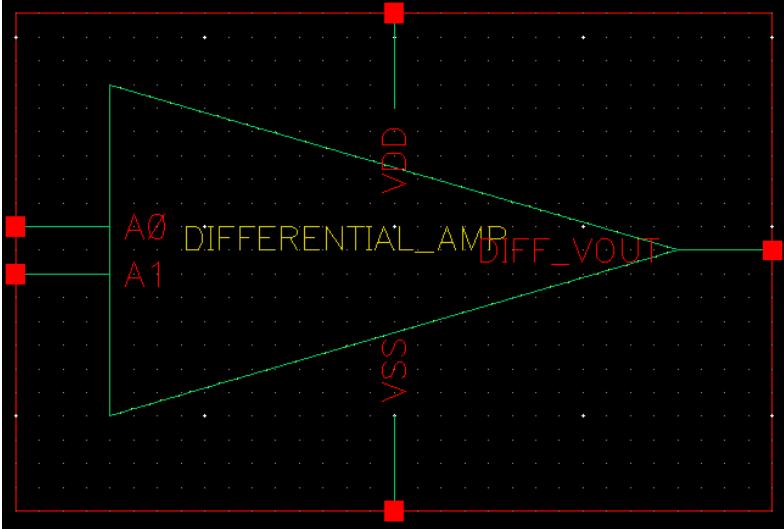
The gain is half that of the stage with differential output.

DIFFERENTIAL AMP

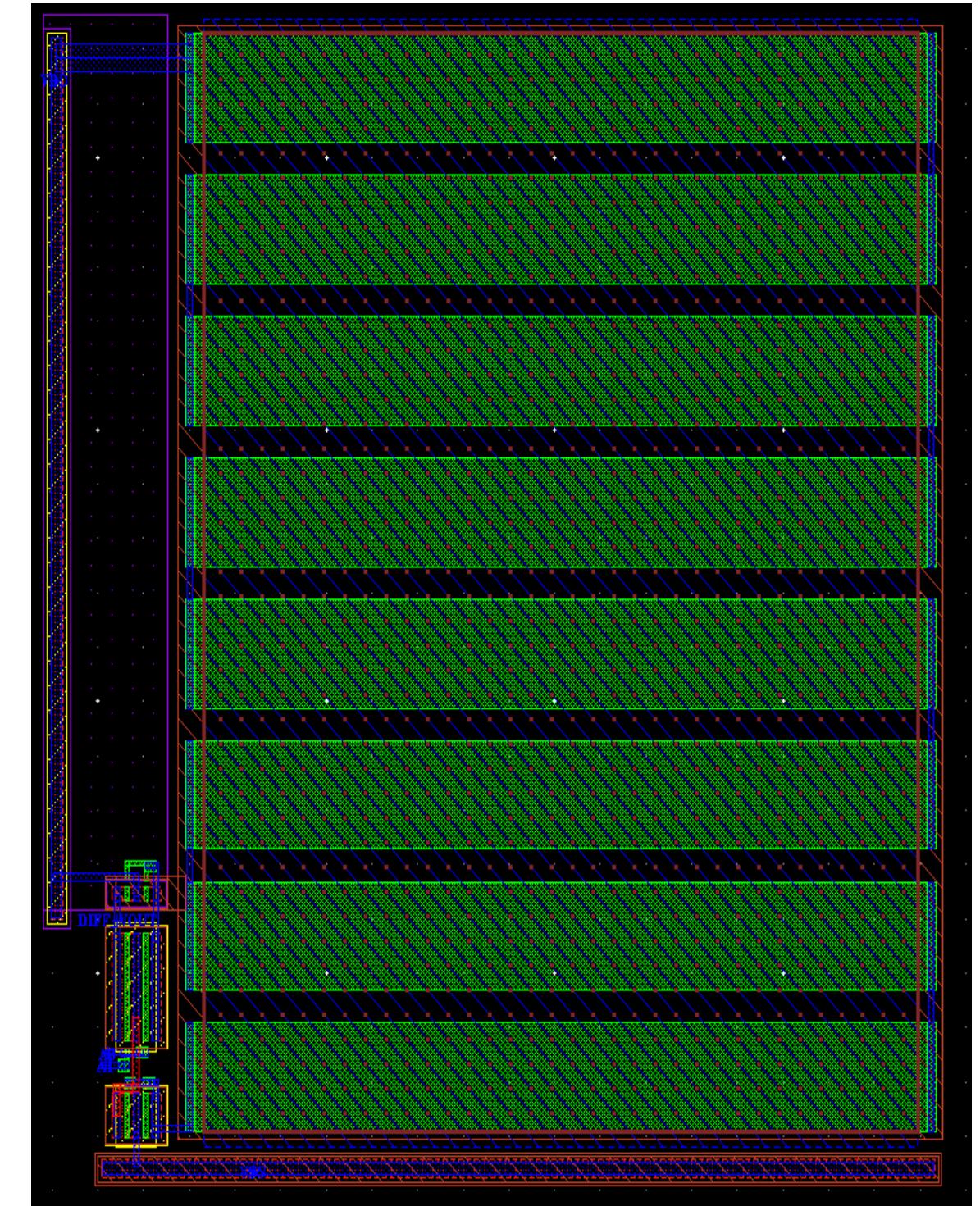
Schematic



Symbol

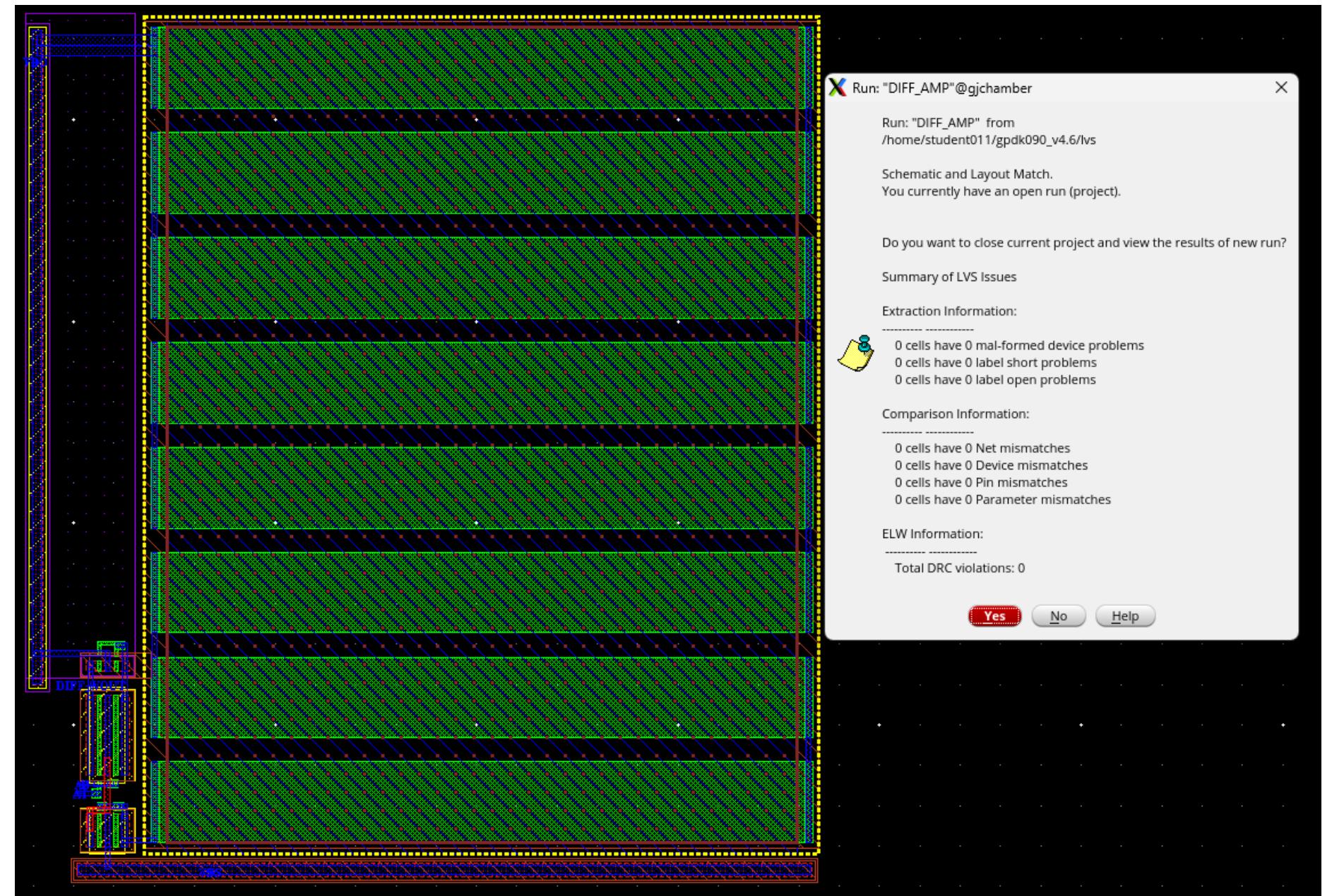
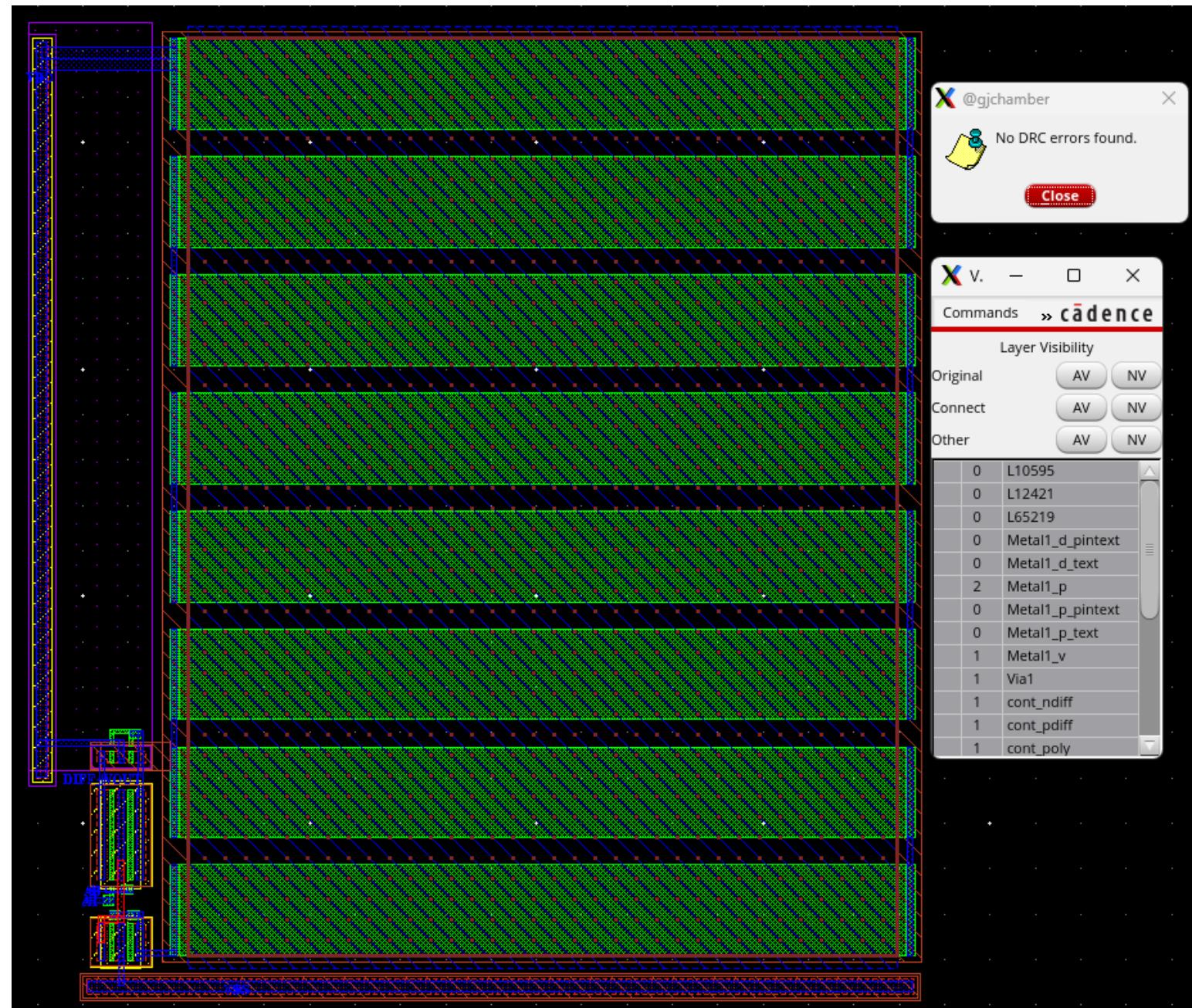


Layout



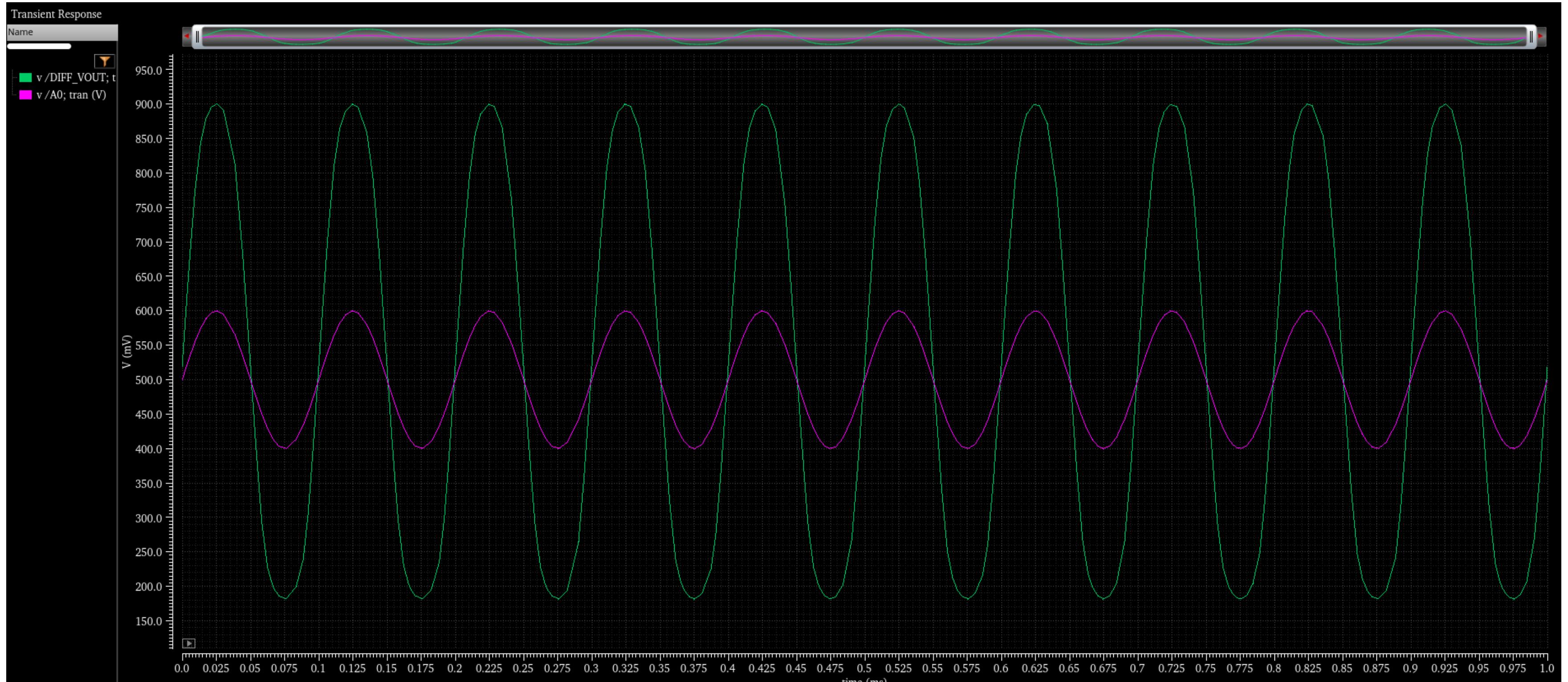
DIFFERENTIAL AMP

DRC / LVS
PASS



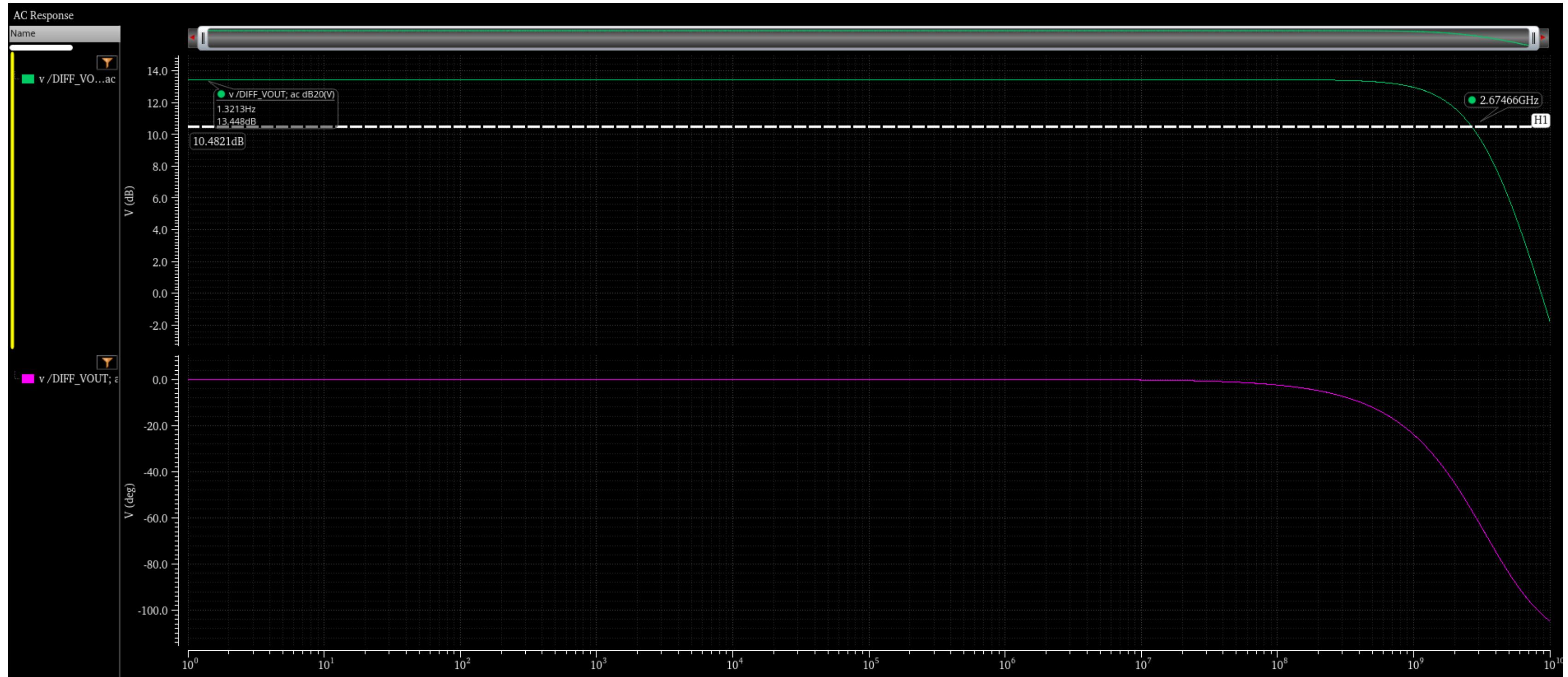
DIFFERENTIAL AMP

Simulation



DIFFERENTIAL AMP _ Simulation

Simulation



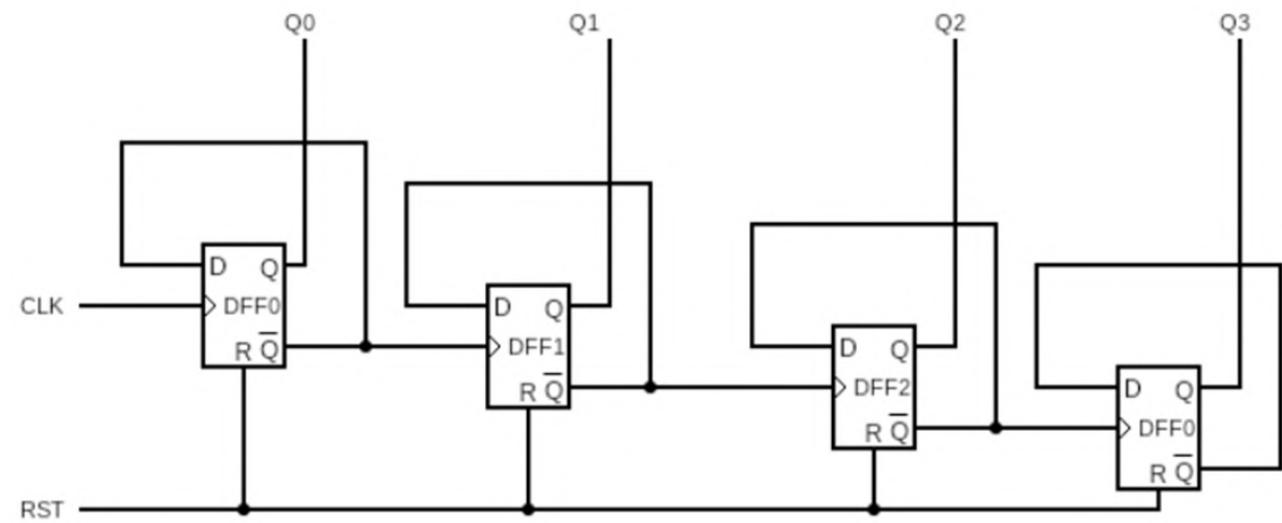
TEAM PROJECT

- Asynchronous Counter / Synchronous Counter
- PIPO Shift Register
- Synchronous Counter + PIPO Shift Register

COUNTER

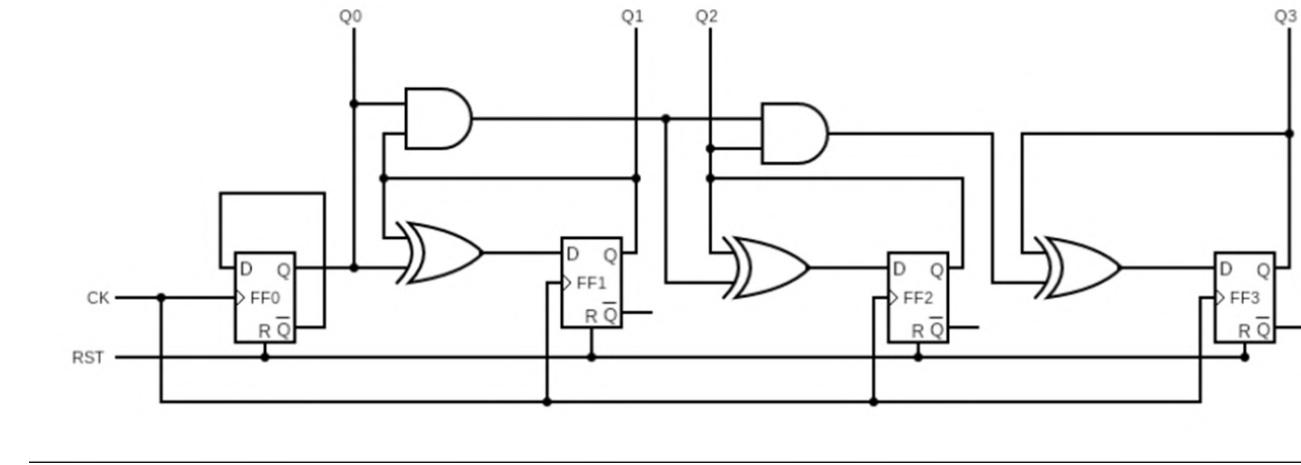
*Type

Asynchronous Counter



- Output of the previous DFF → CLK
=> Only the first DFF receives external CLK; others are triggered internally

Synchronous Counter

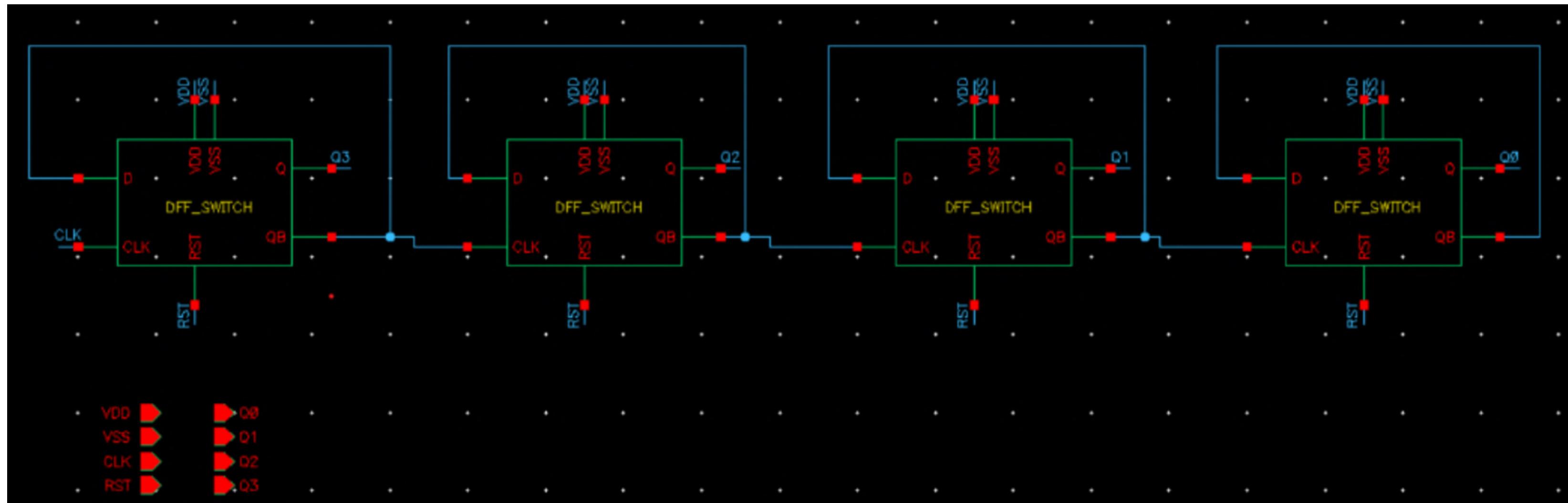


- Simultaneously common CLK
=> All DFFs are triggered by the external CLK

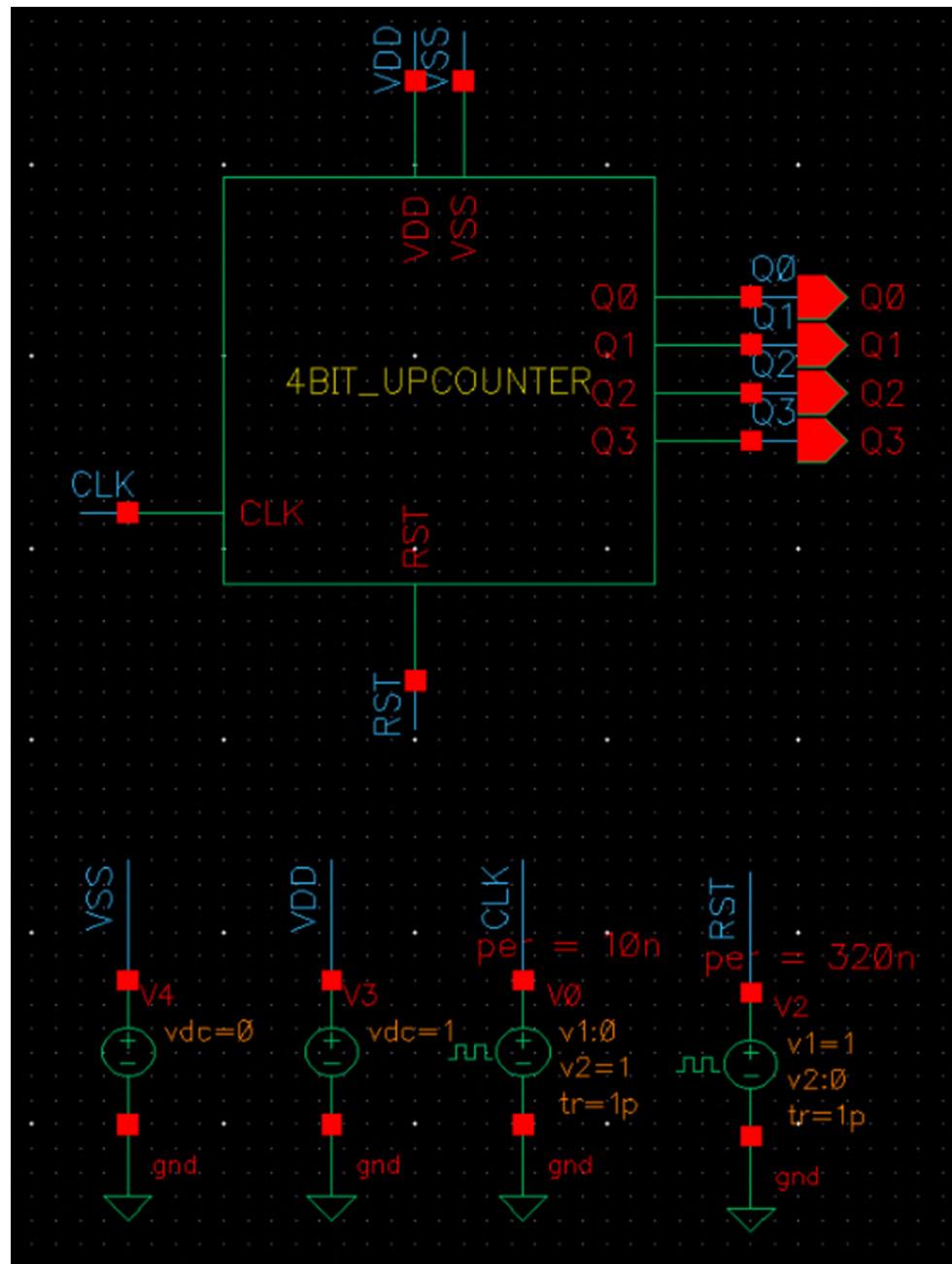
Whether or not delay occurs depends on how the clock is applied

Asynchronous Counter

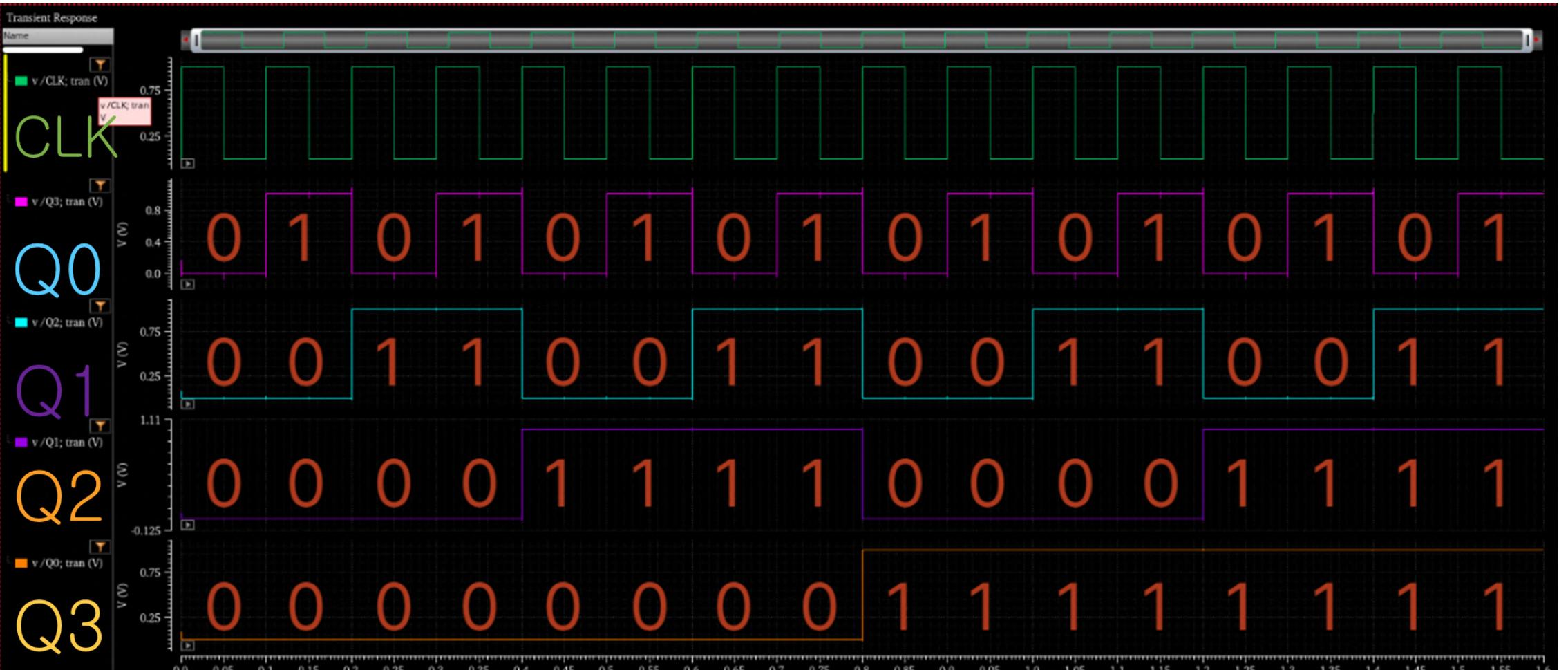
Schematic



Asynchronous Counter

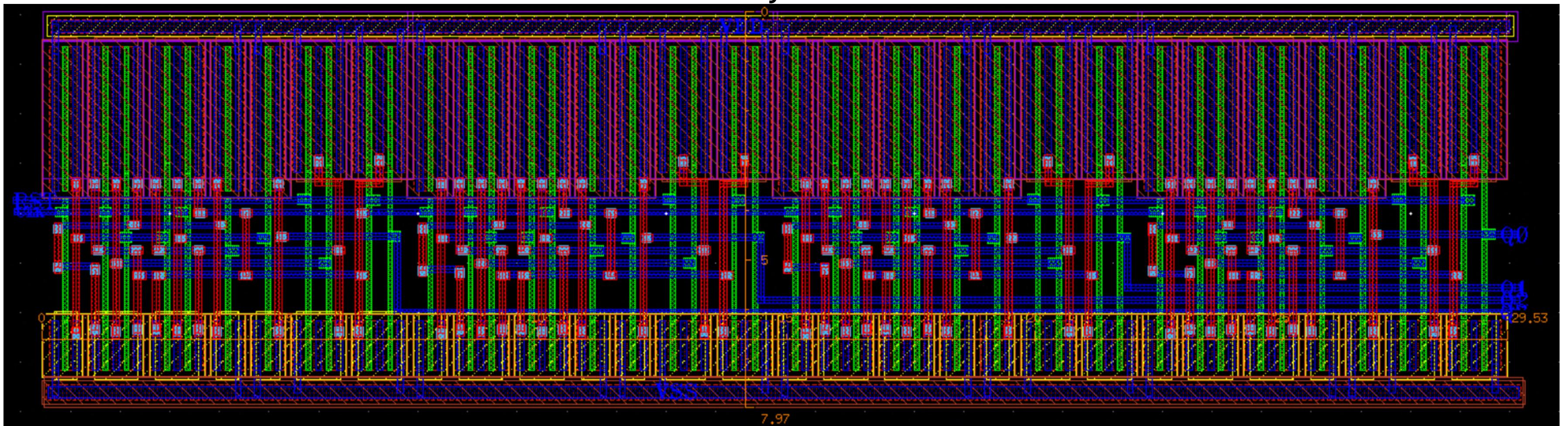


Simulation



Asynchronous Counter

Layout



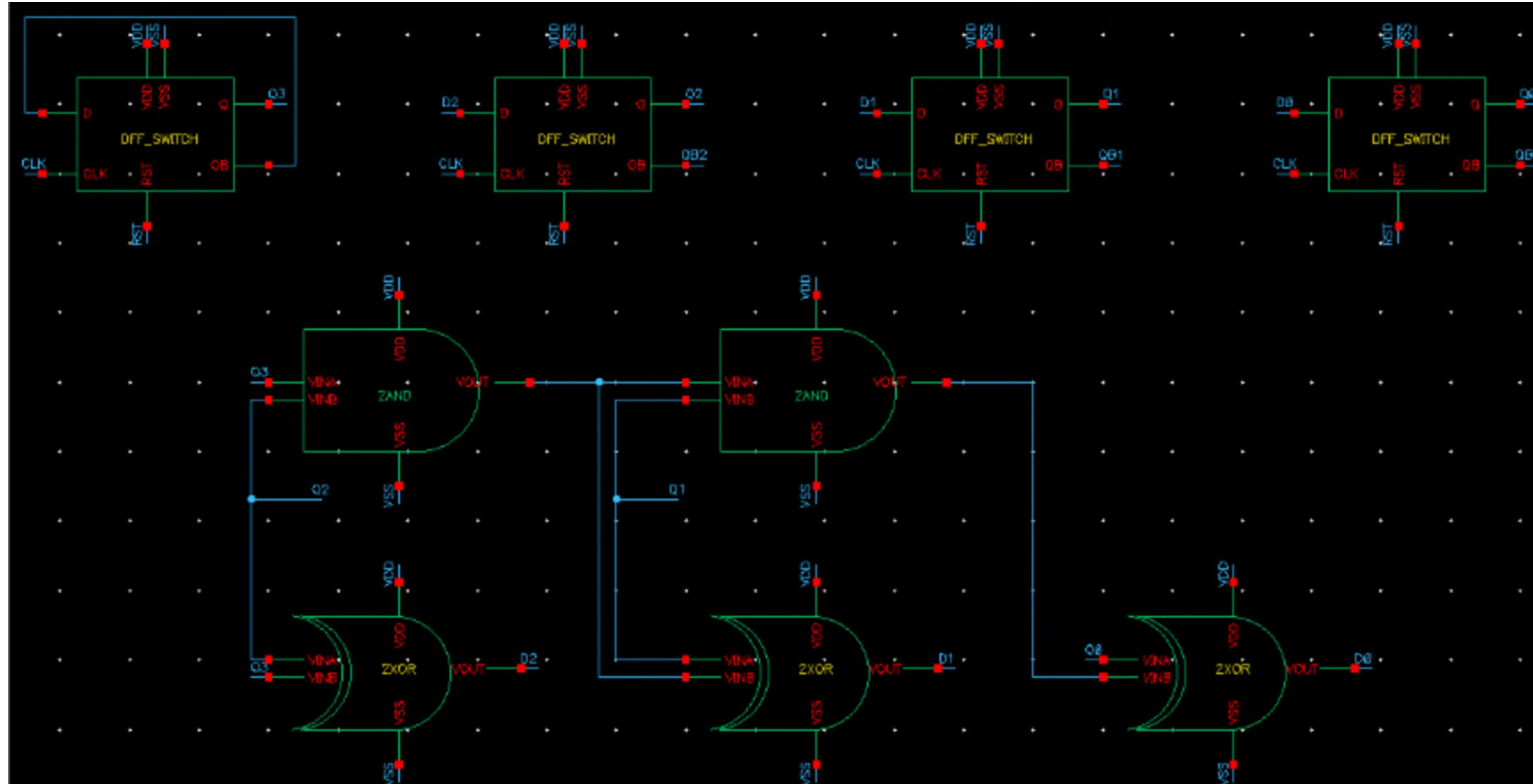
- total size: $235.35[\mu\text{m}^2]$

- width: $29.54[\mu\text{m}]$

- height: $7.97[\mu\text{m}]$

Synchronous Counter

Schematic



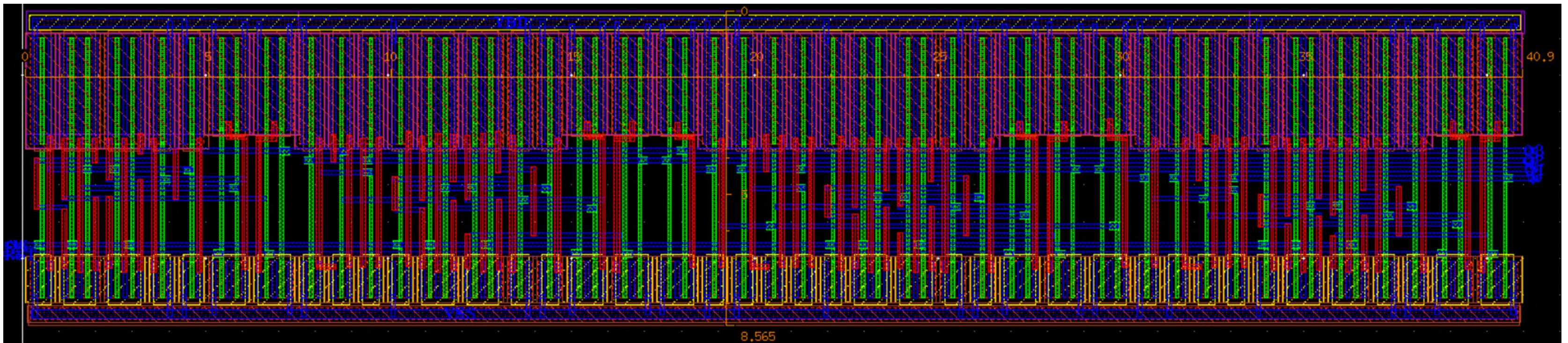
Synchronous Counter

Simulation



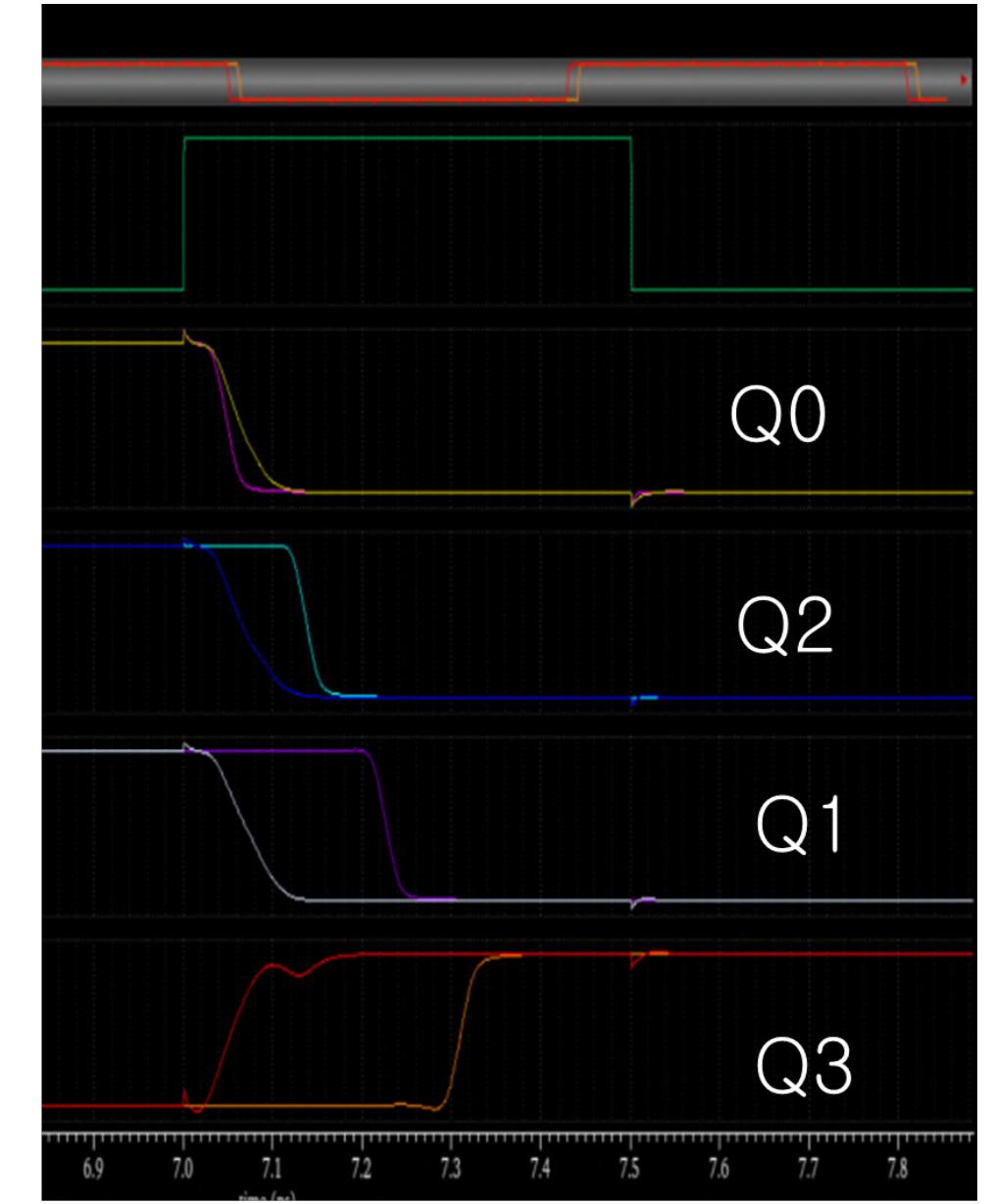
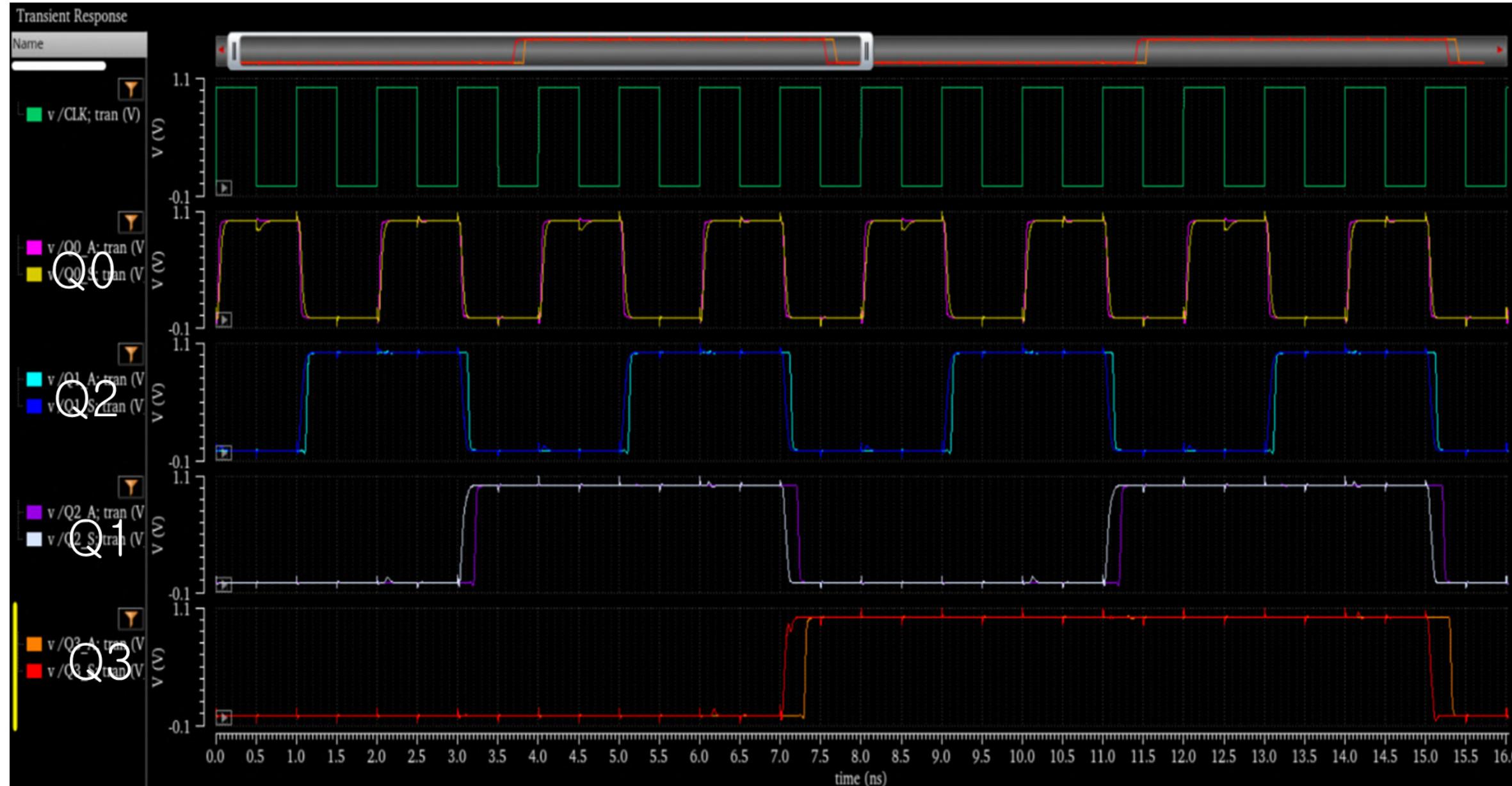
Synchronous Counter

Layout



- total size: 350.5[μm^2]
- width: 40.9[μm]
- height: 8.57[μm]

Asynchronous vs Synchronous Counter

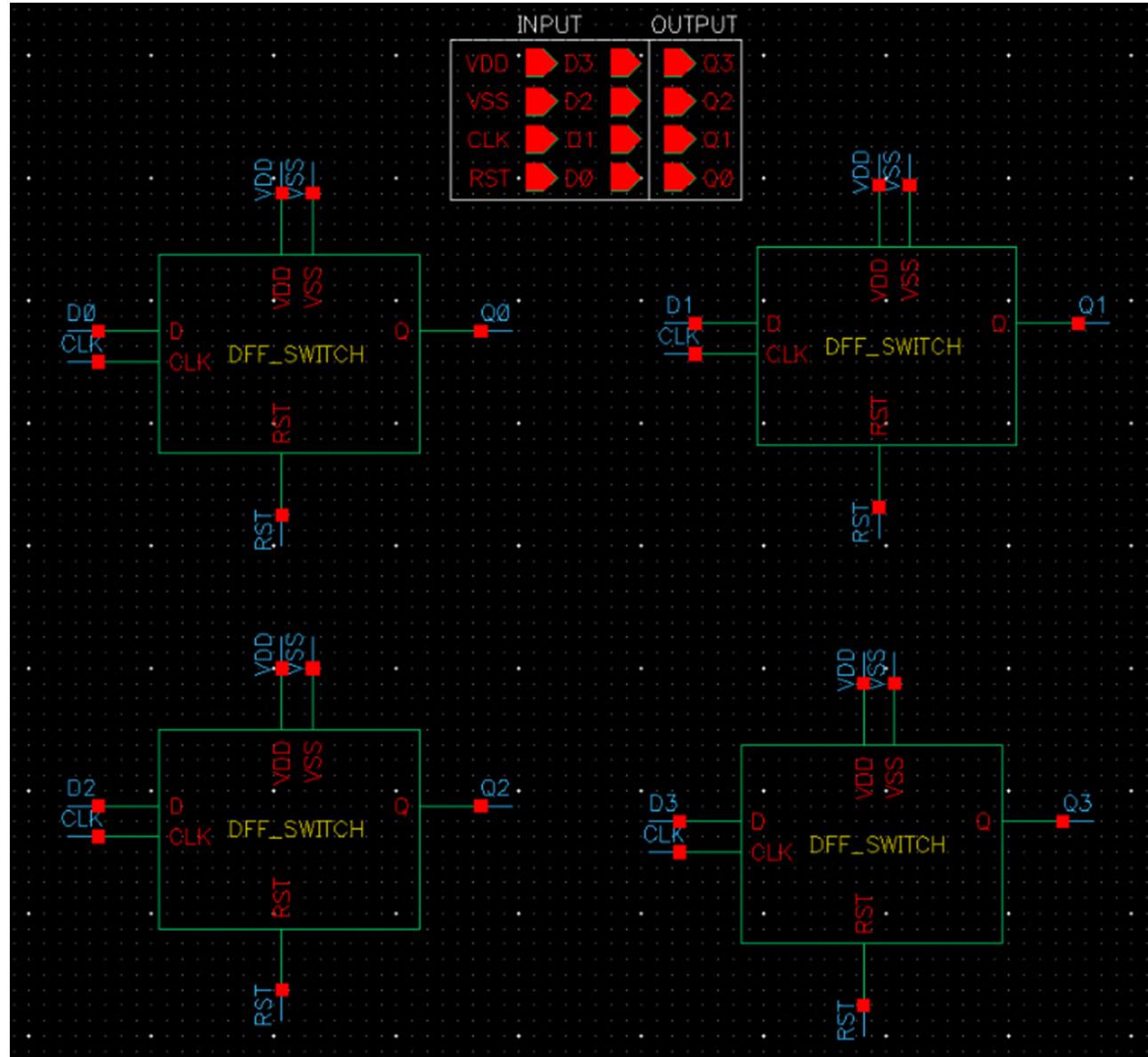


In an asynchronous counter, delay increases progressively from Q3 to Q0. (Q3>Q2>Q1>Q0)

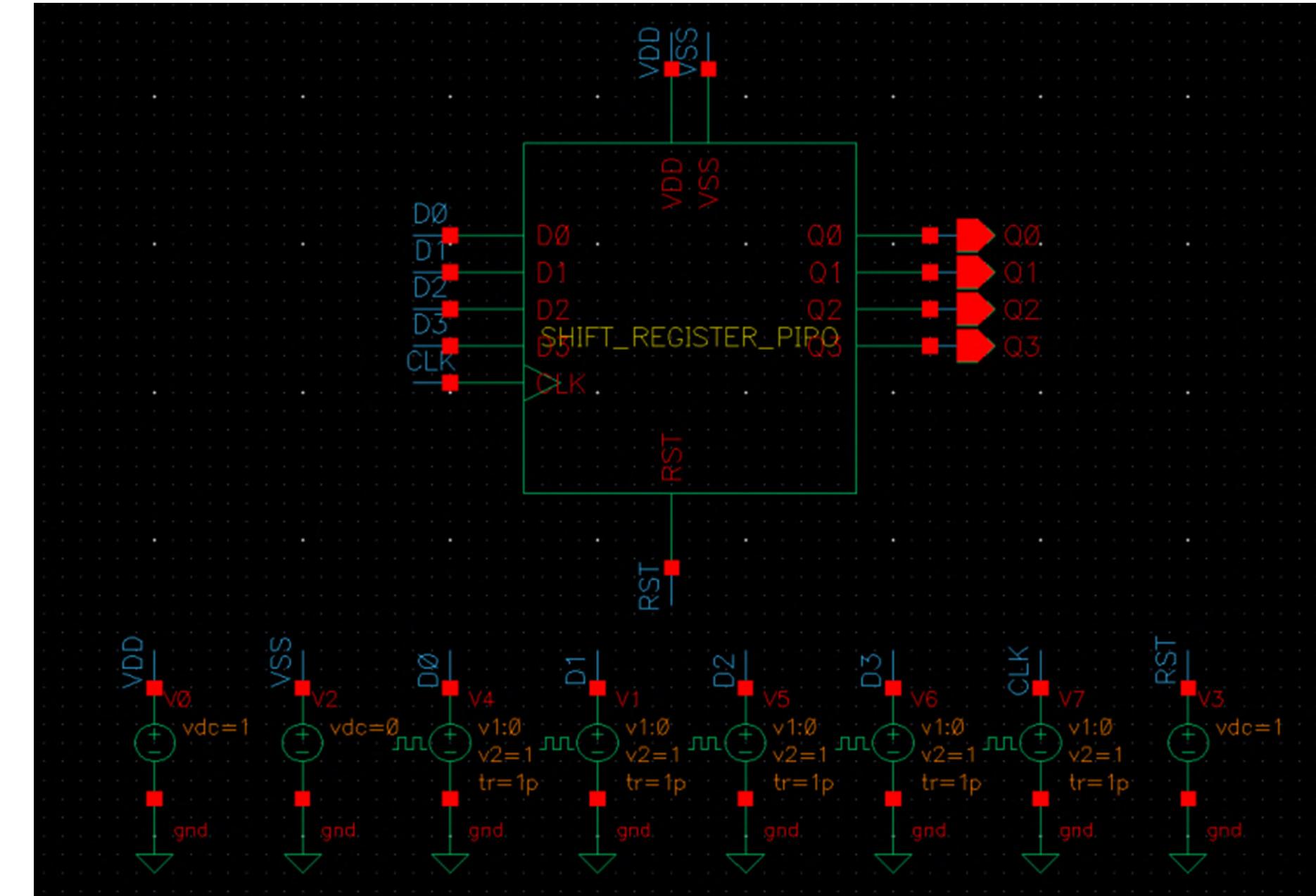
AREA : Sync(350.5um²) > Async(235.35um²)

PIPO Shift Register

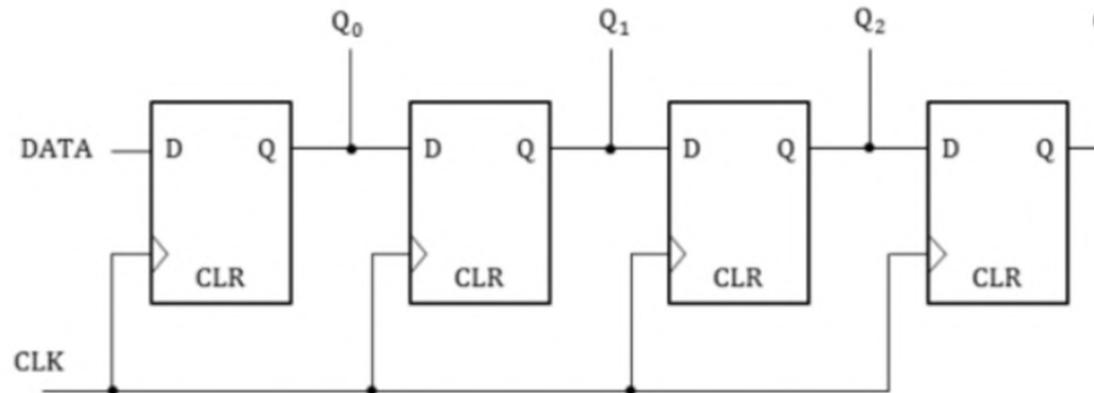
Schematic



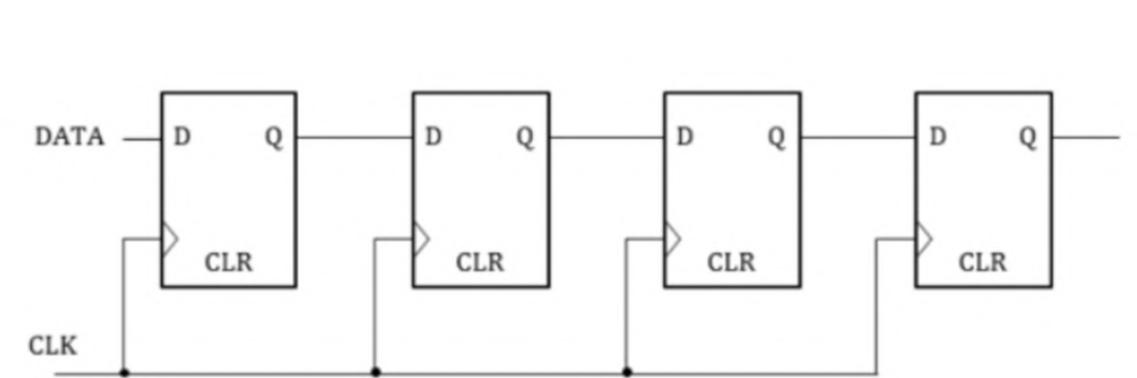
Schematic_for_Sim



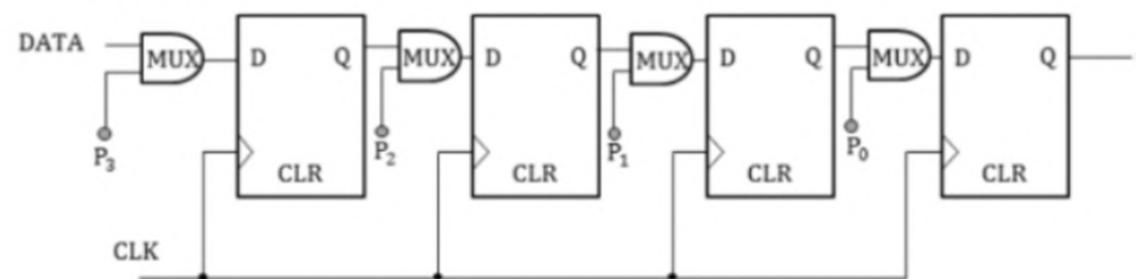
Shift Register (TYPE)



(Serial-in to Parallel-out(SIPO) Shift Register)
=>1 In , 4 Out

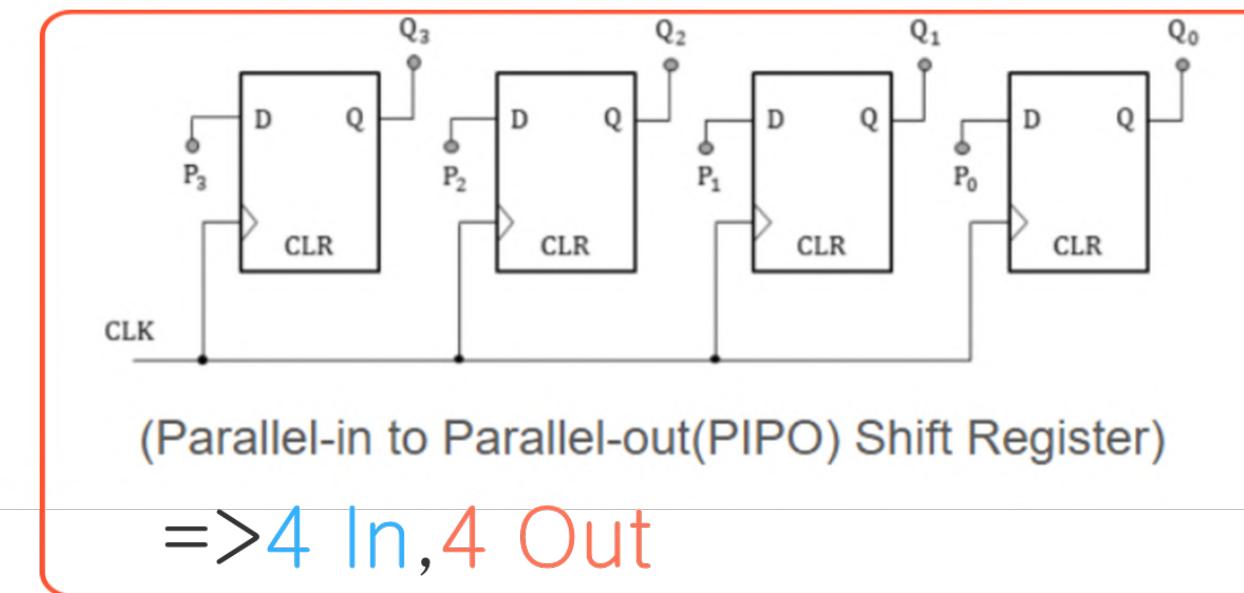


(Serial-in to Serial-out(SISO) Shift Register)
=>1 In, 1 Out



(Parallel-in to Serial-out(PISO) Shift Register)
=> 4 In, 1 Out

Out



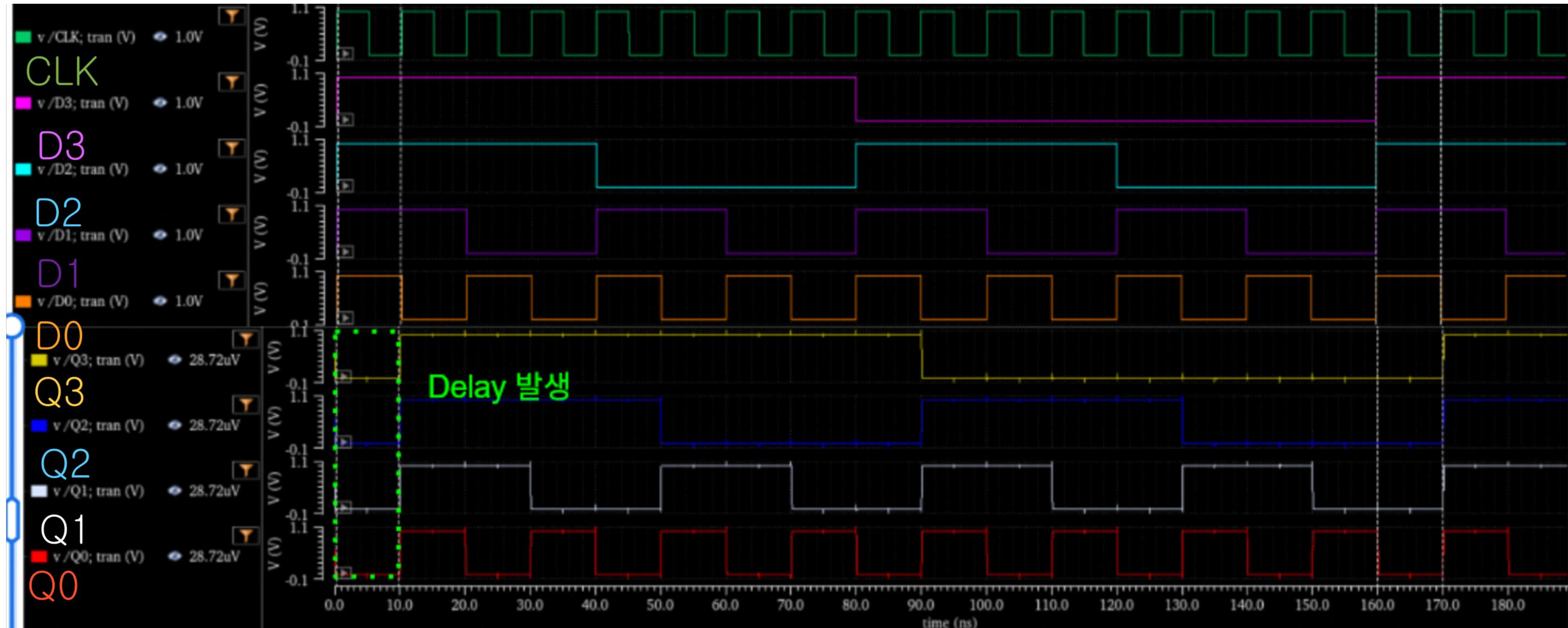
(Parallel-in to Parallel-out(PIPO) Shift Register)
=>4 In,4 Out

- Parallel-in loading is adopted to interface with the 4-bit counter.

- PIPO (Parallel-In, Parallel-Out): Successfully used to feed counter outputs into the shift register.
- PISO (Parallel-In, Serial-Out): Failed due to clock-timing and control-signal complexity.

PIPO Shift Register

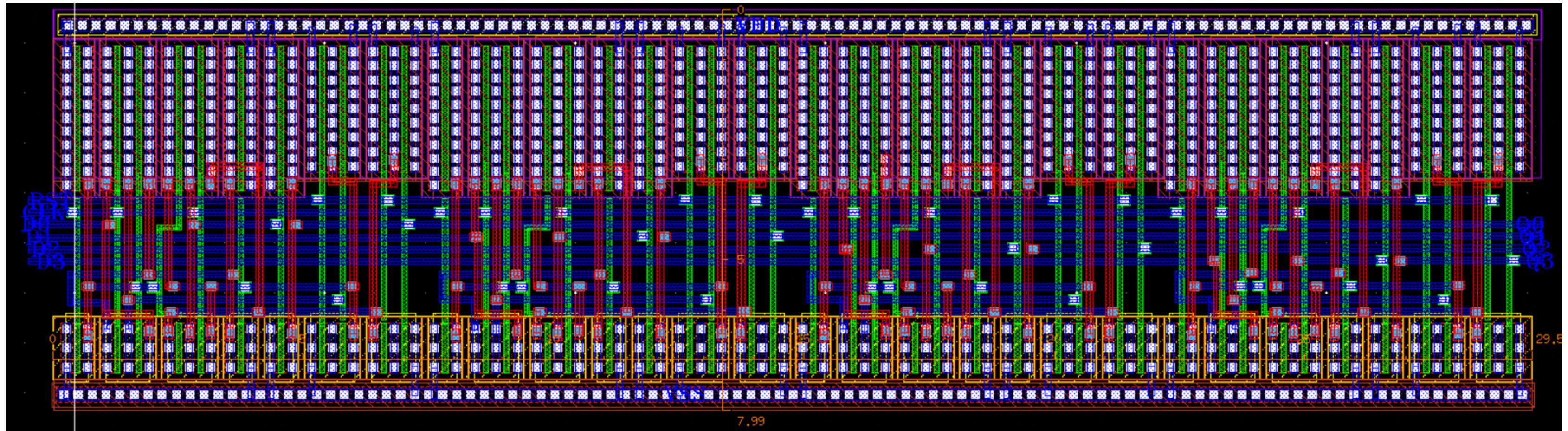
Simulation



Outputs are delayed by one CLK cycle \Rightarrow shift operation.

PIPO Shift Register

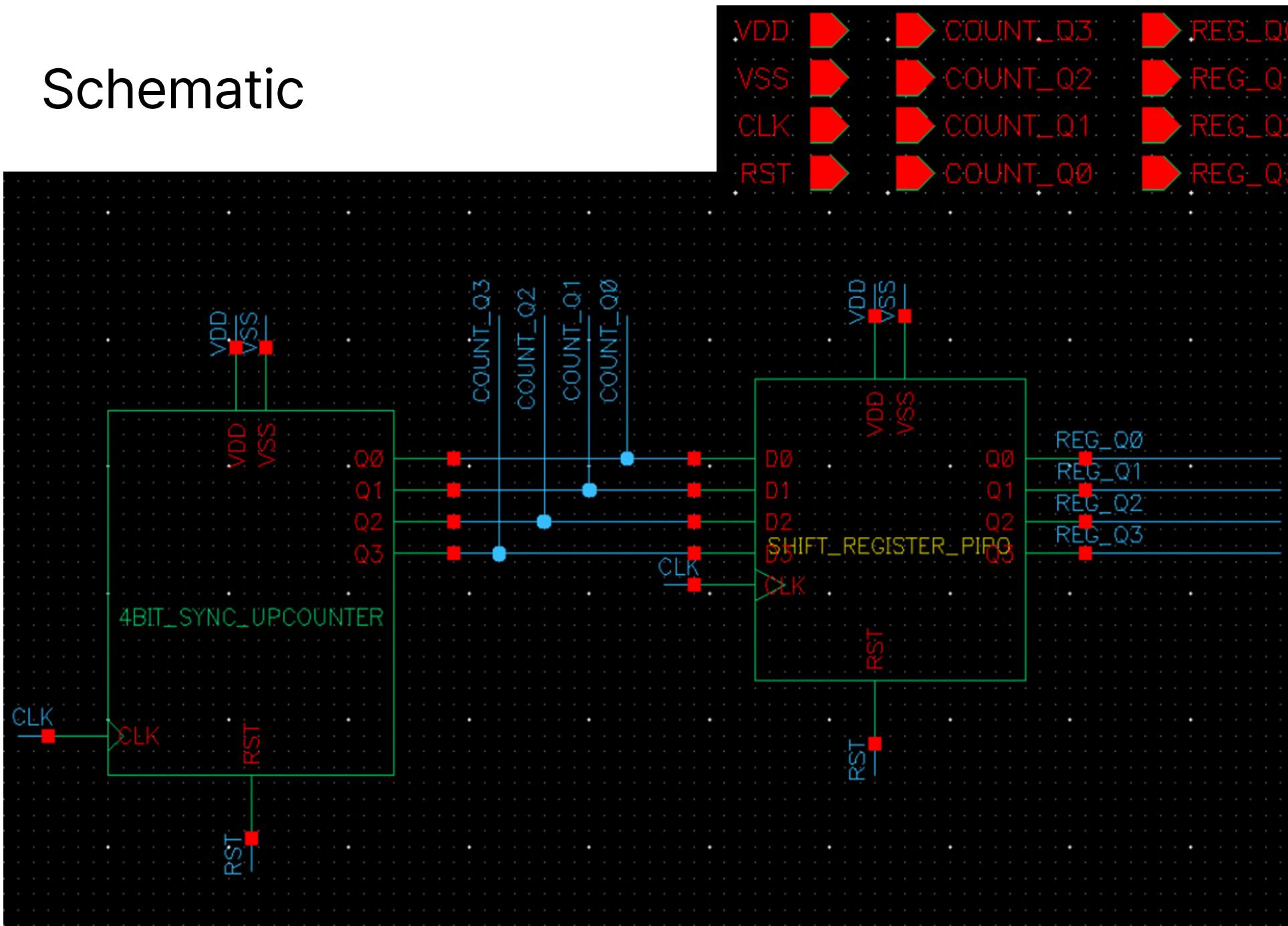
layout



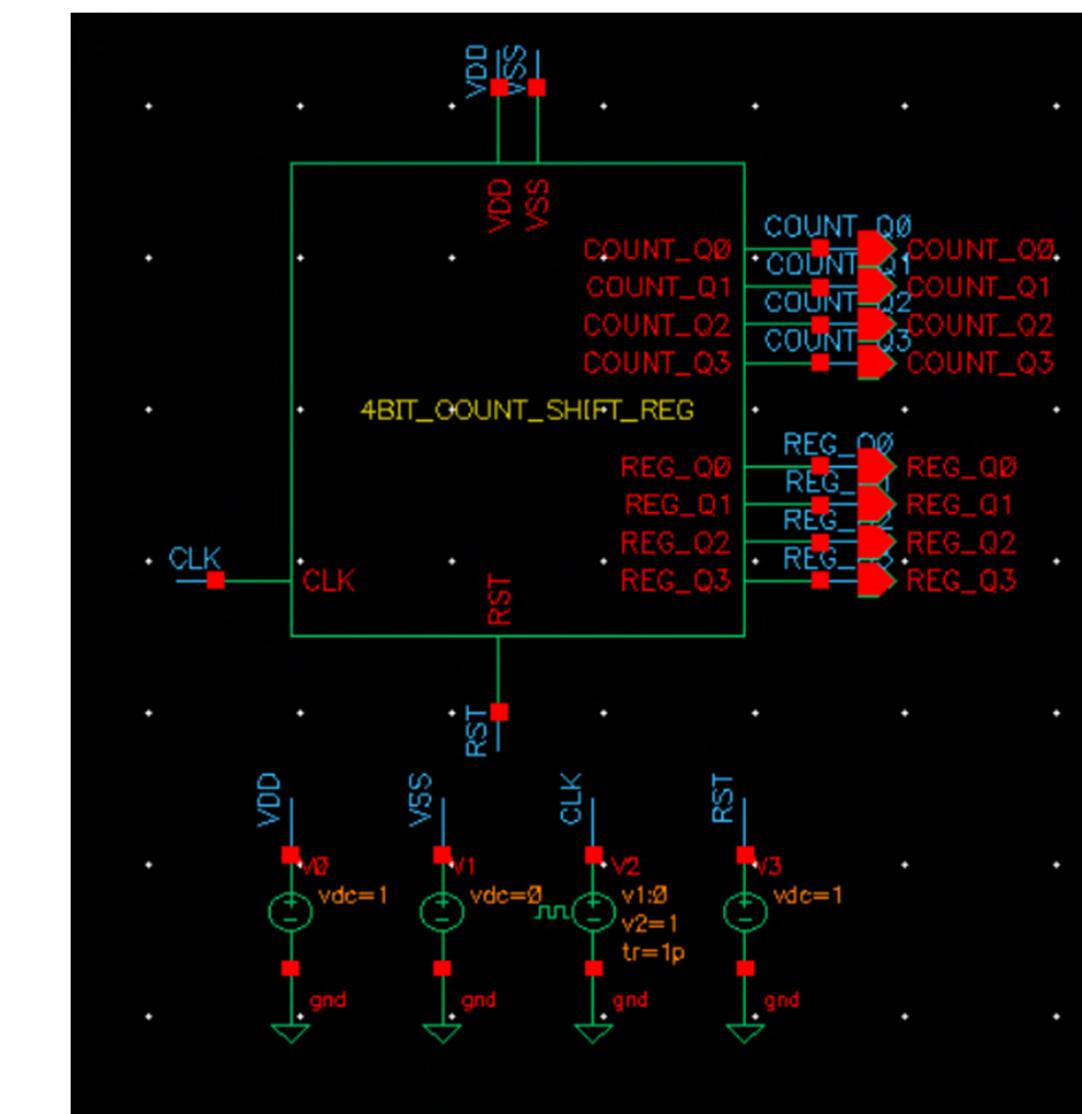
- total size: 235.94[um²]
- width: 29.53[um]
- height: 7.99[um]

Synchronous Counter + PIPO Shift Register

Schematic

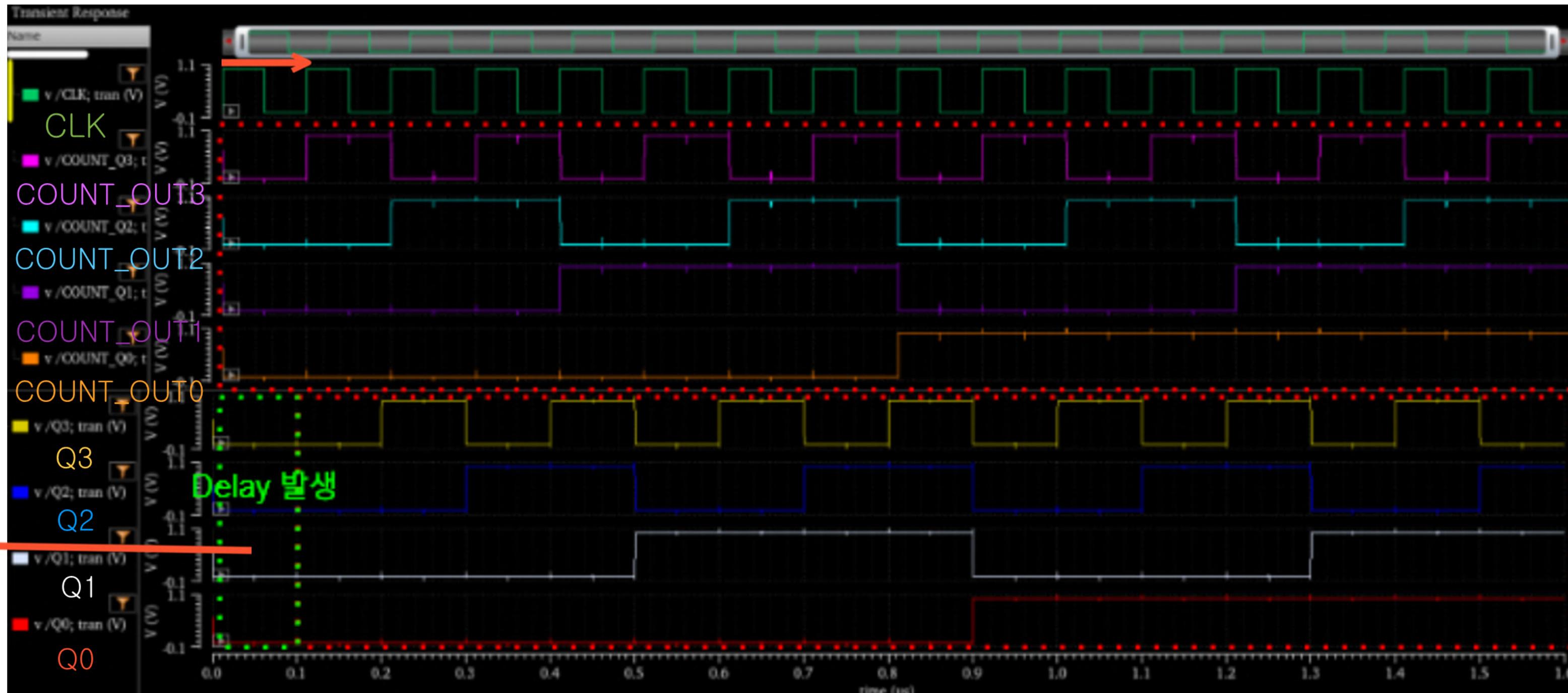


Schematic_for_Sim



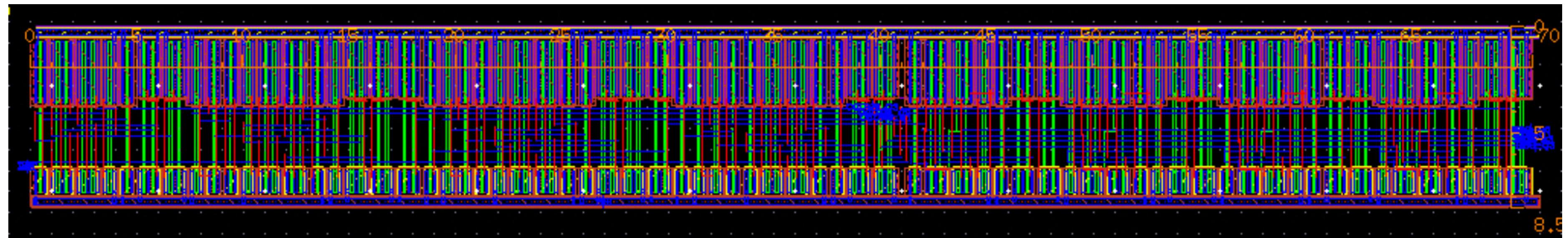
Synchronous Counter + PIPO Shift Register

Simulation



Synchronous Counter + PIPO Shift Register

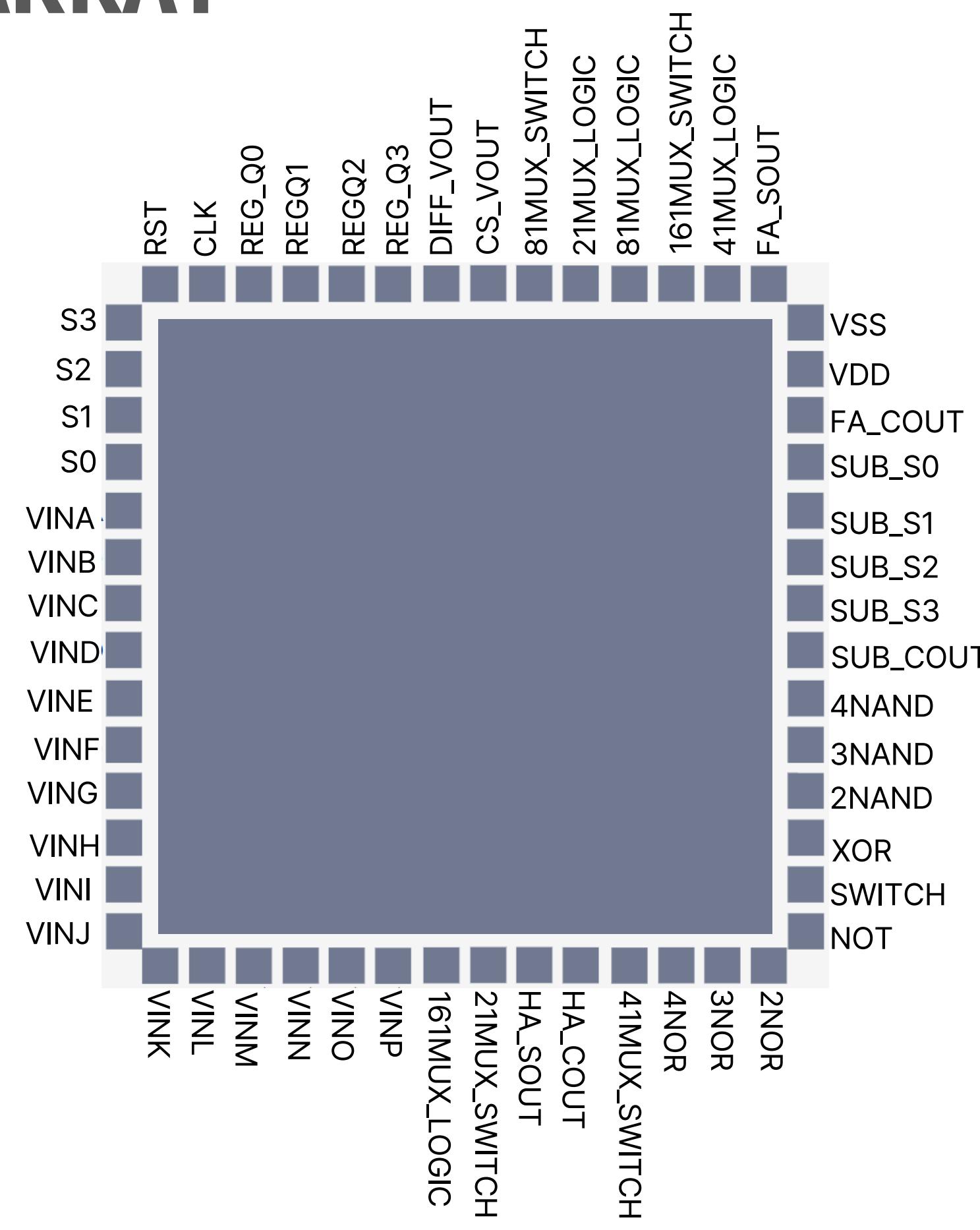
Layout



- total size: 605.29[um²]
- width: 70.67[um]
- height: 8.57[um]

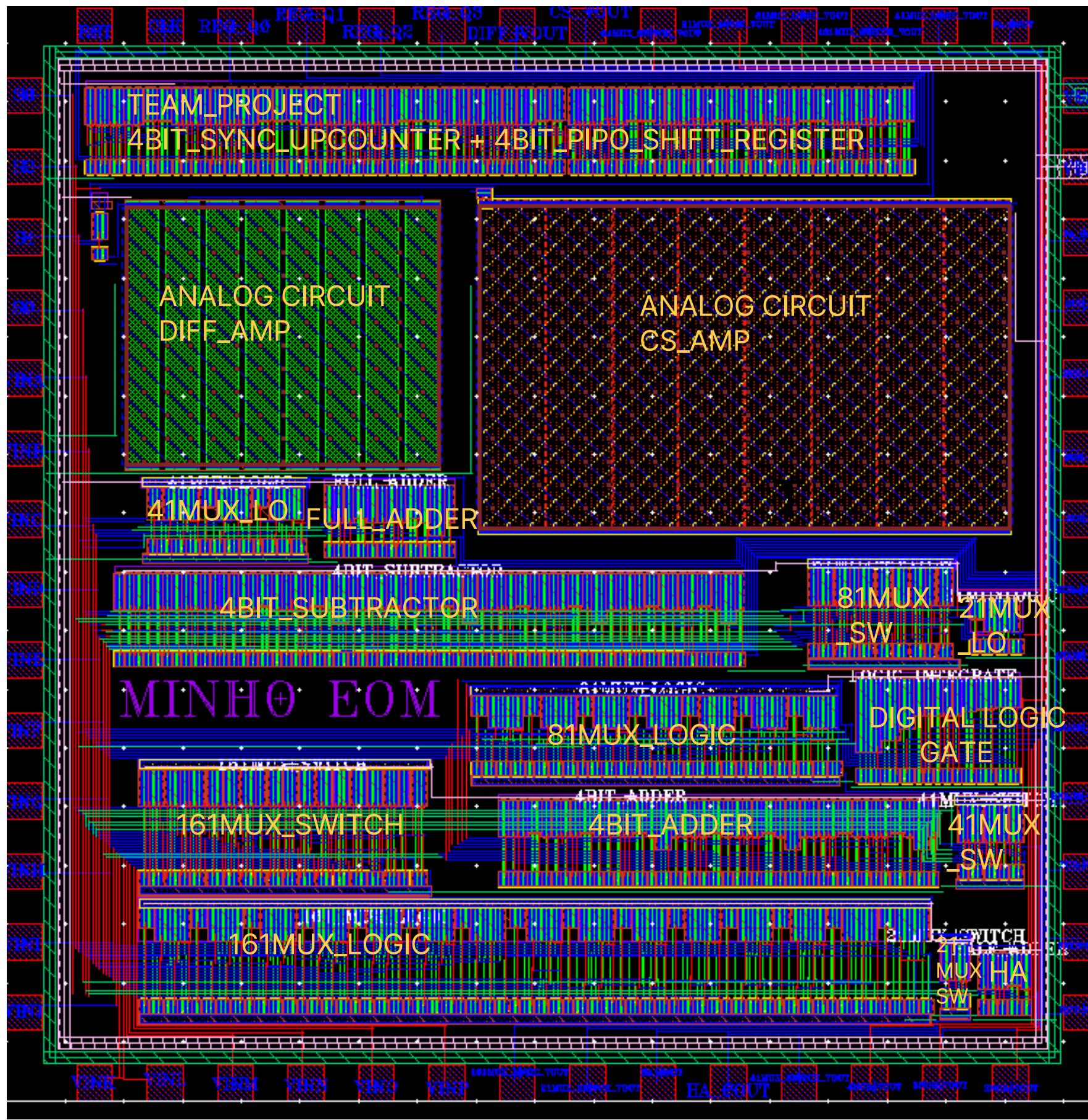
ONE CHIP

ONE CHIP - PIN ARRAY

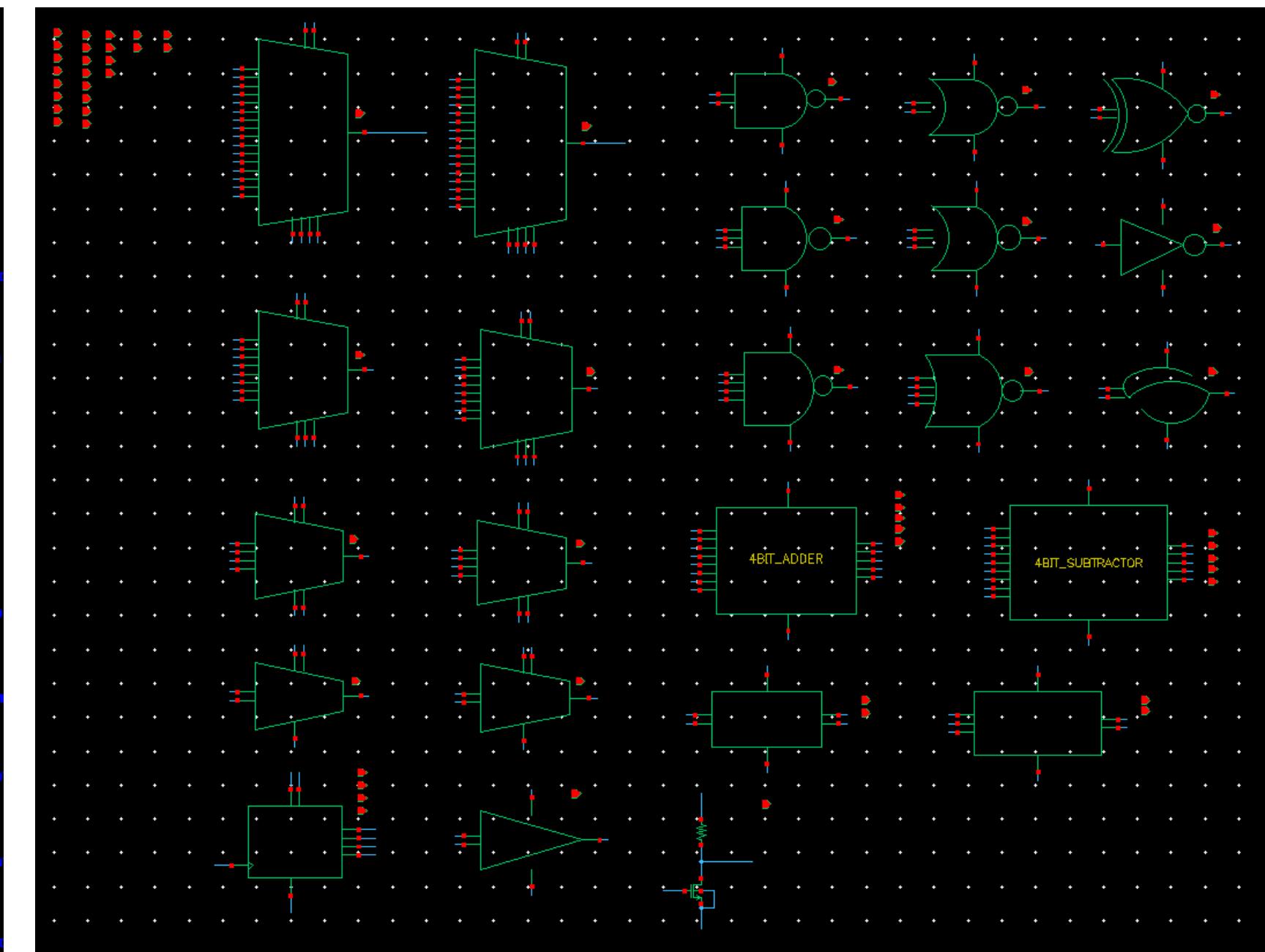


ONE CHIP

Layout

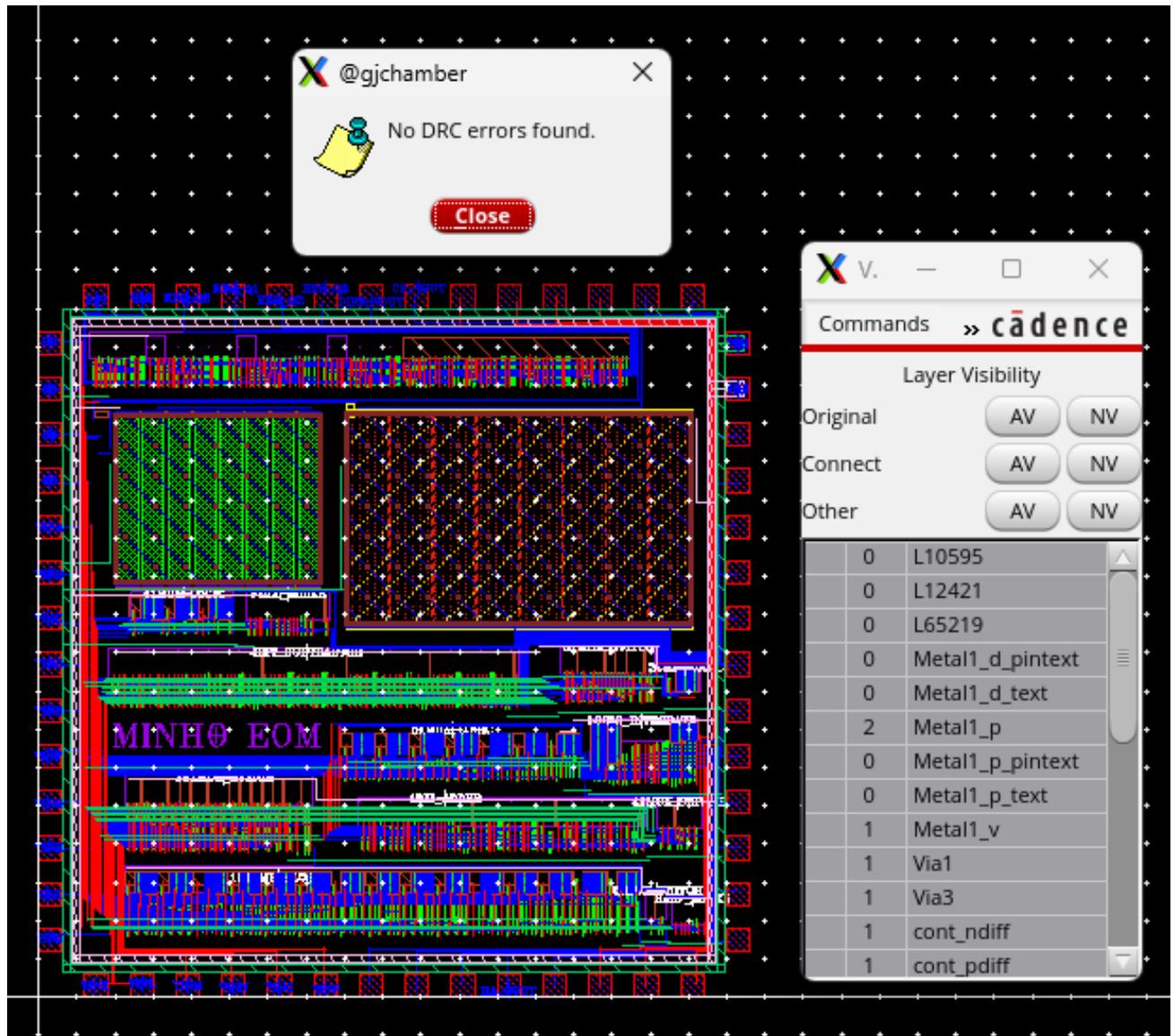


Schematic

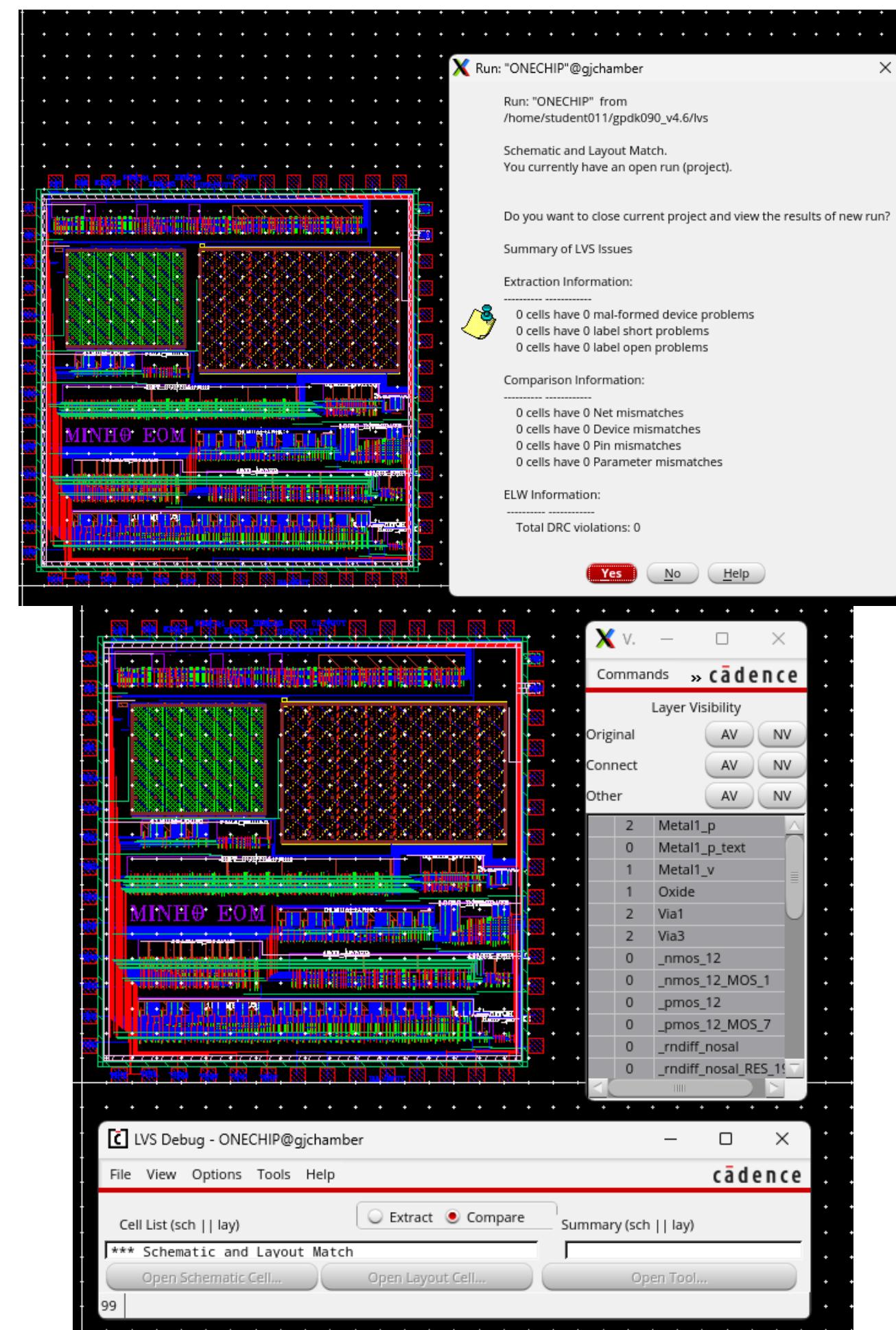


ONE CHIP

DRC PASS



LVS PASS



CONTECT



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