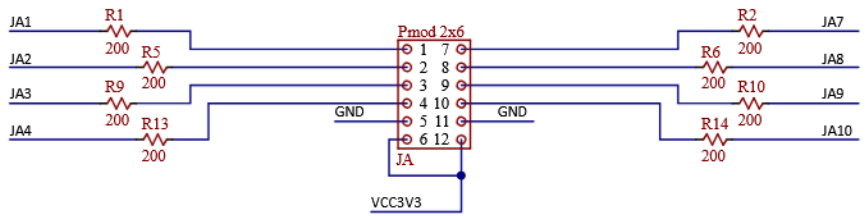
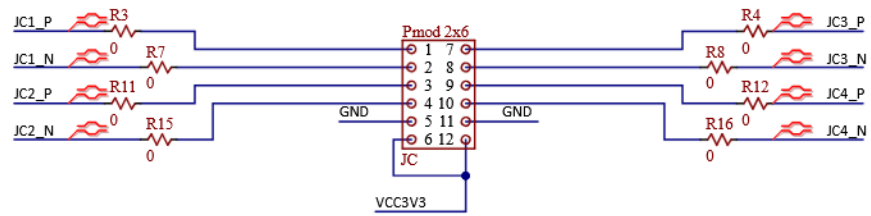
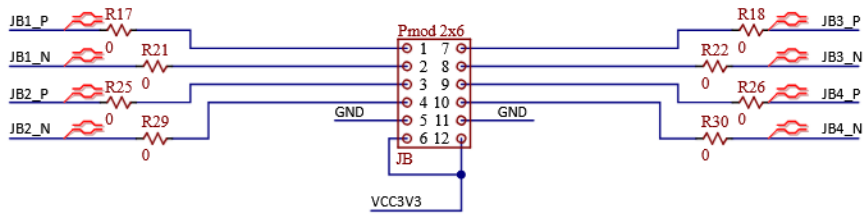
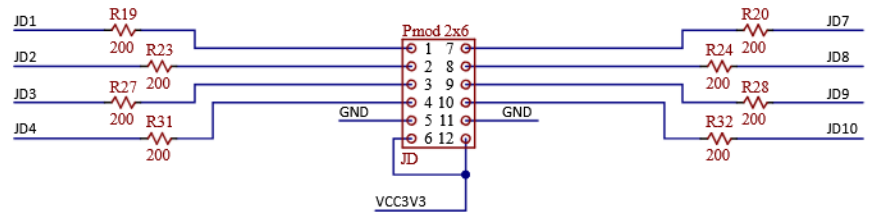
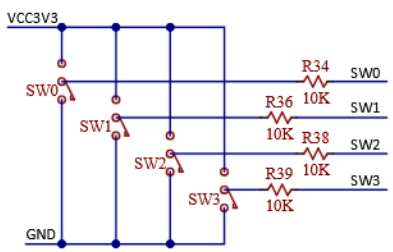
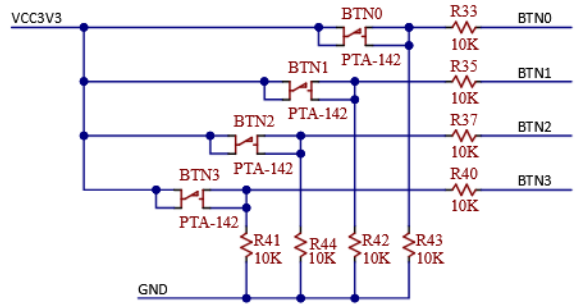












Foot F1
Foot F2
Foot F3
Foot F4

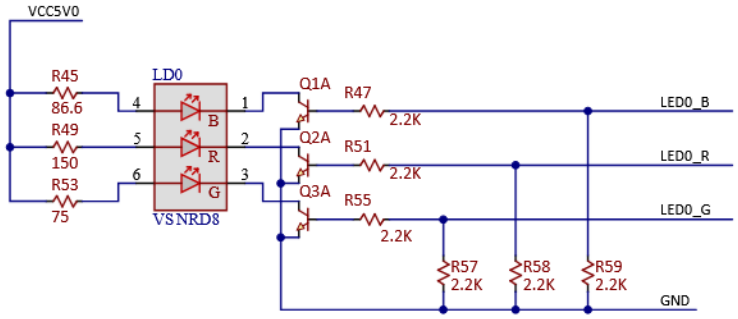
Title	Rev
Arty A7	E.2

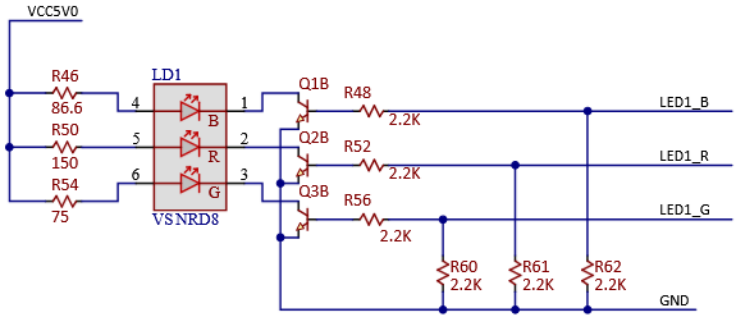
Circuit	PMOD, BTN, SWTs
Doc#	500-319
Engineer	MTA
Author	GMA
Date	1/25/2022
Sheet#	1 out of 12

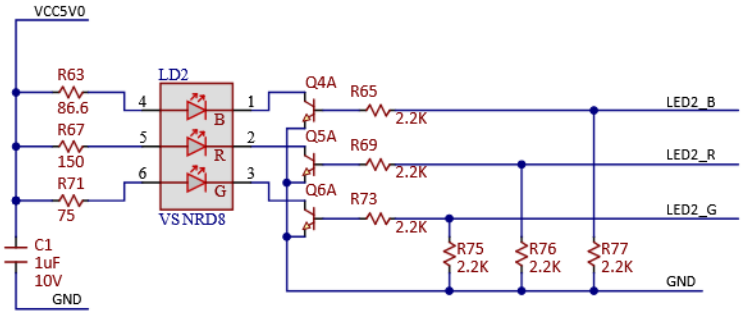
DIGILENT

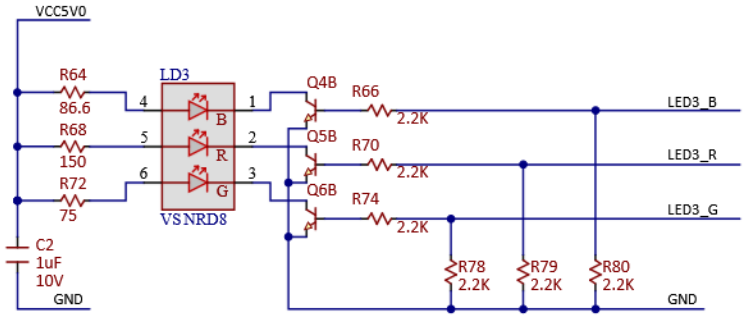
Copyright 2022

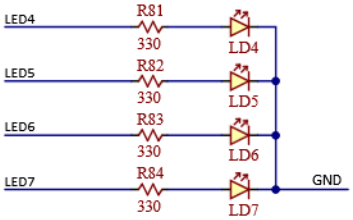
Avnet Xilinx Digilent Inc. CE ROHS Chinese ROHS Arty A7









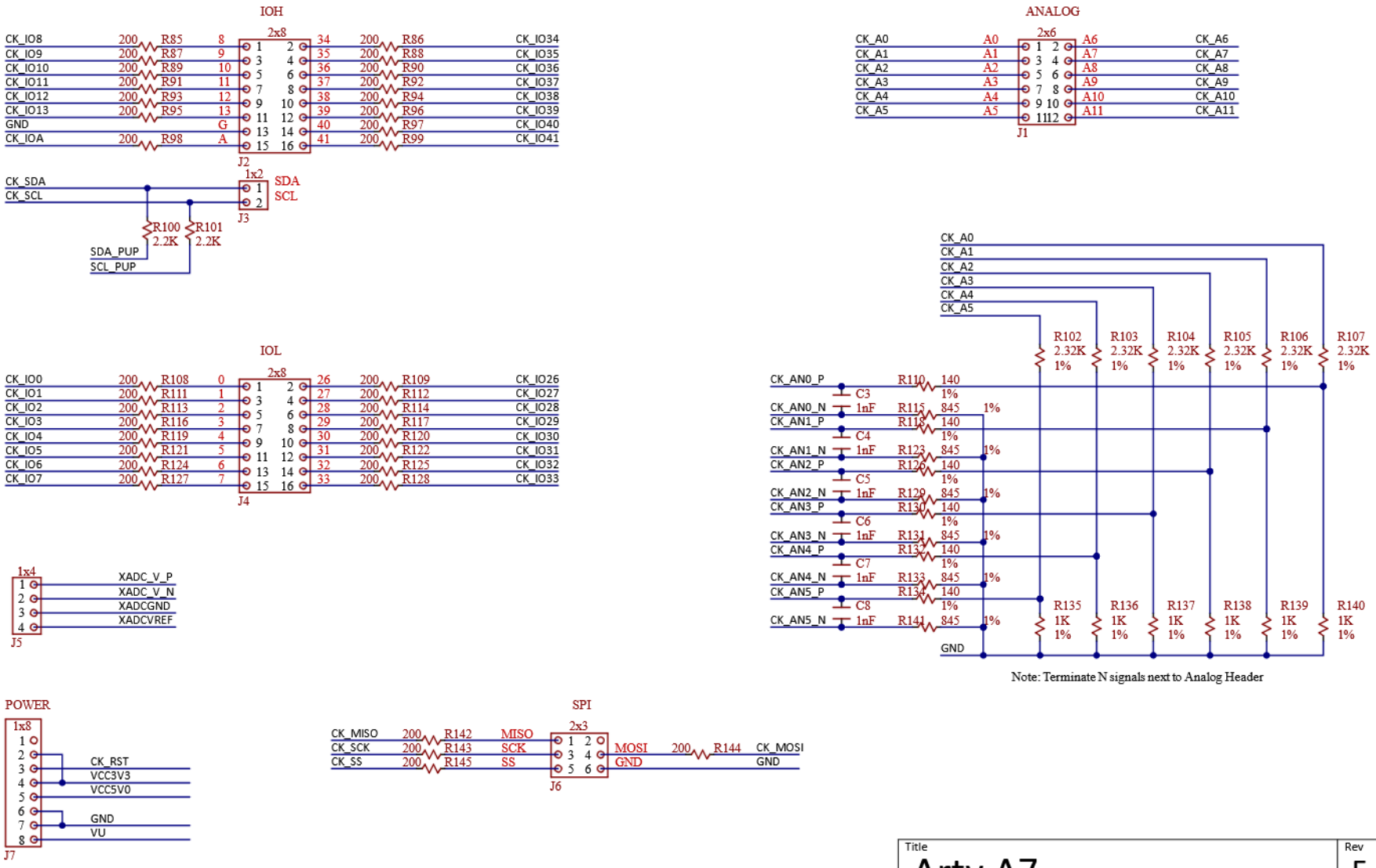


Title	Rev
Arty A7	E.2

Circuit	LEDs
Doc#	500-319
Engineer	MTA
Author	GMA
Date	1/25/2022
Sheet#	2 out of 12

DIGILENT®

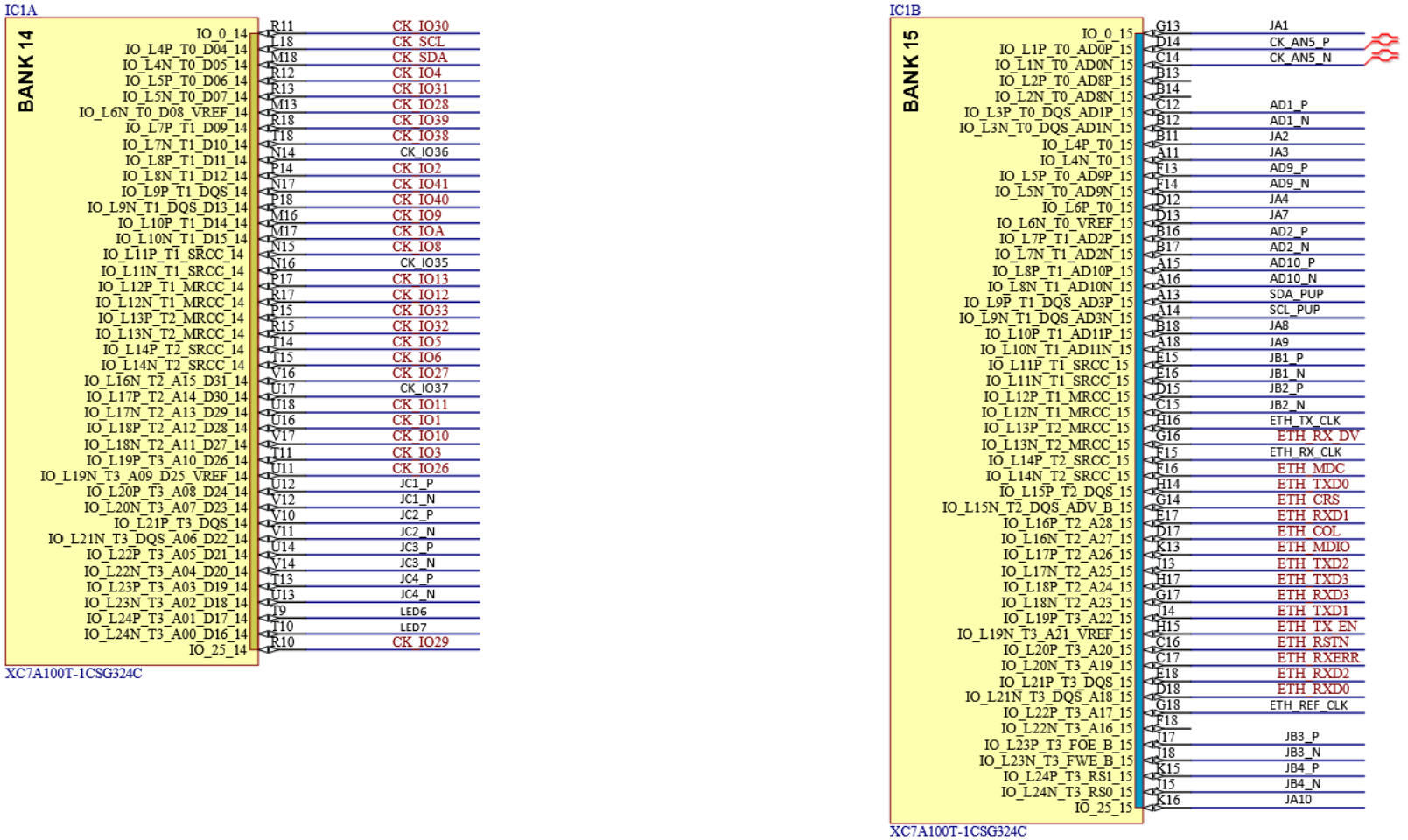
Copyright 2022



Title	Arty A7
Rev	E.2
Circuit	CHipKIT IO
Doc#	500-319
Engineer	MTA
Author	GMA
Date	1/25/2022
Sheet#	3 out of 12

DIGILENT

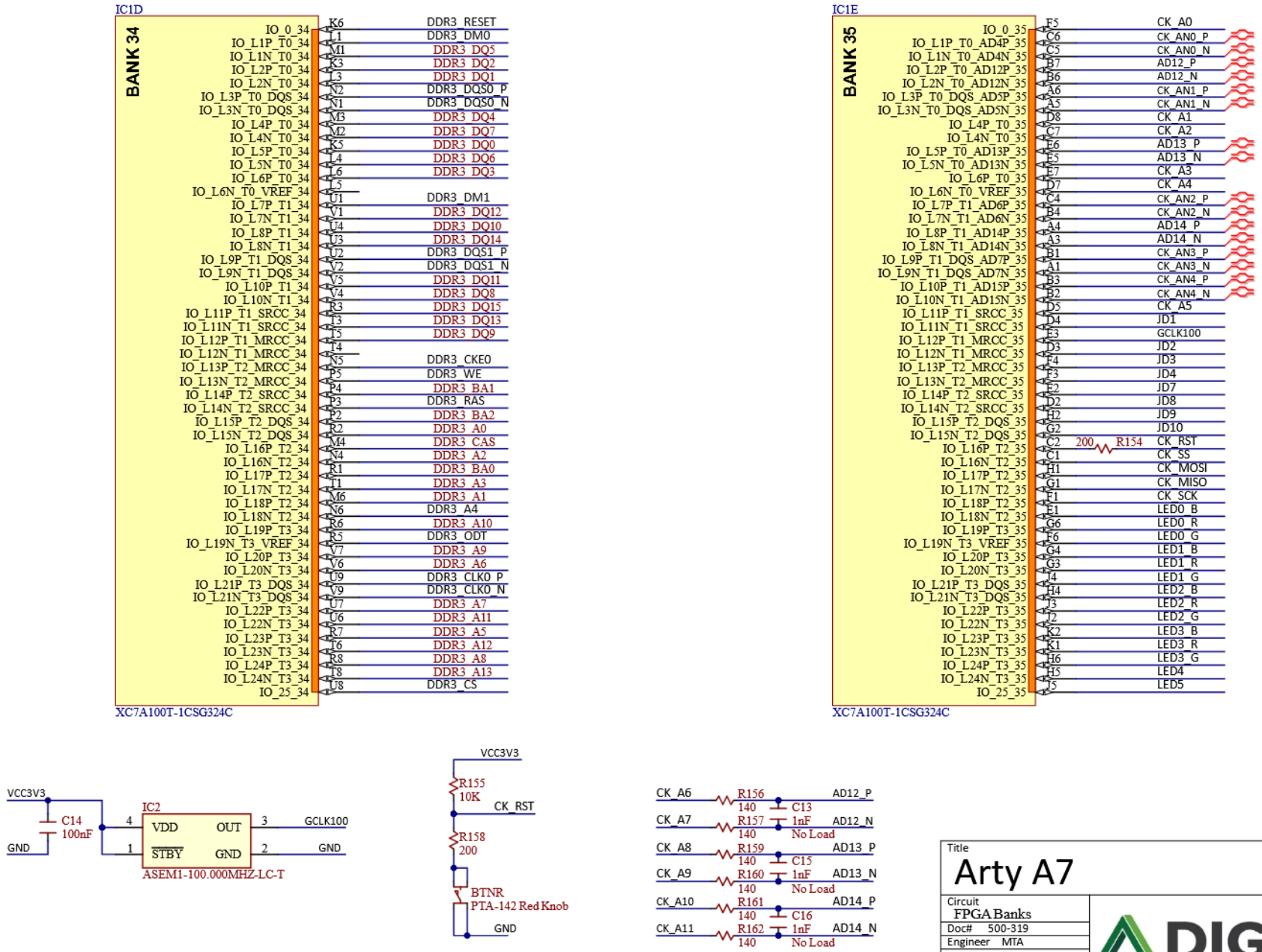
Copyright 2022



Title	Arty A7
Rev	E.2
Circuit	FPGA Banks
Doc#	500-319
Engineer	MTA
Author	GMA
Date	1/25/2022
Sheet#	4 out of 12

DIGILENT

Copyright 2022



Title
Arty A7

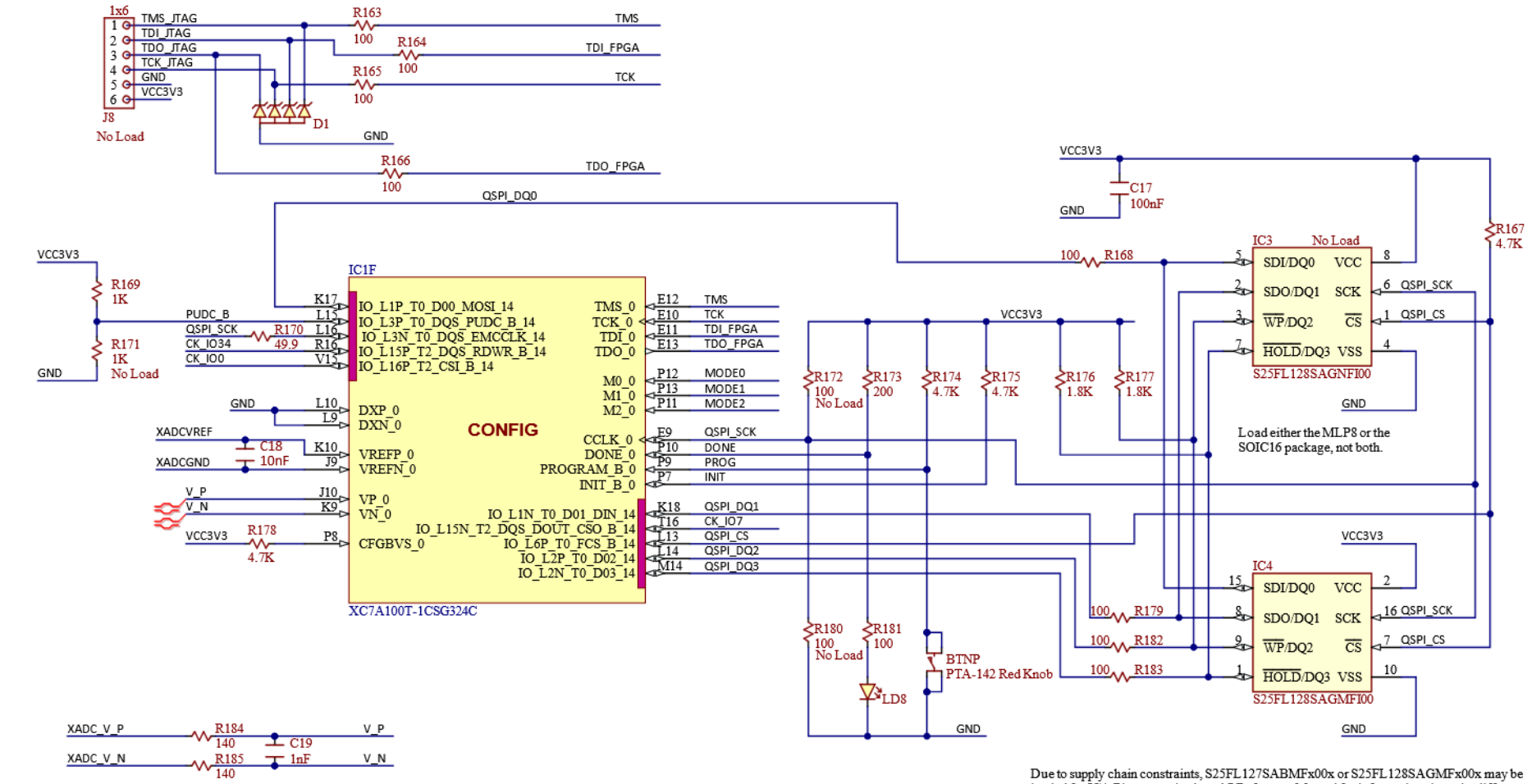
Rev
E.2

Circuit
FPGA Banks

Doc#	500-319
Engineer	MTA
Author	GMA
Date	1/25/2022
Sheet#	5 out of 12

DIGILENT®

Copyright 2022

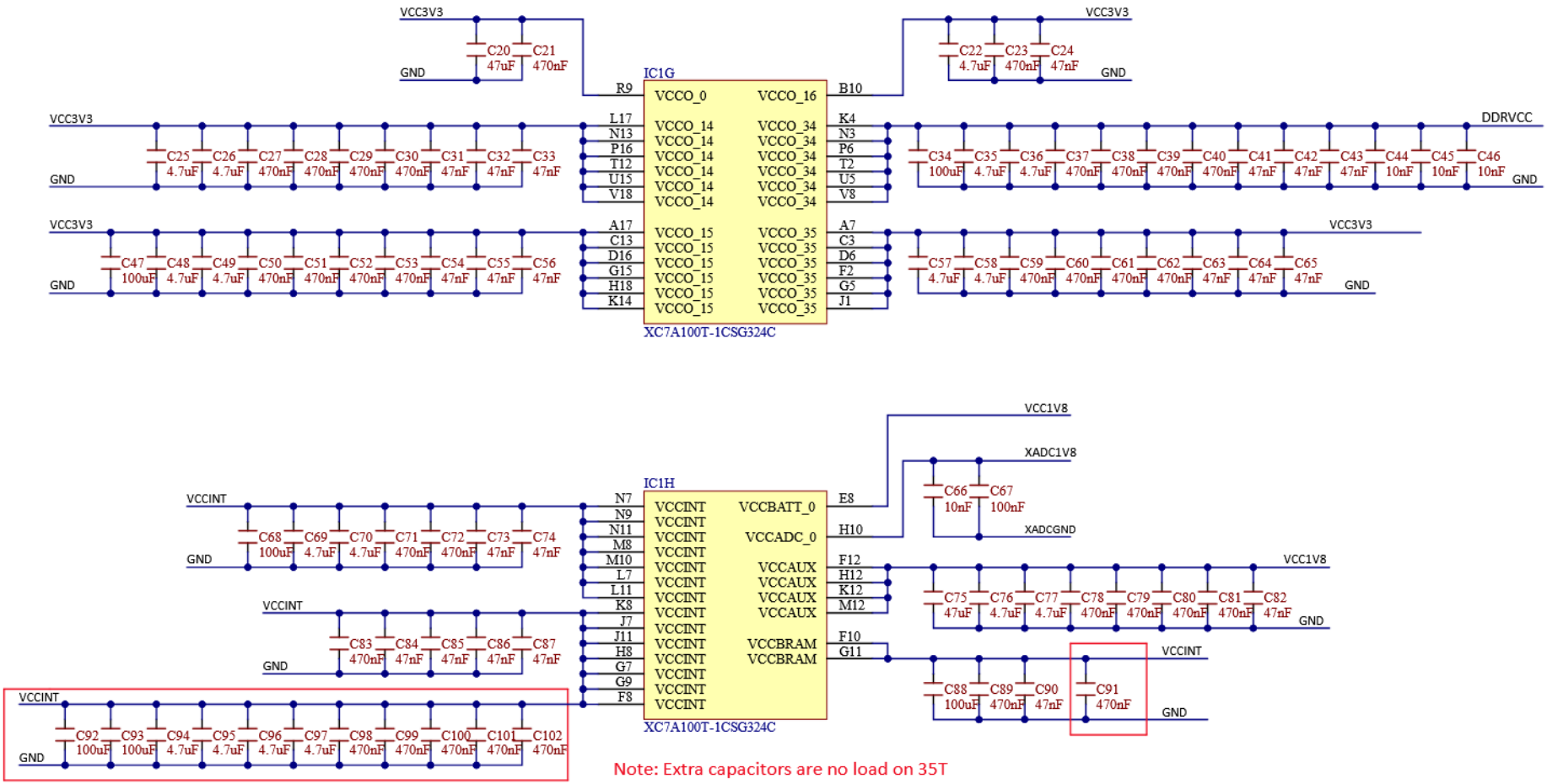


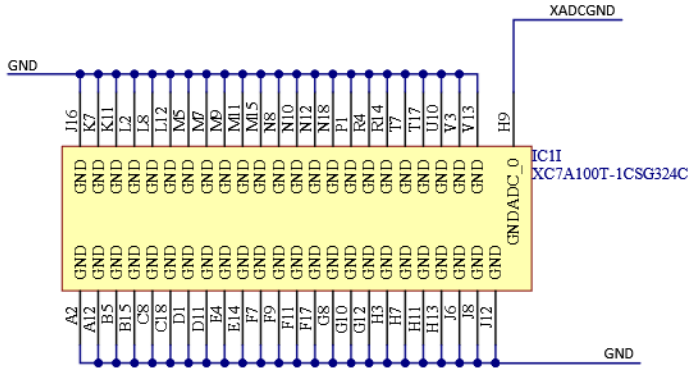
Due to supply chain constraints, S25FL127SABMFx00x or S25FL128SAGMFx00x may be loaded for IC4. Please see the Arty A7 Reference Manual for information about the differences between these Quad-SPI Flash Memories and how to identify which memory is installed on your board.

Title	Arty A7
Rev	E.2
Circuit	CONFIG, SPI FLASH
Doc#	500-319
Engineer	MTA
Author	GMA
Date	1/25/2022
Sheet#	6 out of 12

DIGILENT

Copyright 2022

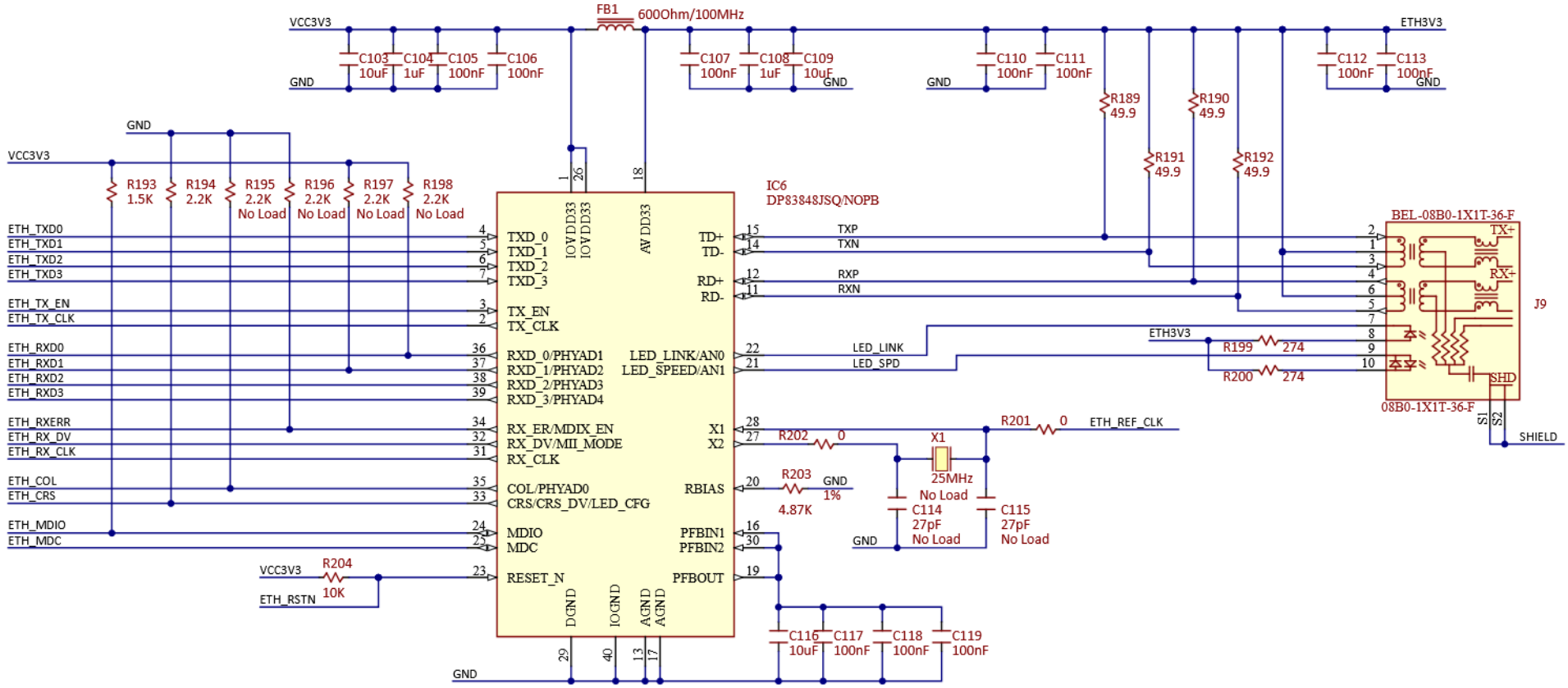




Title	Arty A7
Rev	E.2
Circuit	FPGA Power
Doc#	500-319
Engineer	MTA
Author	GMA
Date	1/25/2022
Sheet#	7 out of 12

DIGILENT

Copyright 2022



NOTE: REF_CLK In Mode (ETH_REF_CLK = 25MHz)

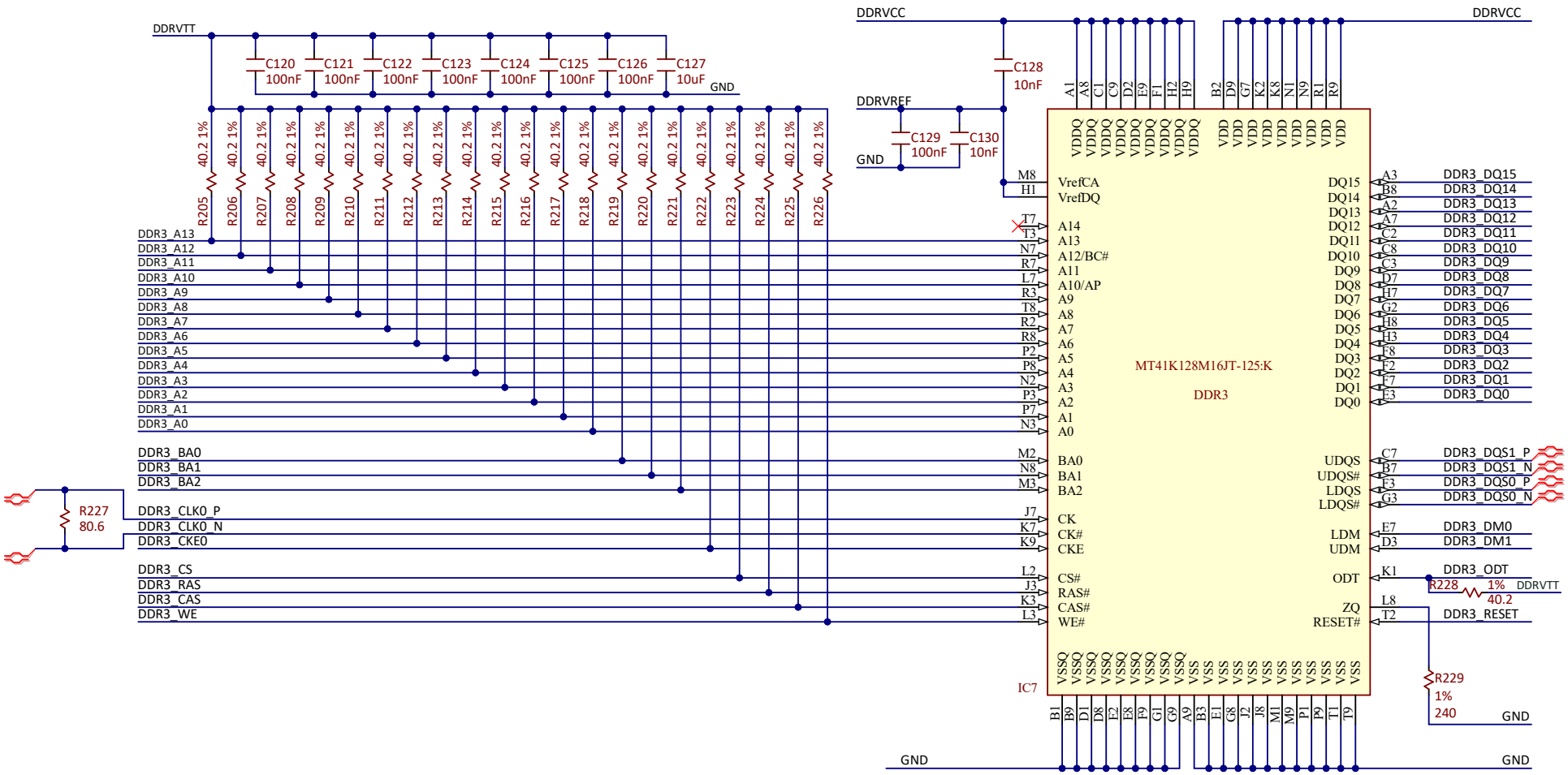
NOTE: PHY MDIO Address = 00001

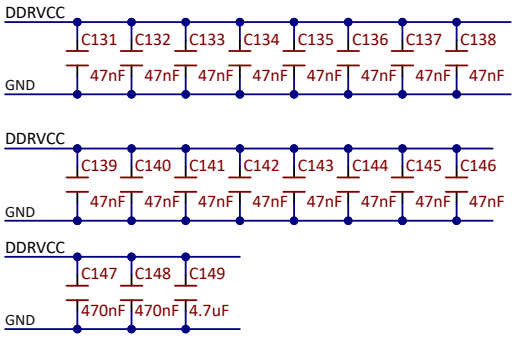
Title	Rev
Arty A7	E.2

Circuit	ETHERNET
Doc#	500-319
Engineer	MTA
Author	GMA
Date	1/25/2022
Sheet#	8 out of 12

DIGILENT

Copyright 2022





Title	Rev
Arty A7	E.2

Circuit	DDR3
Doc#	500-319
Engineer	MTA
Author	GMA
Date	1/25/2022
Sheet#	9 out of 12

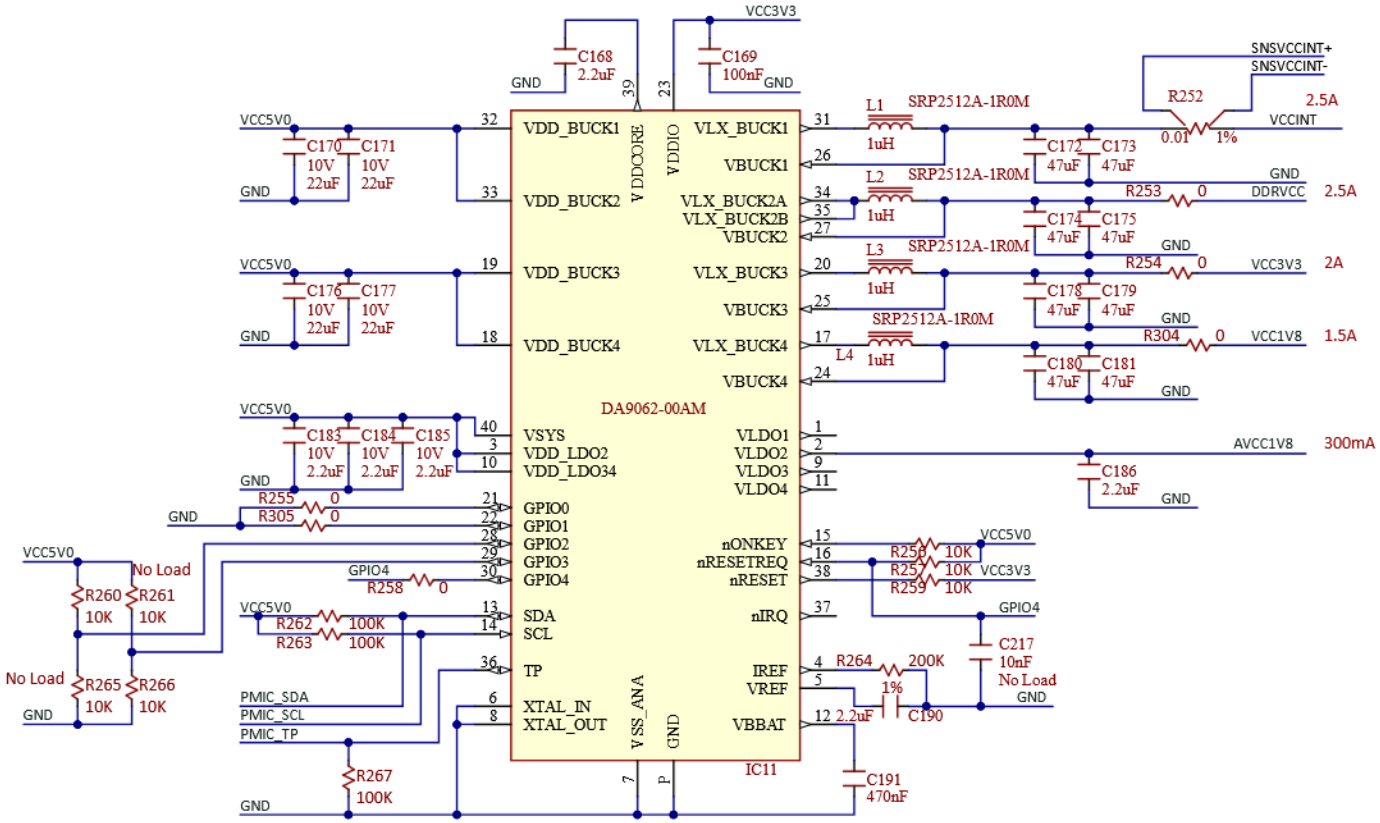
DIGILENT

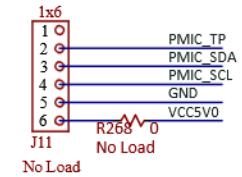
Copyright 2022

This page intentionally left blank.

Title	Arty A7
Rev	E.2
Circuit	USB PROG/UART
Doc#	500-319
Engineer	MTA
Author	GMA
Date	1/25/2022
Sheet#	10 out of 12

Copyright 2022





VCCINT Voltage Configuration

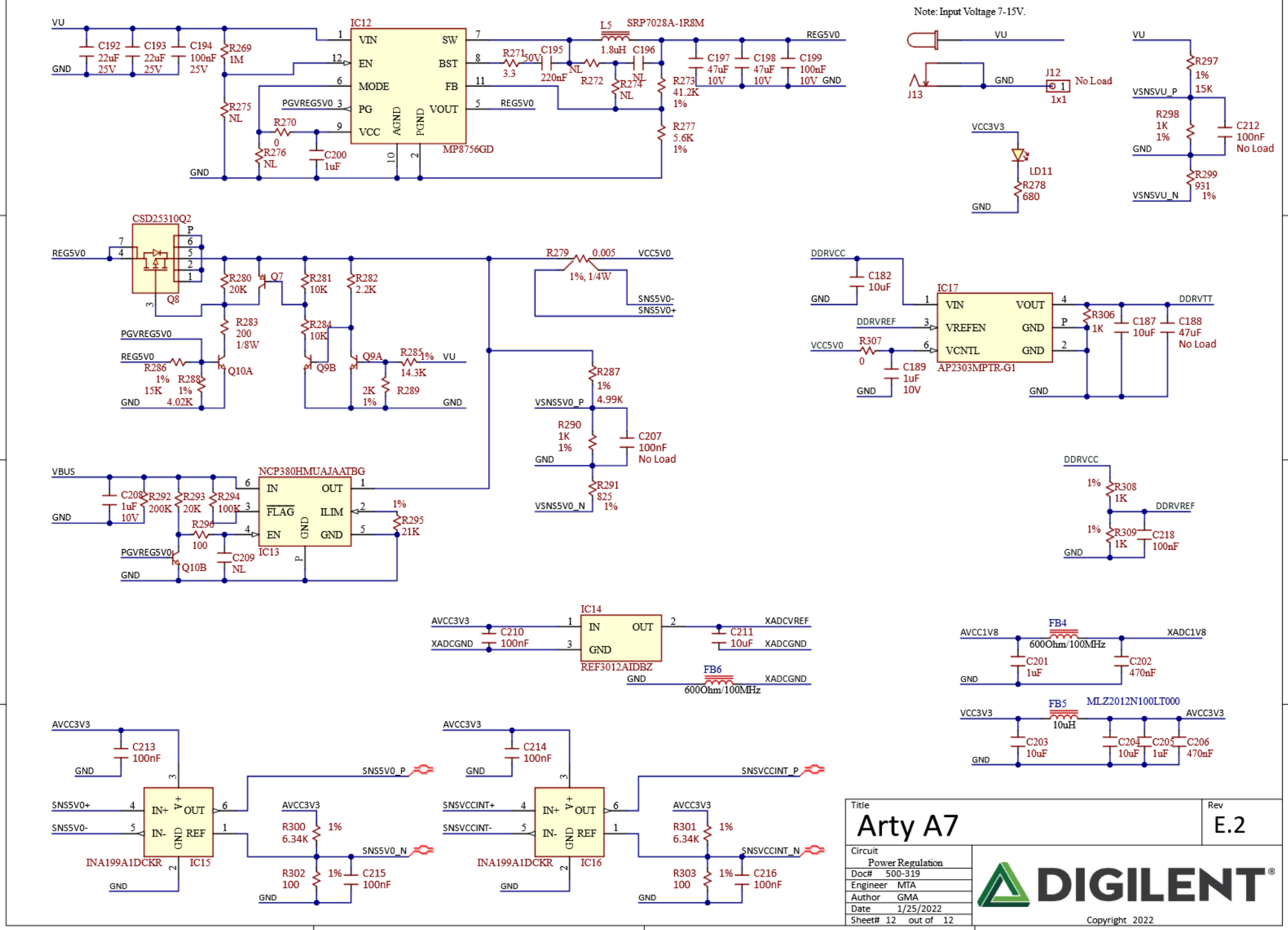
R260	R265	VCCINT
Load	No Load	1.0V
No Load	Load	0.95V

DDR Voltage Configuration

R261	R266	DDRVCC	DDRVTT
Load	No Load	1.5V	0.75V
No Load	Load	1.35V	0.675V

Title	Arty A7
Rev	E.2
Circuit	Power Regulation
Doc#	500-319
Engineer	MTA
Author	GMA
Date	1/25/2022
Sheet#	11 out of 12

Copyright 2022



Title: Arty A7

Rev: E.2

Circuit: Power Regulation

Doc# 500-319

Engineer MTA

Author GMA

Date 1/25/2022

Sheet# 12 out of 12

DIGILENT

Copyright 2022