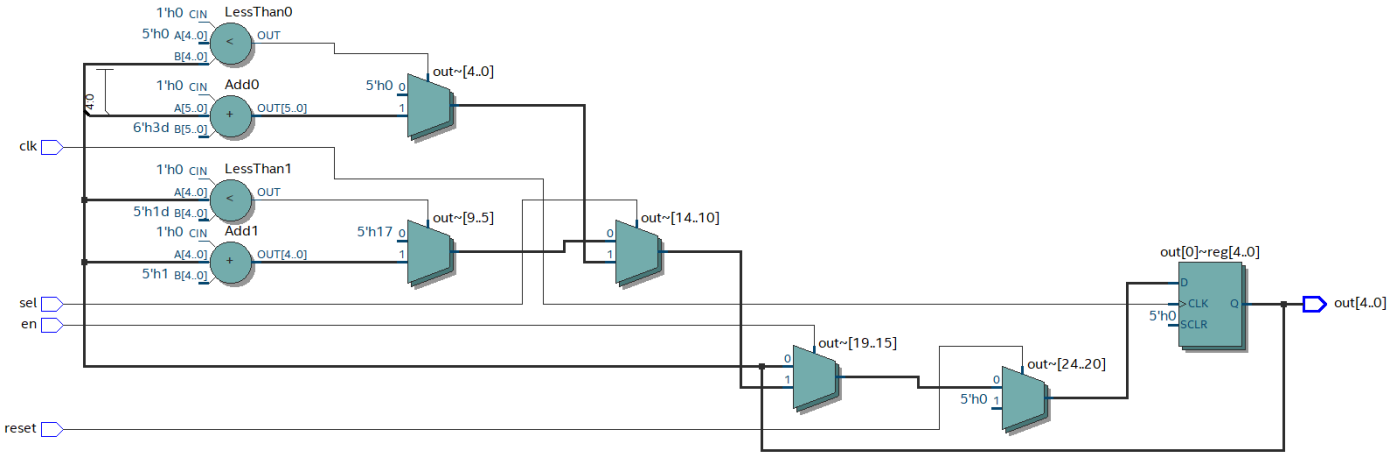
VSD HW2

F64091130 楊采語

Behavioral

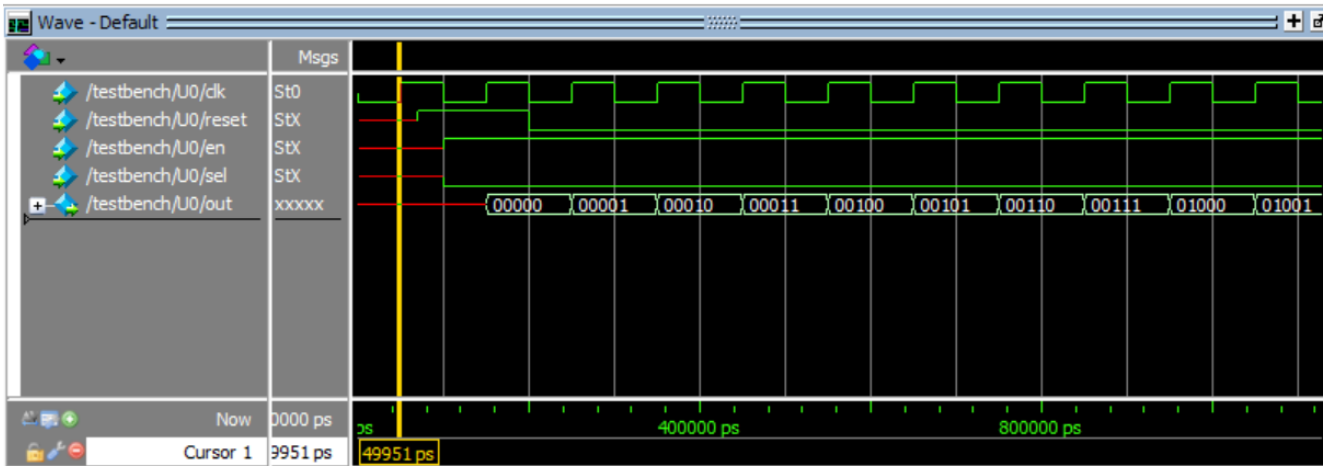
(1) 設計原理(硬體架構圖)



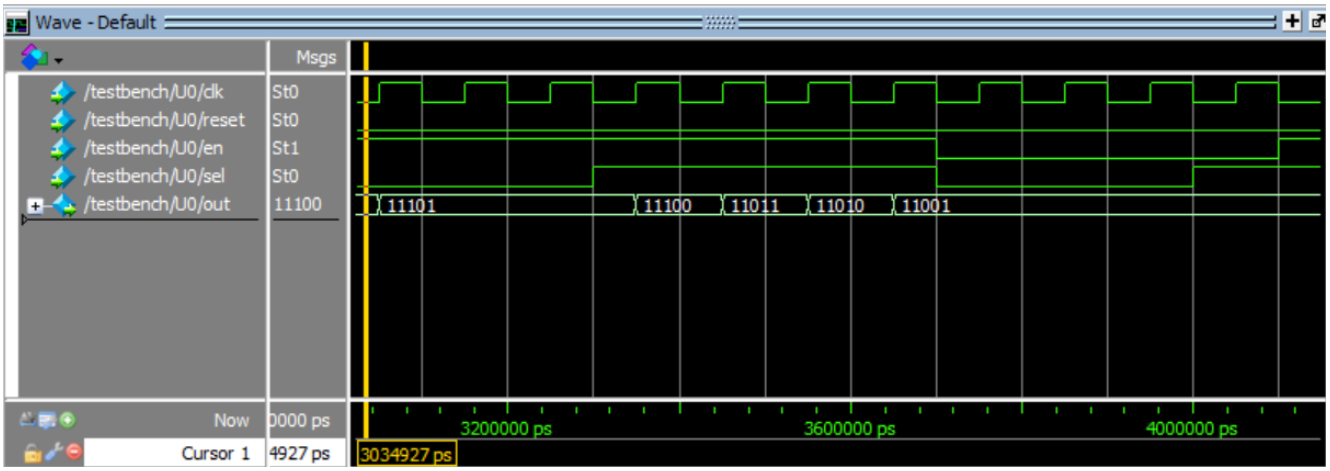
(2) 模擬結果 (波型及結果分析)

```
Command: /home/ncku_class/vsd_2024/vsd202472/F64091130_hw2/Behavior/./simv -a vcs.log
Chronologic VCS simulator copyright 1991-2023
Contains Synopsys proprietary information.
Compiler version V-2023.12-SP1_Full164; Runtime version V-2023.12-SP1_Full164;  Oct 19 14:53 2024
************************************************
***********      Simulation Start      ***********
************************************************
************************************************
***********          ALL PASS          ***********
************************************************
$finish called from file "testbench.v", line 74.
$finish at simulation time             10150000
           V C S   S i m u l a t i o n   R e p o r t
Time: 10150000 ps
CPU Time:      0.180 seconds;       Data structure size:   0.0Mb
Sat Oct 19 14:53:24 2024
CPU time: .237 seconds to compile + .197 seconds to elab + .165 seconds to link + .208 seconds in simulation
```

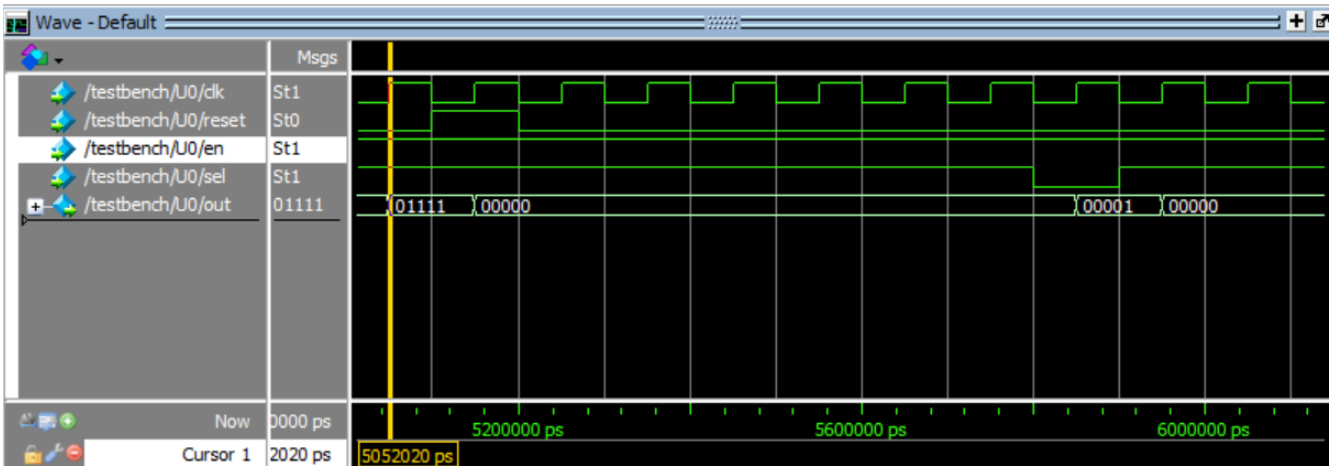
波型：reset + count up



波型：count up(維持在 29)、count down、en = 0 (維持)

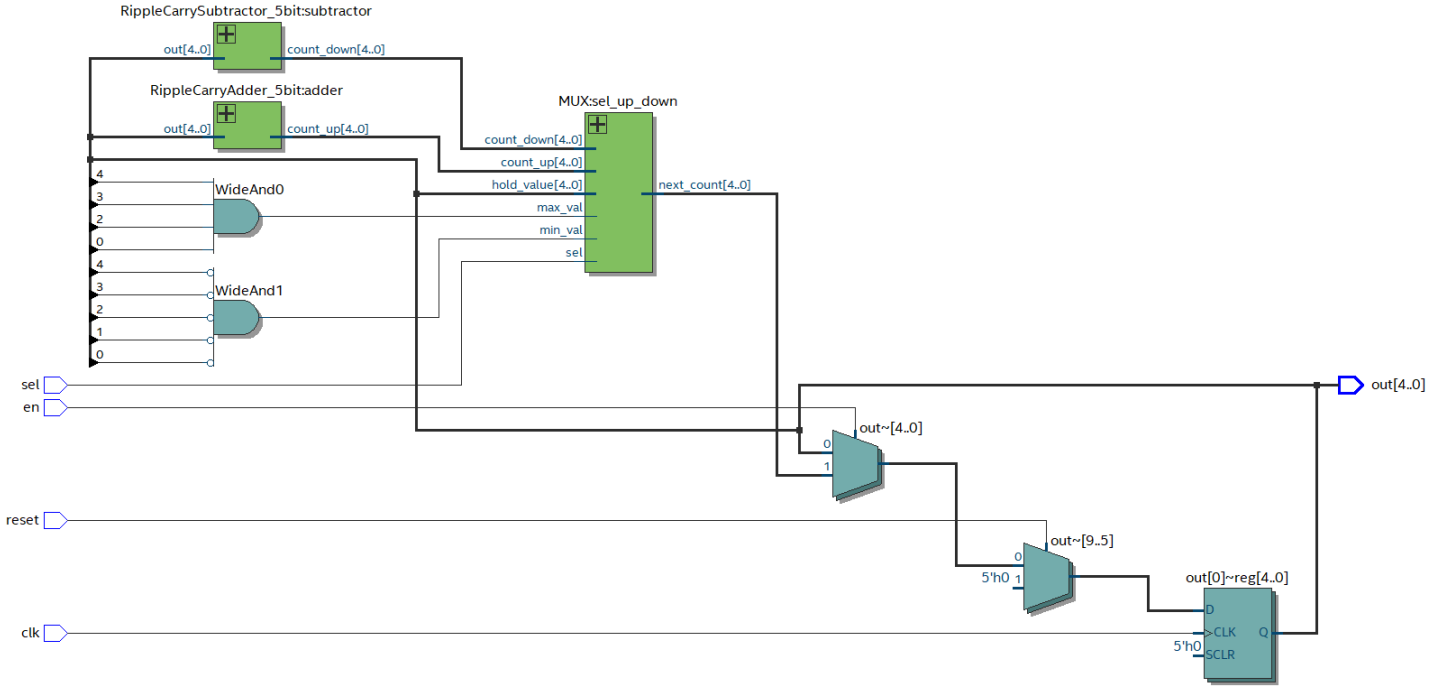


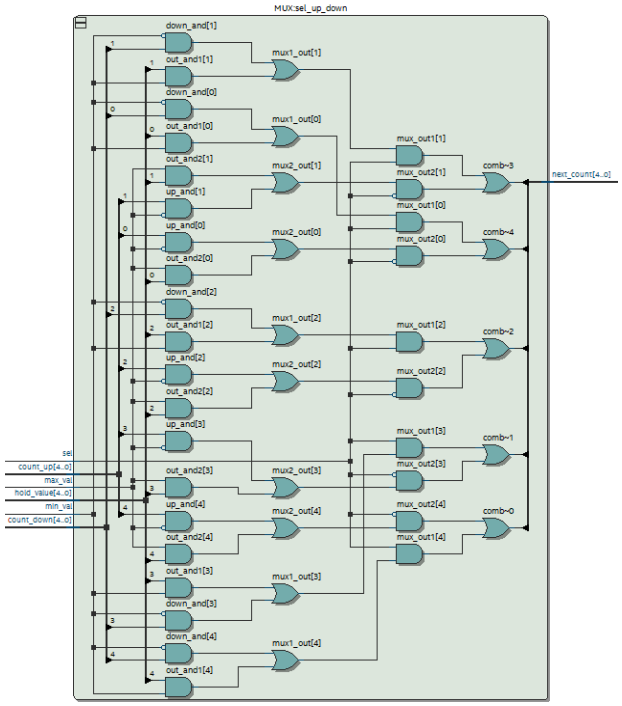
波型：reset、count down(維持在 0)

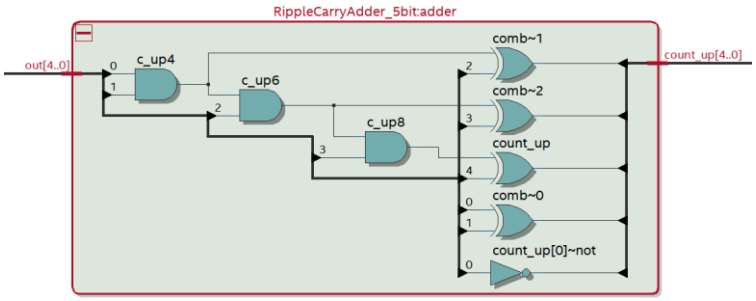


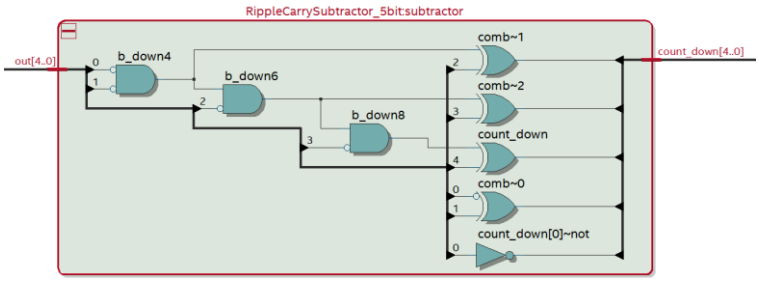
Structural

(1) 設計原理(硬體架構圖)





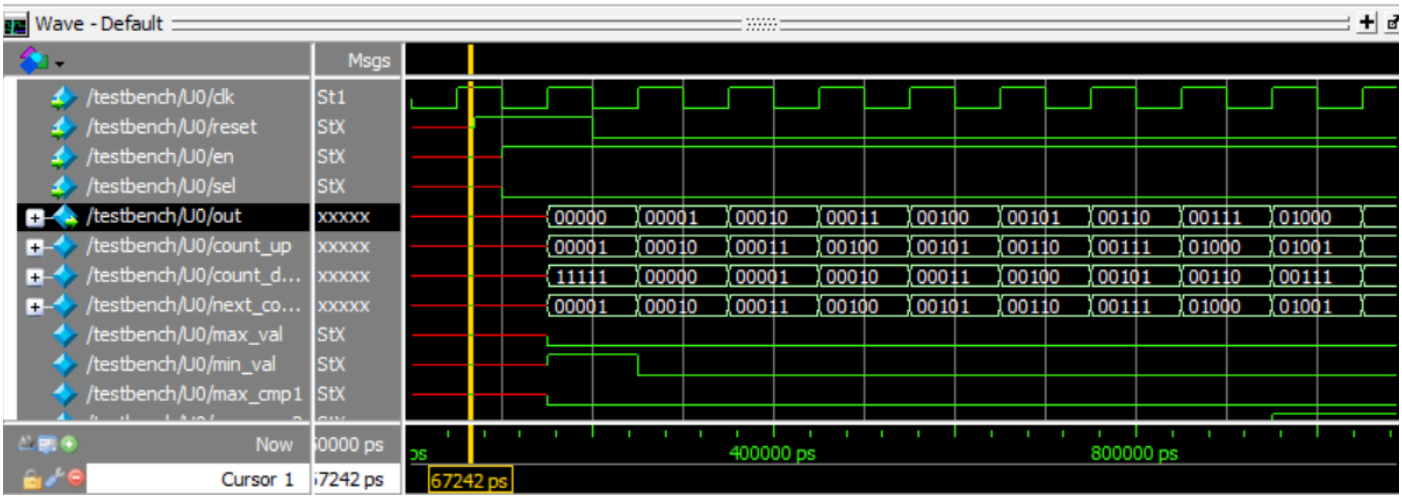




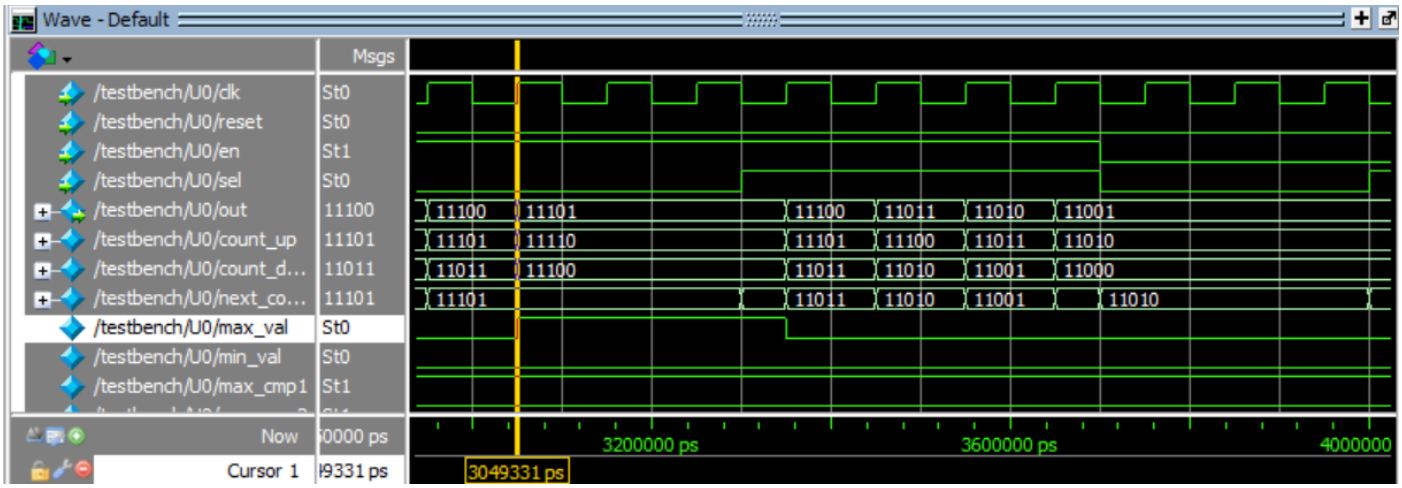
(3) 模擬結果 (波型及結果分析)

```
Compiler version V-2023.12-SP1_Full64; Runtime version V-2023.12-SP1_Full64;  Oct 19 15:00 2024
************************************************
***********      Simulation Start      ***********
************************************************
************************************************
***********          ALL PASS          ***********
************************************************
$finish called from file "testbench.v", line 74.
$finish at simulation time             10150000
           V C S   S i m u l a t i o n   R e p o r t
Time: 10150000 ps
CPU Time:      0.200 seconds;       Data structure size:   0.0Mb
Sat Oct 19 15:00:19 2024
CPU time: .242 seconds to compile + .206 seconds to elab + .161 seconds to link + .227 seconds in simulation
[vsd202472@tsri17 Structure]$
```

波型：reset、count up



波型：count up(維持在 29)、count down、en = 0 (維持)



波型：reset、count down(維持在 0)