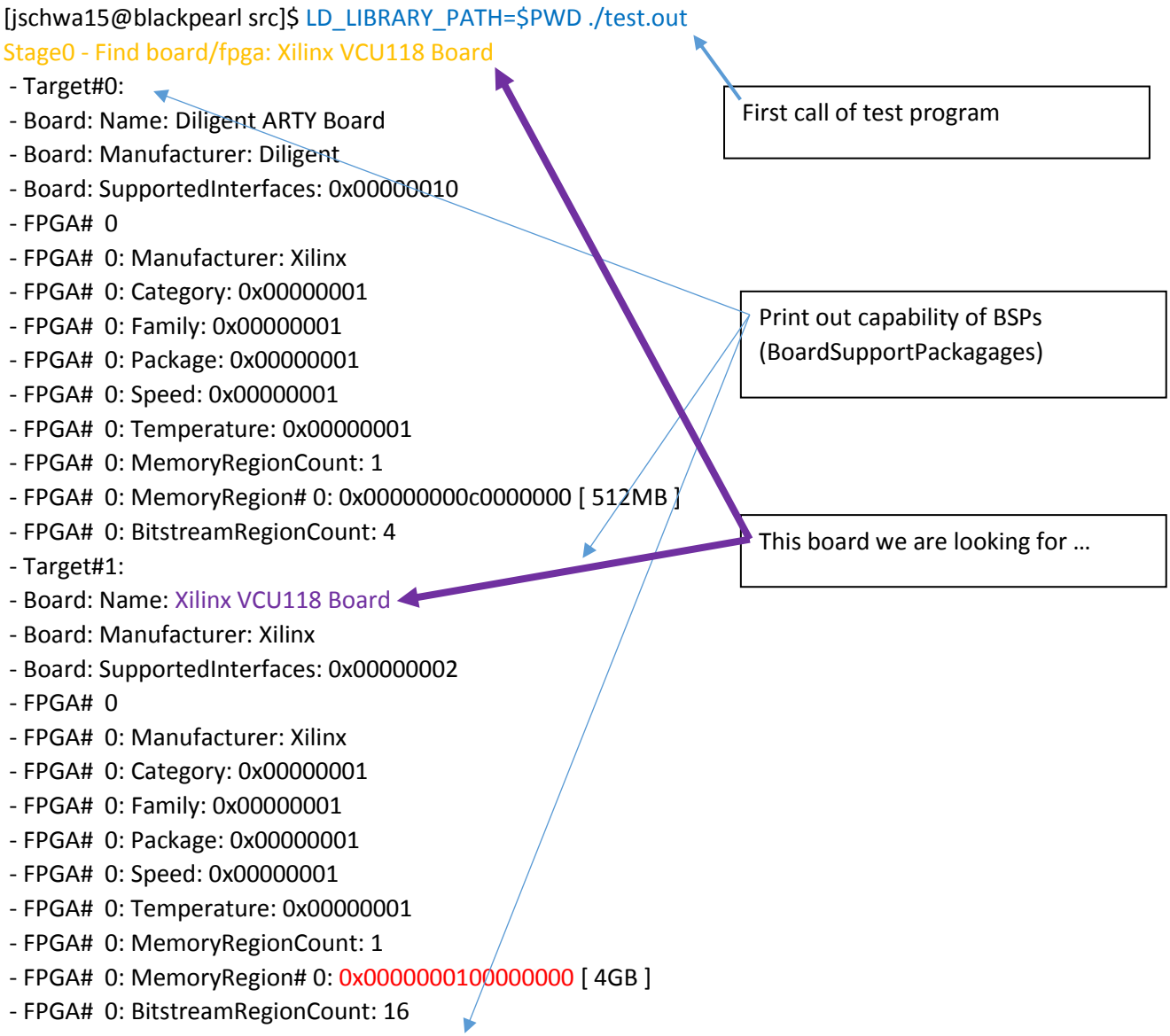
[jschwa15@blackpearl src]$ LD_LIBRARY_PATH=$PWD ./test.out
Stage0 - Find board/fpga: Xilinx VCU118 Board
- Target#0:
- Board: Name: Diligent ARTY Board
- Board: Manufacturer: Diligent
- Board: SupportedInterfaces: 0x00000010
- FPGA# 0
- FPGA# 0: Manufacturer: Xilinx
- FPGA# 0: Category: 0x00000001
- FPGA# 0: Family: 0x00000001
- FPGA# 0: Package: 0x00000001
- FPGA# 0: Speed: 0x00000001
- FPGA# 0: Temperature: 0x00000001
- FPGA# 0: MemoryRegionCount: 1
- FPGA# 0: MemoryRegion# 0: 0x00000000c0000000 [512MB]
- FPGA# 0: BitstreamRegionCount: 4
- Target#1:
- Board: Name: Xilinx VCU118 Board
- Board: Manufacturer: Xilinx
- Board: SupportedInterfaces: 0x00000002
- FPGA# 0
- FPGA# 0: Manufacturer: Xilinx
- FPGA# 0: Category: 0x00000001
- FPGA# 0: Family: 0x00000001
- FPGA# 0: Package: 0x00000001
- FPGA# 0: Speed: 0x00000001
- FPGA# 0: Temperature: 0x00000001
- FPGA# 0: MemoryRegionCount: 1
- FPGA# 0: MemoryRegion# 0: 0x0000000100000000 [4GB]
- FPGA# 0: BitstreamRegionCount: 16
- Target#2:
- Board: Name: Xilinx VC709 Board
- Board: Manufacturer: Xilinx
- Board: SupportedInterfaces: 0x00000001
- FPGA# 0
- FPGA# 0: Manufacturer: Xilinx
- FPGA# 0: Category: 0x00000001
- FPGA# 0: Family: 0x00000001
- FPGA# 0: Package: 0x00000001
- FPGA# 0: Speed: 0x00000001
- FPGA# 0: Temperature: 0x00000001
- FPGA# 0: MemoryRegionCount: 1
- FPGA# 0: MemoryRegion# 0: 0x0000000080000000 [8GB]
- FPGA# 0: BitstreamRegionCount: 10
- FPGA Memory usage (max values)
- Address: 0x0000000100000000-0x00000001ffffffff [0x0000000100000000 Bytes]
Stage1 - OpenFPGA
: Handles(4): 3, 4, 5, 6
: MMap: 0x0x7f1cac832000
First call of test program
Print out capability of BSPs
(BoardSupportPackagages)
This board we are looking for …

: ORKAGD_TargetOpen: rv=0
Stage2 - Operate on FPGA
Stage3 - Copy memory to FPGA
Stage4 - Start IP
Stage5 - Wait for IP
: NumLoops=1
Stage6 - Copy back memory from FPGA

Print out first 4 memory bytes ...
Value @ 0x0000000100000000: 0x00000001

Stage7 - Close FPGA
Stage8 - Close Board

(Clears memory)

(Busy waiting)

HLS IP:

```
#include "mm.h"
#include <stdint.h>
#include <memory.h>

void MatrixMul( volatile uint32_t *axi )
{
#pragma HLS INTERFACE s_axilite port=return
#pragma HLS INTERFACE m_axi depth=64 offset=slave port=axi

  axi[0]++;
}
```

The Address we got from the BSP

[jschwa15@blackpearl src]$ LD_LIBRARY_PATH=$PWD ./test.out -n
Parameter given: -n
* no initial memcopy ...
Stage0 - Find board/fpga: Xilinx VCU118 Board
- Target#0:
- Board: Name: Diligent ARTY Board
- Board: Manufacturer: Diligent
- Board: SupportedInterfaces: 0x00000010
- FPGA# 0
- FPGA# 0: Manufacturer: Xilinx
- FPGA# 0: Category: 0x00000001
- FPGA# 0: Family: 0x00000001
- FPGA# 0: Package: 0x00000001
- FPGA# 0: Speed: 0x00000001
- FPGA# 0: Temperature: 0x00000001
- FPGA# 0: MemoryRegionCount: 1
- FPGA# 0: MemoryRegion# 0: 0x00000000c0000000 [512MB]
- FPGA# 0: BitstreamRegionCount: 4
- Target#1:
- Board: Name: Xilinx VCU118 Board
- Board: Manufacturer: Xilinx
- Board: SupportedInterfaces: 0x00000002
- FPGA# 0
- FPGA# 0: Manufacturer: Xilinx
- FPGA# 0: Category: 0x00000001
- FPGA# 0: Family: 0x00000001
- FPGA# 0: Package: 0x00000001
- FPGA# 0: Speed: 0x00000001
- FPGA# 0: Temperature: 0x00000001
- FPGA# 0: MemoryRegionCount: 1
- FPGA# 0: MemoryRegion# 0: 0x0000000100000000 [4GB]
- FPGA# 0: BitstreamRegionCount: 16
- Target#2:
- Board: Name: Xilinx VC709 Board

Second call of test program. This time we use parameter '-n'.

Here we omit stage 3 where the memory is cleared:

So we DO NOT CLEAR memory.

```
 - Board: Manufacturer: Xilinx
 - Board: SupportedInterfaces: 0x00000001
 - FPGA#  0
 - FPGA#  0: Manufacturer: Xilinx
 - FPGA#  0: Category: 0x00000001
 - FPGA#  0: Family: 0x00000001
 - FPGA#  0: Package: 0x00000001
 - FPGA#  0: Speed: 0x00000001
 - FPGA#  0: Temperature: 0x00000001
 - FPGA#  0: MemoryRegionCount: 1
 - FPGA#  0: MemoryRegion# 0: 0x0000000080000000 [ 8GB ]
 - FPGA#  0: BitstreamRegionCount: 10
 - FPGA Memory usage (max values)
 - Address: 0x0000000100000000-0x00000001ffffffff [0x0000000100000000 Bytes]
Stage1 - OpenFPGA
 : Handles(4): 3, 4, 5, 6
 : MMap: 0x0x7f704d6e1000
 : ORKAGD_TargetOpen: rv=0
Stage2 - Operate on FPGA
Stage3 - nothing happens here (switched off by parameter '-n')
Stage4 - Start IP
Stage5 - Wait for IP
 : NumLoops=1
Stage6 - Copy back memory from FPGA

Print out first 4 memory bytes ...
Value @ 0x0000000100000000: 0x00000002

Stage7 - Close FPGA
Stage8 - Close Board
```

Thats what we want to see: A prove that the first seen 0x000000001 from the first test was not a random number.

Our IP incremented the first 0x00000001 into 0x00000002 !

Hurray ☺!