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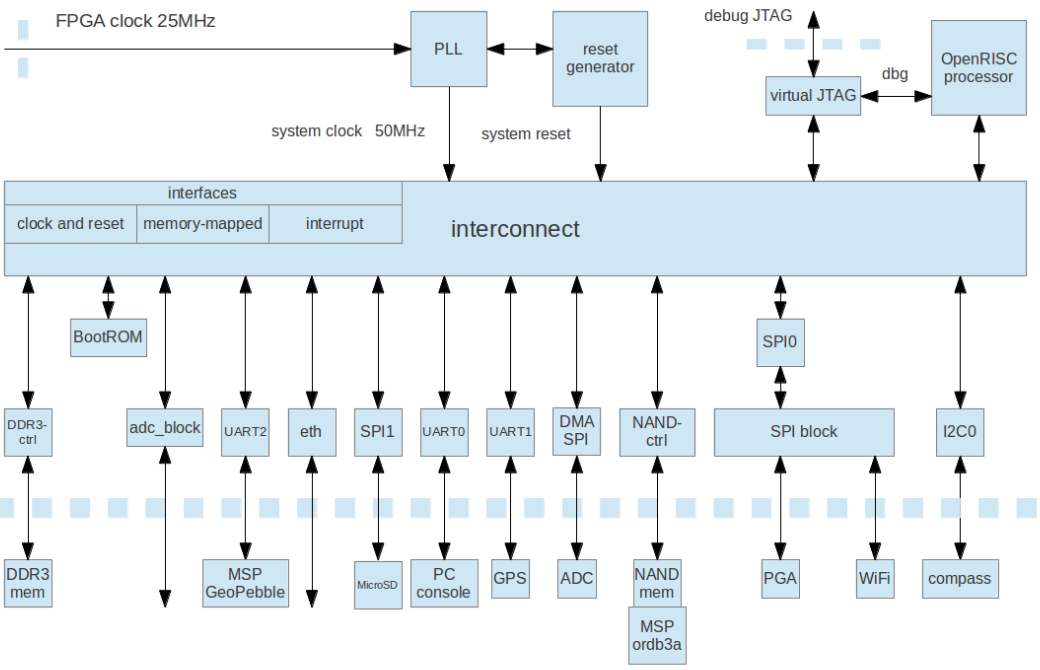
FPGA System



Interconnect

The interconnect handles clock and reset networks, memory-mapped networks and the interrupt networks. The system with the OpenRISC processor runs at a frequency of 50MHz. The memory-mapped network is a shared bus system with round-robin arbitration where all master have the same weight.

Memory

DDR3

2 685 075 456 bytes of memory and runs at a frequency of 305MHz.

NAND

1 342 537 728 bytes of memory. Holds the FPGA programming file and Linux OS.

Reset

After power up reset is released when the PLL acquires lock.

OpenRISC Processor

When reset is released the processor starts to read the BootROM.

BootROM

~~The BootROM contains a small program that loads the Linux OS from the NAND-flash memory and store it to the DDR3 memory. The processor then boot Linux OS from the DDR3 memory.~~

The BootROM contains a small program that set register r0 to zero and then loops.

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Memory-Mapped address

Slave	Address	
	Base	End
BootROM	0xf0000100	0xf00001ff
DDR3	0x00000000	0x0fffffff
NAND-ctrl	0xf1000000	0xf100001f
UART0	0x90000000	0x90000007
UART1	0x91000000	0x91000007
UART2	0x93000000	0x93000007
SPI0	0xb0000000	0xb000001f
DMA_SPI	0xb1000000	0xb100003f
I2C0	0xa0000000	0xa0000007
adc_block	0xc0000000	0xc00003ff
SPI1	0xb2000000	0x9e0000ff
eth	0x92000000	0x92000fff

Memory-Mapped IRQ

Slave	IRQ
UART0	2
UART1	3
UART2	4
SPI0	7
DMA_SPI(SPI)	8
DMA_SPI(DMA)	9
I2C0	14
adc_block	20
SPI1	10
eth	26

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SPI Block

There is one SPI-controller for both the WiFi and the PGA:as. Use the slave select signal to select the right device.

SS SPI Block	SS Device	SS register SPI-controller
ss_0	PGA(u2)	0x1
ss_1	PGA(u4)	0x2
ss_2	PGA(u6)	0x4
ss_3	PGA(u8)	0x8
ss_4	reserved	reserved
ss_5	reserved	reserved
ss_6	WiFi	0x40
ss_7	reserved	reserved

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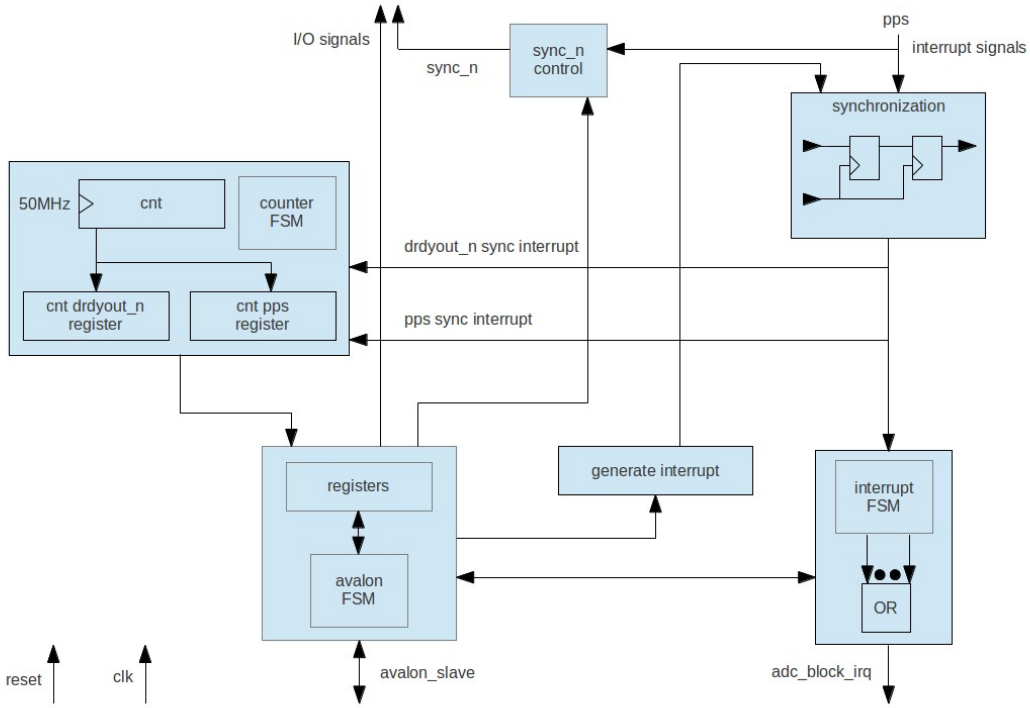
ADC Block



Registers

All registers are cleared on reset.

CNT register

Description

This counter runs on the system clock. It counts up one every clock cycle. This counter value is sampled and store into two other counter registers CNT PPS and CNT DRDYOUT_N.

Register bits

Nr	Name	Access	Description
Bit32..0	counter value	none	This register holds a 32-bit value. This register is cleared on a gps_pps interrupt.

INTERRUPT register

Description

There is only one interrupt signal to the OpenRISC processor from the adc-block. All interrupt signals from the GeoPebble board are OR:ed to this signal. Use this register to see which interrupt that triggered and to clear a interrupt. All interrupts are edge-triggered.

Address

0xc0000000

Register bits

Nr	Name	Access	Description
bit0	gps_pps	r/w	Handles interrupt on the gps_pps signal.

bit1	adc_drdyout_n	r/w	Handles interrupt on the adc_drdyout_n signal.
bit2	wifi_intr	r/w	Handles interrupt on the wifi_intr signal.
bit3	compass_int1	r/w	Handles interrupt on the compass_int1 signal.

Read
Reading a 1 for a bit in this register indicates interrupt on that signal. This bit will stay 1 until cleared.

Write
Writing a 1 to a bit in this register will clear that bit.

IRQ MASK register

Description
Use this register to mask the different interrupts.

Address
0xc0000010

Register bits

Nr	Name	Access	Description
bit0	irq_gps_pps	r/w	If bit is zero, interrupt is disable.
bit1	irq_drdyout_n	r/w	If bit is zero, interrupt is disable.
bit2	irq_intr	r/w	If bit is zero, interrupt is disable.
bit3	irq_compass_int1	r/w	If bit is zero, interrupt is disable.

DRDYOUT_N CNT register

Description
This register samples and holds the value that CNT register has when there is a interrupt on the adc_drdyout_n signal.

Address
0xc0000004

Register bits

Nr	Name	Access	Description
bit31..0	counter value	r	This register holds a 32-bit value. This value changes only on a adc_drdyout_n interrupt.

PPS CNT register

Description
This register samples and holds the value that CNT register has when there is a interrupt on the gps_pps signal.

Address
0xc0000008

Register bits

Nr	Name	Access	Description

bit31..0	counter value	r	This register holds a 32-bit value. This value changes only on a gps_pps interrupt.

ADC register

Description
This register controls the adc signals and for generating a adc_drdyout_n interrupt.

Address
0xc0000040

Register bits

Nr	Name	Access	Description
bit0	enable bit1/bit2 function	r/w	This bit set to 1 enables bit1 function, bit set to 0 enables bit2 function.
bit1	pps to sync_n	r/w	This bit set to 1 will drive the sync_n signal on the adc with the incoming pps signal(sync_n = !pps). If set to 0 sync_n will have the value 1.
bit2	sync_n	r/w	This bit is for testing and sets the value of the sync_n signal on the adc.
bit3	enable bit4 function	r/w	This bit set to 1 enables bit4 function.
bit4	generate drdyout_n irq	r/w	This bit is for testing and can be used to generate a adc_drdyout_n interrupt. Toggle this bit from 0 to 1 to generate.
bit5	ovrflw_n	r	This bit has the value of the ovrflw_n signal on the adc.

GPS register

Description
This register controls the gps signals and for generating a gps_pps interrupt.

Address
0xc0000080

Register bits

Nr	Name	Access	Description
bit0	reset_n	r/w	This bit sets the value of the reset_n signal on the gps.
bit1	extint0	r/w	This bit sets the value of the extint0 signal on the gps.
bit2	enable bit3 function	r/w	This bit set to 1 enables bit3 function.
bit3	generate pps irq	r/w	This bit is for testing and can be used to generate a gps_pps interrupt. Toggle this bit from 0 to 1 to generate.
bit4	pps_valid	r/w	This bit sets the value of the pps_valid signal to the AND gate controlling 1PPS_GATED.

WIFI register

Description
This register controls the wifi signals.

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Address
0xc00000c0

Register bits

Nr	Name	Access	Description
bit0	reset_n	r/w	This bit sets the value of the reset_n signal on the wifi.

MUX register

Description
This register controls the analog switches.

Address
0xc0000100

Register bits

Nr	Name	Access	Description
bit0	in3-in4 (u7, GPIO0)	r/w	This bit sets the value of the in3-in4(GPIO) signal on u7.
bit1	in1-in2 (u7, GPIO1)	r/w	This bit sets the value of the in1-in2(GPIO1) signal on u7.
bit2	in3-in4 (u3, GPIO2)	r/w	This bit sets the value of the in3-in4(GPIO2) signal on u3.
bit3	in1-in2 (u3, GPIO3)	r/w	This bit sets the value of the in1-in2(GPIO3) signal on u3.

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DMA SPI Block

ADC SPI

Description
The SPI connected to the ADC is accessed as normal through it's address space.

Address
0xb1000000

Registers

All registers are cleared on reset.

start_address register

Description
This register holds the address to where the DMA stores data. This register can be read at anytime and it's value increases during a transfer. Gets the value of next_start_address if a new transfer starts.

Address
0xb1000024

Register bits

Nr	Name	Access	Description
bit31..0	start_address	r	This register holds a 32-bit value.

number_of_samples register

Description
This register holds the number of samples the DMA have left. This register can be read at anytime and it's value decreases during a transfer. Gets the value of next_number_of_samples if a new transfer starts.

Address
0xb1000028

Register bits

Nr	Name	Access	Description
bit31..0	number_of_samples	r	This register holds a 32-bit value.

next_start_address register

Description
This register holds the start address of the next DMA transfer. Use this register together with next_number_of_samples. This register can be written during a transfer.

Address
0xb1000030

Register bits

Nr	Name	Access	Description
bit31..0	next_start_address	w	This register holds a 32-bit value.

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next_number_of_samples register

Description
This register holds the number of samples of the next DMA transfer. Use this register when starting a DMA transfer and when the DMA is running. If the DMA is running the next transfer will start seamlessly and without using the DMA Command. If the DMA is not running use the DMA Command to start the DMA.

Address
0xb1000034

Register bits

Nr	Name	Access	Description
bit31..0	start_address	w	This register holds a 32-bit value.

Commands

DMA

Description
Write to this address to start the DMA transfer.

Address
0xb1000020

Clear interrupt

Description
Write to this address to clear the interrupt that is generated for each finished DMA transfer (number_of_samples).

Address
0xb100002c

Sample data

Each sample stored to the DDR3 memory is the four channels from the ADC and the two ADC Block counter values for a total of six words and 24 bytes.

Sample data

Address DDR3 (word)	Data
x = start_address or next_start_address	sample 1, ADC channel 3
x + 0x4	sample 1, ADC channel 2
x + 0x8	sample 1, ADC channel 1
x + 0xc	sample 1, ADC channel 0
x + 0x10	sample 1, cnt pps
x + 0x14	sample 1, cnt drdyout_n
x + 0x18	sample 2, ADC channel 3
•	•

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NAND-ctrl

Description
The NAND-ctrl is used to read the Linux image from the NAND-flash memory and store it to the DDR3 memory when the system boots up. After that it can also be used as a write-only communication to the MSP on the FPGA board. This functionality is described here.

The NAND-ctrl uses the eight NAND IO data lines that also goes to the MSP for the communication. IO0 is used as a strobe signal and the rest IO1-IO7 for data. The MSP will read the data when the strobe signal goes high. Therefore two writes to the NAND-ctrl is needed to transfer seven bytes.

Address
0xf1000000

Registers

All registers are cleared on reset.

write_enable_msp register

Description
Write a one to this register to enable the write to MSP function. Write a zero to disable.

Address
0xf1000010

Register bits

Nr	Name	Access	Description
bit0	write_enable_msp	r	This register holds a 1-bit value.

msp_data register

Description
When the write to MSP function is enabled this register is writable and connected to the NAND-IO signals.

Address
0xf1000014

Register bits

Nr	Name	Access	Description
bit7..0	msp_data	r	This register holds a 8-bit value.