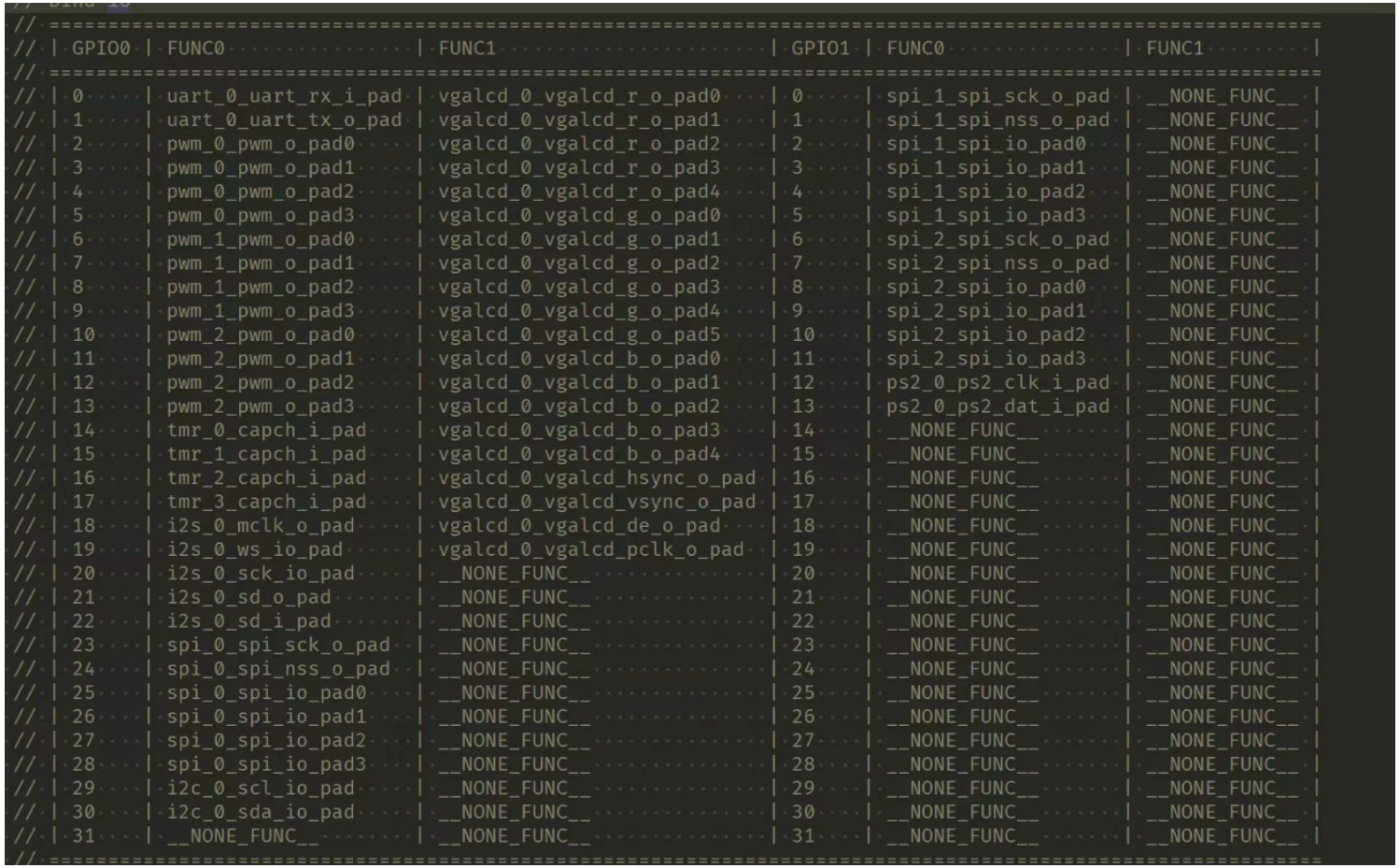
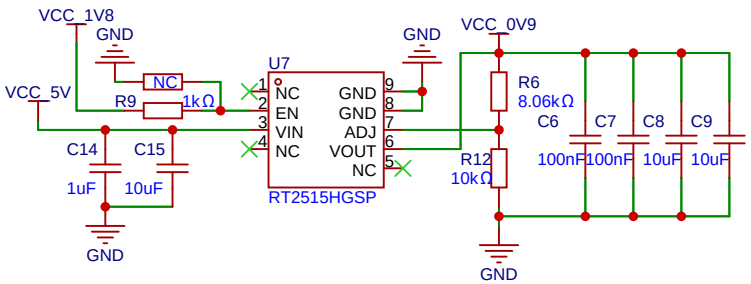
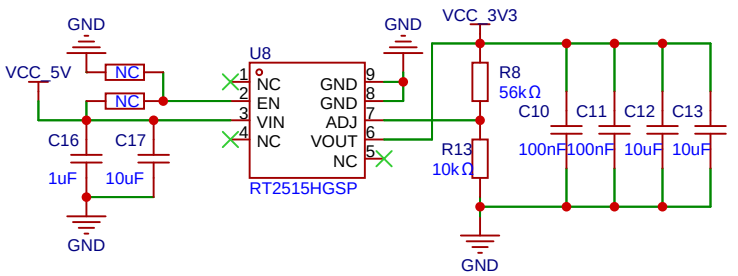


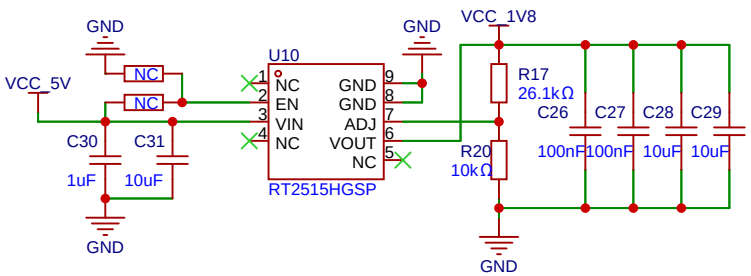
GPIO0	FUNC0	FUNC1	GPIO1	FUNC0	FUNC1
0	uart_0_uart_rx_i_pad	vgalcd_0_vgalcd_r_o_pad0	0	spi_1_spi_sck_o_pad	__NONE_FUNC__
1	uart_0_uart_tx_o_pad	vgalcd_0_vgalcd_r_o_pad1	1	spi_1_spi_nss_o_pad	__NONE_FUNC__
2	pwm_0_pwm_o_pad0	vgalcd_0_vgalcd_r_o_pad2	2	spi_1_spi_io_pad0	__NONE_FUNC__
3	pwm_0_pwm_o_pad1	vgalcd_0_vgalcd_r_o_pad3	3	spi_1_spi_io_pad1	__NONE_FUNC__
4	pwm_0_pwm_o_pad2	vgalcd_0_vgalcd_r_o_pad4	4	spi_1_spi_io_pad2	__NONE_FUNC__
5	pwm_0_pwm_o_pad3	vgalcd_0_vgalcd_g_o_pad0	5	spi_1_spi_io_pad3	__NONE_FUNC__
6	pwm_1_pwm_o_pad0	vgalcd_0_vgalcd_g_o_pad1	6	spi_2_spi_sck_o_pad	__NONE_FUNC__
7	pwm_1_pwm_o_pad1	vgalcd_0_vgalcd_g_o_pad2	7	spi_2_spi_nss_o_pad	__NONE_FUNC__
8	pwm_1_pwm_o_pad2	vgalcd_0_vgalcd_g_o_pad3	8	spi_2_spi_io_pad0	__NONE_FUNC__
9	pwm_1_pwm_o_pad3	vgalcd_0_vgalcd_g_o_pad4	9	spi_2_spi_io_pad1	__NONE_FUNC__
10	pwm_2_pwm_o_pad0	vgalcd_0_vgalcd_g_o_pad5	10	spi_2_spi_io_pad2	__NONE_FUNC__
11	pwm_2_pwm_o_pad1	vgalcd_0_vgalcd_b_o_pad0	11	spi_2_spi_io_pad3	__NONE_FUNC__
12	pwm_2_pwm_o_pad2	vgalcd_0_vgalcd_b_o_pad1	12	ps2_0_ps2_clk_i_pad	__NONE_FUNC__
13	pwm_2_pwm_o_pad3	vgalcd_0_vgalcd_b_o_pad2	13	ps2_0_ps2_dat_i_pad	__NONE_FUNC__
14	tmr_0_capch_i_pad	vgalcd_0_vgalcd_b_o_pad3	14	__NONE_FUNC__	__NONE_FUNC__
15	tmr_1_capch_i_pad	vgalcd_0_vgalcd_b_o_pad4	15	__NONE_FUNC__	__NONE_FUNC__
16	tmr_2_capch_i_pad	vgalcd_0_vgalcd_hsync_o_pad	16	__NONE_FUNC__	__NONE_FUNC__
17	tmr_3_capch_i_pad	vgalcd_0_vgalcd_vsync_o_pad	17	__NONE_FUNC__	__NONE_FUNC__
18	i2s_0_mclk_o_pad	vgalcd_0_vgalcd_de_o_pad	18	__NONE_FUNC__	__NONE_FUNC__
19	i2s_0_ws_io_pad	vgalcd_0_vgalcd_pclk_o_pad	19	__NONE_FUNC__	__NONE_FUNC__
20	i2s_0_sck_io_pad	__NONE_FUNC__	20	__NONE_FUNC__	__NONE_FUNC__
21	i2s_0_sd_o_pad	__NONE_FUNC__	21	__NONE_FUNC__	__NONE_FUNC__
22	i2s_0_sd_i_pad	__NONE_FUNC__	22	__NONE_FUNC__	__NONE_FUNC__
23	spi_0_spi_sck_o_pad	__NONE_FUNC__	23	__NONE_FUNC__	__NONE_FUNC__
24	spi_0_spi_nss_o_pad	__NONE_FUNC__	24	__NONE_FUNC__	__NONE_FUNC__
25	spi_0_spi_io_pad0	__NONE_FUNC__	25	__NONE_FUNC__	__NONE_FUNC__
26	spi_0_spi_io_pad1	__NONE_FUNC__	26	__NONE_FUNC__	__NONE_FUNC__
27	spi_0_spi_io_pad2	__NONE_FUNC__	27	__NONE_FUNC__	__NONE_FUNC__
28	spi_0_spi_io_pad3	__NONE_FUNC__	28	__NONE_FUNC__	__NONE_FUNC__
29	i2c_0_scl_io_pad	__NONE_FUNC__	29	__NONE_FUNC__	__NONE_FUNC__
30	i2c_0_sda_io_pad	__NONE_FUNC__	30	__NONE_FUNC__	__NONE_FUNC__
31	__NONE_FUNC__	__NONE_FUNC__	31	__NONE_FUNC__	__NONE_FUNC__

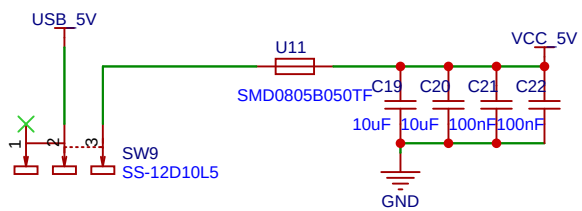
原理图	Schematic1	创建日期	2025-06-05
		更新日期	2025-06-11
板子	Board1	图页	设计概览
绘制		StarrySkyPi	
审阅			
		版本 / 尺寸	页 1 共 7
嘉立创EDA		V1.0 / A4	嘉立创EDA

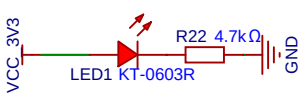
1.8V -> 0.9V <=> 3.3V



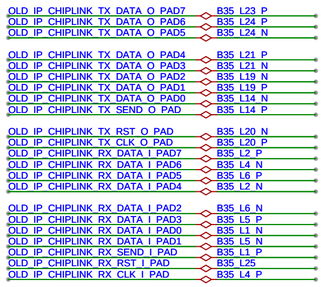


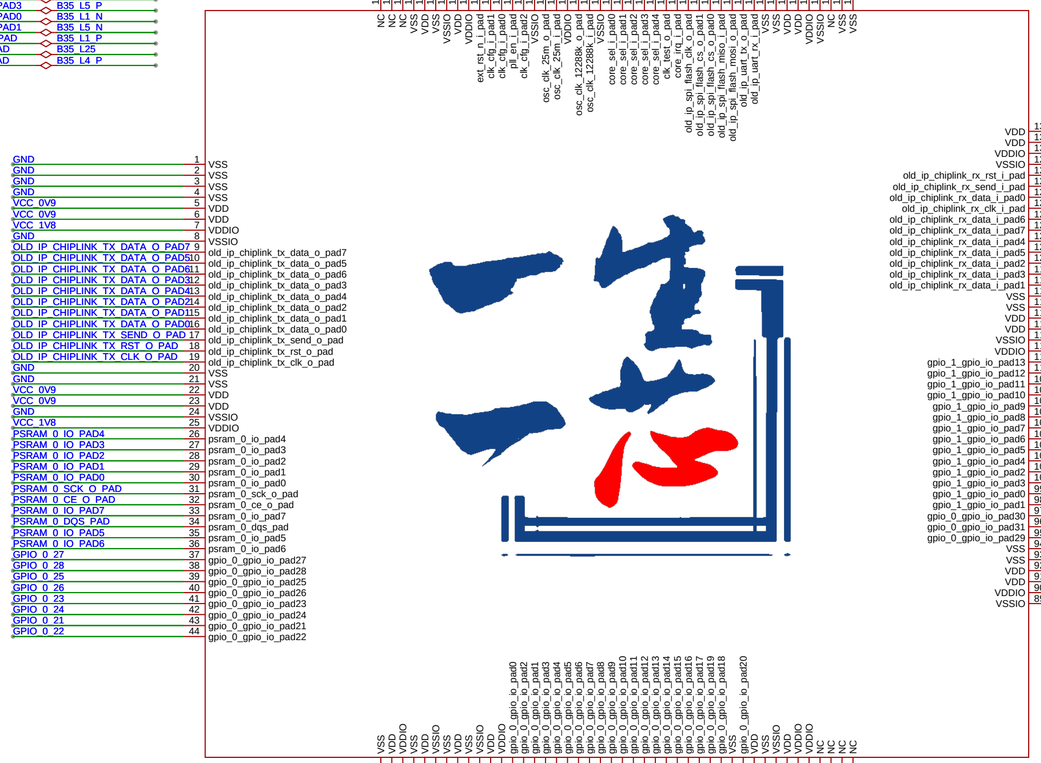






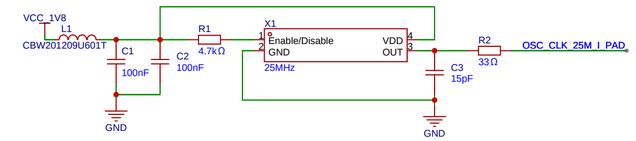
原理图	Schematic1	创建日期	2025-06-05
		更新日期	2025-06-05
板子	Board1	图页	电源模块
绘制		StarrySkyPi	
审阅			
		版本 / 尺寸	页 2 共 7
嘉立创EDA		V1.0 / A4	嘉立创EDA

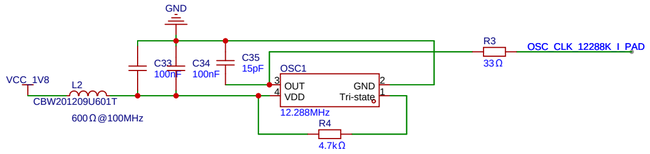




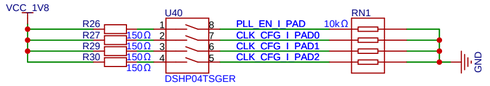
Device
U1

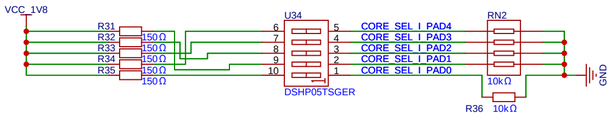
CHIP



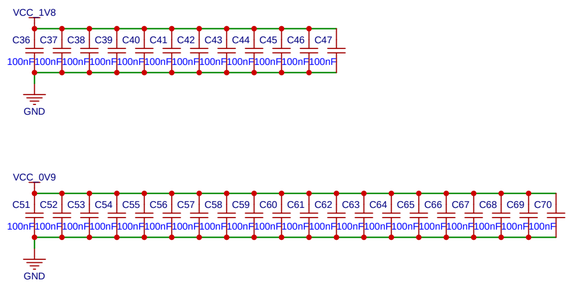


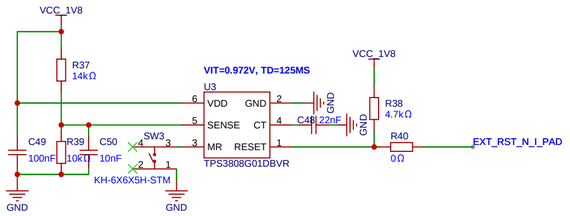
CLK





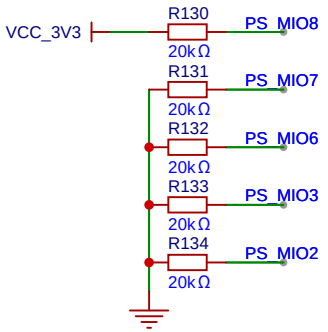
CONFIG_SWITCH



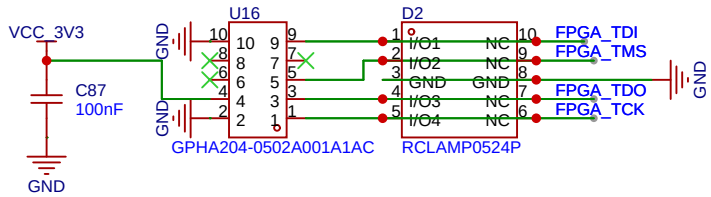


RESET

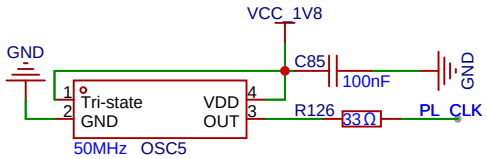
原理图	Schematic1	创建日期	2025-06-05
		更新日期	2025-06-11
板子	Board1	图页	芯片外围
绘制		StarrySkyPi	
审阅			
		版本	V1.0
		尺寸	A4
		页 3 共 7	
嘉立创EDA		嘉立创EDA	



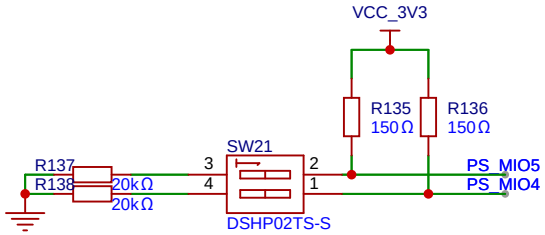
POWER LEVEL



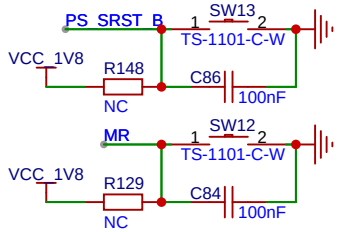
JTAG



PL_CLK

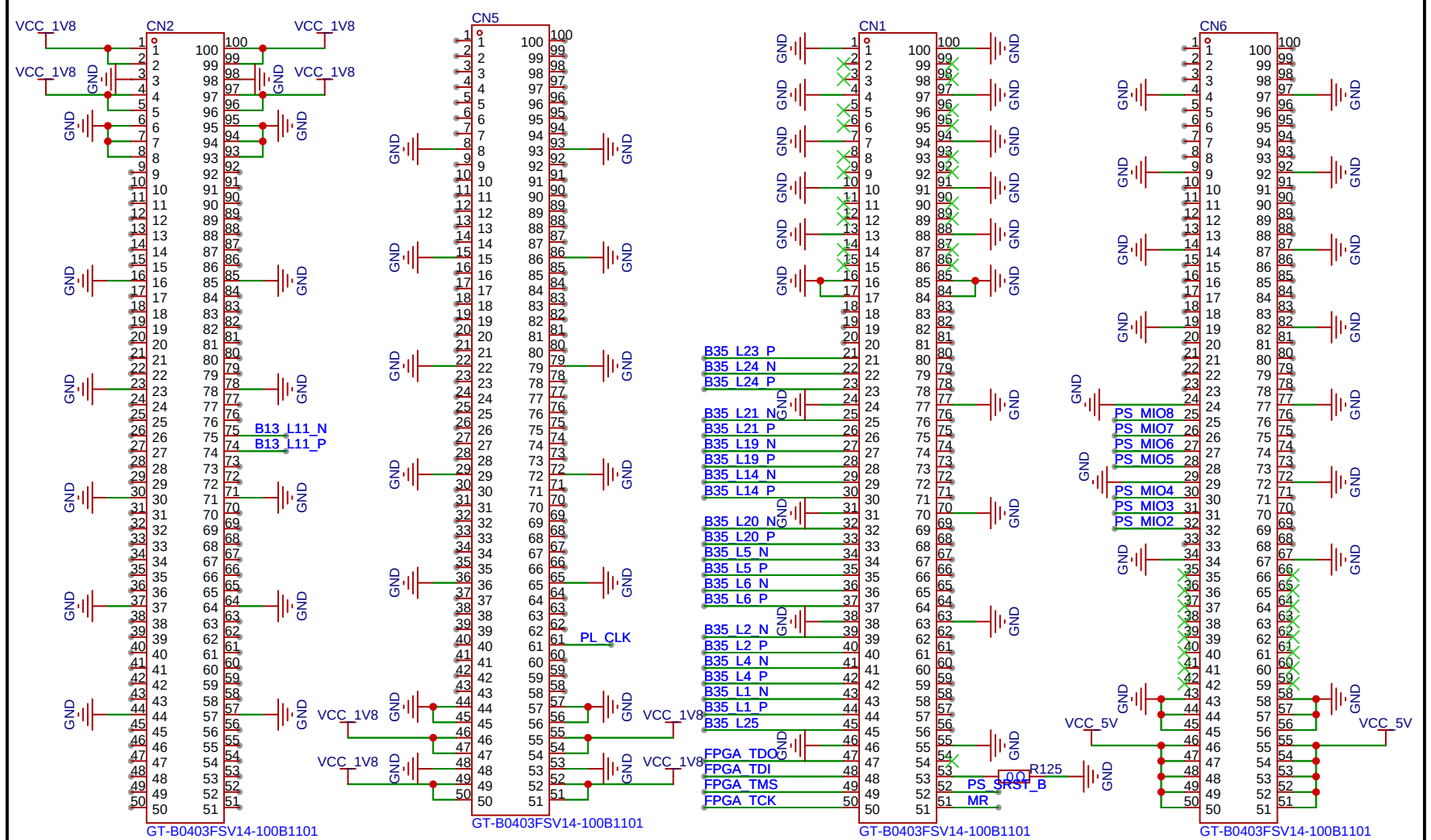


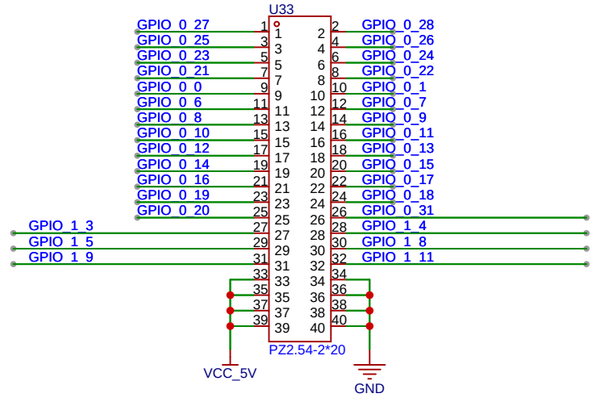
BOOT MODE

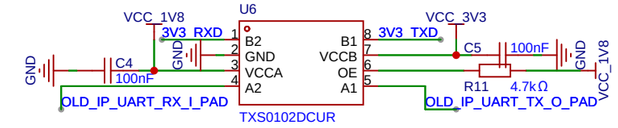


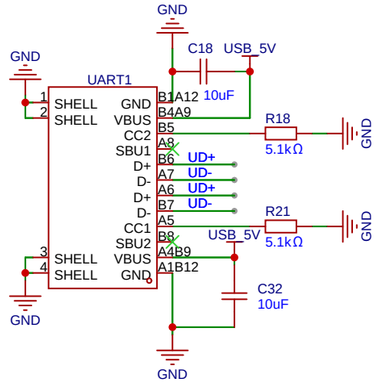
KEY

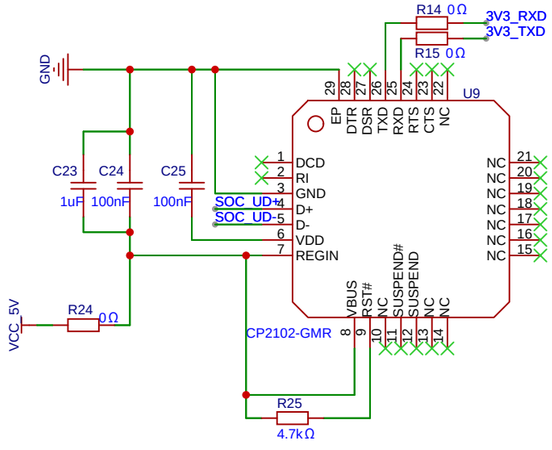
原理图	Schematic1	创建日期	2025-06-05
		更新日期	2025-06-11
板子	Board1	图页	FPGA外围
绘制		StarrySkyPi	
审阅			
		版本	尺寸	页 4 共 7
嘉立创EDA		V1.0	A4	嘉立创EDA





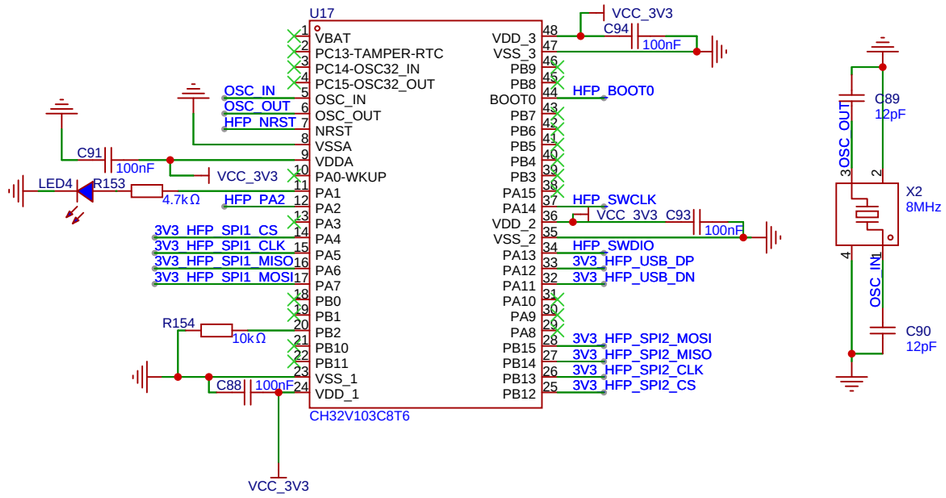




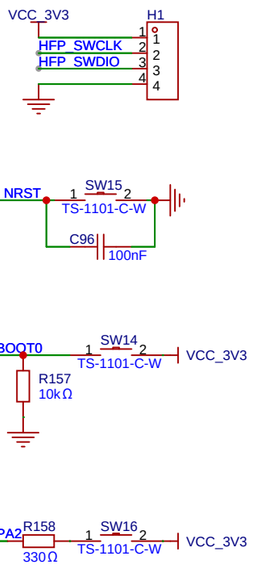


TYPEC

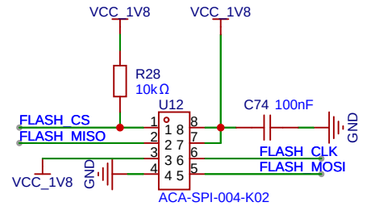
原理图	Schematic1	创建日期	2025-06-05
		更新日期	2025-06-11
板子	Board1	图页	接口电路
绘制		StarrySkyPi	
审阅			
		版本	V1.0
		尺寸	A4
嘉立创EDA		页 5 共 7	嘉立创EDA



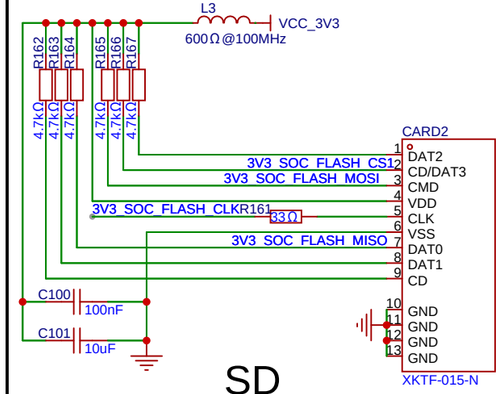
CH32V103C8T6



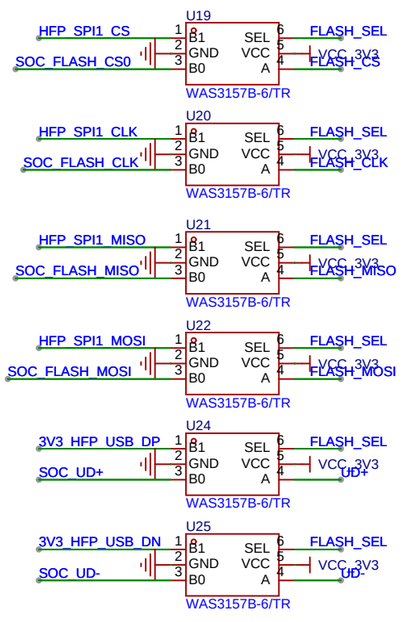
BOOT & JTAG

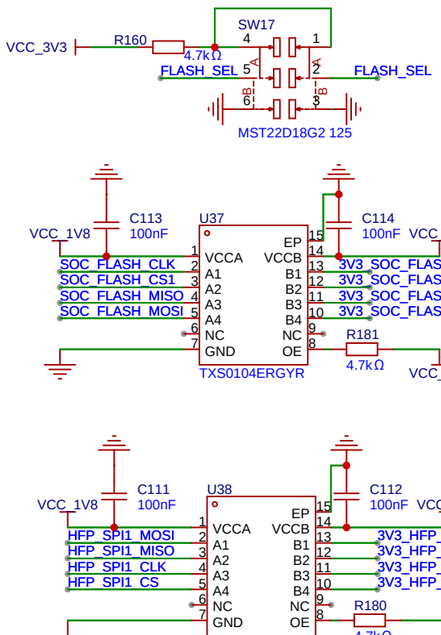


FLASH-SOCKET



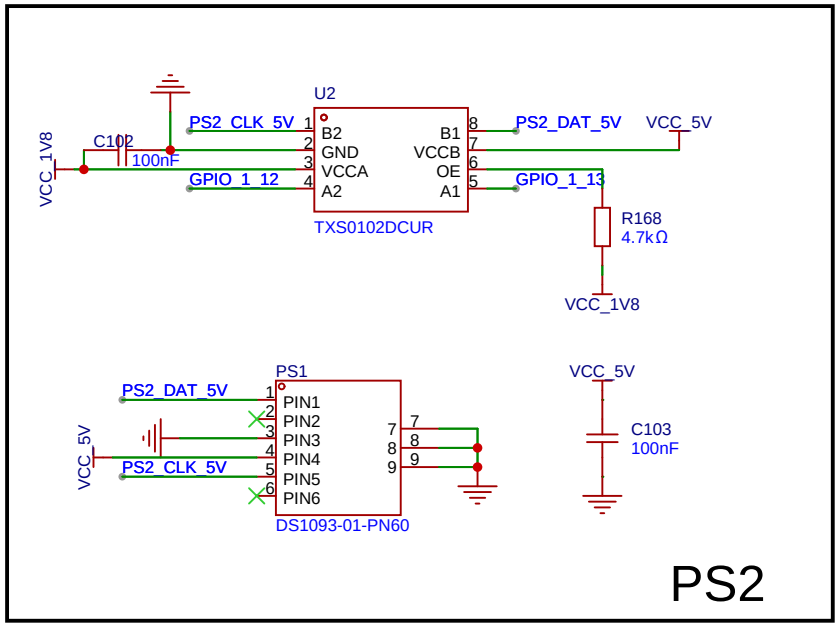
SD

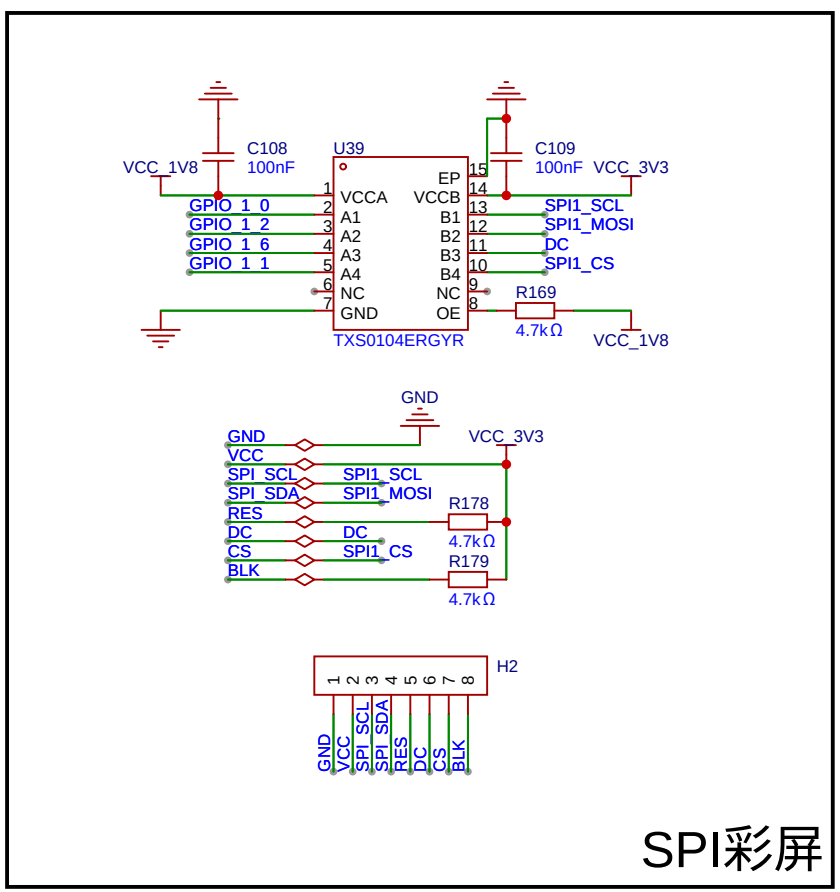


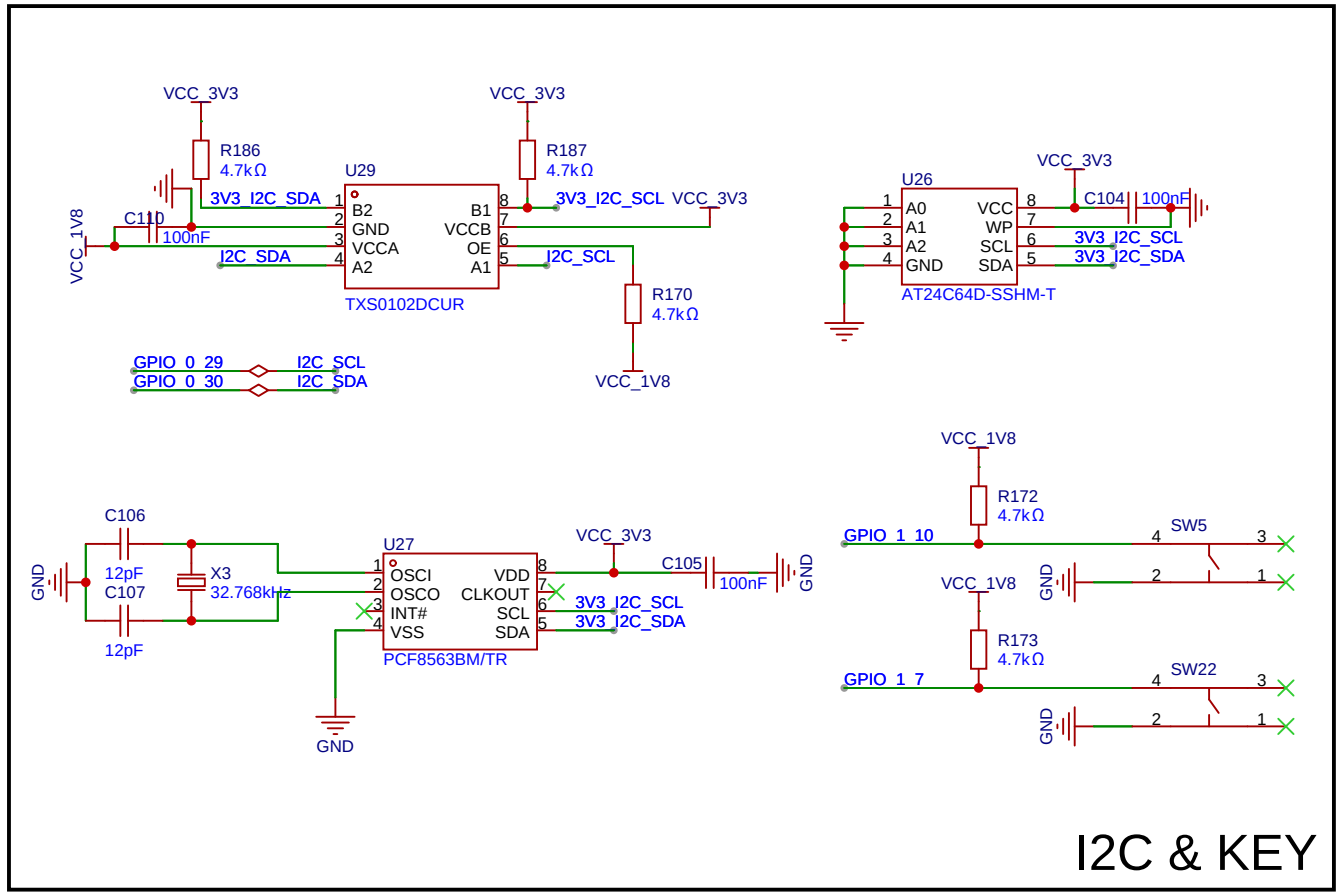


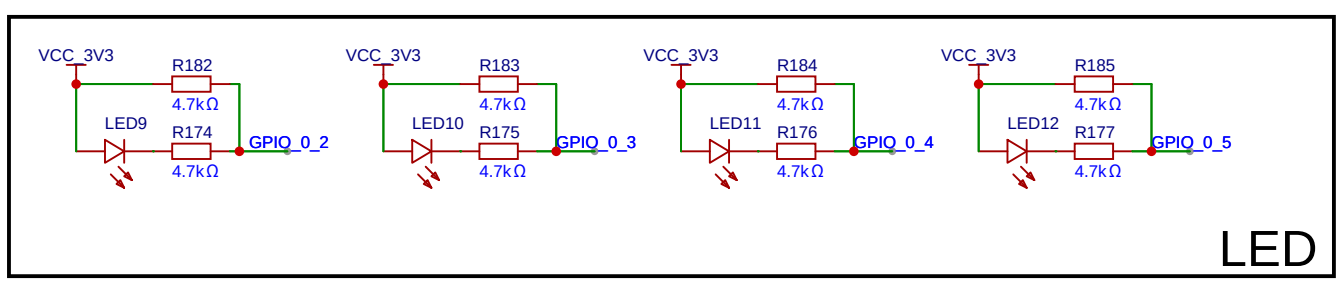
SWITCH & SHITF

原理图	Schematic1	创建日期	2025-06-05
		更新日期	2025-06-05
板子	Board1	图页	外部存储
绘制		StarrySkyPi	
审阅			
		版本	尺寸	页 6 共 7
嘉立创EDA		V1.0	A4	嘉立创EDA









原理图	Schematic1	创建日期	2025-06-05
		更新日期	2025-06-18
板子	Board1	图页	外设
绘制		StarrySkyPi	
审阅			
		版本	尺寸	页 7 共 7
嘉立创EDA		V1.0	A4	嘉立创EDA