

SN5470, SN7470 AND-GATED J-K POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET AND CLEAR

SDLS116 – DECEMBER 1983 – REVISED MARCH 1988

- Package Options Include Plastic and Ceramic DIPs and Ceramic Flat Packages
- Dependable Texas Instruments Quality and Reliability

description

These monolithic, edge-triggered J-K flip-flops feature gated inputs, direct clear and preset inputs, and complementary Q and \bar{Q} outputs. Input information is transferred to the outputs on the positive edge of the clock pulse.

Direct-coupled clock triggering occurs at a specific voltage level of the clock pulse, and after the clock input threshold voltage has been passed, the gated inputs are locked out.

These flip-flops are ideally suited for medium-to-high-speed applications and can result in a significant saving in system power dissipation and package count where input gating is required.

The SN5470 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN7470 is characterized for operation from 0°C to 70°C .

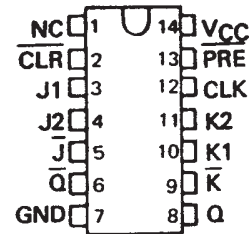
FUNCTION TABLE

| INPUTS | | | | | OUTPUTS | |
|--------|-----|-----|---|---|----------------|----------------|
| PRE | CLR | CLK | J | K | Q | \bar{Q} |
| L | H | L | X | X | H | L |
| H | L | L | X | X | L | H |
| L | L | X | X | X | L [†] | L [†] |
| H | H | ↑ | L | L | Q ₀ | Q ₀ |
| H | H | ↑ | H | L | H | L |
| H | H | ↑ | L | H | L | H |
| H | H | ↑ | H | H | TOGGLE | |
| H | H | L | X | X | Q ₀ | Q ₀ |

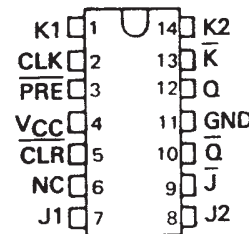
If inputs J and K are not used, they must be grounded. Preset or clear function can occur only when the clock input is low.

[†]This configuration is nonstable; that is, it will not persist when preset and clear inputs return to their inactive (high) level.

SN5470 ... J PACKAGE
SN7470 ... N PACKAGE
(TOP VIEW)

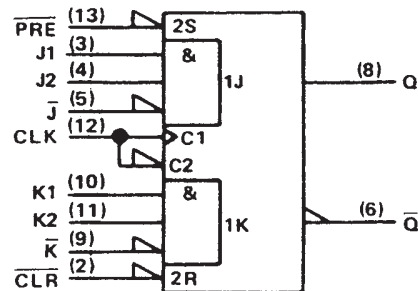


SN5470 ... W PACKAGE
(TOP VIEW)



NC - No internal connection

logic symbol†



[†]This symbol is in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.

Pin numbers shown are for J and N packages only.

positive logic

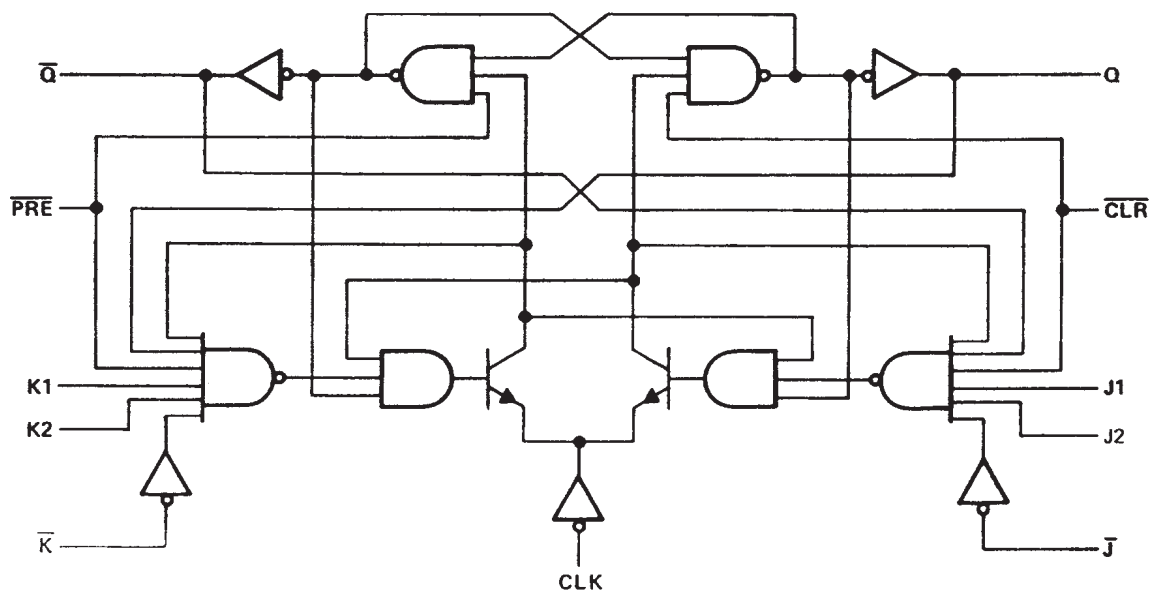
$$J = J1 \cdot J2 \cdot \bar{J}$$

$$K = K1 \cdot K2 \cdot \bar{K}$$

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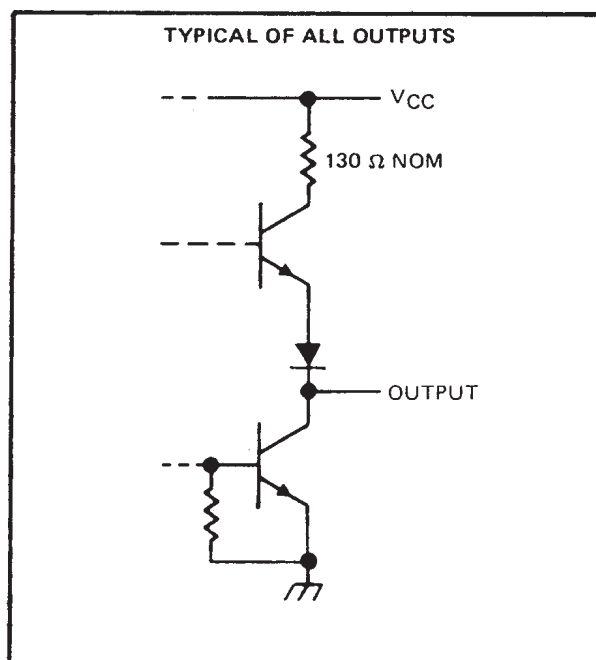
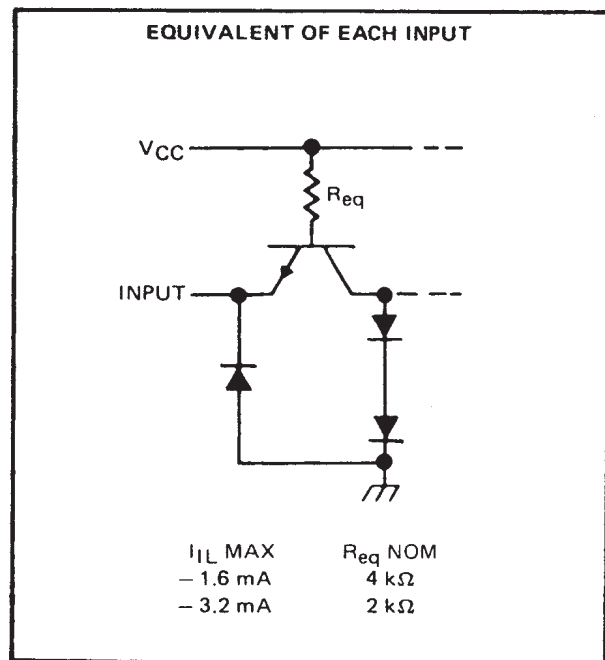
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logic diagram (positive logic)



'70-GATED J-K WITH CLEAR AND PRESET

schematics of input and outputs



SN5470, SN7470

AND-GATED J-K POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET AND CLEAR

SDLS116 – DECEMBER 1983 – REVISED MARCH 1988

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

| | |
|--|-----------------|
| Supply voltage, V_{CC} (see Note 1) | 7 V |
| Input voltage | 5.5 V |
| Operating free-air temperature: SN5470 | – 55°C to 125°C |
| SN7470 | 0°C to 70°C |
| Storage temperature range | – 65°C to 150°C |

NOTE 1: All voltage values are with respect to network ground terminal.

recommended operating conditions

| | | | SN5470 | | | SN7470 | | | UNIT | | |
|-----------------|--------------------------------|----------------|--------|-----|-------|--------|-----|-------|------|----|----|
| | | | MIN | NOM | MAX | MIN | NOM | MAX | | | |
| V _{CC} | Supply voltage | | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V | | |
| V _{IH} | High-level input voltage | | 2 | | | 2 | | | V | | |
| V _{IL} | Low-level input voltage | | | | 0.8 | | | 0.8 | V | | |
| I _{OH} | High-level output current | | | | − 0.4 | | | − 0.4 | mA | | |
| I _{OL} | Low-level output current | | | | 16 | | | 16 | mA | | |
| t _w | Pulse duration | CLK high | 20 | | | 20 | | | ns | | |
| | | CLK low | 30 | | | 30 | | | | | |
| | | PRE or CLR low | 25 | | | 25 | | | | | |
| t _{su} | Setup time before CLK ↑ | | 20 | | | 20 | | | ns | | |
| t _h | Hold time-Data after CLK ↑ | | 5 | | | 5 | | | ns | | |
| T _A | Operating free-air temperature | | − 55 | | | 125 | | | 0 | 70 | °C |

†‡ The arrow indicates the edge of the clock pulse used for reference: \uparrow for the rising edge, \downarrow for the falling edge.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS† | | SN5470 | | | SN7470 | | | UNIT |
|------------|---|---|--|--------|------|-------|--------|------|-------|---------------|
| | | | | MIN | TYP‡ | MAX | MIN | TYP‡ | MAX | |
| V_{IK} | | $V_{CC} = \text{MIN}, I_I = -12 \text{ mA}$ | | – 1.5 | | | – 1.5 | | | V |
| V_{OH} | | $V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OH} = -0.4 \text{ mA}$ | | 2.4 | 3.4 | | 2.4 | 3.4 | | V |
| V_{OL} | | $V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OL} = 16 \text{ mA}$ | | | 0.2 | 0.4 | | 0.2 | 0.4 | V |
| I_I | | $V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$ | | | | 1 | | | 1 | mA |
| I_{IH} | \overline{PRE} or \overline{CLR} | $V_{CC} = \text{MAX}, V_I = 2.4 \text{ V}$ | | | | 80 | | | 80 | μA |
| | All other | | | | | 40 | | | 40 | |
| I_{IL} | \overline{PRE} or $\overline{CLR}\dagger$ | $V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$ | | | | – 3.2 | | | – 3.2 | mA |
| | All other | | | | | – 1.6 | | | – 1.6 | |
| $I_{OS}\S$ | | $V_{CC} = \text{MAX}$ | | – 20 | | – 57 | – 18 | | – 57 | mA |
| I_{CC} | | $V_{CC} = \text{MAX},$ See Note 2 | | | 13 | 26 | | 13 | 26 | mA |

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

§Not more than one output should be shorted at a time.

†Clear is tested with preset high and preset is tested with clear high.

NOTE 2: With all outputs open, I_{CC} is measured with the Q and \overline{Q} outputs high in turn. At the time of measurement, the clock input is at 4.5 V.

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SDLS116 – DECEMBER 1983 – REVISED MARCH 1988

switching characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$ (see note 3)

| PARAMETER† | FROM (INPUT) | TO (OUTPUT) | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|------------------|-----------------|----------------|---|-----|-----|-----|------|
| f _{max} | | | R _L = 400 Ω, C _L = 15 pF | 20 | 35 | | MHz |
| t _{PLH} | PRE or CLR | Q or Q̄ | | | | 50 | ns |
| t _{PHL} | | | | | | 50 | ns |
| t _{PLH} | CLK | Q or Q̄ | | | 27 | 50 | ns |
| t _{PHL} | | | | | 18 | 50 | ns |

† f_{\max} = maximum clock frequency; t_{PLH} = propagation delay time, low-to-high level output;

t_{PHL} = propagation delay time, high-to-low level output.

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.



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