

SN5450, SN7450

DUAL 2-WIDE 2-INPUT AND-OR-INVERT GATES (ONE GATE EXPANDABLE)

SDLS112 – DECEMBER 1983 – REVISED MARCH 1988

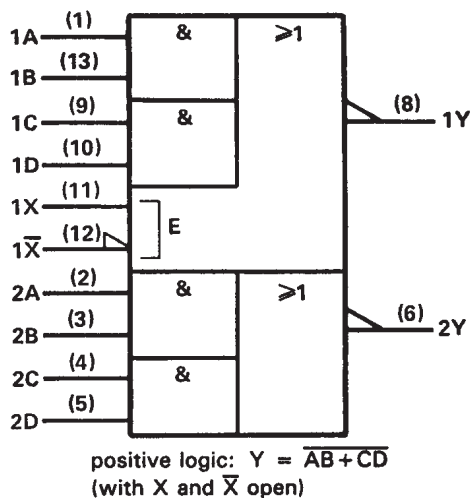
- Package Options Include Plastic and Ceramic DIPs and Ceramic Flat Packages
- Dependable Texas Instruments Quality and Reliability

description

These devices contain two independent 2-wide 2-input AND-OR-INVERT gates with one gate expandable. They perform the Boolean function $Y = \overline{AB + CD}$ with X and \overline{X} left open.

The SN5450 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN7450 is characterized for operation from 0°C to 70°C .

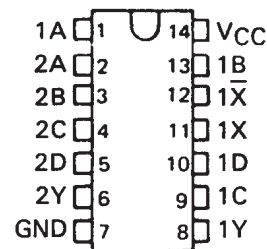
logic symbol†



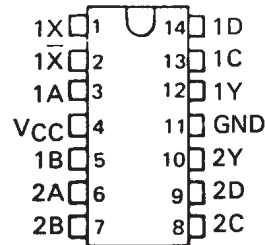
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for J and N packages.

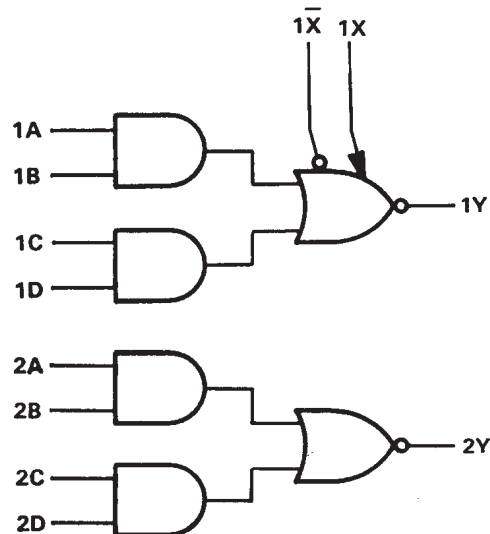
SN5450 . . . J PACKAGE
SN7450 . . . N PACKAGE
(TOP VIEW)



SN5450 . . . W PACKAGE
(TOP VIEW)



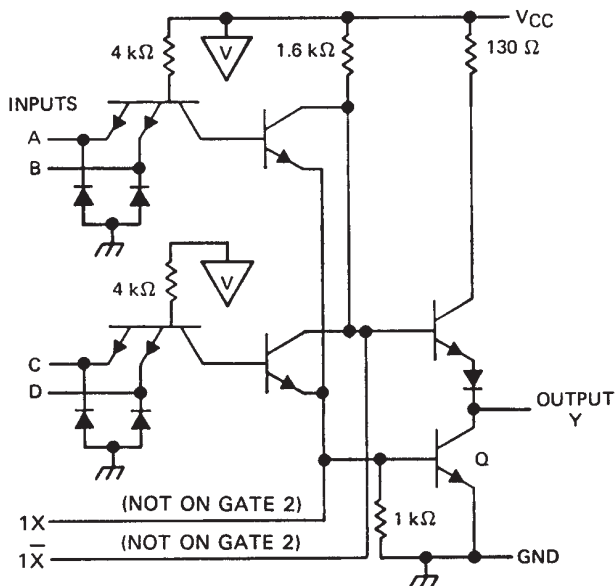
logic diagram (positive logic)



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schematic (each AND-OR-INVERT gate)



Resistor values shown are nominal.

If expander is not used, leave X and \overline{X} open.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	5.5 V
Operating free-air temperature range: SN5450	–55°C to 125°C
SN7450	0°C to 70°C
Storage temperature range	–65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

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recommended operating conditions

		SN5450			SN7450			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			– 0.4			– 0.4	mA
I_{OL}	Low-level output current			16			16	mA
T_A	Operating free-air temperature	– 55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN5450			SN7450			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	$V_{CC} = \text{MIN}$, $I_I = -12 \text{ mA}$			– 1.5			– 1.5	V
V_{OH}	$V_{CC} = \text{MIN}$, $V_{IL} = 0.8 \text{ V}$, $I_{OH} = -0.4 \text{ mA}$	2.4	3.4		2.4	3.4		V
V_{OL}	$V_{CC} = \text{MIN}$, $V_{IH} = 2 \text{ V}$, $I_{OL} = 16 \text{ mA}$	0.2	0.4		0.2	0.4		V
I_I	$V_{CC} = \text{MAX}$, $V_I = 5.5 \text{ V}$			1			1	mA
I_{IH}	$V_{CC} = \text{MAX}$, $V_{IH} = 2.4 \text{ V}$			40			40	μA
I_{IL}	$V_{CC} = \text{MAX}$, $V_{IL} = 0.4 \text{ V}$			– 1.6			– 1.6	mA
$I_{OS}§$	$V_{CC} = \text{MAX}$	– 20		– 55	– 18		– 55	mA
I_{CCH}	$V_{CC} = \text{MAX}$, $V_I = 0 \text{ V}$		4	8		4	8	mA
I_{CCL}	$V_{CC} = \text{MAX}$, See Note 2		7.4	14		7.4	14	mA
$I_{\bar{X}}¶$	$V_{\bar{X}X} = 0.4 \text{ V}$, $I_{OL} = 16 \text{ mA}$			– 2.9			– 3.1	mA
$V_{BE(Q)}¶$	$I_X + I_{\bar{X}} = 0.41 \text{ mA}$, $R_{\bar{X}X} = 0$, $I_{OL} = 16 \text{ mA}$			1.1				V
	$I_X + I_{\bar{X}} = 0.62 \text{ mA}$, $R_{\bar{X}X} = 0$, $I_{OL} = 16 \text{ mA}$						1	
$V_{OH}¶$	$I_X = 0.15 \text{ mA}$, $I_{\bar{X}} = -0.15 \text{ mA}$, $I_{OH} = -0.4 \text{ mA}$	2.4	3.4					V
	$I_X = 0.27 \text{ mA}$, $I_{\bar{X}} = -0.27 \text{ mA}$, $I_{OH} = -0.4 \text{ mA}$				2.4	3.4		
$V_{OL}¶$	$I_X + I_{\bar{X}} = 0.3 \text{ mA}$, $R_{\bar{X}X} = 138 \Omega$, $I_{OL} = 16 \text{ mA}$		0.2	0.4				V
	$I_X + I_{\bar{X}} = 0.43 \text{ mA}$, $R_{\bar{X}X} = 130 \Omega$, $I_{OL} = 16 \text{ mA}$					0.2	0.4	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ \text{C}$.

§ Not more than one output should be shorted at a time.

¶ Using expander inputs, $V_{CC} = \text{MIN}$, $T_A = \text{MIN}$, except typical values.

NOTE 2: All inputs of one AND gate at 4.5 V, all others at GND.

switching characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ \text{C}$ (see note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Any	Y	$R_L = 400 \Omega$, Expander pins open $C_L = 15 \text{ pF}$		13	22	ns
t_{PHL}					8	15	ns

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

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