

# DATA SHEET

For a complete data sheet, please also download:

- The IC06 74HC/HCT/HCU/HCMOS Logic Family Specifications
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Information
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Outlines

## **74HC/HCT165**

8-bit parallel-in/serial-out shift register

Product specification  
File under Integrated Circuits, IC06

December 1990

## 8-bit parallel-in/serial-out shift register

## 74HC/HCT165

## FEATURES

- Asynchronous 8-bit parallel load
- Synchronous serial input
- Output capability: standard
- I<sub>CC</sub> category: MSI

## GENERAL DESCRIPTION

The 74HC/HCT165 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT165 are 8-bit parallel-load or serial-in shift registers with complementary serial outputs ( $\overline{Q_7}$  and  $Q_7$ ) available from the last stage. When the parallel load (PL) input is LOW, parallel data from the  $D_0$  to  $D_7$  inputs are loaded into the register asynchronously.

When  $\overline{PL}$  is HIGH, data enters the register serially at the  $D_S$  input and shifts one place to the right ( $Q_0 \rightarrow Q_1 \rightarrow Q_2$ , etc.) with each positive-going clock transition. This feature allows parallel-to-serial converter expansion by tying the  $Q_7$  output to the  $D_S$  input of the succeeding stage.

The clock input is a gated-OR structure which allows one input to be used as an active LOW clock enable ( $\overline{CE}$ ) input. The pin assignment for the CP and  $\overline{CE}$  inputs is arbitrary and can be reversed for layout convenience. The LOW-to-HIGH transition of input  $\overline{CE}$  should only take place while CP HIGH for predictable operation. Either the CP or the  $\overline{CE}$  should be HIGH before the LOW-to-HIGH transition of PL to prevent shifting the data when  $\overline{PL}$  is activated.

## APPLICATIONS

- Parallel-to-serial data conversion

## QUICK REFERENCE DATA

GND = 0 V; T<sub>amb</sub> = 25 °C; t<sub>r</sub> = t<sub>f</sub> = 6 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay CP to $\overline{Q_7}$ , $Q_7$ PL to $\overline{Q_7}$ , $Q_7$ $D_7$ to $\overline{Q_7}$ , $Q_7$	C <sub>L</sub> = 15 pF; V <sub>CC</sub> = 5 V	16	14	ns
			15	17	ns
			11	11	ns
f <sub>max</sub>	maximum clock frequency		56	48	MHz
C <sub>I</sub>	input capacitance		3.5	3.5	pF
C <sub>PD</sub>	power dissipation capacitance per package	notes 1 and 2	35	35	pF

## Notes

1. C<sub>PD</sub> is used to determine the dynamic power dissipation (P<sub>D</sub> in μW):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f<sub>i</sub> = input frequency in MHz

f<sub>o</sub> = output frequency in MHz

$\sum (C_L \times V_{CC}^2 \times f_o)$  = sum of outputs

C<sub>L</sub> = output load capacitance in pF

V<sub>CC</sub> = supply voltage in V

2. For HC the condition is V<sub>I</sub> = GND to V<sub>CC</sub>  
For HCT the condition is V<sub>I</sub> = GND to V<sub>CC</sub> – 1.5 V

## ORDERING INFORMATION

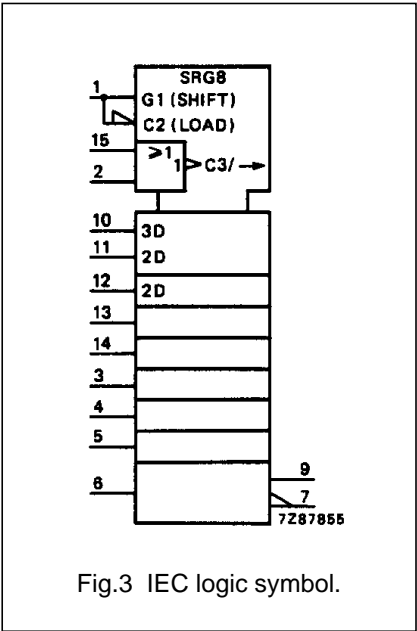
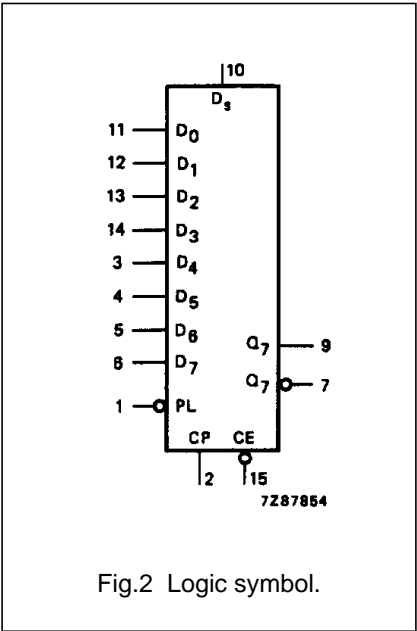
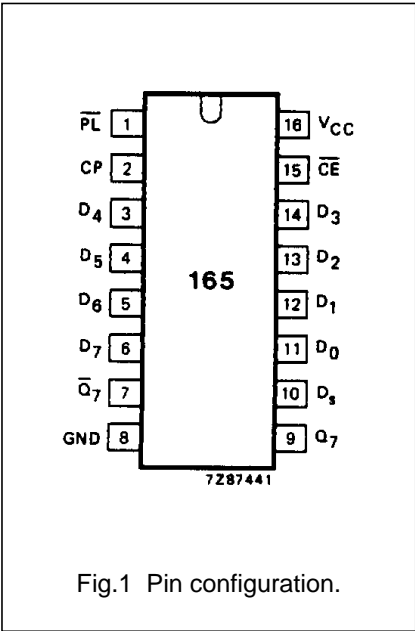
See "74HC/HCT/HCU/HCMOS Logic Package Information".

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PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	$\overline{\text{PL}}$	asynchronous parallel load input (active LOW)
7	$\overline{\text{Q}}_7$	complementary output from the last stage
9	$\text{Q}_7$	serial output from the last stage
2	CP	clock input (LOW-to-HIGH edge-triggered)
8	GND	ground (0 V)
10	$\text{D}_s$	serial data input
11, 12, 13, 14, 3, 4, 5, 6	$\text{D}_0$ to $\text{D}_7$	parallel data inputs
15	$\overline{\text{CE}}$	clock enable input (active LOW)
16	$\text{V}_{\text{CC}}$	positive supply voltage



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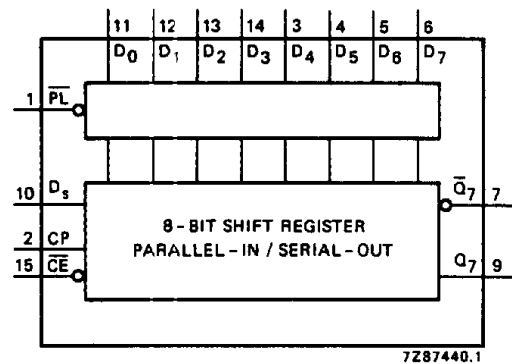


Fig.4 Functional diagram.

FUNCTION TABLE

OPERATING MODES	INPUTS					Q <sub>n</sub> REGISTERS		OUTPUTS	
	PL	CE	CP	DS	D <sub>0</sub> -D <sub>7</sub>	Q <sub>0</sub>	Q <sub>1</sub> -Q <sub>6</sub>	Q <sub>7</sub>	Q <sub>7</sub> -bar
parallel load	L	X	X	X	L	L	L - L	L	H
	L	X	X	X	H	H	H - H	H	L
serial shift	H	L	↑	L	X	L	q <sub>0</sub> -q <sub>5</sub>	q <sub>6</sub>	q <sub>6</sub> -bar
	H	L	↑	h	X	H	q <sub>0</sub> -q <sub>5</sub>	q <sub>6</sub>	q <sub>6</sub>
hold "do nothing"	H	H	X	X	X	q <sub>0</sub>	q <sub>1</sub> -q <sub>6</sub>	q <sub>7</sub>	q <sub>7</sub>

Note

- 1. H = HIGH voltage level  
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH clock transition  
L = LOW voltage level  
l = LOW voltage level one set-up time prior to the LOW-to-HIGH clock transition  
q = lower case letters indicate the state of the referenced output one set-up time prior to the LOW-to-HIGH clock transition  
X = don't care  
↑ = LOW-to-HIGH clock transition

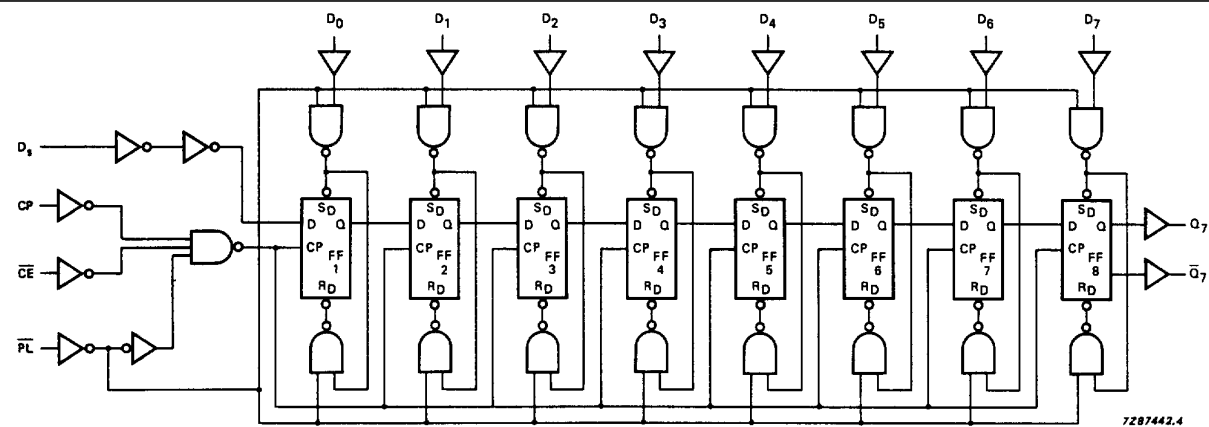


Fig.5 Logic diagram.

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**DC CHARACTERISTICS FOR 74HC**

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: standard

I<sub>CC</sub> category: MSI

**AC CHARACTERISTICS FOR HC**

GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)							UNIT	TEST CONDITIONS	
		74HC								V <sub>CC</sub> (V)	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay CE, CP to Q <sub>7</sub> , Q <sub>7</sub>		52 19 15	165 33 28		205 41 35		250 50 43	ns	2.0 4.5 6.0	Fig.6
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay PL to Q <sub>7</sub> , Q <sub>7</sub>		50 18 14	165 33 28		205 41 35		250 50 43	ns	2.0 4.5 6.0	Fig.6
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay D <sub>7</sub> to Q <sub>7</sub> , Q <sub>7</sub>		36 13 10	120 24 20		150 30 26		180 36 31	ns	2.0 4.5 6.0	Fig.6
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig.6
t <sub>W</sub>	clock pulse width HIGH or LOW	80 16 14	17 6 5		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig.6
t <sub>W</sub>	parallel load pulse width; LOW	80 16 14	14 5 4		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig.6
t <sub>rem</sub>	removal time PL to CP, CE	100 20 17	22 8 6		125 25 21		150 30 26		ns	2.0 4.5 6.0	Fig.6
t <sub>su</sub>	set-up time D <sub>s</sub> to CP, CE	80 16 14	11 4 3		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig.6
t <sub>su</sub>	set-up time CE to CP; CP to CE	80 16 14	17 6 5		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig.6
t <sub>su</sub>	set-up time D <sub>n</sub> to PL	80 16 14	22 8 6		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig.6

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SYMBOL	PARAMETER	T <sub>amb</sub> (°C)							UNIT	TEST CONDITIONS	
		74HC								V <sub>CC</sub> (V)	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t <sub>h</sub>	hold time D <sub>s</sub> to CP, $\overline{\text{CE}}$ D <sub>n</sub> to PL	5	6		5		5		ns	2.0	Fig.6
		5	2		5		5			4.5	
		5	2		5		5			6.0	
t <sub>h</sub>	hold time $\overline{\text{CE}}$ to CP CP to $\overline{\text{CE}}$	5	−17		5		5		ns	2.0	Fig.6
		5	−6		5		5			4.5	
		5	−5		5		5			6.0	
f <sub>max</sub>	maximum clock pulse frequency	6	17		5		4		MHz	2.0	Fig.6
		30	51		24		20			4.5	
		35	61		28		24			6.0	

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**DC CHARACTERISTICS FOR 74HCT**

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: standard

I<sub>CC</sub> category: MSI

**Note to HCT types**

The value of additional quiescent supply current ( $\Delta I_{CC}$ ) for a unit load of 1 is given in the family specifications. To determine  $\Delta I_{CC}$  per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
D <sub>n</sub>	0.35
D <sub>s</sub>	0.35
CP	0.65
$\overline{CE}$	0.65
PL	0.65

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## AC CHARACTERISTICS FOR 74HCT

GND = 0 V;  $t_r = t_f = 6$  ns;  $C_L = 50$  pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)							UNIT	TEST CONDITIONS	
		74HCT								V <sub>CC</sub> (V)	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay CE, CP to Q <sub>7</sub> , Q <sub>7</sub>		17	34		43		51	ns	4.5	Fig.6
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay PL to Q <sub>7</sub> , Q <sub>7</sub>		20	40		50		60	ns	4.5	Fig.6
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay D <sub>7</sub> to Q <sub>7</sub> , Q <sub>7</sub>		14	28		35		42	ns	4.5	Fig.6
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		7	15		19		22	ns	4.5	Fig.6
t <sub>W</sub>	clock pulse width HIGH or LOW	16	6		20		24		ns	4.5	Fig.6
t <sub>W</sub>	parallel load pulse width; LOW	20	9		25		30		ns	4.5	Fig.6
t <sub>rem</sub>	removal time PL to CP, CE	20	8		25		30		ns	4.5	Fig.6
t <sub>su</sub>	set-up time D <sub>s</sub> to CP, CE	20	2		25		30		ns	4.5	Fig.6
t <sub>su</sub>	set-up time CE to CP; CP to CE	20	7		25		30		ns	4.5	Fig.6
t <sub>su</sub>	set-up time D <sub>n</sub> to PL	20	10		25		30		ns	4.5	Fig.6
t <sub>h</sub>	hold time D <sub>s</sub> to CP, CE; D <sub>n</sub> to PL	7	−1		9		11		ns	4.5	Fig.6
t <sub>h</sub>	hold time CE to CP, CP to CE	0	−7		0		0		ns	4.5	Fig.6
f <sub>max</sub>	maximum clock pulse frequency	26	44		21		17		MHz	4.5	Fig.6



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## AC WAVEFORMS

The changing to output assumes internal  $Q_6$  opposite state from  $Q_7$ .

- (1) HC :  $V_M = 50\%$ ;  $V_I = \text{GND to } V_{CC}$ .  
HCT:  $V_M = 1.3 \text{ V}$ ;  $V_I = \text{GND to } 3 \text{ V}$ .

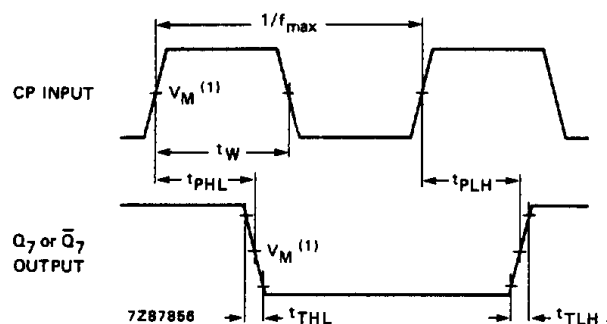


Fig.6 Waveforms showing the clock (CP) to output ( $Q_7$  or  $\bar{Q}_7$ ) propagation delays, the clock pulse width, the output transition times and the maximum clock frequency.

The changing to output assumes internal  $Q_6$  opposite state from  $Q_7$ .

- (1) HC :  $V_M = 50\%$ ;  $V_I = \text{GND to } V_{CC}$ .  
HCT:  $V_M = 1.3 \text{ V}$ ;  $V_I = \text{GND to } 3 \text{ V}$ .

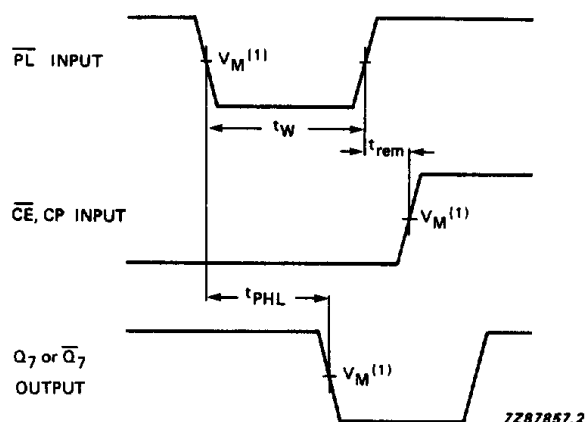


Fig.7 Waveforms showing the parallel load ( $\overline{PL}$ ) pulse width, the parallel load to output ( $Q_7$  or  $\bar{Q}_7$ ) propagation delays, the parallel load to clock (CP) and clock enable ( $\overline{CE}$ ) removal time.

- (1) HC :  $V_M = 50\%$ ;  $V_I = \text{GND to } V_{CC}$ .  
HCT:  $V_M = 1.3 \text{ V}$ ;  $V_I = \text{GND to } 3 \text{ V}$ .

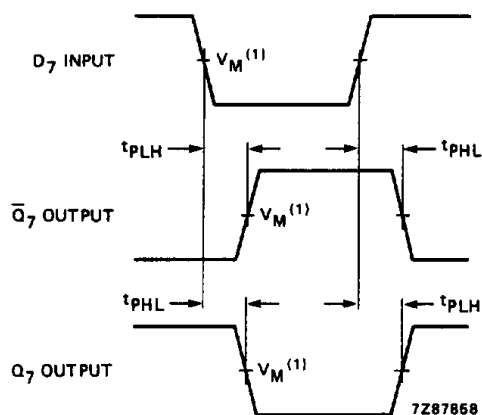


Fig.8 Waveforms showing the data input ( $D_n$ ) to output ( $Q_7$  or  $\bar{Q}_7$ ) propagation delays when  $\overline{PL}$  is LOW.

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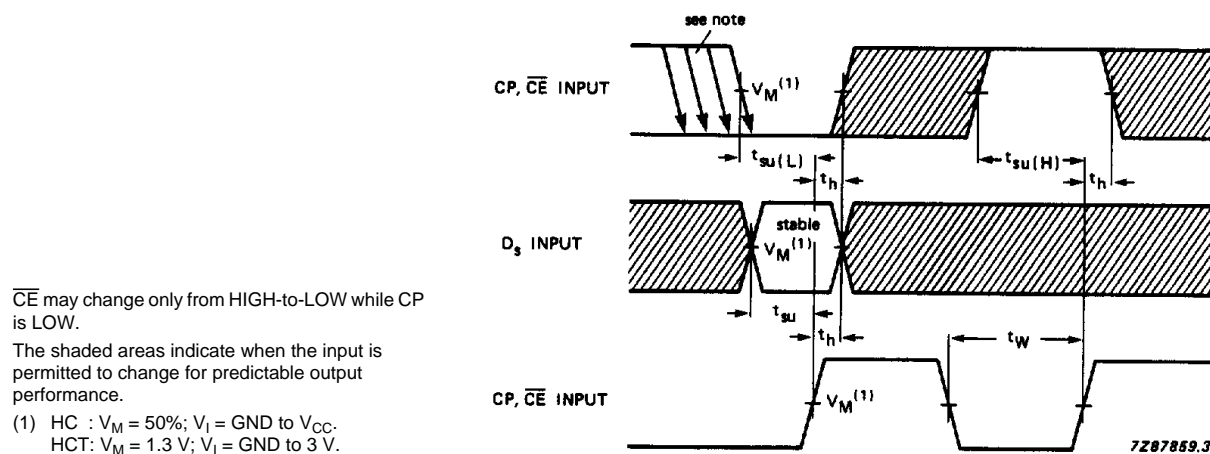


Fig.9 Waveforms showing the set-up and hold times from the serial data input ( $D_s$ ) to the clock (CP) and clock enable ( $\overline{CE}$ ) inputs, from the clock enable input ( $\overline{CE}$ ) to the clock input (CP) and from the clock input (CP) to the clock enable input ( $\overline{CE}$ ).

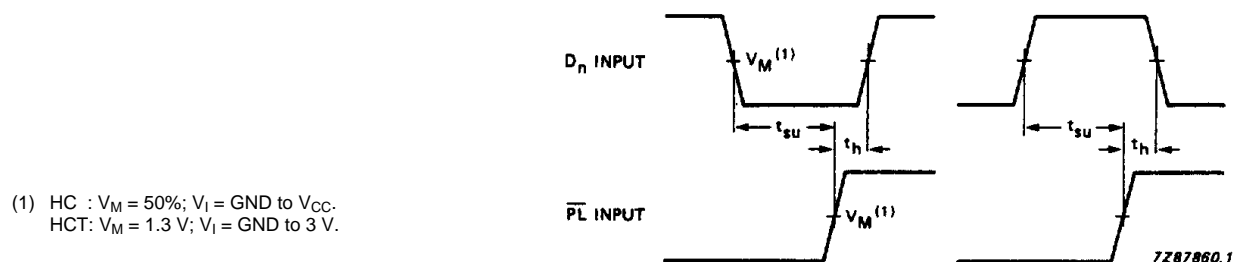


Fig.10 Waveforms showing the set-up and hold times from the data inputs ( $D_n$ ) to the parallel load input ( $\overline{PL}$ ).

## PACKAGE OUTLINES

See "74HC/HCT/HCU/HCMOS Logic Package Outlines".