

# DATA SHEET

**74ALS273**

Octal D-type flip-flop

Product specification  
IC05 Data Handbook

1991 Feb 08

# Octal D-type flip-flop

74ALS273

## FEATURES

- Eight edge-triggered D-type flip-flops
- Buffered common clock
- Buffered asynchronous master reset
- See 74ALS377 for clock enable version
- See 74ALS373 for transparent latch version
- See 74ALS374 for 3-State version

## DESCRIPTION

The 74ALS273 has eight edge-triggered D-type flip-flops with individual D inputs and Q outputs. The common buffered clock (CP) and master reset ( $\overline{\text{MR}}$ ) inputs load and reset all flip-flops simultaneously.

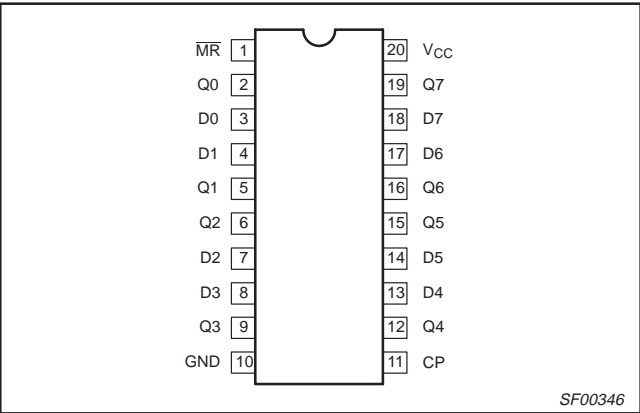
The register is fully edge-triggered. The state of each D input, one setup time before the Low-to-High clock transition, is transferred to the corresponding flip-flop's Q output.

All outputs will be forced Low independently of clock or data inputs by a Low voltage level on the  $\overline{\text{MR}}$  input.

The device is useful for applications where the true output only is required and the CP and  $\overline{\text{MR}}$  are common to all flip-flops.

TYPE	TYPICAL $f_{\text{MAX}}$	TYPICAL SUPPLY CURRENT (TOTAL)
74ALS273	95MHz	16mA

## PIN CONFIGURATION



## ORDERING INFORMATION

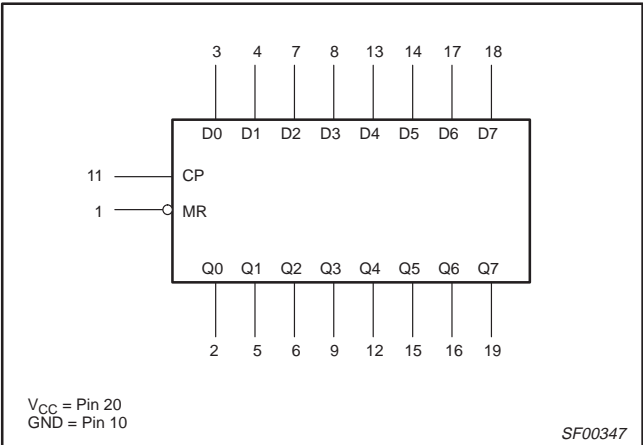
DESCRIPTION	ORDER CODE	DRAWING NUMBER
	COMMERCIAL RANGE $V_{\text{CC}} = 5\text{V} \pm 10\%$ , $T_{\text{amb}} = 0^{\circ}\text{C to } +70^{\circ}\text{C}$	
20-pin plastic DIP	74ALS273N	SOT146-1
20-pin plastic SO	74ALS273D	SOT163-1
20-pin plastic SSOP Type II	74ALS273DB	SOT339-1

## INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

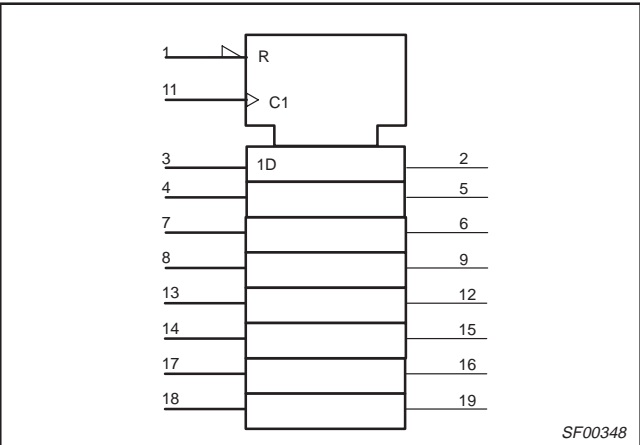
PINS	DESCRIPTION	74ALS (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D0 – D7	Data inputs	1.0/2.0	20 $\mu$ A/0.2mA
CP	Clock pulse input (active rising edge)	1.0/1.0	20 $\mu$ A/0.1mA
$\overline{\text{MR}}$	Master Reset input (active-Low)	1.0/1.0	20 $\mu$ A/0.1mA
Q0 – Q7	3-State outputs	130/240	2.6mA/24mA

NOTE: One (1.0) ALS unit load is defined as: 20 $\mu$ A in the High state and 0.1mA in the Low state.

## LOGIC SYMBOL



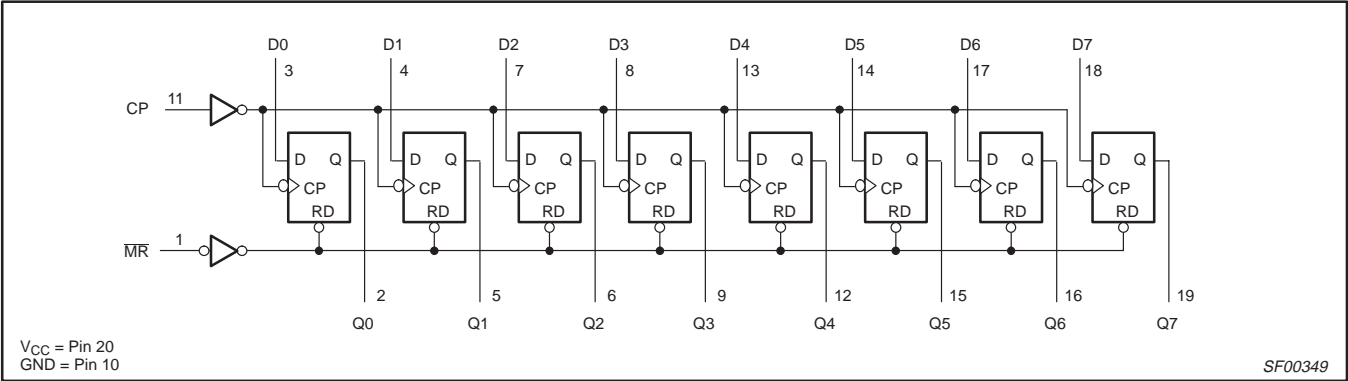
## IEC/IEEE SYMBOL



Octal D-type flip-flop

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LOGIC DIAGRAM



FUNCTION TABLE

INPUTS			OUTPUTS	OPERATING MODE
MR	CP	Dn	Qn	
L	X	X	L	Reset (clear)
H	↑	h	H	Load "1"
H	↑	l	L	Load "0"

H = High-voltage level  
h = High state must be present one setup time before the Low-to-High clock transition  
L = Low-voltage level  
l = Low state must be present one setup time before the Low-to-High clock transition  
X = Don't care  
↑ = Low-to-High clock transition

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limit set forth in this table may impair the useful life of the device.  
Unless otherwise noted these limits are over the operating free air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V <sub>CC</sub>	Supply voltage	−0.5 to +7.0	V
V <sub>IN</sub>	Input voltage	−0.5 to +7.0	V
I <sub>IN</sub>	Input current	−30 to +5	mA
V <sub>OUT</sub>	Voltage applied to output in High output state	−0.5 to V <sub>CC</sub>	V
I <sub>OUT</sub>	Current applied to output in Low output state	48	mA
T <sub>amb</sub>	Operating free-air temperature range	0 to +70	°C
T <sub>stg</sub>	Storage temperature range	−65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
V <sub>CC</sub>	Supply voltage	4.5	5.0	5.5	V
V <sub>IH</sub>	High-level input voltage	2.0			V
V <sub>IL</sub>	Low-level input voltage			0.8	V
I <sub>IK</sub>	Input clamp current			−18	mA
I <sub>OH</sub>	High-level output current			−2.6	mA
I <sub>OL</sub>	Low-level output current			24	mA
T <sub>amb</sub>	Operating free-air temperature range	0		+70	°C

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## DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS <sup>1</sup>	LIMITS			UNIT
			MIN	TYP <sup>2</sup>	MAX	
V <sub>OH</sub>	High-level output voltage	V <sub>CC</sub> ± 10%, V <sub>IL</sub> = MAX, V <sub>IH</sub> = MIN	I <sub>OH</sub> = -0.4mA	V <sub>CC</sub> - 2		V
			I <sub>OH</sub> = MAX	2.4	3.2	V
V <sub>OL</sub>	Low-level output voltage	V <sub>CC</sub> = MIN, V <sub>IL</sub> = MAX, V <sub>IH</sub> = MIN	I <sub>OL</sub> = 12mA		0.25	V
			I <sub>OL</sub> = 24mA		0.35	V
V <sub>IK</sub>	Input clamp voltage	V <sub>CC</sub> = MIN, I <sub>I</sub> = I <sub>IK</sub>		-0.73	-1.5	V
I <sub>I</sub>	Input current at maximum input voltage	V <sub>CC</sub> = MAX, V <sub>I</sub> = 7.0V			0.1	mA
I <sub>IH</sub>	High-level input current	V <sub>CC</sub> = MAX, V <sub>I</sub> = 2.7V			20	μA
I <sub>IL</sub>	Low-level input current	MR, CP Dn	V <sub>CC</sub> = MAX, V <sub>I</sub> = 0.4V		-0.1	mA
					-0.2	mA
I <sub>O</sub>	Output current <sup>3</sup>	V <sub>CC</sub> = MAX, V <sub>O</sub> = 2.25V	-30		-112	mA
I <sub>CC</sub>	Supply current (total)	I <sub>CCH</sub> I <sub>CCL</sub>	V <sub>CC</sub> = MAX	12	18	mA
				21	29	mA

## NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V<sub>CC</sub> = 5V, T<sub>amb</sub> = 25°C.
- The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I<sub>OS</sub>.

## AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS		UNIT
			T <sub>amb</sub> = 0°C to +70°C V <sub>CC</sub> = +5.0V ± 10% C <sub>L</sub> = 50pF, R <sub>L</sub> = 500Ω		
			MIN	MAX	
f <sub>MAX</sub>	Maximum clock frequency	Waveform 1	65		MHz
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay CP to Qn	Waveform 1	2.0 3.0	8.0 11.0	ns
t <sub>PHL</sub>	Propagation delay MR to Qn	Waveform 2	4.0	12.0	ns

## AC SETUP REQUIREMENTS

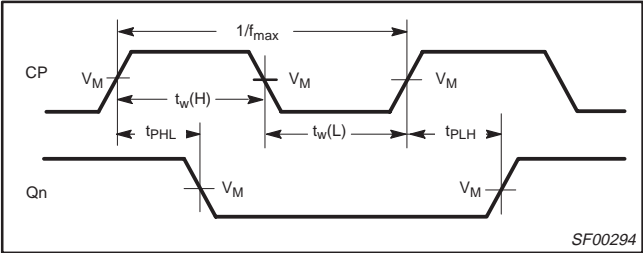
SYMBOL	PARAMETER	TEST CONDITION	LIMITS		UNIT
			T <sub>amb</sub> = 0°C to +70°C V <sub>CC</sub> = +5.0V ± 10% C <sub>L</sub> = 50pF, R <sub>L</sub> = 500Ω		
			MIN	MAX	
t <sub>su</sub> (H) t <sub>su</sub> (L)	Setup time, High or Low Dn to CP	Waveform 3	5.0 5.0		ns
t <sub>h</sub> (H) t <sub>h</sub> (L)	Hold time, High or Low Dn to CP	Waveform 3	0.0 0.0		ns
t <sub>w</sub> (H) t <sub>w</sub> (L)	CP pulse width, High or Low	Waveform 1	6.0 8.0		ns
t <sub>w</sub> (L)	MR pulse width, Low	Waveform 2	7.0		ns
t <sub>REC</sub>	Recovery time, MR to CP	Waveform 2	12.0		ns

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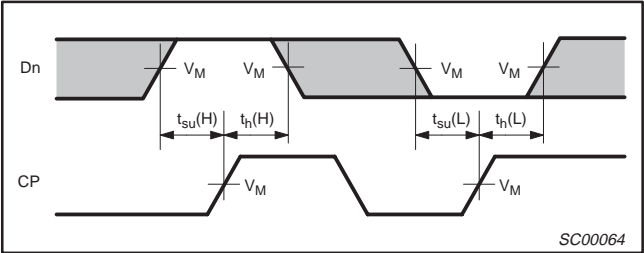
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AC WAVEFORMS

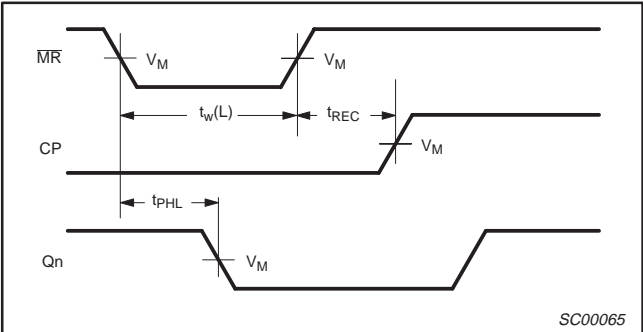
For all waveforms,  $V_M = 1.3V$ .



Waveform 1. Propagation Delay for Clock Input to Output, Clock Pulse Width, and Maximum Clock Frequency



Waveform 3. Data Setup and Hold Times



Waveform 2. Master Reset Pulse Width, Master Reset to Output Delay, and Master Reset to Clock Recovery Time

TEST CIRCUIT AND WAVEFORMS

Test Circuit for Totem-pole Outputs

**DEFINITIONS:**

$R_L$  = Load resistor; see AC electrical characteristics for value.

$C_L$  = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.

$R_T$  = Termination resistance should be equal to  $Z_{OUT}$  of pulse generators.

Input Pulse Definition

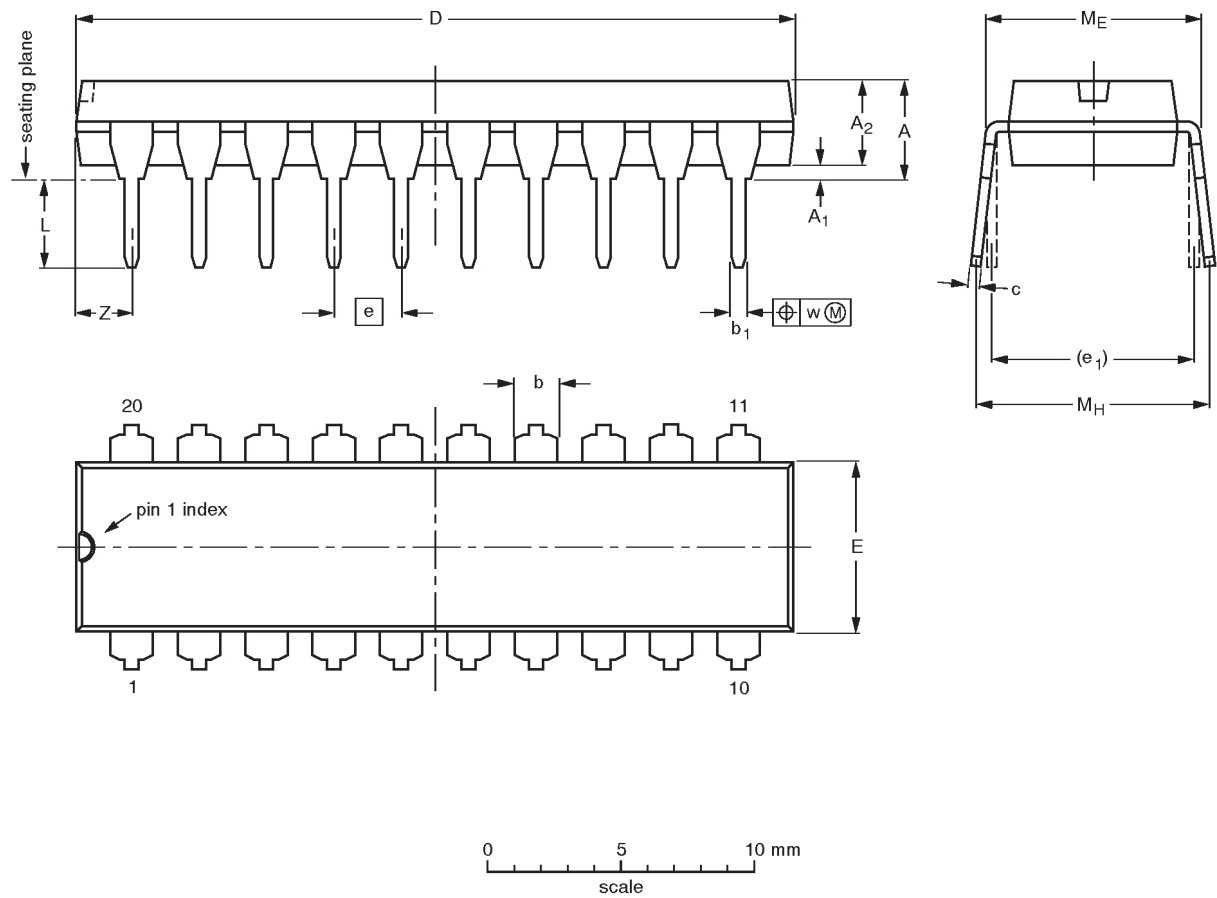
Family	INPUT PULSE REQUIREMENTS					
	Amplitude	$V_M$	Rep.Rate	$t_w$	$t_{THL} (t_f)$	$t_{THL} (t_r)$
74ALS	3.5V	1.3V	1MHz	500ns	2.0ns	2.0ns

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DIP20: plastic dual in-line package; 20 leads (300 mil)

SOT146-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A <sub>1</sub> min.	A <sub>2</sub> max.	b	b <sub>1</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	e <sub>1</sub>	L	M <sub>E</sub>	M <sub>H</sub>	w	Z <sup>(1)</sup> max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	0.36 0.23	26.92 26.54	6.40 6.22	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	2.0
inches	0.17	0.020	0.13	0.068 0.051	0.021 0.015	0.014 0.009	1.060 1.045	0.25 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.078

Note
1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

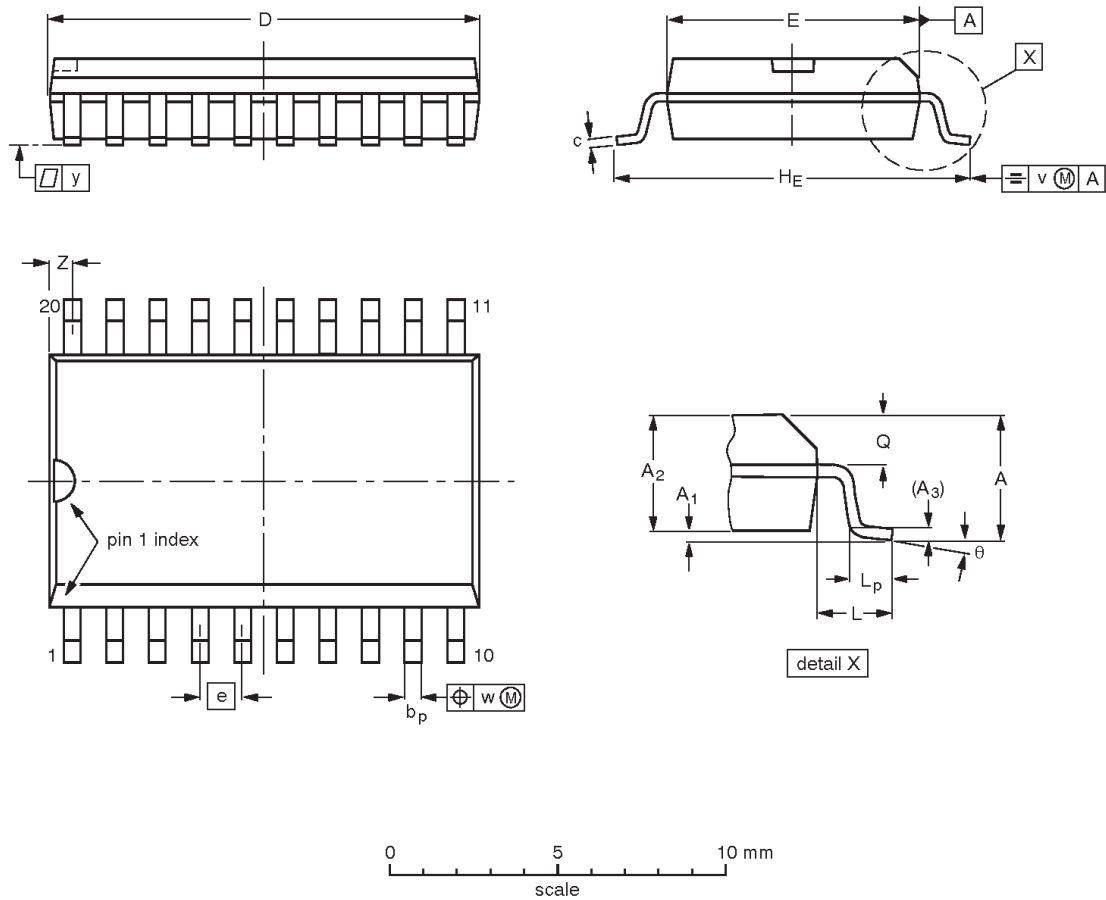
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT146-1			SC603			92-11-17 95-05-24

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SO20: plastic small outline package; 20 leads; body width 7.5 mm

SOT163-1




DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	Z <sup>(1)</sup>	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	13.0 12.6	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.51 0.49	0.30 0.29	0.050	0.42 0.39	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

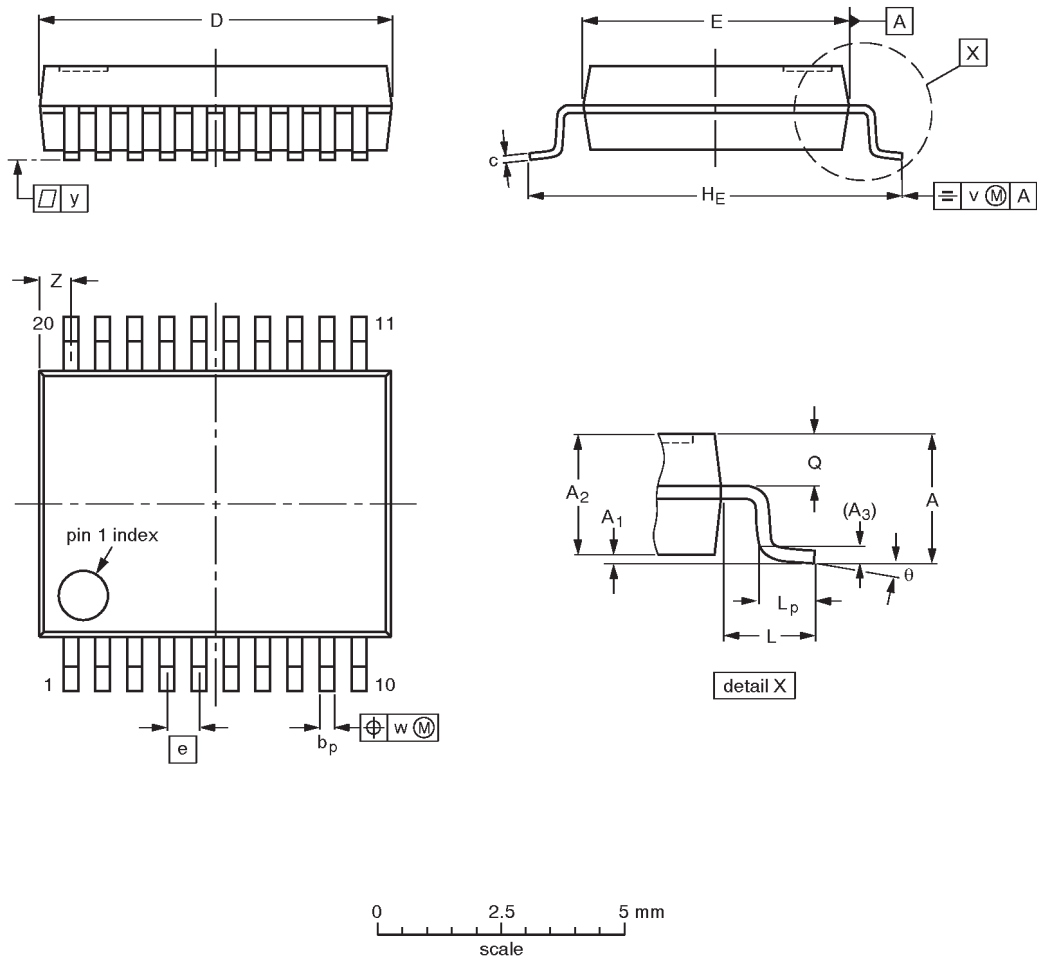
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT163-1	075E04	MS-013AC				92-11-17 95-01-24

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SSOP20: plastic shrink small outline package; 20 leads; body width 5.3 mm

SOT339-1




DIMENSIONS (mm are the original dimensions)

UNIT	A <sub>max.</sub>	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	Z <sup>(1)</sup>	θ
mm	2.0	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	7.4 7.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	0.9 0.5	8° 0°

Note

1. Plastic or metal protrusions of 0.20 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT339-1		MO-150AE				93-09-08 95-02-04



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DEFINITIONS		
Data Sheet Identification	Product Status	Definition
Objective Specification	Formative or in Design	This data sheet contains the design target or goal specifications for product development. Specifications may change in any manner without notice.
Preliminary Specification	Preproduction Product	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
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