DATA SHEET

For a complete data sheet, please also download:

- The IC06 74HC/HCT/HCU/HCMOS Logic Family Specifications
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Information
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Outlines

74HC/HCT20

Dual 4-input NAND gate

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Dual 4-input NAND gate

74HC/HCT20

FEATURES

- Output capability: standard
- I_{CC} category: SSI

GENERAL DESCRIPTION

The 74HC/HCT20 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A. The 74HC/HCT20 provide the 4-input NAND function.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/ t_{PLH}	propagation delay nA, nB, nC, nD to nY	C_L = 15 pF; V_{CC} = 5 V	8	13	ns
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per package	notes 1 and 2	22	17	pF

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):

    $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:

    f_i = input frequency in MHz

    f_o = output frequency in MHz

    C_L = output load capacitance in pF

    V_{CC} = supply voltage in V

    $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs

2. For HC   the condition is V_I = GND to V_{CC}
    For HCT the condition is V_I = GND to $V_{CC} - 1.5$ V

ORDERING INFORMATION

See *"74HC/HCT/HCU/HCMOS Logic Package Information"*.

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PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 9	1A, 2A	data inputs
2, 10	1B, 2B	data inputs
3, 11	n.c.	not connected
4, 12	1C, 2C	data inputs
5, 13	1D, 2D	data inputs
6, 8	1Y, 2Y	data outputs
7	GND	ground (0 V)
14	V_{CC}	positive supply voltage

Fig.1 Pin configuration.

Fig.2 Logic symbol.

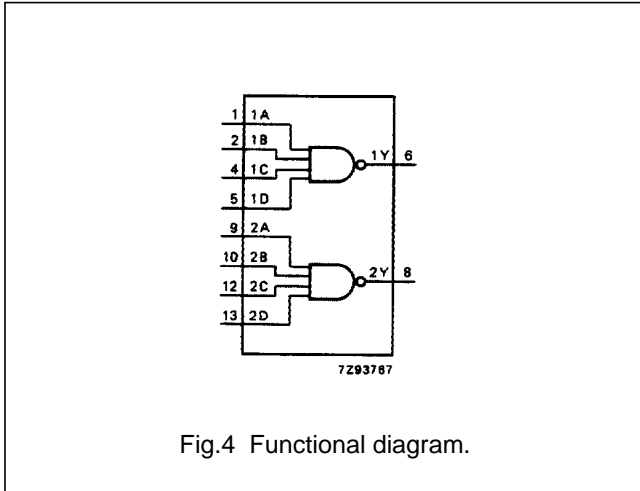Fig.3 IEC logic symbol.
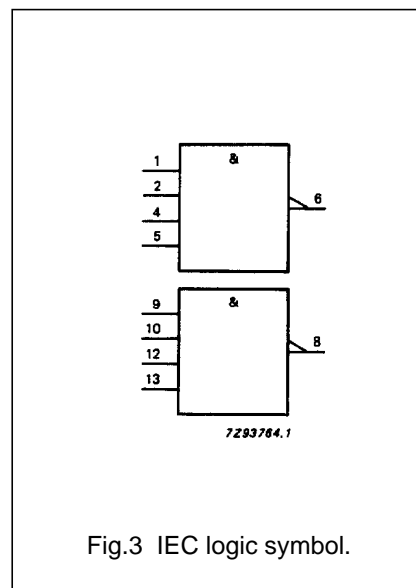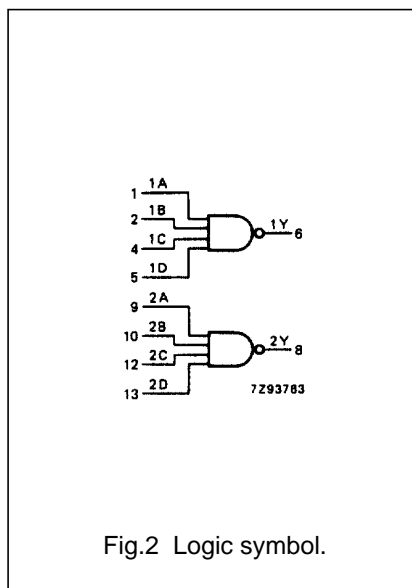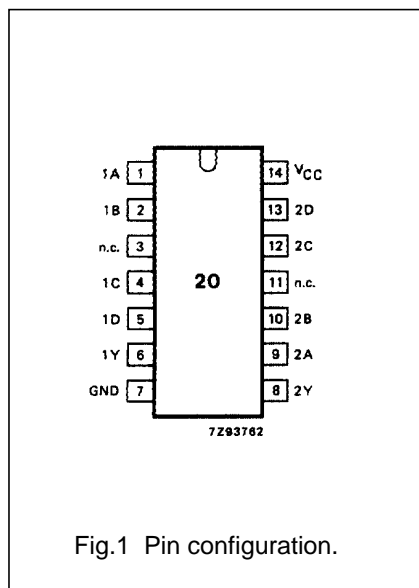
Dual 4-input NAND gate

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Fig.4 Functional diagram.
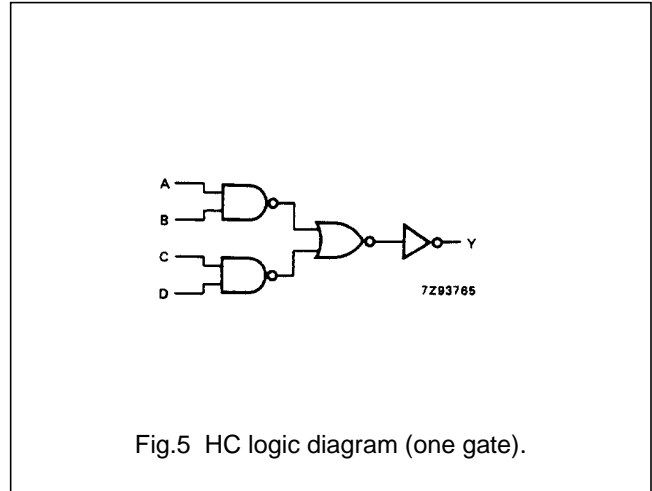
Fig.5 HC logic diagram (one gate).
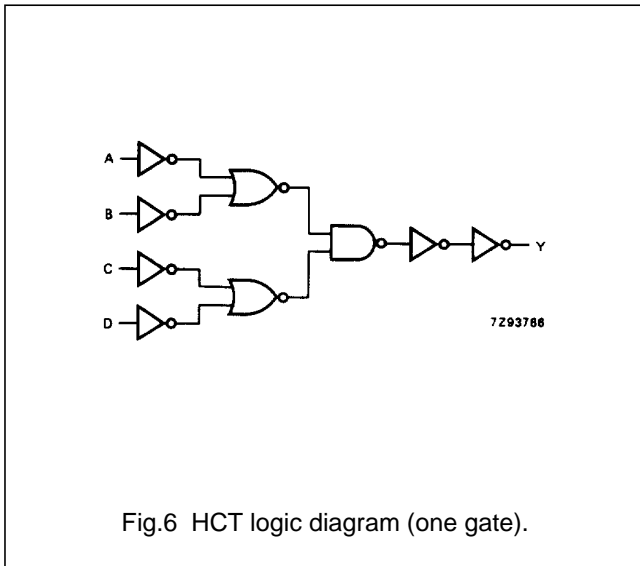
Fig.6 HCT logic diagram (one gate).

FUNCTION TABLE

INPUTS				OUTPUT
nA	**nB**	**nC**	**nD**	**nY**
L	X	X	X	H
X	L	X	X	H
X	X	L	X	H
X	X	X	L	H
H	H	H	H	L

Notes

1. H = HIGH voltage level
   L = LOW voltage level
   X = don't care

Dual 4-input NAND gate

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: standard
I_{CC} category: SSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f = 6$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} (V)	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/ t_{PLH}	propagation delay nA, nB, nC, nD to nY		28 10 8	90 18 15		115 23 20		135 27 23	ns	2.0 4.5 6.0	Fig.7
t_{THL}/ t_{TLH}	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig.7

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: standard
I_{CC} category: SSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications.
To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.
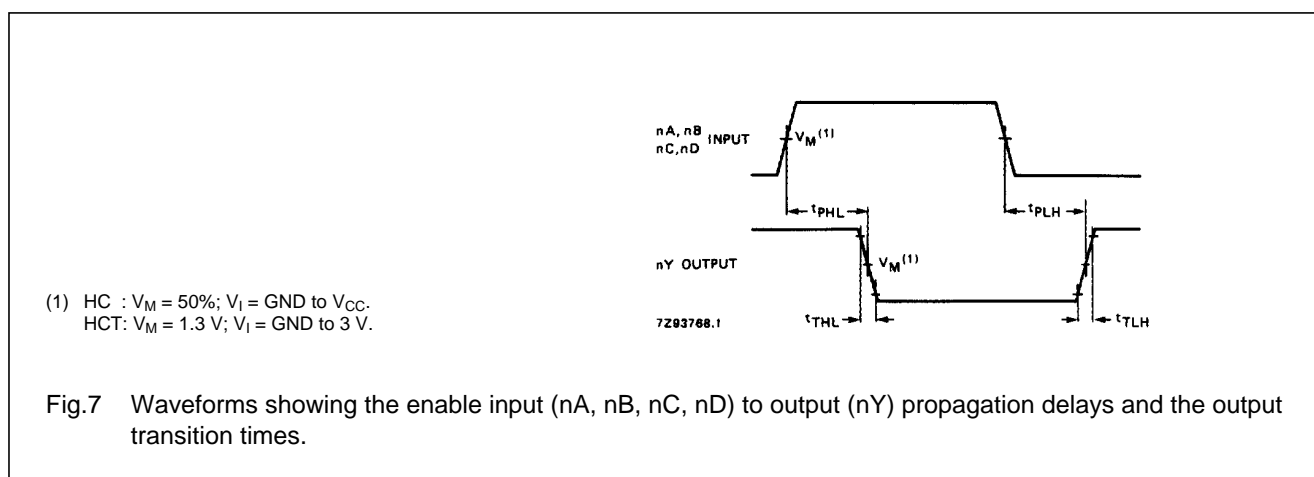
INPUT	UNIT LOAD COEFFICIENT
nA, nB, nC, nD	0.3

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} (V)	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/ t_{PLH}	propagation delay nA, nB, nC, nD to nY		16	28		35		42	ns	4.5	Fig.7
t_{THL}/ t_{TLH}	output transition time		7	15		19		22	ns	4.5	Fig.7

AC WAVEFORMS

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

Fig.7   Waveforms showing the enable input (nA, nB, nC, nD) to output (nY) propagation delays and the output transition times.

PACKAGE OUTLINES

See *"74HC/HCT/HCU/HCMOS Logic Package Outlines"*.