

# DATA SHEET

For a complete data sheet, please also download:

- The IC06 74HC/HCT/HCU/HCMOS Logic Family Specifications
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Information
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Outlines

## **74HC/HCT30** 8-input NAND gate

Product specification  
File under Integrated Circuits, IC06

December 1990

## 8-input NAND gate

## 74HC/HCT30

## FEATURES

- Output capability: standard
- $I_{CC}$  category: SSI

## GENERAL DESCRIPTION

The 74HC/HCT30 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT30 provide the 8-input NAND function.

## QUICK REFERENCE DATA

GND = 0 V;  $T_{amb} = 25\text{ }^{\circ}\text{C}$ ;  $t_r = t_f = 6\text{ ns}$

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
$t_{PHL}/t_{PLH}$	propagation delay A, B, C, D, E, F, G, H to Y	$C_L = 15\text{ pF}$ ; $V_{CC} = 5\text{ V}$	12	12	ns
$C_I$	input capacitance		3.5	3.5	pF
$C_{PD}$	power dissipation capacitance per gate	notes 1 and 2	15	15	pF

## Notes

1.  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu\text{W}$ ):  

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$$
 where:  
 $f_i$  = input frequency in MHz  
 $f_o$  = output frequency in MHz  
 $\sum (C_L \times V_{CC}^2 \times f_o)$  = sum of outputs  
 $C_L$  = output load capacitance in pF  
 $V_{CC}$  = supply voltage in V
2. For HC the condition is  $V_I = \text{GND to } V_{CC}$   
 For HCT the condition is  $V_I = \text{GND to } V_{CC} - 1.5\text{ V}$

## ORDERING INFORMATION

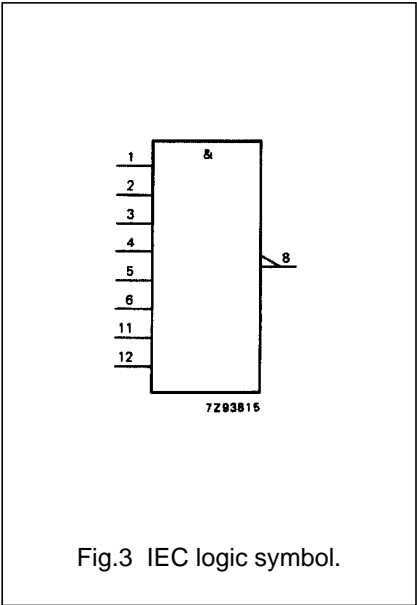
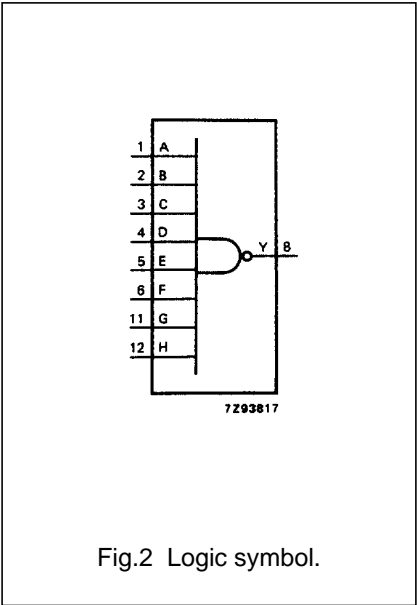
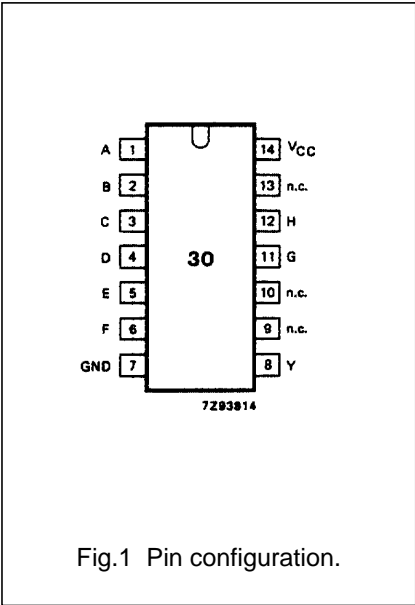
See *"74HC/HCT/HCU/HCMOS Logic Package Information"*.

8-input NAND gate

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PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	A	data input
2	B	data input
3	C	data input
4	D	data input
5	E	data input
6	F	data input
7	GND	ground (0 V)
8	Y	data output
9, 10, 13	n.c.	not connected
11	G	data input
12	H	data input
14	V <sub>CC</sub>	positive supply voltage



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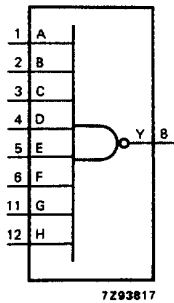


Fig.4 Functional diagram;  
 $Y = ABCDEFGH$ .

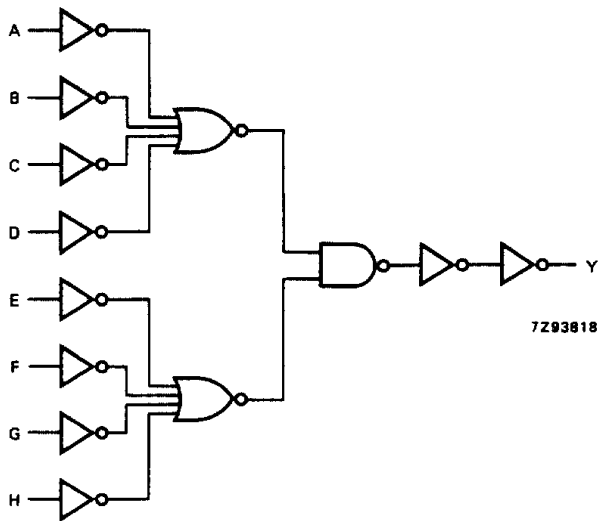


Fig.5 Logic diagram.

FUNCTION TABLE

INPUTS								OUTPUT
A	B	C	D	E	F	G	H	Y
L	X	X	X	X	X	X	X	H
X	L	X	X	X	X	X	X	H
X	X	L	X	X	X	X	X	H
X	X	X	L	X	X	X	X	H
X	X	X	X	L	X	X	X	H
X	X	X	X	X	L	X	X	H
X	X	X	X	X	X	L	X	H
X	X	X	X	X	X	X	L	H
H	H	H	H	H	H	H	H	L

Notes

1. H = HIGH voltage level  
L = LOW voltage level  
X = don't care

## 8-input NAND gate

## 74HC/HCT30

**DC CHARACTERISTICS FOR 74 HC**

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: standard

I<sub>CC</sub> category: SSI

**AC CHARACTERISTICS FOR 74HC**

GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)							UNIT	TEST CONDITIONS	
		74HC								V <sub>CC</sub> (V)	WAVEFORMS
		+25			−40 to + 85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay A, B, C, D, E, F, G, H to Y		41 15 12	130 26 22		165 33 28		195 39 33	ns	2.0 4.5 6.0	Fig.6
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig.6

**DC CHARACTERISTICS FOR 74HCT**

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: standard

I<sub>CC</sub> category: SSI

**Note to HCT types**

The value of additional quiescent supply current (ΔI<sub>CC</sub>) for a unit load of 1 is given in the family specifications. To determine ΔI<sub>CC</sub> per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
A, B, C, D, E, F, G, H	0.60

**AC CHARACTERISTICS FOR 74HCT**

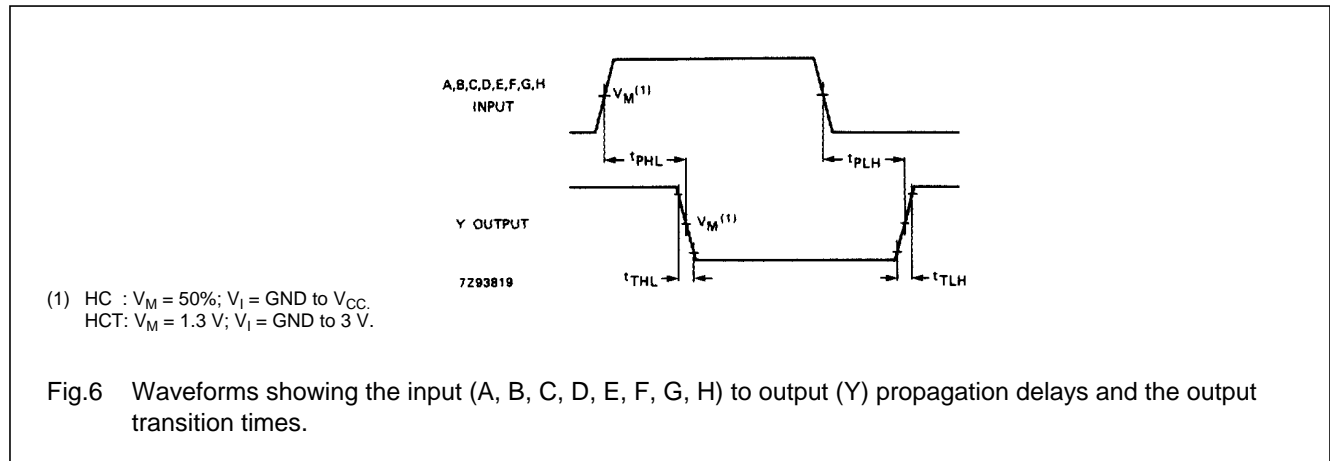
GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)							UNIT	TEST CONDITIONS	
		74HCT								V <sub>CC</sub> (V)	WAVEFORMS
		+25			−40 to + 85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay A, B, C, D, E, F, G, H to Y		16	28		35		42	ns	4.5	Fig.6
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		7	15		19		22	ns	4.5	Fig.6

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## AC WAVEFORMS



## PACKAGE OUTLINES

See *"74HC/HCT/HCU/HCMOS Logic Package Outlines"*.