

2-wide 3-Input, 2-wide 2-Input AND-OR-Invert Gate IC in bare die form

Rev 1.1 24/01/24

Description

The 74ALS51 is fabricated using a 2µm 40V Bipolar process. The device consists of two independent combinations of gates each performing the logic AND-OR-INVERT function. The IC integrates one 2-wide 3-input gates and one 2-wide 2-input gates each performing Boolean functions $1Y = (1A \cdot 1B \cdot 1C) + (1D \cdot 1E \cdot 1F)$ and $2Y = (2A \cdot 2B) + (2C \cdot 2D)$ respectively. All inputs are protected against ESD and excess voltage transients.

Ordering Information

The following part suffixes apply:

No suffix - MIL-STD-883 /2010B Visual Inspection

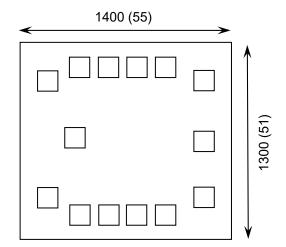
For High Reliability versions of this product please see

54ALS51

Features:

- High speed 14ns (Max) propagation delay
- Industrial Temperature Range
- Direct drop-in replacement for obsolete components in long term programs.

Die Dimensions in µm (mils)



Supply Formats:

- Default Die in Waffle Pack (400 per tray capacity)
- Sawn Wafer on Tape On request
- Unsawn Wafer On request
- Die Thickness <> 350µm(14 Mils) On request
- Assembled into Ceramic Package On request

Mechanical Specification

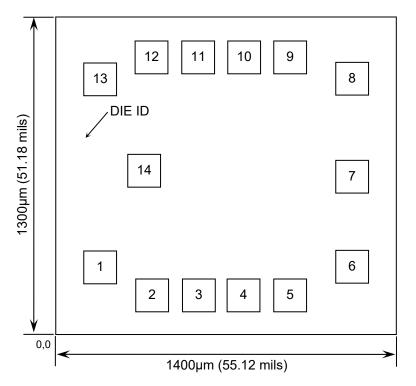
Die Size (Unsawn)	1400 x1300 55 x 51	μm mils	
Minimum Bond Pad Size	130 x 130 5.12 x 5.12	μm mils	
Die Thickness	350 (±20) 13.78 (±0.79)	μm mils	
Top Metal Composition	Al 1%Si 1.1μm		
Back Metal Composition	N/A – Bare Si		





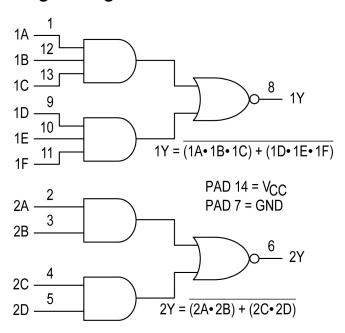
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Pad Layout and Functions



PAD	FUNCTION	COORDINATES (mm)			
		X	Υ		
1	1A	0.110	0.215		
2	2A	0.325	0.100		
3	2B	0.515	0.100		
4	2C	0.705	0.100		
5	2D	0.895	0.100		
6	2Y	1.150	0.215		
7	GND	1.150	0.585		
8	1Y	1.150	0.985		
9	1D	0.895	1.070		
10	1E	0.705	1.070		
11	1F	0.515	1.070		
12	1B	0.325	1.070		
13	1C	0.110	0.985		
14	V_{CC}	0.295	0.610		

Logic Diagram



Truth Table

INPUTS						OUTPUT
1A	1B	1C	1D	1E	1F	1Y
Н	Н	Н	Χ	Χ	Х	L
X	Χ	Х	Н	Н	Н	L
	All other combinations					
INPUTS					OUTPUT	
2A		2B	2C	2D		2Y
Н		Н	Χ	X		L
Х		Χ	Н		Н	L
	All other combinations H					
H = High level (steady state)						
	L = Low level (steady state)					
X = don't care						





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Absolute Maximum Ratings¹

PARAMETER	SYMBOL	VALUE	UNIT
DC Supply Voltage	V _{CC}	7.0	V
DC Input Voltage	V _{IN}	7.0	V
Storage Temperature Range	T _{STG}	-65 to 150	°C

^{1.} Operation above the absolute maximum rating may cause device failure. Operation at the absolute maximum ratings, for extended periods, may reduce device reliability.

Recommended Operating Conditions

PARAMETER	SYMBOL	MIN	MAX	UNITS
Supply Voltage	V_{CC}	4.5	5.5	V
High-Level Input Voltage	V_{IH}	2	-	V
Low-Level Input Voltage	V_{IL}	-	0.8	V
High-Level Output Current	I _{OH}	-	-0.4	mA
Low-Level Output Current	I _{OL}	-	8	mA
Operating Temperature Range	TJ	-40	+85	°C

DC Electrical Characteristics² T_J = -40°C to 85°C unless otherwise specified

PARAMETER	SYMBOL	CONDITIONS		LIMITS		
TAKAMETEK	STWIDGE	CONDITIONS	MIN	TYP	MAX	UNITS
Minimum High-Level Input Voltage	V _{IH}	-	2	-	-	V
Maximum Low-Level Input Voltage	V _{IL}	-	-	-	0.7	V
Input Clamp Diode Voltage	V _{IK}	$V_{CC} = MIN$ $I_{IN} = -18mA$	-	-	-1.5	V
Output Voltage High	V _{OH}	V_{CC} = MIN, I_{OH} = MAX V_{IN} = V_{IL} or V_{IH} per Truth Table	V _{cc} -2	-	-	V
Output Voltage Low	V _{OL}	$ \begin{array}{c c} V_{CC} = V_{CC} \ MIN \\ I_{OH} = MAX \\ V_{IN} = V_{IL} \ or \ V_{IH} \\ per \ Truth \ Table \end{array} I_{OL} = 8 $	BmA -	0.35	0.5	V
Input Current	I _{IN}	$V_{CC} = MAX, V_{IN} = 7.0$	-	-	0.1	mA
Input High Current	I _{IH}	$V_{CC} = MAX, V_{IN} = 2.7$	-	-	20	μA
Input Low Current	I _{IL}	$V_{CC} = MAX, V_{IN} = 0.4$	-	-	-0.1	mA
Short Circuit Current ³	Ios	V _{CC} = MAX	-30	-	-112	mA
Power Supply	laa	V _{CC} = MAX ,Output Hig	gh -	-	1.2	mA
Current (Total)		V _{CC} = MAX ,Output Lo	w -	-	1.5	

^{2.} All typical values @ V_{CC} = 5V, T_J = 25°C. 3. Not more than one output should be shorted at a time, nor for more than 1 second.





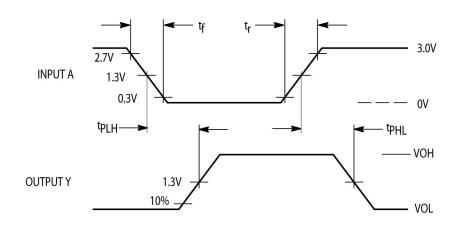
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AC Electrical Characteristics⁴

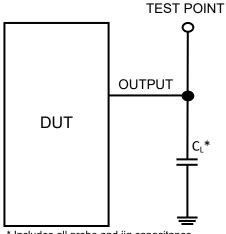
PARAMETER	SYMBOL CONDITIONS	CONDITIONS	LIMITS			UNITS
		MIN	TYP	MAX	Oiliro	
Turn-Off Delay, Input to Output	t _{PLH}	$V_{CC} = 5V, C_L = 50pF,$ $R_L = 500\Omega$	2	-	14	
Turn-On Delay, Input to Output	t _{PHL}	$V_{CC} = 5V, C_{L} = 50pF,$ $R_{L} = 500\Omega$	3	-	12	ns

^{4.} Not production tested in die form, characterized by chip design and tested in package.

Switching Waveform



Test Circuit



* Includes all probe and jig capacitance

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