

# DATA SHEET

## **74ALS175** Quad D flip–flop

Product specification  
IC05 Data Handbook

1991 Feb 08

Quad D flip-flop

74ALS175

FEATURES

- Four edge-triggered D flip-flops
- Buffered common clock
- Buffered asynchronous master reset
- True and complementary outputs

DESCRIPTION

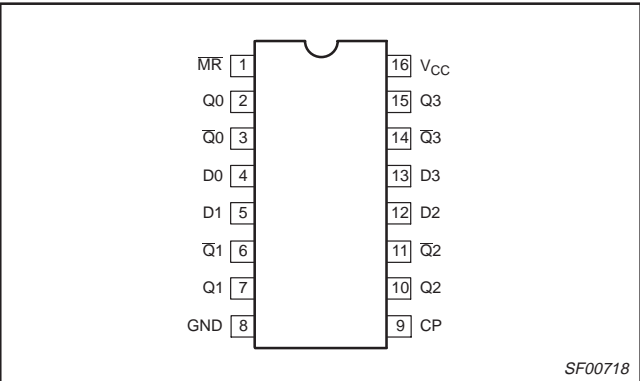
The 74ALS175 is a quad, edge-triggered D-type flip-flops with individual D inputs and both Q and  $\bar{Q}$  outputs. The common buffered clock (CP) and master reset ( $\overline{MR}$ ) inputs load and reset (clear) all flip-flops simultaneously.

The register is fully edge-triggered. The state of each D input, one setup time before the Low-to-High clock transition is transferred to the corresponding flip-flop's Q output.

All Q outputs will be forced Low independent of clock or data inputs by a Low voltage level on the  $\overline{MR}$  input. The device is useful for applications where both true and complement outputs are required, and the clock and master reset are common to all storage elements.

TYPE	TYPICAL $f_{\text{MAX}}$	TYPICAL SUPPLY CURRENT (TOTAL)
74ALS175	70MHz	7mA

PIN CONFIGURATION



ORDERING INFORMATION

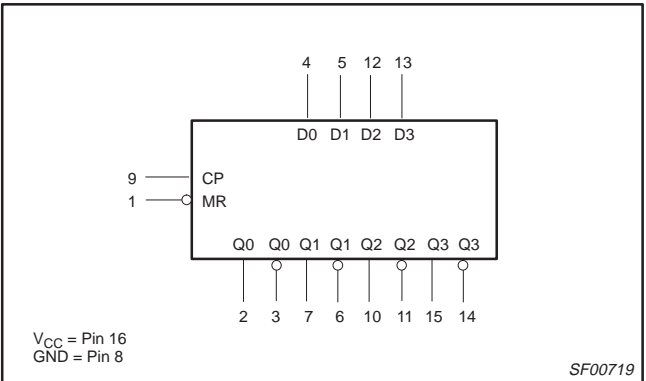
DESCRIPTION	ORDER CODE	DRAWING NUMBER
	COMMERCIAL RANGE $V_{\text{CC}} = 5\text{V} \pm 10\%$ , $T_{\text{amb}} = 0^{\circ}\text{C to } +70^{\circ}\text{C}$	
16-pin plastic DIP	74ALS175N	SOT38-4
16-pin plastic SO	74ALS175D	SOT109-1

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

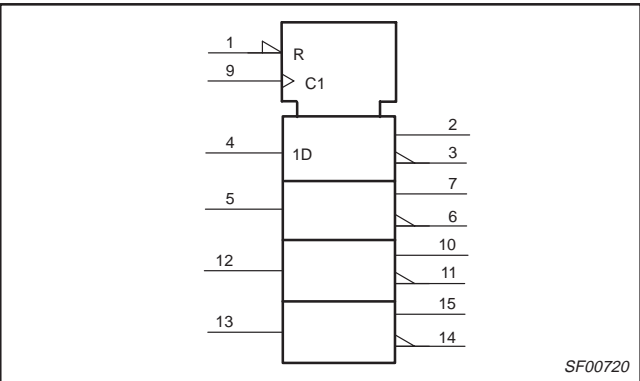
PINS	DESCRIPTION	74ALS (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D0 – D3	Data inputs	1.0/1.0	20 $\mu$ A/0.1mA
CP	Clock Pulse input (active rising edge)	1.0/1.0	20 $\mu$ A/0.1mA
$\overline{MR}$	Master Reset input (active-Low)	1.0/1.0	20 $\mu$ A/0.1mA
Q0 – Q3	True outputs	20/80	0.4mA/8mA
$\bar{Q}$ 0 – $\bar{Q}$ 3	Complementary outputs	20/80	0.4mA/8mA

NOTE: One (1.0) ALS unit load is defined as: 20 $\mu$ A in the High state and 0.1mA in the Low state.

LOGIC SYMBOL



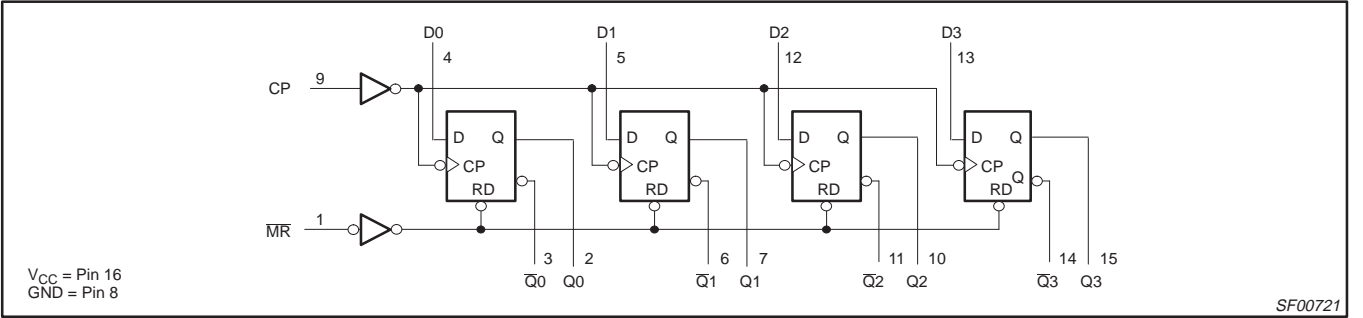
IEC/IEEE SYMBOL



Quad D flip-flop

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LOGIC DIAGRAM



FUNCTION TABLE

INPUTS			OUTPUTS		OPERATING MODE
MR	CP	D	$Q_n$	$\bar{Q}_n$	
L	X	X	L	H	Reset (clear)
H	$\uparrow$	h	H	L	Load "1"
H	$\uparrow$	l	L	H	Load "0"

NOTES:

- H = High-voltage level  
h = High state must be present one setup time before the Low-to-High clock transition  
L = Low-voltage level  
l = Low state must be present one setup time before the Low-to-High clock transition  
X = Don't care  
 $\uparrow$  = Low-to-High clock transition

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limit set forth in this table may impair the useful life of the device.  
Unless otherwise noted these limits are over the operating free air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
$V_{CC}$	Supply voltage	-0.5 to +7.0	V
$V_{IN}$	Input voltage	-0.5 to +7.0	V
$I_{IN}$	Input current	-30 to +5	mA
$V_{OUT}$	Voltage applied to output in High output state	-0.5 to $V_{CC}$	V
$I_{OUT}$	Current applied to output in Low output state	16	mA
$T_{amb}$	Operating free-air temperature range	0 to +70	°C
$T_{stg}$	Storage temperature range	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
$V_{CC}$	Supply voltage	4.5	5.0	5.5	V
$V_{IH}$	High-level input voltage	2.0			V
$V_{IL}$	Low-level input voltage			0.8	V
$I_{IK}$	Input clamp current			-18	mA
$I_{OH}$	High-level output current			-0.4	mA
$I_{OL}$	Low-level output current			8	mA
$T_{amb}$	Operating free-air temperature range	0		+70	°C

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## DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS <sup>1</sup>	LIMITS			UNIT
			MIN	TYP <sup>2</sup>	MAX	
$V_{OH}$	High-level output voltage	$V_{CC} \pm 10\%$ , $V_{IL} = \text{MAX}$ , $V_{IH} = \text{MIN}$ , $I_{OH} = \text{MAX}$	$V_{CC} - 2$			V
$V_{OL}$	Low-level output voltage	$V_{CC} = \text{MIN}$ , $V_{IL} = \text{MAX}$ , $V_{IH} = \text{MIN}$		0.25	0.4	V
				0.35	0.50	V
$V_{IK}$	Input clamp voltage	$V_{CC} = \text{MIN}$ , $I_I = I_{IK}$		-0.73	-1.5	V
$I_I$	Input current at maximum input voltage	$V_{CC} = \text{MAX}$ , $V_I = 7.0\text{V}$			100	$\mu\text{A}$
$I_{IH}$	High-level input current	$V_{CC} = \text{MAX}$ , $V_I = 2.7\text{V}$			20	$\mu\text{A}$
$I_{IL}$	Low-level input current	$V_{CC} = \text{MAX}$ , $V_I = 0.5\text{V}$			-0.1	mA
$I_O$	Output current <sup>3</sup>	$V_{CC} = \text{MAX}$ , $V_O = 2.25\text{V}$	-30		-112	mA
$I_{CC}$	Supply current (total)	$V_{CC} = \text{MAX}$		7	14	mA

## NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at  $V_{CC} = 5\text{V}$ ,  $T_{\text{amb}} = 25^\circ\text{C}$ .
- The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current,  $I_{OS}$ .

## AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS		UNIT
			$T_{\text{amb}} = 0^{\circ}\text{C to } +70^{\circ}\text{C}$ $V_{\text{CC}} = +5.0\text{V} \pm 10\%$ $C_{\text{L}} = 50\text{pF}, R_{\text{L}} = 500\Omega$		
			MIN	MAX	
f <sub>MAX</sub>	Maximum clock frequency	Waveform 1	60		MHz
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay CP to Qn or CP to $\overline{\text{Qn}}$	Waveform 1	3.0 5.0	13.0 16.0	ns
t <sub>PLH</sub>	Propagation delay, $\overline{\text{MR}}$ to Qn	Waveform 2	3.0	13.0	ns
t <sub>PHL</sub>	Propagation delay, $\overline{\text{MR}}$ to $\overline{\text{Qn}}$	Waveform 2	8.0	18.0	ns

## AC SETUP REQUIREMENTS

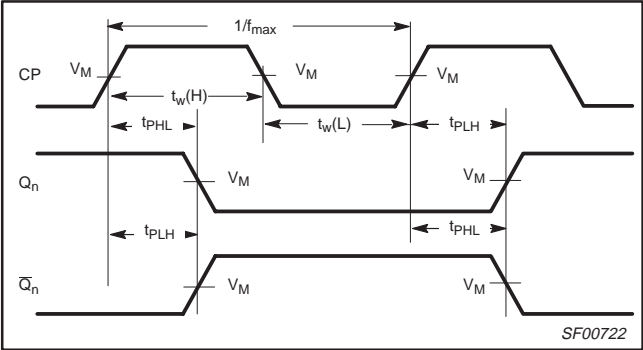
SYMBOL	PARAMETER	TEST CONDITION	LIMITS		UNIT
			T <sub>amb</sub> = 0°C to +70°C V <sub>CC</sub> = +5.0V ± 10% C <sub>L</sub> = 50pF, R <sub>L</sub> = 500Ω		
			MIN	MAX	
t <sub>su</sub> (H) t <sub>su</sub> (L)	Setup time, High or Low Dn to CP	Waveform 3	6.0 6.0		ns
t <sub>h</sub> (H) t <sub>h</sub> (L)	Hold time, High or Low Dn to CP	Waveform 3	0.0 0.0		ns
t <sub>w</sub> (H) t <sub>w</sub> (L)	CP pulse width, High or Low	Waveform 1	8.0 8.0		ns
t <sub>w</sub> (L)	$\overline{\text{MR}}$ pulse width, Low	Waveform 2	6.0		ns
t <sub>REC</sub>	Recovery time, $\overline{\text{MR}}$ to CP	Waveform 2	6.0		ns

Quad D flip-flop

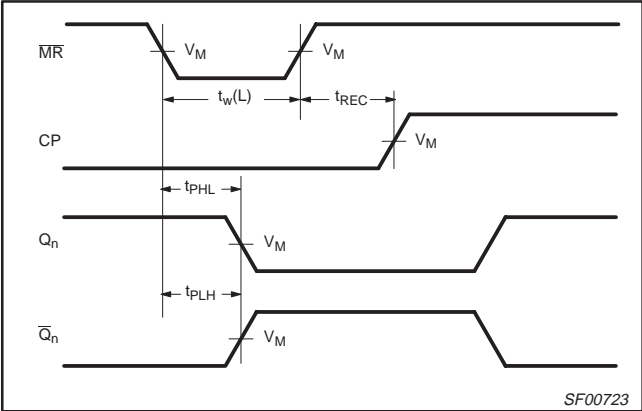
74ALS175

AC WAVEFORMS

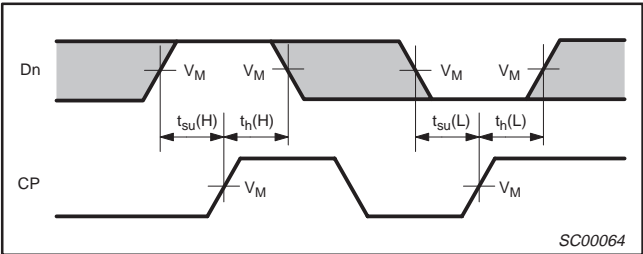
For all waveforms,  $V_M = 1.3V$ .  
The shaded areas indicate when the input is permitted to change for predictable output performance.



Waveform 1. Propagation Delay for Clock Input to Output, Clock Pulse Width, and Maximum Clock Frequency

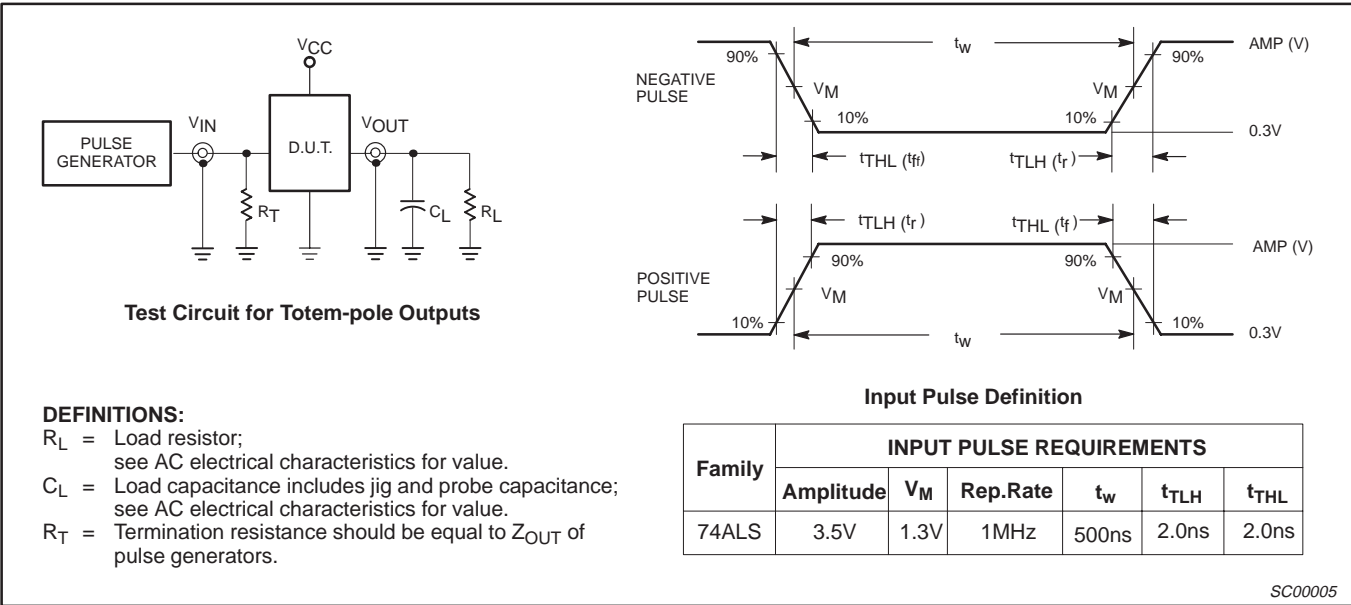


Waveform 2. Master Reset Pulse Width, Master Reset to Output Delay, and Master Reset to Clock Recovery Time



Waveform 3. Data Setup and Hold Times

TEST CIRCUIT AND WAVEFORMS

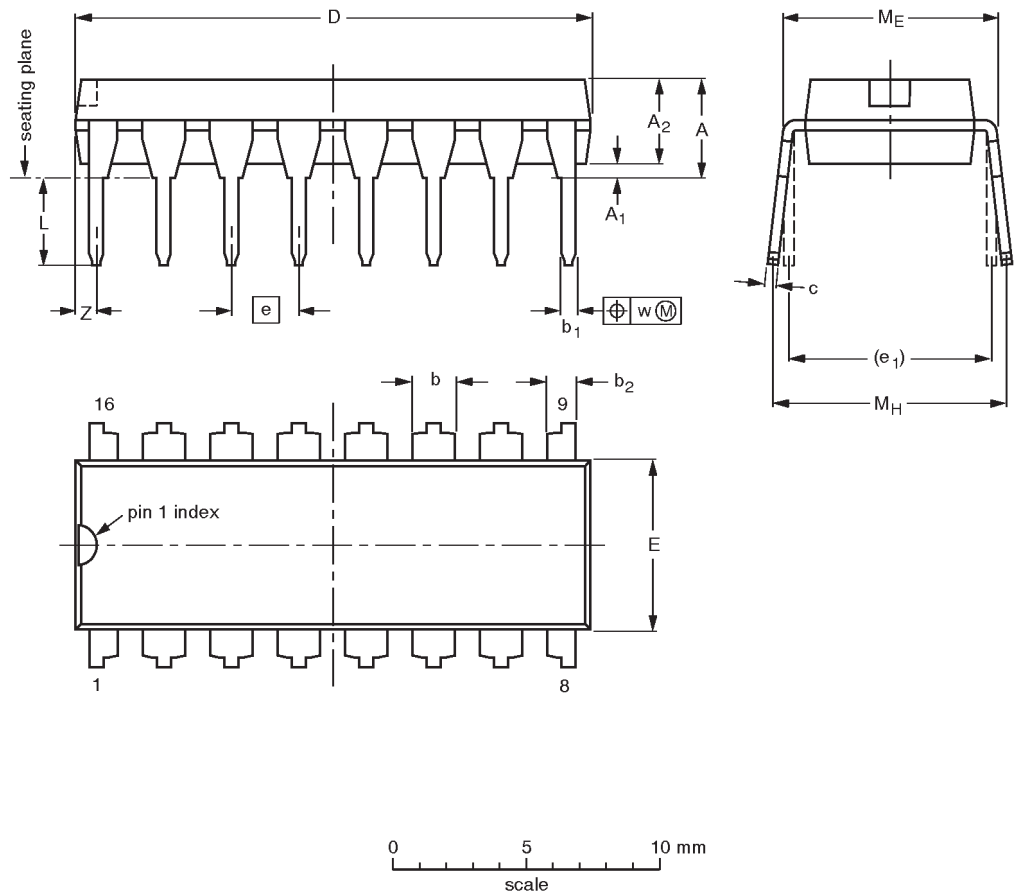


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DIP16: plastic dual in-line package; 16 leads (300 mil)

SOT38-4



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A <sub>1</sub> min.	A <sub>2</sub> max.	b	b <sub>1</sub>	b <sub>2</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	e <sub>1</sub>	L	M <sub>E</sub>	M <sub>H</sub>	w	Z <sup>(1)</sup> max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	1.25 0.85	0.36 0.23	19.50 18.55	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	0.76
inches	0.17	0.020	0.13	0.068 0.051	0.021 0.015	0.049 0.033	0.014 0.009	0.77 0.73	0.26 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.030

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

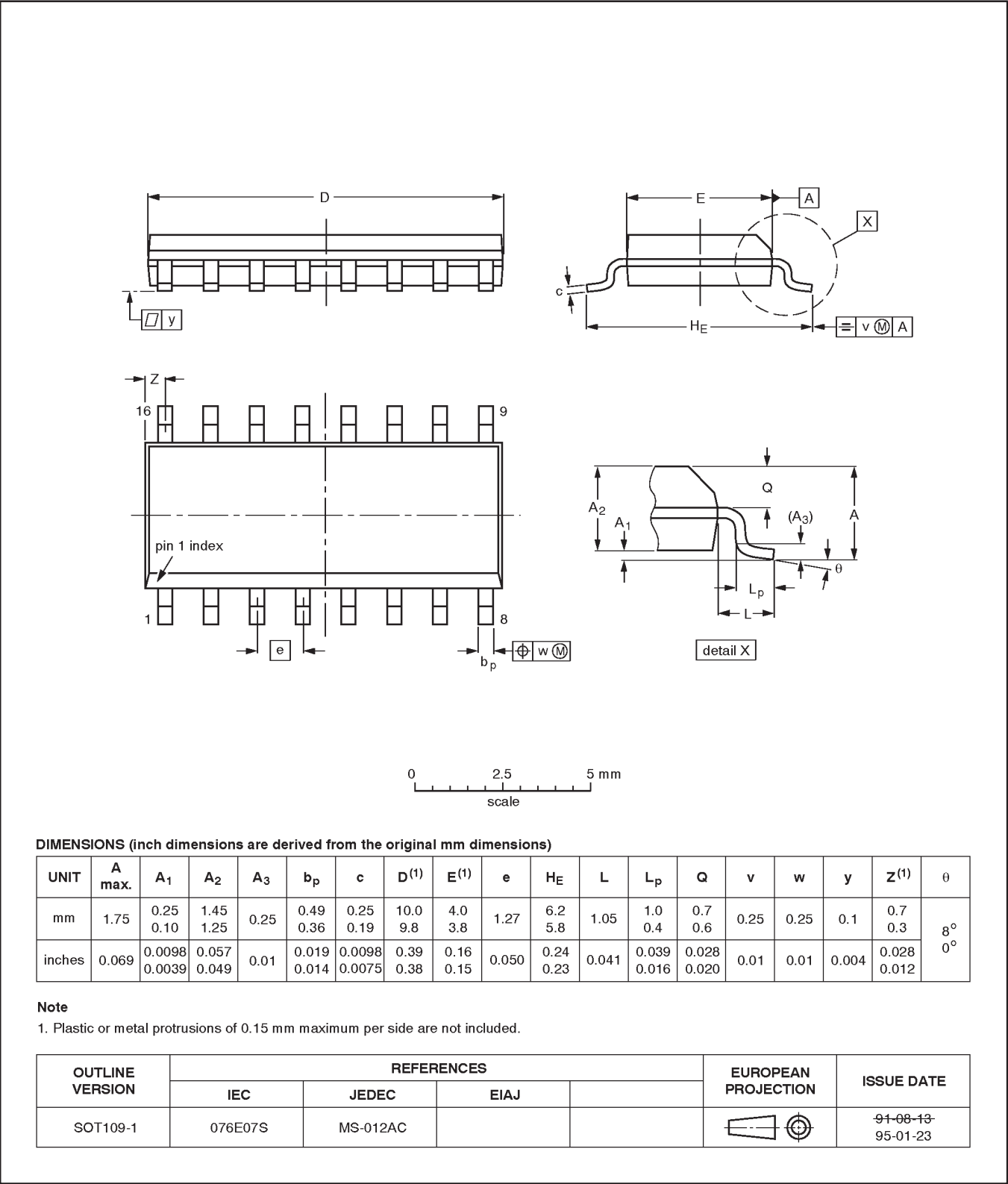
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT38-4						92-11-17 95-01-14

Quad D flip-flop

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SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1



Quad D flip-flop

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DEFINITIONS		
Data Sheet Identification	Product Status	Definition
Objective Specification	Formative or in Design	This data sheet contains the design target or goal specifications for product development. Specifications may change in any manner without notice.
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