DATA SHEET

For a complete data sheet, please also download:

- The IC06 74HC/HCT/HCU/HCMOS Logic Family Specifications
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Information
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Outlines

74HC/HCT182
Look-ahead carry generator

Product specification
File under Integrated Circuits, IC06

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Philips
Semiconductors

PHILIPS

Look-ahead carry generator 74HC/HCT182

FEATURES

- Provides carry look-ahead across a group of four ALU's
- Multi-level look-ahead for high-speed arithmetic operation over long word length
- Output capability: standard
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT182 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT182 carry look-ahead generators accept up to four pairs of active LOW carry propagate ($\overline{P}_0$, $\overline{P}_1$, $\overline{P}_2$, $\overline{P}_3$) and carry generate ($\overline{G}_0$, $\overline{G}_1$, $\overline{G}_2$, $\overline{G}_3$) signals and an active HIGH carry input (C_n). The devices provide anticipated active HIGH carries (C_{n+x}, C_{n+y}, C_{n+z}) across four groups of binary adders.

The "182" also has active LOW carry propagate ($\overline{P}$) and carry generate ($\overline{G}$) outputs which may be used for further levels of look-ahead.

The logic equations provided at the outputs are:

$$C_{n+x} = G_0 + P_0C_n$$
$$C_{n+y} = G_1 + P_1G_0 + P_1P_0C_n$$
$$C_{n+z} = G_2 + P_2G_1 + P_2P_1G_0 + P_2P_1P_0C_n$$
$$\overline{G} = \overline{G_3 + P_3G_2 + P_3P_2G_1 + P_3P_2P_1G_O}$$
$$\overline{P} = \overline{P_3P_2P_1P_0}$$

The "182" can also be used with binary ALU's in an active LOW or active HIGH input operand mode. The connections to and from the ALU to the carry look-ahead generator are identical in both cases.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/ t_{PLH}	propagation delay $\overline{P}_n$ to $\overline{P}$ C_n to any output $\overline{P}_n$ or $\overline{G}_n$ to any output	C_L = 15 pF; V_{CC} = 5 V	 11 17 14	 14 21 17	 ns ns ns
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per package	notes 1 and 2	50	50	pF

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):

   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where:

   f_i = input frequency in MHz

   f_o = output frequency in MHz

   $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs

   C_L = output load capacitance in pF

   V_{CC} = supply voltage in V
2. For HC the condition is V_I = GND to V_{CC}

   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

ORDERING INFORMATION

See *"74HC/HCT/HCU/HCMOS Logic Package Information"*.

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
3, 1, 14, 5	$\overline{G}_0$ to $\overline{G}_3$	carry generate inputs (active LOW)
4, 2, 15, 6	$\overline{P}_0$ to $\overline{P}_3$	carry propagate inputs (active LOW)
7	$\overline{P}$	carry propagate output (active LOW)
8	GND	ground (0 V)
9	C_{n+z}	function output
10	$\overline{G}$	carry generate output (active LOW)
11	C_{n+y}	function output
12	C_{n+x}	function output
13	C_n	carry input (active HIGH)
16	V_{CC}	positive supply voltage

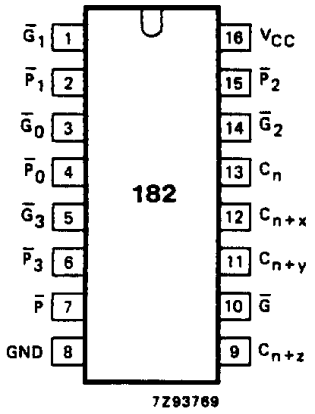


Fig.1 Pin configuration.

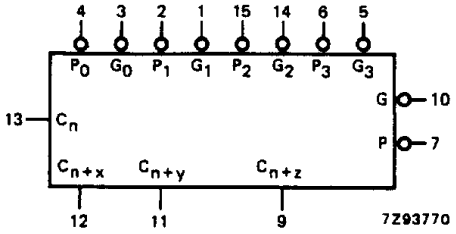


Fig.2 Logic symbol.

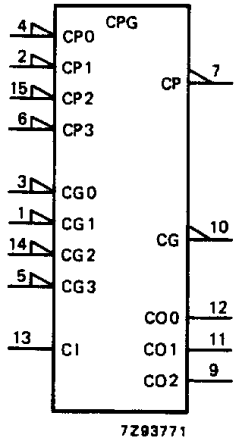


Fig.3 IEC logic symbol.

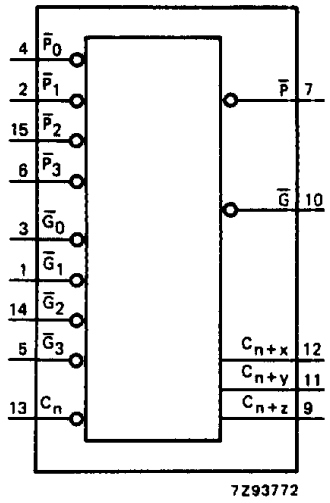


Fig.4 Functional diagram.

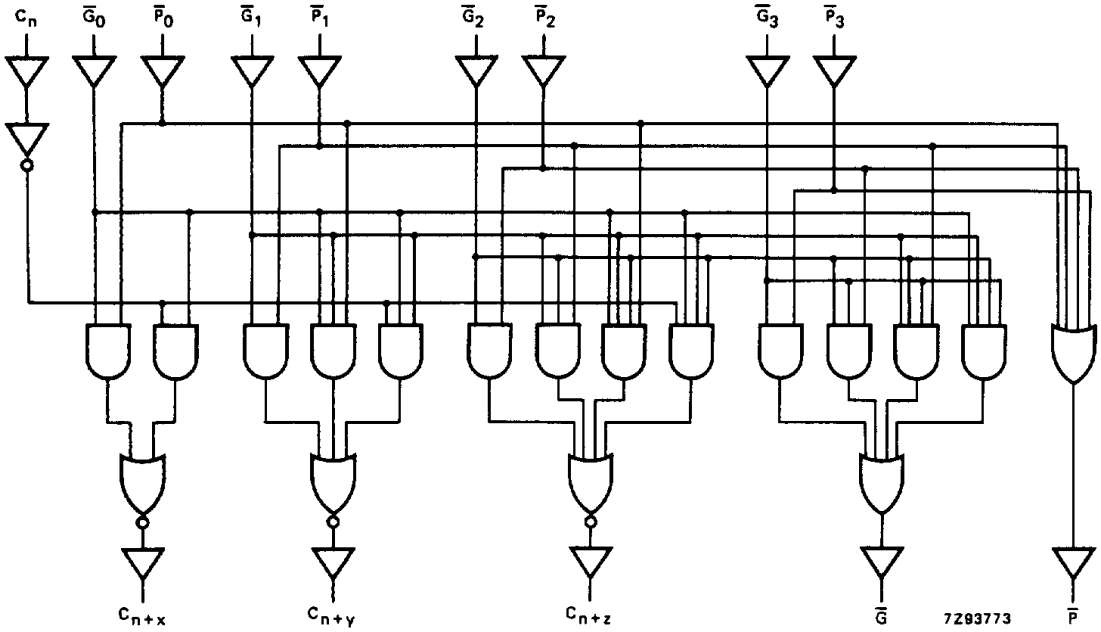


Fig.5 Logic diagram.

FUNCTION TABLE

INPUTS									OUTPUTS				
C_n	$\overline{G}_0$	$\overline{P}_0$	$\overline{G}_1$	$\overline{P}_1$	$\overline{G}_2$	$\overline{P}_2$	$\overline{G}_3$	$\overline{P}_3$	C_{n+x}	C_{n+y}	C_{n+z}	$\overline{G}$	$\overline{P}$
X L X H	H H L X	H X X L							L L H H				
X X L X X H	X H H X L X	X H X X X L	H H H L X X	H X X X L L						L L L H H H			
X X X L X X X H	X X H H X X L X	X X H X X X X L	X H H H X L X X	X H X X X L L	H H H H L X X X	H X X X X L L L					L L L L H H H H		
	X X X H X X X L		X X H H X X L X	X X H X X X X L	X H H H X L X X	X H X X X X L L	H H H H L X X X	H X X X X L L L				H H H H L L L L	
		H X X X L		X H X X L		X X H X L		X X X H L					H H H H L

Notes

1. H = HIGH voltage level
   L = LOW voltage level
   X = don't care

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: standard
I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} (V)	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/ t_{PLH}	propagation delay $\overline{P}_n$ to $\overline{P}$		30 14 11	120 24 20		150 30 26		180 36 31	ns	2.0 4.5 6.0	Fig.6
t_{PHL}/ t_{PLH}	propagation delay C_n to any output		55 20 16	170 34 29		215 43 37		255 51 43	ns	2.0 4.5 6.0	Fig.6
t_{PHL}/ t_{PLH}	propagation delay $\overline{P}_n$ to $\overline{G}$		47 17 14	145 29 25		180 36 31		220 44 38	ns	2.0 4.5 6.0	Fig.6
t_{PHL}/ t_{PLH}	propagation delay $\overline{P}_n$ to C_{n+n}		47 17 14	145 29 25		180 36 31		220 44 38	ns	2.0 4.5 6.0	Fig.6
t_{PHL}/ t_{PLH}	propagation delay $\overline{G}_n$ to C_{n+n}		44 16 13	135 27 23		170 34 29		205 41 35	ns	2.0 4.5 6.0	Fig.6
t_{PHL}/ t_{PLH}	propagation delay $\overline{G}_n$ to $\overline{G}$		41 15 12	135 27 23		170 34 29		205 41 35	ns	2.0 4.5 6.0	Fig.6
t_{THL}/ t_{TLH}	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig.6

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: standard
I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
$\overline{G}_0$, $\overline{G}_1$, $\overline{P}_0$, $\overline{P}_1$, $\overline{P}_2$	1.50
$\overline{G}_3$	0.30
$\overline{G}_2$, $\overline{P}_3$, C_n	1.25

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} (V)	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/ t_{PLH}	propagation delay $\overline{P}_n$ to $\overline{P}$		17	28		35		42	ns	4.5	Fig.6
t_{PHL}/ t_{PLH}	propagation delay C_n to any output		26	43		54		65	ns	4.5	Fig.6
t_{PHL}/ t_{PLH}	propagation delay $\overline{P}_n$ to $\overline{G}$		20	33		41		50	ns	4.5	Fig.6
t_{PHL}/ t_{PLH}	propagation delay $\overline{P}_n$ to C_{n+n}		20	33		41		50	ns	4.5	Fig.6
t_{PHL}/ t_{PLH}	propagation delay $\overline{G}_n$ to C_{n+n}, $\overline{G}_n$ to $\overline{G}$		18	32		40		48	ns	4.5	Fig.6
t_{THL}/ t_{TLH}	output transition time		7	15		19		22	ns	4.5	Fig.6

AC WAVEFORMS

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

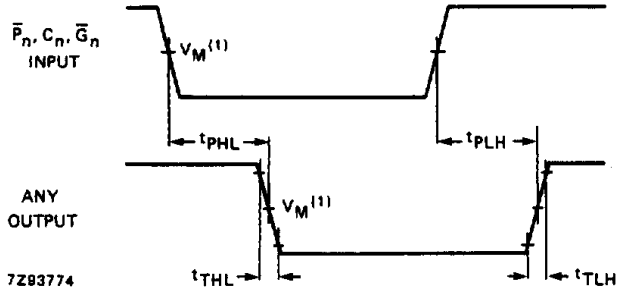
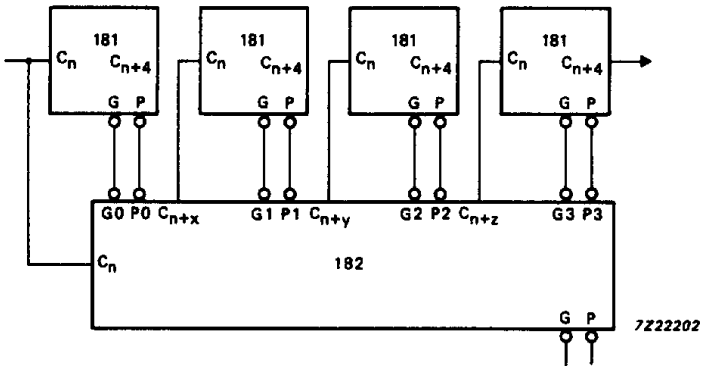


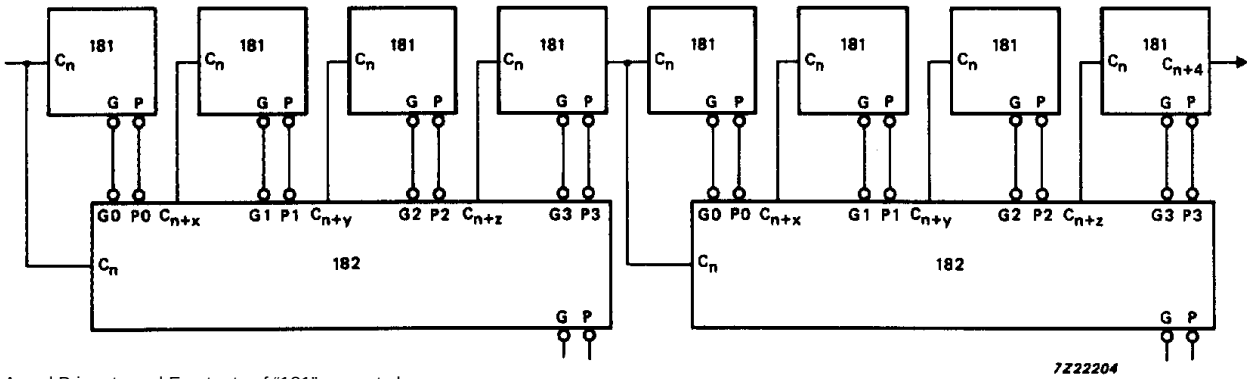
Fig.6 Waveforms showing the input ($\overline{P}_n$, C_n, $\overline{G}_n$) to any output propagation delays and the output transition times.

APPLICATION INFORMATION



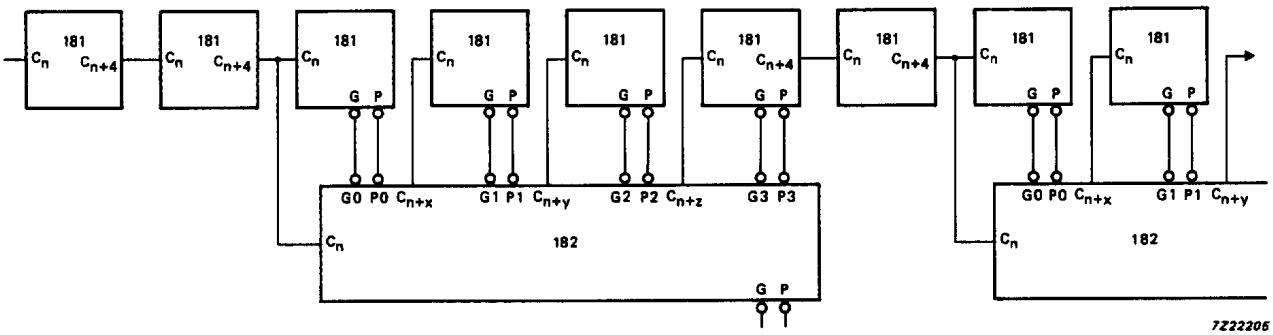
A and B inputs and F outputs of “181” are not shown.

Fig.7 16-bit ALU two-level look-ahead.



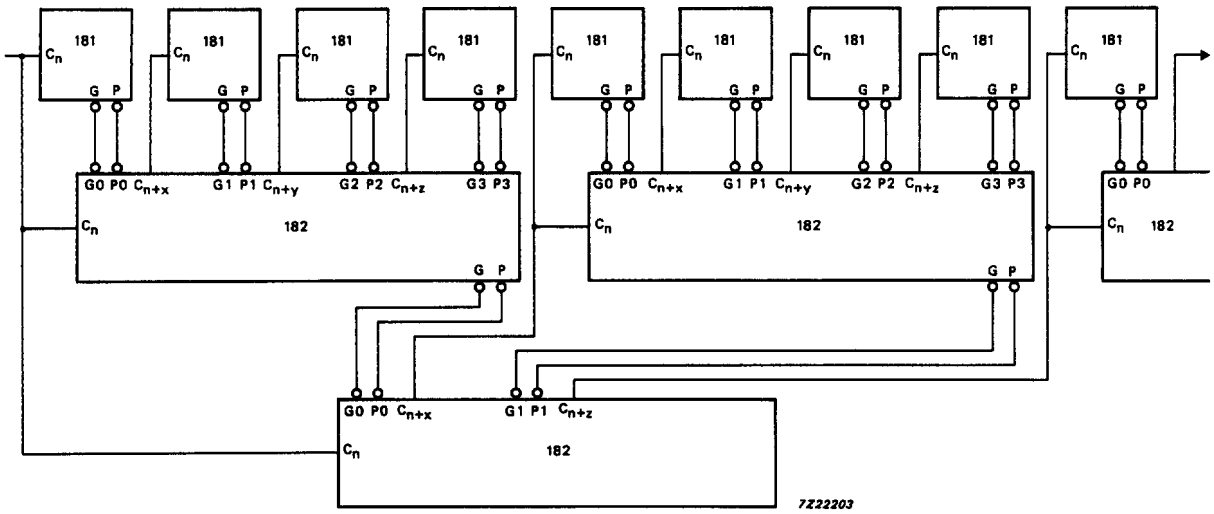
A and B inputs and F outputs of “181” are not shown.

Fig.8 32-bit ALU two-level look-ahead over 16-bit groups.



A and B inputs and F outputs of “181” are not shown.

Fig.9 Combined two-level look-ahead and ripple-carry ALU.



A and B inputs and F outputs of “181” are not shown.

Fig.10 64-bit ALU full-carry three-level look-ahead.

PACKAGE OUTLINES

See *“74HC/HCT/HCU/HCMOS Logic Package Outlines”*.