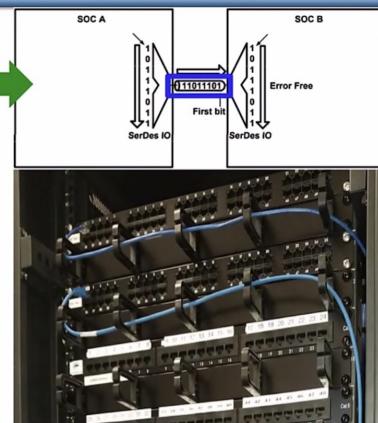
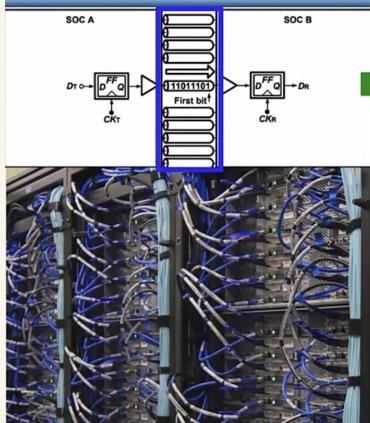


serdes deep dive



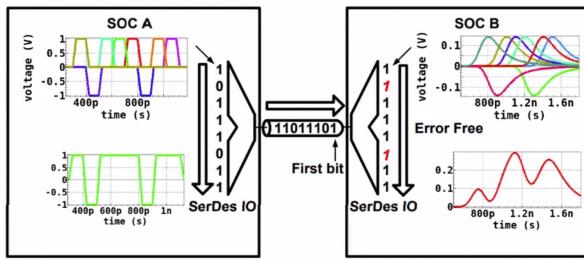
## Summary (I)



如果频率响应 flat, 即没有衰耗和阻抗  
则无需 EQ.

### ISI\* in SerDes (BER)

- Long-reach or low-cost channel  $\rightarrow$  BW  $\downarrow \rightarrow$  ISI  $\uparrow$
- Apply EQ  $\rightarrow$  ISI  $\downarrow \rightarrow$  BER  $\downarrow$  (SERDES link's goal)



单串行线减少了线数，但增加了速度，加剧了 ISI

容抗和感抗的影响使得频率越高，损耗越大  
EQ的作用为频率越高，增益越大，是通道衰减函数的反面

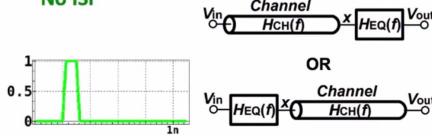
EQ可在TX端做，也可以在RX端做  
实际情况EQ可以改善 ISI，但不能完全消除，经过  
CHANNEL后，信号能量分散，在时域上表现如峰  
值变低，上升沿和下降沿坡度变缓。  
EQ是个抽象概念，实际上实现有三种方式

### How is the Equalization in Time?

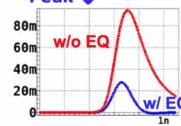


- Pulse response or PRBS bit stream are mainly applied in this talk.
- With the aid of the equalization:

- Sharp Trf
- No ISI



- Pulse shaping
- Reduced ISI
- Peak ↓



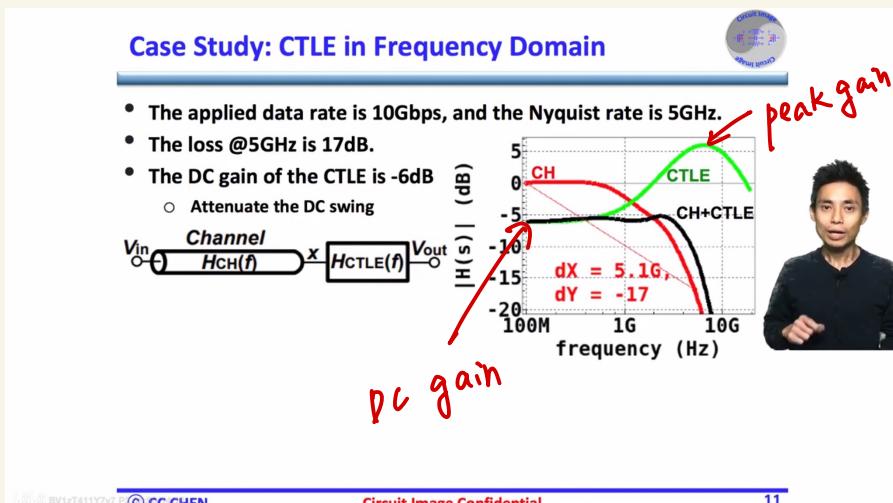
# CTLE - Continuous Time Linear Equalizer

下

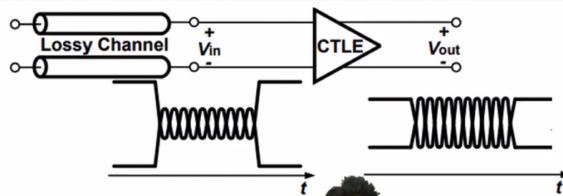
和离散相对. 当无时钟驱动

输出信号与输入信号  
为线性关系

和EQ一样. CTLE 也有高通滤波器



现实中 CTLE 的频率响应会在一定频率后  
增益下降. 在此频率前后增益和通道相合  
后保证不衰减



BV1zT411Y7V7

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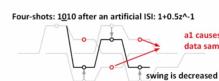
14

在时域里显示为高步频：信号和低频信号保持同一幅值。

### Data Sample with ISI

- Single-shot (pulse):
    - Current bit may create a nonzero value at the next bit's sample point ( $T_{S1}$ )
- Single-shot after an artificial ISI:  $1+0.5z^{-1}$
- 

- Multi-shots (pulses):
  - Due to the ISI, the 1010 or 1101 sequence outputs are  $+0.5, -0.5, +0.5, -0.5$  or  $+3.5, -0.5, +0.5, ..$



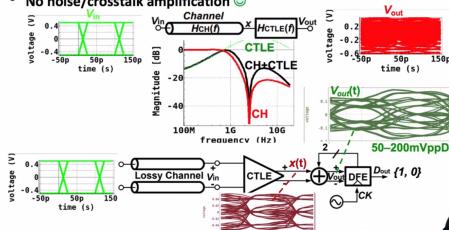
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### Summary

- Can cancel reflection from discontinuities
- No noise/crosstalk amplification



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- DFE
- 非线性, 时钟驱动
  - 依靠电历史变化决定前脉冲对后脉冲信号
  - 半模似半判决逻辑
  - TBP 单位应满足 UI
  - DFE 延时最大 DELAY 不超过 1UI

TX FFE - feed-forward EQ, 通常实现为FIR  
 放在TX的原因是FFE(FIR)由数字域实现, TX受限  
 的有数领域

### How to Implement the TX FFE?

- Simple FIR in digital ☺
- Can cancel pre-cursor and post-cursor ISI ☺

Digital → Analog

$x[n]$ ,  $x[n-1]$ ,  $x[n-2]$

$y(t)$

3-tap FIR

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在时域上FIR表现为发送端高频部分(比如clock pattern)有极高幅值, 经过衰减后和低频部分保持一致幅值

### How to Implement the TX FFE?

- Simple FIR in digital ☺
- Can cancel pre-cursor and post-cursor ISI ☺

Digital → Analog

$x[n]$ ,  $x[n-1]$ ,  $x[n-2]$

$y(t)$

3-tap FIR

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### Summary

- Simplicity: digital delay (flip-flop) is easier than analog delay ☺
- Performance: the degradation of clock feed-through is minimal
- Reduce ISI ☺
  - Can cancel bumping channel ISI ☺
  - Can cancel pre-cursor ISI ☺

Bumpy Response

Both LF/HF dynamic range are minimized

Both LF/HF signal swing are equalized

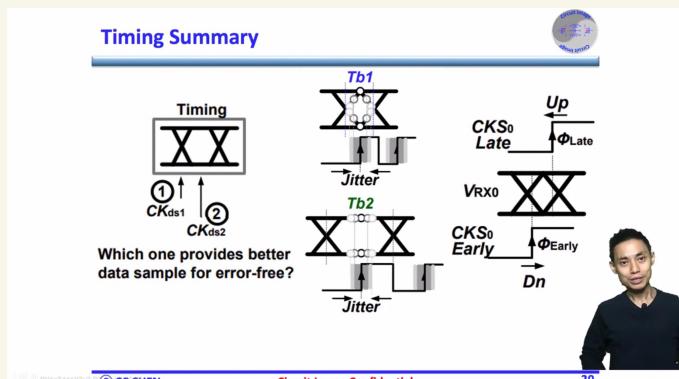
FFE:  $[C_0, C_1, C_2] = [-0.113, 0.615, -0.28]$

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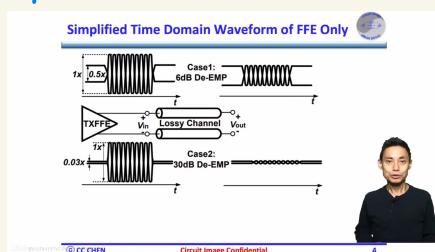
CTLE不能处理由噪声引起的bumpy, 即加大动态范围

信号的同时放大了高频噪声，DFE解决了高频噪声问题（如阻抗不连续造成反射，串扰等）

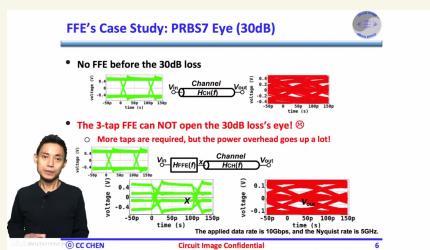
PLL 的作用是提供稳定时钟并作 ADC, DAC.  
同时现实世界中 PLL 时钟与抖动使得信号出现 jitter

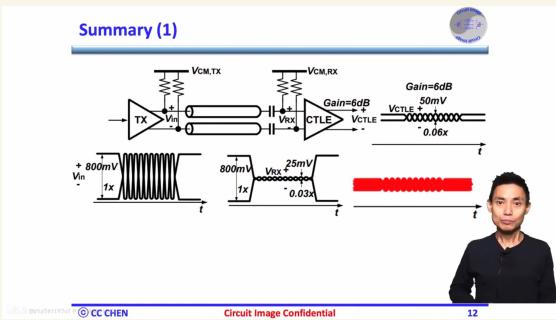


另外差分信号的好处不再讨论。

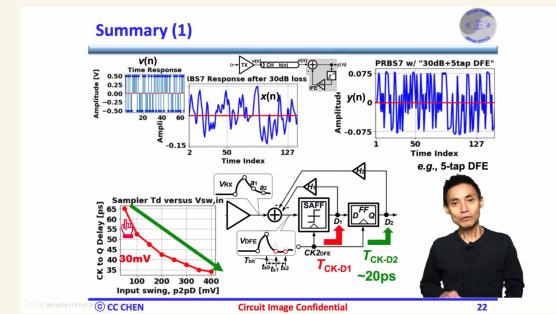


← 只有 TXFFE 时无法  
处理高损耗情况，  
所有信号幅值低





只用CTLE，当衰减较大时高步进信号幅值低



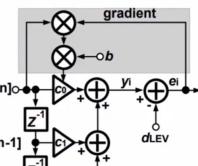
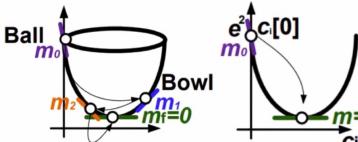
只用DFE，较大的衰减导致判决一个UI会使得产生 burst error，可以通过增加TAP解决

## Update of the Coefficients ( $C_i$ )



- $y_i \sim d_{LEV} \rightarrow \text{minimize the error:}$   
 $e = (y_i - d_{LEV})$
- LMS (Least mean squares):  $(y_i - d_{LEV})^2 = e^2$

$$c_i[n+1] = c_i[n] - b * e * x[n-i]$$



S. Haykin, *Adaptive Filter Theory*, Fourth Edition, Prentice Hall, 2001.

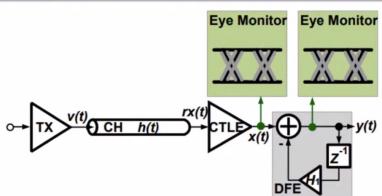
8

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eye monitor 是另外一种的自适应滤波方法，通常  
设置于 DFE 中靠模拟实现部分

## Internal Built-in Eye Monitor



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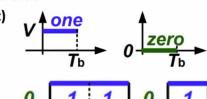
4

## What's the NRZ (Non-Return-To-Zero) Data?



- Non-return-to-zero (NRZ):
  - Pulse amplitude modulation 2 (PAM-2)
  - 1 bit/symbol
  - 2 voltage levels

- Symbol (Bit)



- Bit stream



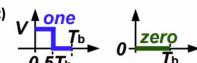
2

## What's the RZ (Return-To-Zero) Data?

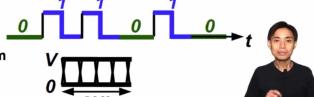


- Return-to-zero (RZ):
  - Pulse amplitude modulation 2 (PAM-2)
  - 1 bit/symbol
  - 2 voltage levels, but ...

- Symbol (Bit)



- Bit stream



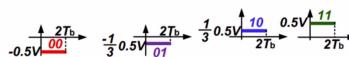
3

## Pulse Amplitude Modulation 4 (PAM4)

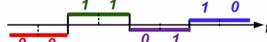


- PAM4
  - 2 bit/symbol
  - 4 voltage levels

- Symbol



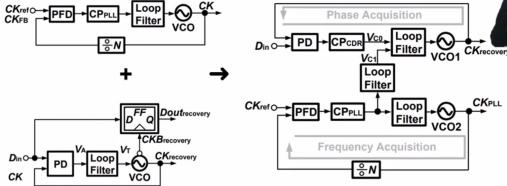
- Bit stream



7

} → 常用編碼方式

## PLL + CDR = PLL-based CDR



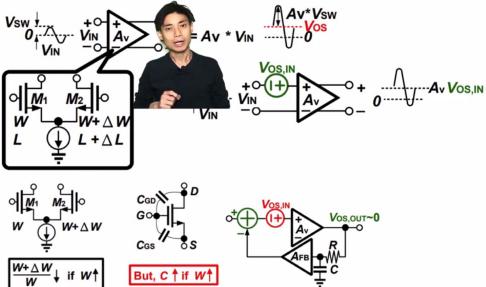
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在 sample 前需要锁住时钟 (实际也指锁住相位), 靠的是本地 PLL 及外部基准 CDR

## Summary



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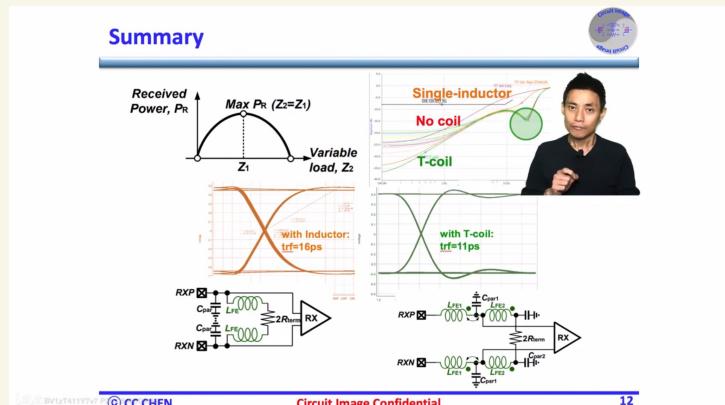
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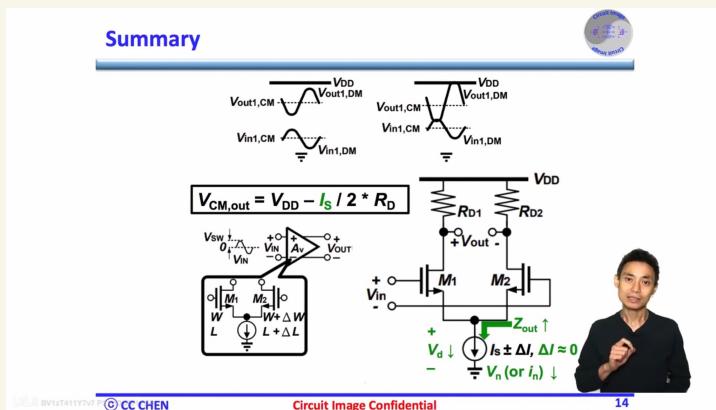
直流分量会缩小某一路：余量，简单来说  
加电容消除

隨機噪聲 - 高斯, DC. mosfet, pn

決定型噪聲 - 反射,串擾, 地氈



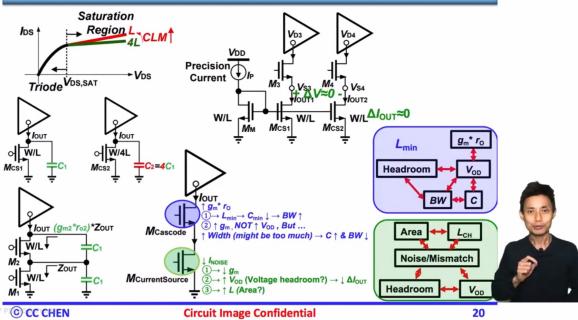
T-coils 是減少  
回波損耗之 T  
方案



電流源 + 差分由  
壓縮出保證  $I_S$  稳定  
信號增益與源  
噪音影響

进一步共源共栅电  
源设计由于稳定性  
和线性带宽应用。

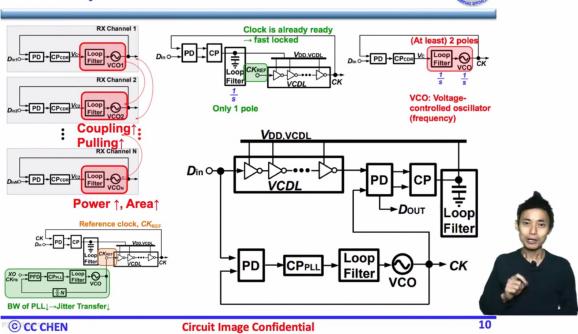
## Summary



DLL - 使用 VCDL 调整 delay 捕获高精度同相时钟  
PLL - 使用 VCO 调整振荡频率进行分频占空比调整

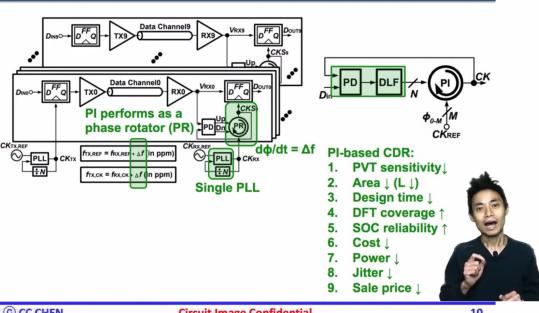
DLL 相对 PLL 有更高的  
精度 (通过调整 delay)  
但分频功能严重不足  
将 PLL 和 DLL 结合  
做 CDR

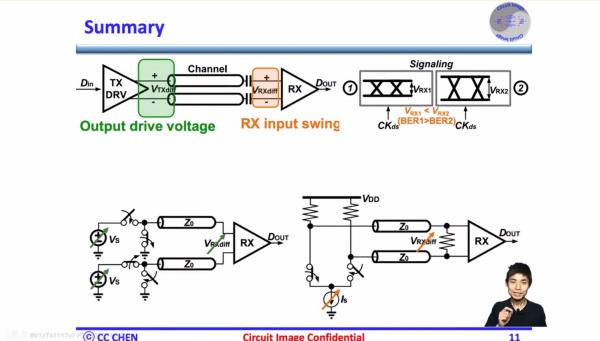
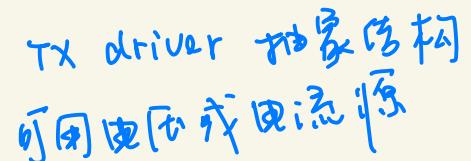
## Summary



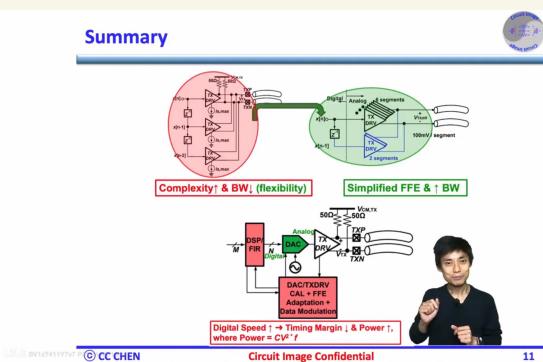
PI 是数字逻辑，通过  
离散的相位匹配来锁  
定时钟  
vco 向 PI (即 PR)，提  
供相位，解决了 PI 自离  
散相位问题，可提高  
CDR 的性能

## Summary





纯模拟 TX 相叶带 DAC  
与 TX 更有鬼  
DAC 的好处是可以产生各种  
编码：NRZ, PAM4



※ 有兩種中類型在 Loopback

1. 只經過 DFE 的 Digital Loopback.
2. 經過 FFE, CTE, DFE 的 ATE Loopback

此時已經知道

3. 經過 FFE 不經過 CTE 是  
在此處問題是 Loopback 下應該  
子端條件為甚麼應該是固定  
的

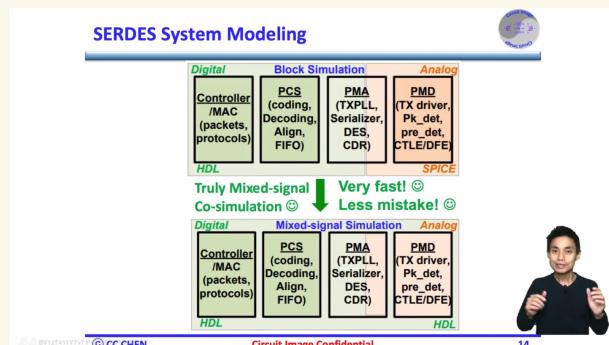
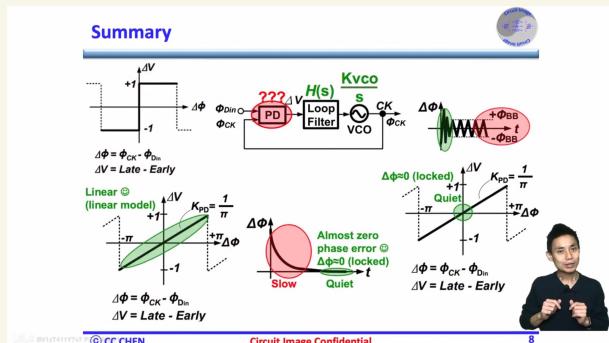
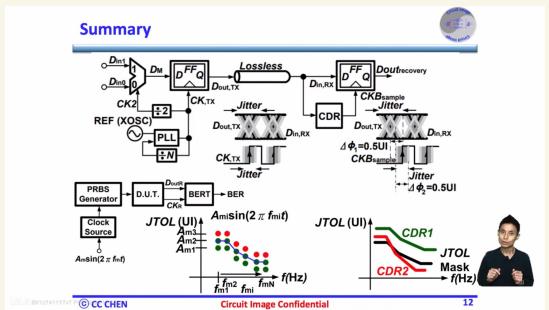
JTOL 是测试 CDR 在不同频率 jitter 的 tolerance

PLL - 部分

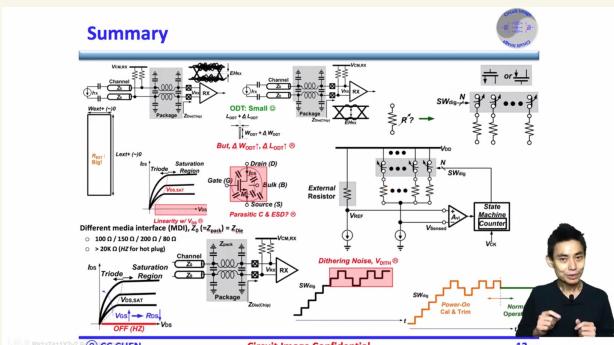
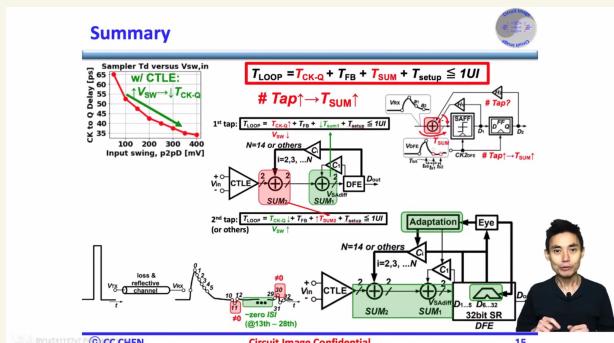
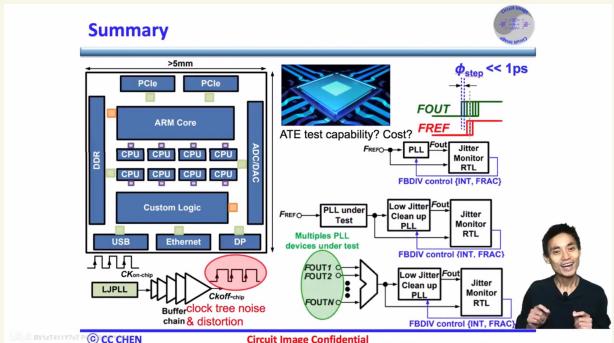
非线性鉴相器 (数字)  
由于输出状态单一 (只有 0 和 1)，所以更细和调整，所以要用波特 PD 检

serdes 在系统中的分类

1. PLL 串并转换，CDR 属于 PMA 中一部分。另外一部分是差空逻辑并中
2. CTLE / DFE 在 PMD 中

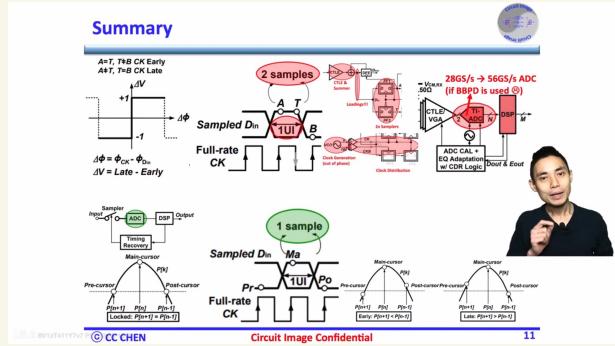


測試芯片時鐘 jitter  
在某內部實現的邏輯由  
何 jitter monitor  
<注：不是通用功能>

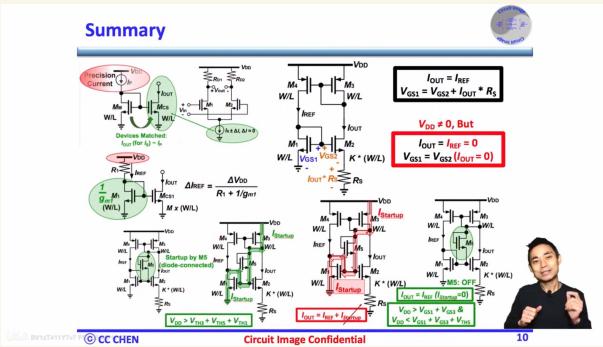


DAUL-sum DFE 解決  
多 TAP F timing 亂問題

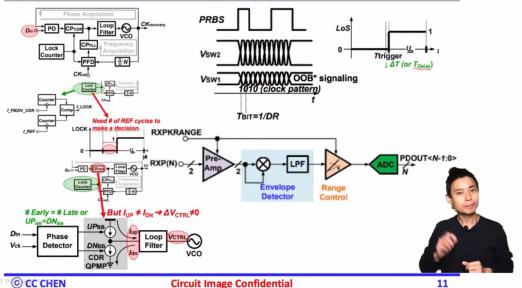
串行端接是保持阻  
抗連續之避免反射的  
常用方式  
on-chip 端接相比  
外接在反射上更優  
是什麼



BB - Bang - Bang  
MM - multiter - multiter



## Summary



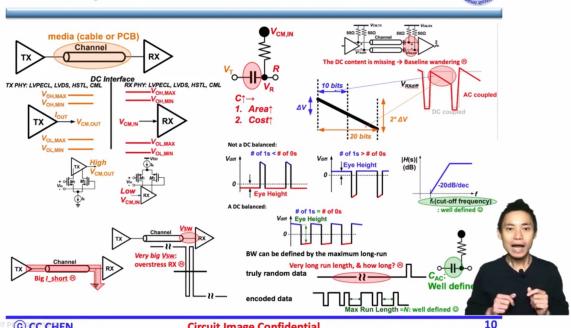
CDR一般有两种工作模式

1. 相位获取. 此时 CDR 尝试解析信号相位. 在无信号时处于此模式

2. 频率获取. 此时 CDR 解析信号上下沿得出频率并控制 VCO 及后续数字逻辑, 为正常工作模式

为了使 CDR 在无信号时  
(此时只有噪声信号)  
切模式1而不失模式2  
对后续模式造成影响  
便用 peak detector 检测  
信号并控制 CDR

## Summary

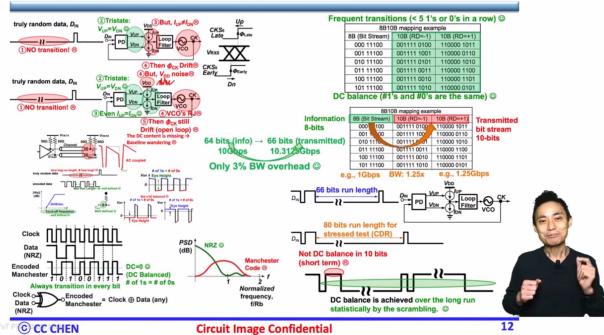


各器件工作电压范围不一致, 所以不能用 DC 耦合信号(即带直流分量)则使用 AC 耦合, 通过加电容, 然后为了防止 DC wandering <长>长, 导致电压无摆幅>所以要编码

# 对子编码

## 1. 曼彻斯特每个bit都有边沿,所以无DC balance,但是BW提高,不适合高速串通信

### Summary



## 2. 8B/10B 缩长5↑

今0合1，并且DC balance，但有25% power/design overhead, 不适用IGW上

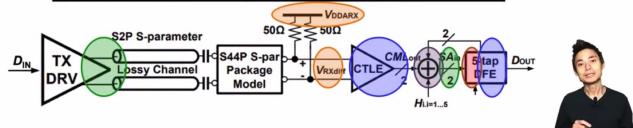
## 3. 64/66, 128/130, 128/132

用于高速场景，扰码在位计上对于long run保持DC balance.

## Summary



Voltage Parameter	Unit	EH,p2pD (mV)	Comments
Residual ISI (w/ CTLE+DFE)	mV	190	TX=800mVp2pD
N (# of sigma) at BER=1e-12	N/A	14	
RMS noise	mV	5	
P2P RMS noise	mV	70	
Residual DC offset	mV	10	
Reflection/Xtalk/Supply Noise	mV	10	
Sampler sensitivity	mV	40	
Voltage Margin	mV	60	



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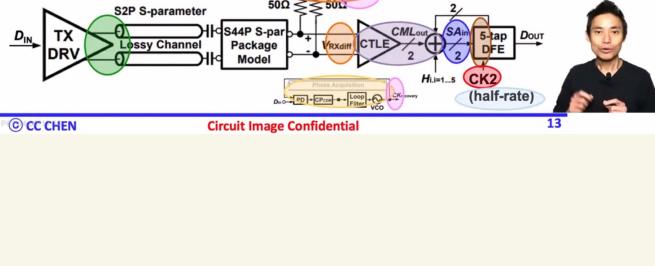
影响眼高  
主要参数  
当量增益

影响眼宽的  
主要参数  
抖动

## Summary



Timing Parameter	Units	Jitter,p2p	Comment
TX Total Output Jitter	%UI	30	Most standards
Residual ISI DJ (w/ CTLE & DFE)	%UI	12	
RJ of RX Data Path (BER=1e-12)	%UI	1	HPF at CDR BW
DJ of Reflection/Xtalk/Supply Noise	%UI	3	HPF at CDR BW
Sampler sensitivity (setup/hold time)	%UI	10	
RJ of sampling clock (BER=1e-12)	%UI	3.0	HPF at CDR BW
CDR's DJ Hunting Jitter	%UI	10	
Supply noise jitter of DFE clock	%UI	2	HPF at CDR BW
Phase error of 1/2-rate clock	%UI	2	
Total jitter	%UI	73	
Timing Margin	%UI	27	



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