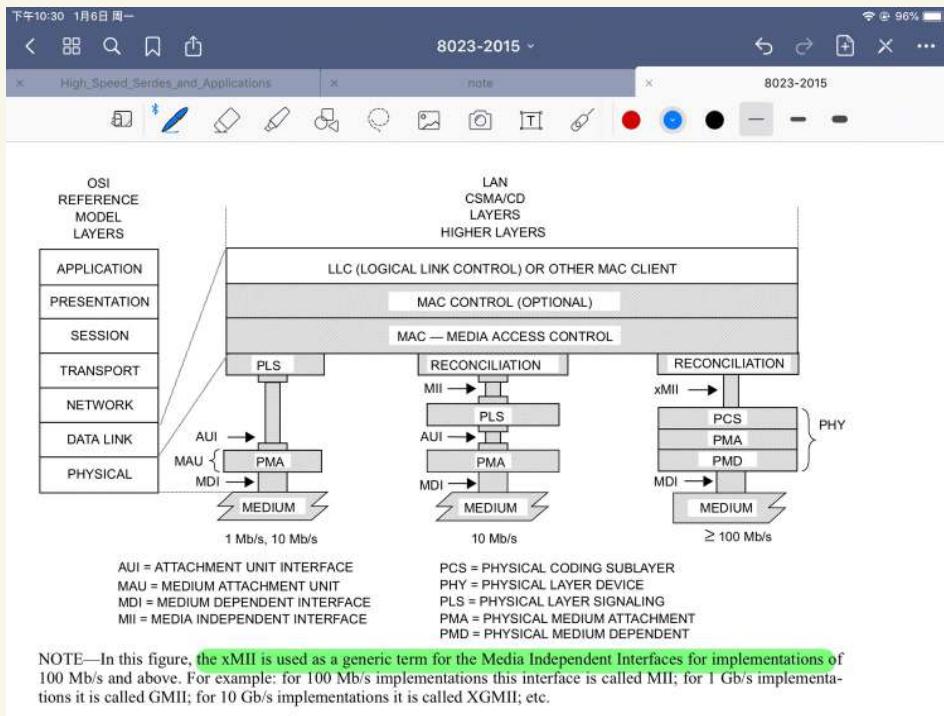






IEEE  
NOTE



Preamble (7 bytes)	SFD (1)	Destination Address (6 bytes)	Source Address (6 bytes)	Length (2)	Data (Up to 1500 bytes)	FCS (4 bytes)
-----------------------	------------	----------------------------------	-----------------------------	---------------	----------------------------	------------------

**Preamble:** Idles which set timing.

**Start Frame Delimiter (SFD):** ‘AB’ indicating start of frame.

**Destination Address:** Six byte unique MAC address of recipient device.

**Source Address:** Six byte unique MAC address of sending device.

**Length:** Two bytes indicating length of data field.

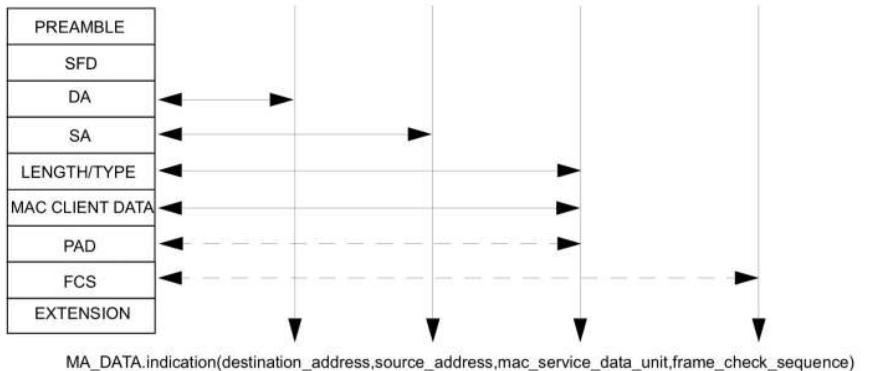
**Data:** Layer 2 Payload Data field. Generally contains a Logical Link Control (LLC) header and between 46 and 1500 bytes of payload data.

**Data is padded if shorter than 46 bytes.**

**Frame Check Sequence (FCS):** Cyclic Redundancy Check (CRC) remainder for error detection.

**Fig. 5.15 IEEE 802.3 ethernet frame**

MA\_DATA.request(destination\_address,source\_address,mac\_service\_data\_unit,frame\_check\_sequence)

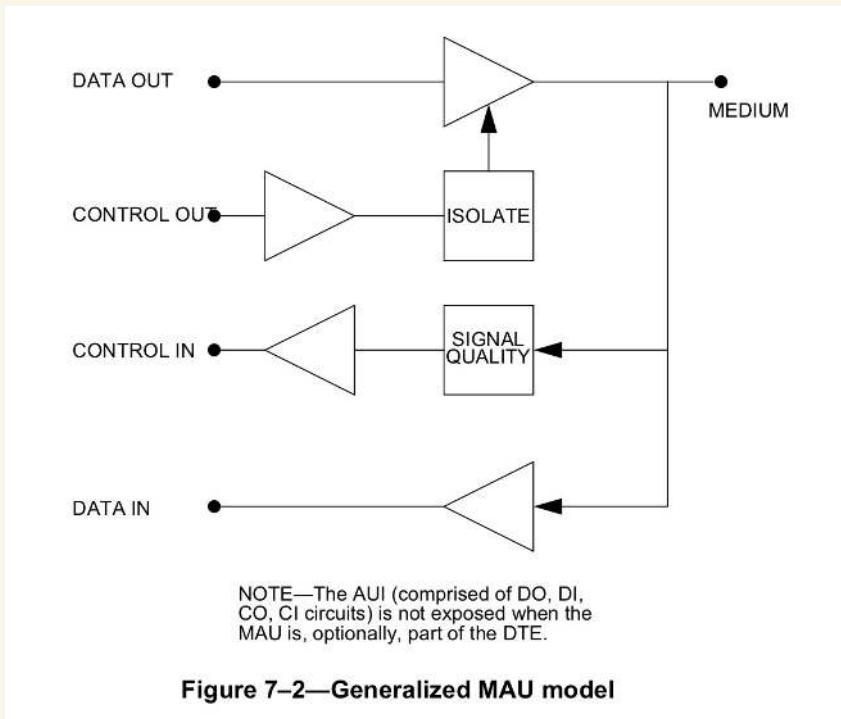


**Figure 3–2—Service primitive mappings**

**Table 4–2—MAC parameters**

Parameters	MAC data rate			
	Up to and including 100 Mb/s	1 Gb/s	10 Gb/s	40 Gb/s and 100 Gb/s
slotTime	512 bit times	4096 bit times	not applicable	not applicable
interPacketGap <sup>a</sup>	96 bits	96 bits	96 bits	96 bits
attemptLimit	16	16	not applicable	not applicable
backoffLimit	10	10	not applicable	not applicable
jamSize	32 bits	32 bits	not applicable	not applicable
maxBasicFrameSize	1518 octets	1518 octets	1518 octets	1518 octets
maxEnvelopeFrameSize	2000 octets	2000 octets	2000 octets	2000 octets
minFrameSize	512 bits (64 octets)	512 bits (64 octets)	512 bits (64 octets)	512 bits (64 octets)
burstLimit	not applicable	65 536 bits	not applicable	not applicable
ipgStretchRatio	not applicable	not applicable	104 bits	not applicable

<sup>a</sup>References to interFrameGap or interFrameSpacing in other clauses (e.g., 13, 35, and 42) shall be interpreted as inter-PacketGap.



**Figure 7–2—Generalized MAU model**

Circuit	Name	Signal direction		Remarks
		to MAU	from MAU	
DO	Data Out	X		Encoded Data
DI	Data In		X	Encoded Data
CO	Control Out	X		Encoded Control
CI	Control In		X	Encoded Control
VP	Voltage Plus	X		12 V
VC	Voltage Common	X		Return for VP
PG	Protective Ground	X		Shield

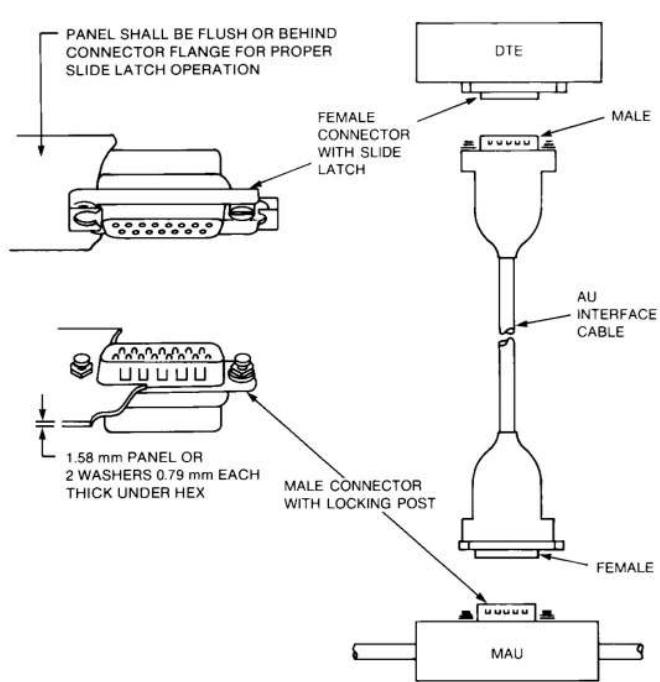


Figure 7–20—Connector hardware and AUI cable configuration

#### 8.2.2.1 DTE Physical Layer to MAU Physical Layer messages

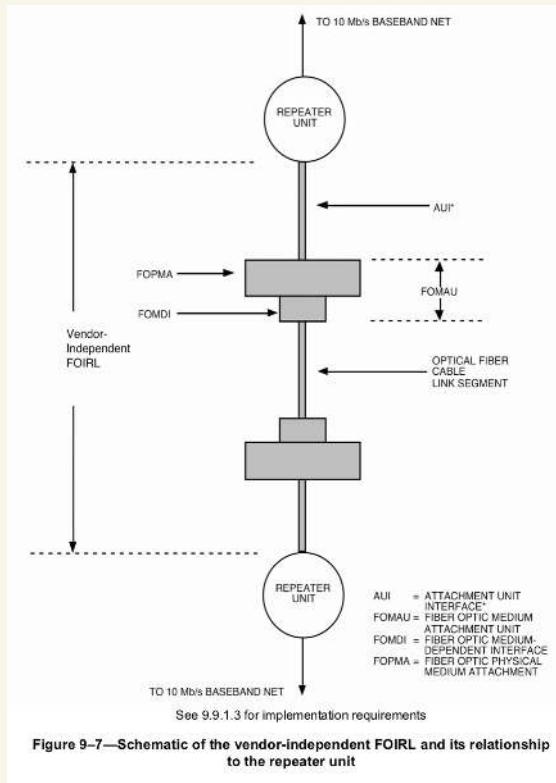
The following messages can be sent by the DTE Physical Layer entities to the MAU Physical Layer entities:

Message	Circuit	Signal	Meaning
<i>output</i>	DO	CD1, CD0	Output information
<i>output_idle</i>	DO	IDL	No data to be output
<i>normal</i>	CO	IDL	Assume the nonintrusive state on the trunk coaxial medium
(Optional circuit)			
<i>isolate</i>	CO	CS0(BR)	Positively disable the trunk coaxial medium transmitter

### 8.2.2.2 MAU Physical Layer to DTE Physical Layer

The following messages can be sent by the MAU Physical Layer entities to the DTE Physical Layer entities:

Message	Circuit	Signal	Meaning
<i>input</i>	DI	CD1, CD0	Input information
<i>input_idle</i>	DI	IDL	No information to be input
<i>mau_available</i>	CI	IDL	MAU is available for output
<i>signal_quality_error</i>	CI	CS0	Error detected by MAU



### 9.9.2.6 Repeater Unit to FOMAU Physical Layer messages

The following messages can be received by the FOMAU Physical Layer entities from the repeater unit:

Message	Circuit	Signal	Meaning
output	DO	CD1, CTX0	Output information
output_idle	DO	IDL	No data to be output

### 9.9.2.7 FOMAU Physical Layer to repeater unit messages

The following messages can be sent by the FOMAU Physical Layer entities to the repeater unit:

Message	Circuit	Signal	Meaning
input	DI	CD1, CD0	Input information
input_idle	DI	IDL	No information to be input
fomau_available	CI	IDL	FOMAU is available for output
signal_quality_error	CI	CS0	Collision or error detected by FOMAU

## 10. Medium attachment unit and baseband medium specifications, type 10BASE2

NOTE—This MAU is not recommended for new installations. Since September 2011, maintenance changes are no longer being considered for this clause.

### 10.1 Scope

#### 10.1.1 Overview

This standard defines the functional, electrical, and mechanical characteristics of the Medium Attachment Unit (MAU) and one specific medium for use with LANs. The relationship of this specification to the OSI Reference Model is shown in Figure 10–1.

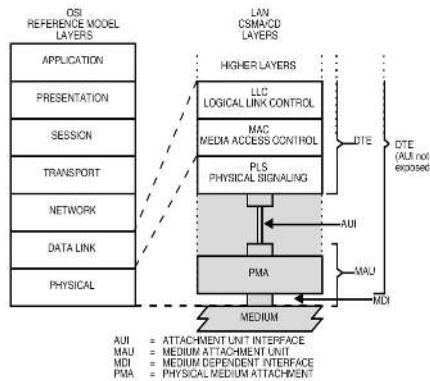
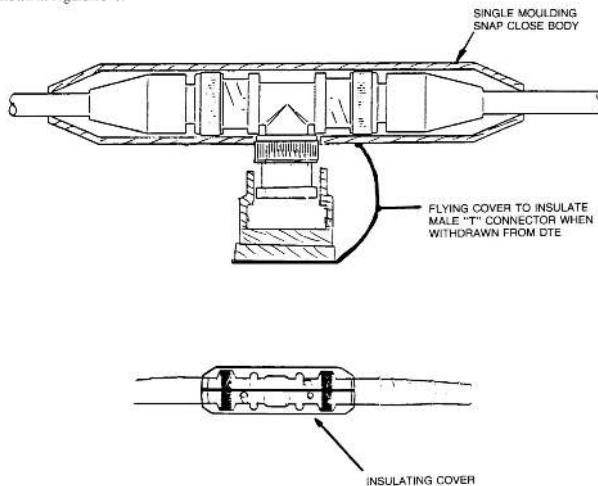


Figure 10–1—Physical Layer partitioning, relationship to the ISO/IEC Open Systems Interconnection (OSI) reference model

The trunk coaxial medium requires termination and is partitioned into sections. Devices to be attached to the medium require a means of connection to the medium. This means is provided by a BNC "T" adapter, as shown in Figure 10-7.



(Tutorial only and not part of the standard.)

Figure 10-7—Examples of insulated connector cover

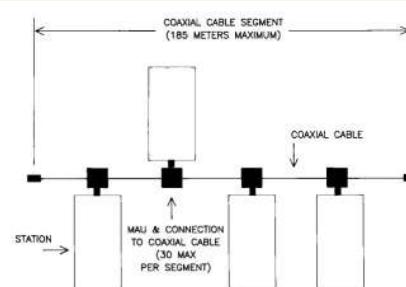


Figure 10-8—The minimum system configuration

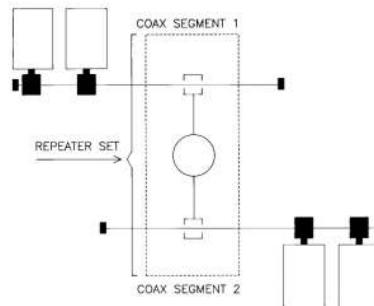


Figure 10-9—The minimum system configuration requiring a repeater set

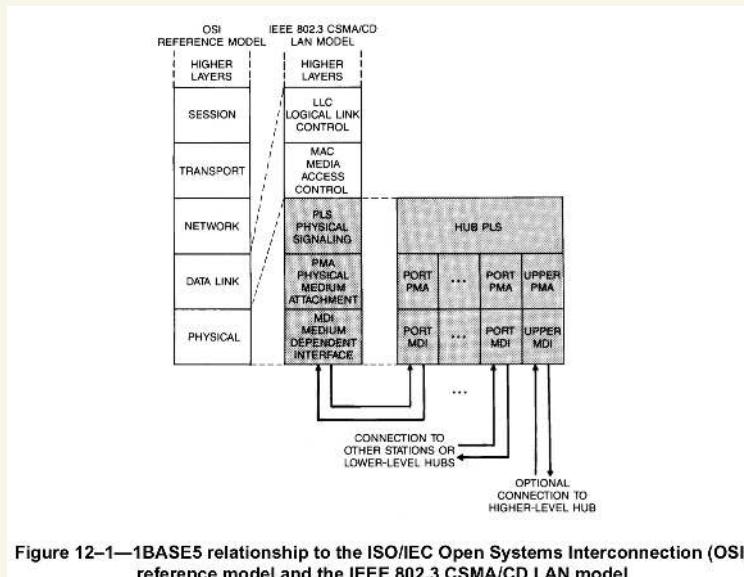


Figure 12-1—1BASE5 relationship to the ISO/IEC Open Systems Interconnection (OSI) reference model and the IEEE 802.3 CSMA/CD LAN model

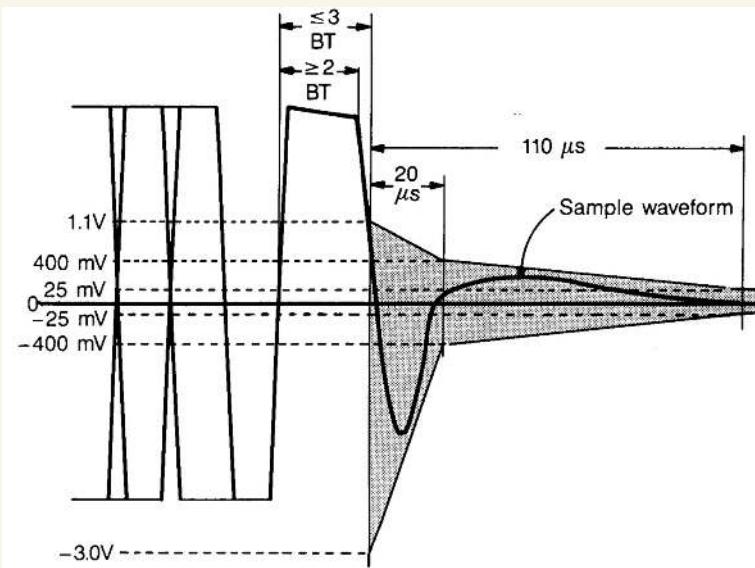


Figure 12-21—Transmitter waveform for idle

Contact	Signal
1	Upward Data+ (positive for HI signal)
2	Upward Data- (negative for HI signal)
3	Downward Data+ (positive for HI signal)
4	not used by IEEE802.3
5	not used by IEEE802.3
6	Downward Data- (negative for HI signal)
7	reserved
8	reserved

For DTEs and the upper MDI of hubs, contacts 1 and 2 are used for transmitting and contacts 3 and 6 are used for receiving. For the port MDIs of hubs, however, contacts 1 and 2 are used for receiving and contacts 3 and 6 are used for transmitting.

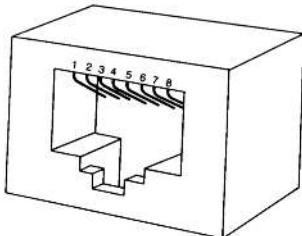


Figure 12-30—DTE and hub connector

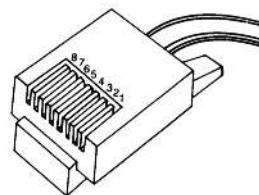
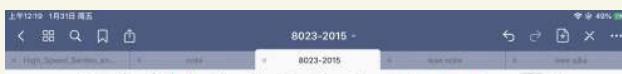


Figure 12-31—Cable connector

如果在物理层上实现了 AUI 那么就必须遵守,  
AUI 层是 10BASE-T 内部的 MAU, AUI 是连接的  
那个部分 / 全双工



Jabber function. If these optional capabilities are implemented in a MAU connected to a full duplex mode DTE, either all of the optional functions shall be implemented, or none of them shall be.

The MAU function requirements are summarized in the table below:

不是全双工支持

MAU connected to:			
Functions	Repeater	Half duplex DTE	Full duplex DTE
Transmit	Required	Required	Required
Receive	Required	Required	Required
Loopback	Required	Required	Required
Jabber	Required	Required	Required
Link Integrity Test	Required	Required	Required
Collision Presence	Required	Required	Optional (Note 2)
SQE Test	Required	Required	Optional (Note 2)
Generation of CS0 signal on the CI circuit by jabber	Required	Required	Optional (Note 2)

NOTE 1—The functional requirements of a MAU connected to a full duplex DTE are a proper subset of the requirements for half duplex operation.

NOTE 2—Optional capabilities, if implemented, must be implemented as a group (i.e., all or none).

#### 14.2.2.1 PLS to PMA messages

The following messages are sent by the PLS in the DTE or repeater to the PMA in the MAU:

Message	Circuit	Signal	Meaning
output	DO	CD1,CD0	Output information
output_idle	DO	IDL	No data to be output

#### 14.2.2.1.1 PMA to PLS messages

The following messages are sent by the MAU to the PLS in the DTE or repeater:

Message	Circuit	Signal	Meaning
input	DI	CD1,CD0	Input information
input_idle	DI	IDL	No information to input
mau_available	CI	IDL	MAU is available for output
signal_quality_error	CI	CS0	Error detected by MAU

Retiming of CD1 and CD0 signals within the MAU is neither prohibited nor required. Considerable jitter may be present (see 14.3.1.3.1).

#### 14.2.2.2 PMA to twisted-pair link segment messages

Message	Circuit	Signal	Meaning
TD_output	ID	CD1,CD0	Output information
TD_idle	ID	TP_IDL	No information to output

The encoding for TP\_IDL is defined in 14.2.1.1. The encoding for CD1 and CD0 is the same as that used on the AUI. Retiming of CD1 and CD0 signals within the MAU is neither prohibited nor required.

#### 14.2.2.3 Twisted-pair link segment to PMA messages

Message	Circuit	Signal	Meaning
RD_input	RD	CD1,CD0	Input information
RD_idle	RD	TP_IDL	No information to input

The encoding for TP\_IDL is defined in 14.2.1.1. The encoding for CD1 and CD0 is the same as that used on the AUI.

Contact	MDI signal
1	TD+
2	TD-
3	RD+
4	Not used by 10BASE-T
5	Not used by 10BASE-T
6	RD-
7	Not used by 10BASE-T
8	Not used by 10BASE-T

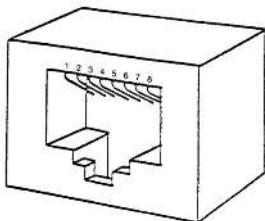


Figure 14–21—MAU MDI connect

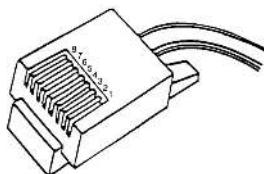


Figure 14–22—Twisted-pair link segment connector

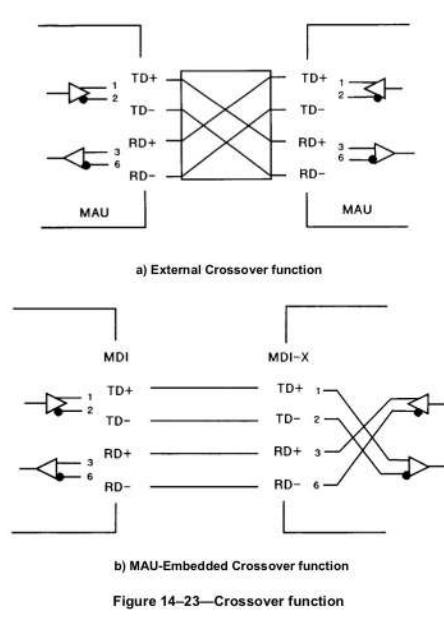


Figure 14-23—Crossover function

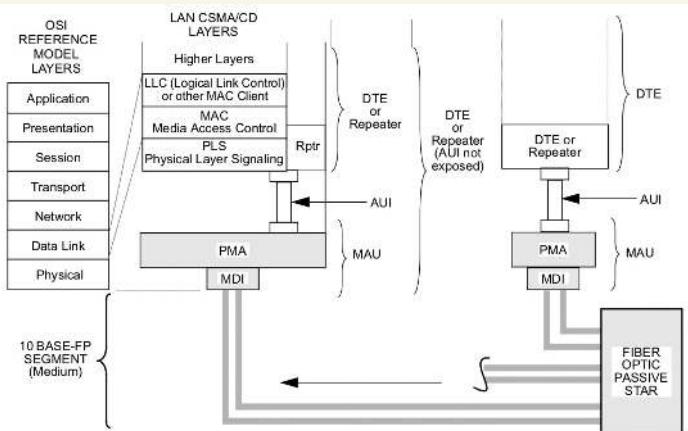
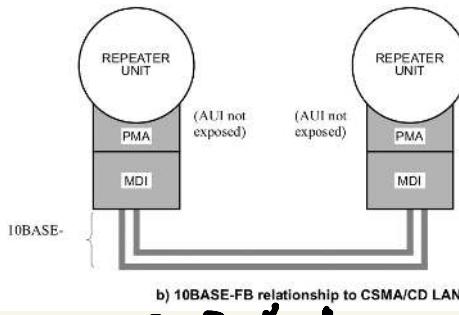


Figure 15-1—10BASE-F relationship to the ISO/IEC Open Systems Interconnection (OSI) reference model and the IEEE 802.3 CSMA/CD LAN model



10BASE-F<sub>FB</sub>关系

光纤的IDLE信号比光功率大于57dBm

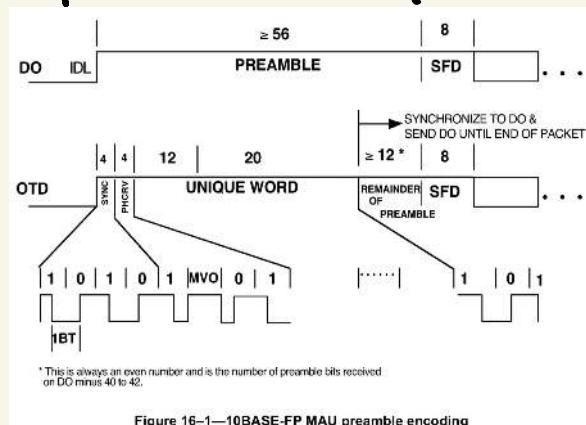
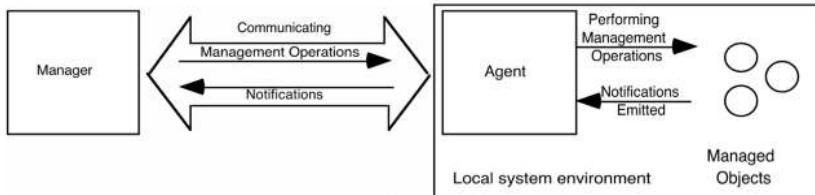


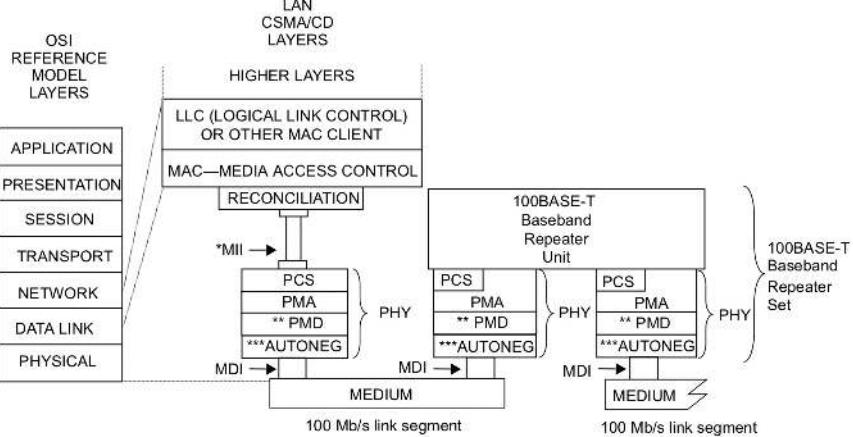
Figure 16-1—10BASE-FP MAU preamble encoding

$pls \rightarrow pma \rightarrow mdi$  时前导码会重新封装。  
反之收到报文时也一样。



NOTE—Figure 1 of ISO/IEC 10040 has been reproduced with the permission of ISO. Copies of the complete standard may be obtained from the International Organization for Standardization, Case Postale 56, 1 rue de Varembé, CH-1211, Genève 20, Switzerland/Suisse.

Figure 19-1—Interaction between manager, agent, and objects



MDI = MEDIUM DEPENDENT INTERFACE  
MII = MEDIA INDEPENDENT INTERFACE

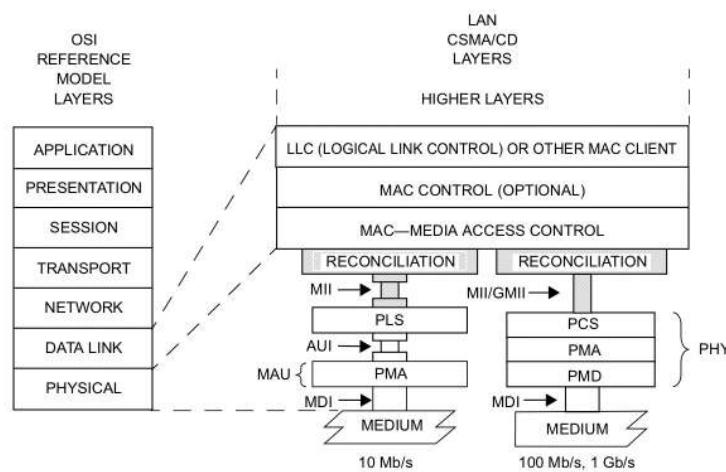
PCS = PHYSICAL CODING SUBLAYER  
PMA = PHYSICAL MEDIUM ATTACHMENT  
PHY = PHYSICAL LAYER DEVICE  
PMD = PHYSICAL MEDIUM DEPENDENT

\* MII is optional for 10 Mb/s DTEs and for 100 Mb/s systems and is not specified for 1 Mb/s systems.

\*\* PMD is specified for 100BASE-X only; 100BASE-T4 does not use this layer.  
Use of MII between PCS and Baseband Repeater Unit is optional.

\*\*\* AUTONEG is optional.

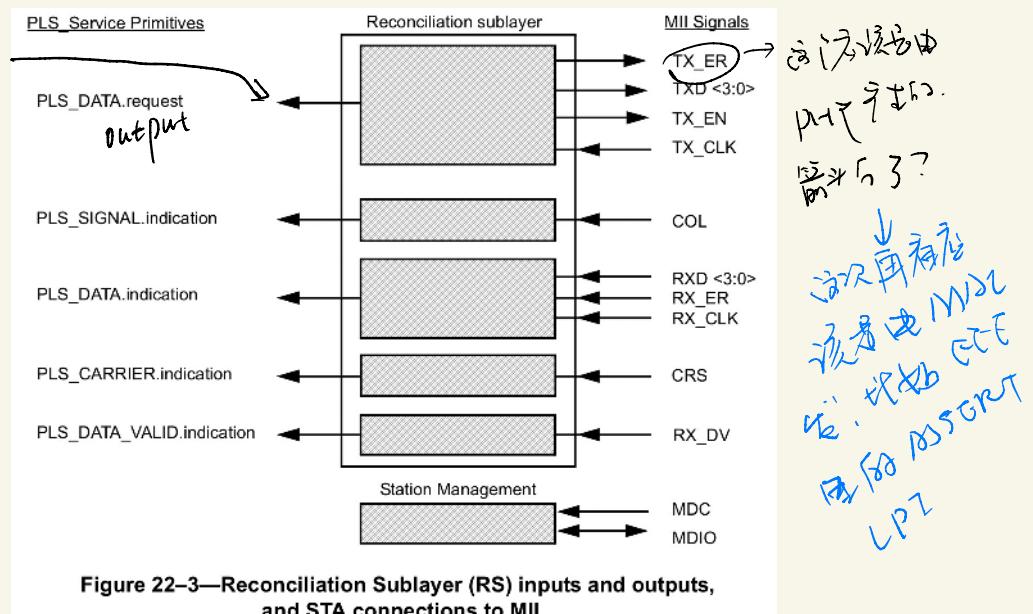
Figure 21-1—Architectural positioning of 100BASE-T



AUI = ATTACHMENT UNIT INTERFACE  
GMII = GIGABIT MEDIA INDEPENDENT INTERFACE  
MAU = MEDIUM ATTACHMENT UNIT  
MDI = MEDIUM DEPENDENT INTERFACE  
MII = MEDIA INDEPENDENT INTERFACE

PCS = PHYSICAL CODING SUBLAYER  
PHY = PHYSICAL LAYER DEVICE  
PLS = PHYSICAL LAYER SIGNALING  
PMA = PHYSICAL MEDIUM ATTACHMENT  
PMD = PHYSICAL MEDIUM DEPENDENT

Figure 22-1—MII relationship to the ISO/IEC Open Systems Interconnection (OSI) reference model and the IEEE 802.3 CSMA/CD LAN model



nibble - 4 bits

Table 22-1—Permissible encodings of TXD<3:0>, TX\_EN, and TX\_ER

<b>TX_EN</b>	<b>TX_ER</b>	<b>TXD&lt;3:0&gt;</b>	<b>Indication</b>
0	0	0000 through 1111	Normal inter-frame
0	1	0000	Reserved
0	1	0001	Assert LPI
0	1	0010 through 1111	Reserved
1	0	0000 through 1111	Normal data transmission
1	1	0000 through 1111	Transmit error propagation

Table 22–2—Permissible encoding of RXD<3:0>, RX ER, and RX DV

<b>RX_DV</b>	<b>RX_ER</b>	<b>RXD&lt;3:0&gt;</b>	<b>Indication</b>
0	0	0000 through 1111	Normal inter-frame
0	1	0000	Normal inter-frame
0	1	0001	Assert LPI
0	1	0010 through 1101	Reserved
0	1	1110	False Carrier indication
0	1	1111	Reserved
1	0	0000 through 1111	Normal data reception
1	1	0000 through 1111	Data reception with errors

在半双工模式下，PLS → PMA & MAn 同逻辑上的 AUI 时  
 (写) loopback TX → RX，而在 MAI & RJ → PLS 时  
 MII 时并不需要 loopback

**Table 22–3—Transmitted preamble and SFD**

Signal	Bit values of nibbles transmitted through MII																		
TXD0	X	1 <sup>a</sup>	1	1	1	1	1	1	1	1	1	1	1	1	1	1 <sup>b</sup>	1	D0 <sup>c</sup>	D4 <sup>d</sup>
TXD1	X	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	D1	D5
TXD2	X	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	D2	D6
TXD3	X	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	D3	D7
TX_EN	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

<sup>a</sup>1st preamble nibble transmitted.

<sup>b</sup>1st SFD nibble transmitted.

<sup>c</sup>1st data nibble transmitted.

<sup>d</sup>D0 through D7 are the first eight bits of the data field from the Protocol Data Unit (PDU).

**Table 22–4—Start of receive with no preamble preceding SFD**

Signal	Bit values of nibbles received through MII											
RXD0	X	X	X	X	X	X	X	1 <sup>a</sup>	1	D0 <sup>b</sup>	D4 <sup>c</sup>	
RXD1	X	X	X	X	X	X	X	0	0	D1	D5	
RXD2	X	X	X	X	X	X	X	1	1	D2	D6	
RXD3	X	X	X	X	X	X	X	0	1	D3	D7	
RX_DV	0	0	0	0	0	0	0	1	1	1	1	

<sup>a</sup>1st SFD nibble received.

<sup>b</sup>1st data nibble received.

<sup>c</sup>D0 through D7 are the first eight bits of the data field from the PDU.

Table 22-5—Start of receive with entire preamble preceding SFD

Signal	Bit values of nibbles received through MII																	
RXD0	X	1 <sup>a</sup>	1	1	1	1	1	1	1	1	1	1	1	1	1	1	D0 <sup>c</sup>	D4 <sup>d</sup>
RXD1	X	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	D1	D5
RXD2	X	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	D2	D6
RXD3	X	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	D3	D7
RX_DV	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1		

<sup>a</sup>1st preamble nibble received.

<sup>b</sup>1st SFD nibble received.

<sup>c</sup>1st data nibble received.

<sup>d</sup>D0 through D7 are the first eight bits of the data field from the PDU.

所以从MII接口接收包时不一定有前导码

→ 22节 16bits, 不强制前导

Table 22-6—MII management register set

Register address	Register name	Basic/Extended	
		MII	GMII
0	Control	B	B
1	Status	B	B
2,3	PHY Identifier	E	E
4	Auto-Negotiation Advertisement	E	E
5	Auto-Negotiation Link Partner Base Page Ability	E	E
6	Auto-Negotiation Expansion	E	E
7	Auto-Negotiation Next Page Transmit	E	E
8	Auto-Negotiation Link Partner Received Next Page	E	E
9	MASTER-SLAVE Control Register	E	E
10	MASTER-SLAVE Status Register	E	E
11	PSE Control register	E	E
12	PSE Status register	E	E
13	MMD Access Control Register	E	E
14	MMD Access Address Data Register	E	E
15	Extended Status	Reserved	B
16 through 31	Vendor Specific	E	E

Table 22-7—Control register bit definitions

Bit(s)	Name	Description	R/W <sup>a</sup>
0.15	Reset	1 = PHY reset 0 = normal operation	R/W SC
0.14	Loopback	1 = enable loopback mode 0 = disable loopback mode	R/W
0.13	Speed Selection (LSB)	0.6 0.13 1 1 = Reserved 1 0 = 1000 Mb/s 0 1 = 100 Mb/s 0 0 = 10 Mb/s	R/W
0.12	Auto-Negotiation Enable	1 = enable Auto-Negotiation process 0 = disable Auto-Negotiation process	R/W
0.11	Power Down	1 = power down 0 = normal operation <sup>b</sup>	R/W
0.10	Isolate	1 = electrically Isolate PHY from MII or GMII 0 = normal operation <sup>b</sup>	R/W
0.9	Restart Auto-Negotiation	1 = restart Auto-Negotiation process 0 = normal operation	R/W SC
0.8	Duplex Mode	1 = full duplex 0 = half duplex	R/W
0.7	Collision Test	1 = enable COL signal test 0 = disable COL signal test	R/W
0.6	Speed Selection (MSB)	0.6 0.13 1 1 = Reserved 1 0 = 1000 Mb/s 0 1 = 100 Mb/s 0 0 = 10 Mb/s	R/W
0.5	Unidirectional enable	When bit 0.12 is one or bit 0.8 is zero, this bit is ignored. When bit 0.12 is zero and bit 0.8 is one: 1 = Enable transmit from media independent interface regardless of whether the PHY has determined that a valid link has been established 0 = Enable transmit from media independent interface only when the PHY has determined that a valid link has been established	R/W
0.4:0	Reserved	Write as 0, ignore on read	R/W

<sup>a</sup>R/W = Read/Write, SC = Self-clearing.<sup>b</sup>For normal operation, both 0.10 and 0.11 must be cleared to zero; see 22.2.4.1.5.

NOTE—This operation may interrupt data communication.

Table 22-8—Status register bit definitions

Bit(s)	Name	Description	R/W <sup>a</sup>
1.15	100BASE-T4	1 = PHY able to perform 100BASE-T4 0 = PHY not able to perform 100BASE-T4	RO
1.14	100BASE-X Full Duplex	1 = PHY able to perform full duplex 100BASE-X 0 = PHY not able to perform full duplex 100BASE-X	RO
1.13	100BASE-X Half Duplex	1 = PHY able to perform half duplex 100BASE-X 0 = PHY not able to perform half duplex 100BASE-X	RO
1.12	10 Mb/s Full Duplex	1 = PHY able to operate at 10 Mb/s in full duplex mode 0 = PHY not able to operate at 10 Mb/s in full duplex mode	RO
1.11	10 Mb/s Half Duplex	1 = PHY able to operate at 10 Mb/s in half duplex mode 0 = PHY not able to operate at 10 Mb/s in half duplex mode	RO
1.10	100BASE-T2 Full Duplex	1 = PHY able to perform full duplex 100BASE-T2 0 = PHY not able to perform full duplex 100BASE-T2	RO
1.9	100BASE-T2 Half Duplex	1 = PHY able to perform half duplex 100BASE-T2 0 = PHY not able to perform half duplex 100BASE-T2	RO
1.8	Extended Status	1 = Extended status information in Register 15 0 = No extended status information in Register 15	RO
1.7	Unidirectional ability	1 = PHY able to transmit from media independent interface regardless of whether the PHY has determined that a valid link has been established 0 = PHY able to transmit from media independent interface only when the PHY has determined that a valid link has been established	RO
1.6	MF Preamble Suppression	1 = PHY will accept management frames with preamble suppressed 0 = PHY will not accept management frames with preamble suppressed	RO
1.5	Auto-Negotiation Complete	1 = Auto-Negotiation process completed 0 = Auto-Negotiation process not completed	RO
1.4	Remote Fault	1 = remote fault condition detected 0 = no remote fault condition detected	RO/ LH
1.3	Auto-Negotiation Ability	1 = PHY is able to perform Auto-Negotiation 0 = PHY is not able to perform Auto-Negotiation	RO
1.2	Link Status	1 = link is up 0 = link is down	RO/ LL
1.1	Jabber Detect	1 = jabber condition detected 0 = no jabber condition detected	RO/ LH
1.0	Extended Capability	1 = extended register capabilities 0 = basic register set capabilities only	RO

<sup>a</sup>RO = Read only, LL = Latching low, LH = Latching high

1.14 indicates that the PHY lacks the ability to perform full duplex link transmission and reception using the 100BASE-X signaling specification.

#### 22.2.4.5 Management frame structure

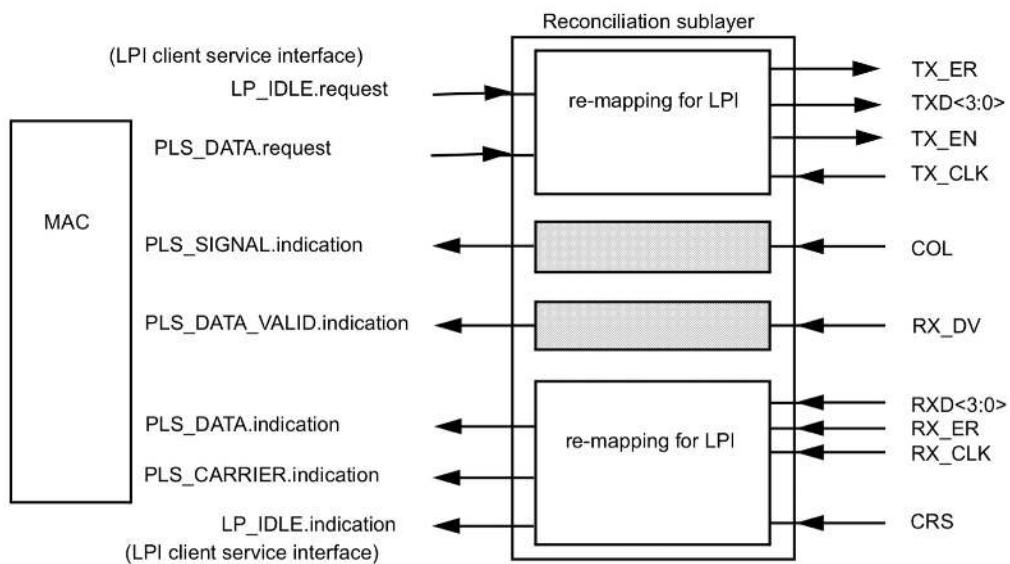
Frames transmitted on the MII Management Interface shall have the frame structure shown in Table 22–12. The order of bit transmission shall be from left to right.

**Table 22–12—Management frame format**

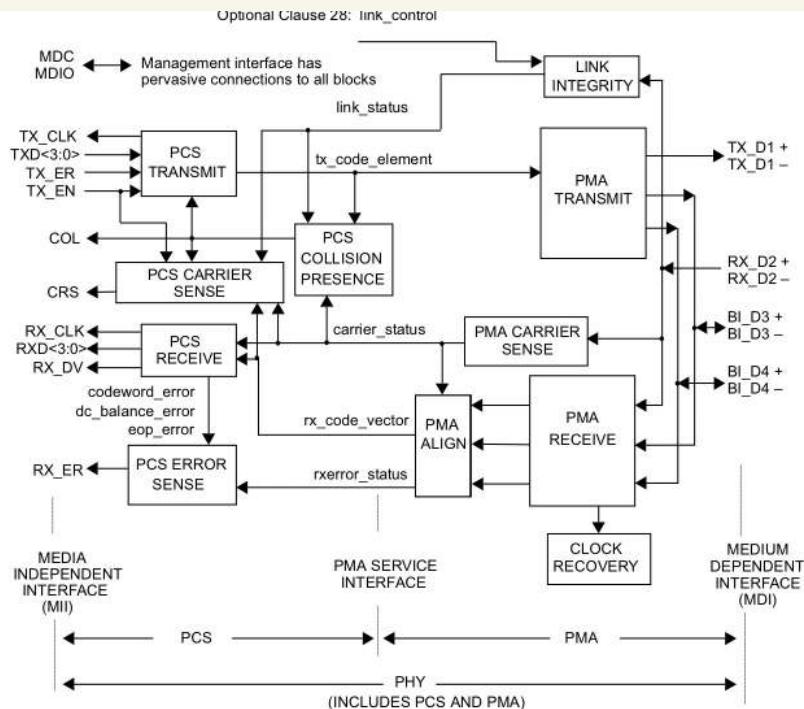
	Management frame fields							
	PRE	ST	OP	PHYAD	REGAD	TA	DATA	IDLE
READ	I...I	01	10	AAAAAA	RRRRR	Z0	DDDDDDDDDDDDDDDDDD	Z
WRITE	I...I	01	01	AAAAAA	RRRRR	10	DDDDDDDDDDDDDDDDDD	Z

PLS\_Service Primitives

MII Signals



**Figure 22–22—LPI assertion and detection mechanism**



TX-D2  
 TX-D1  
 RX-D1  
 没有用

Figure 23–2—Division of responsibilities between 100BASE-T4 PCS and PMA

Table 23–1—MII interface signals

Signal name	Meaning
TX_CLK	Transmit Clock
TXD<3:0>	Transmit Data
TX_ER	Forces transmission of illegal code
TX_EN	Frames Transmit Data
COL	Collision Indication
CRS	Non-Idle Medium Indication
RX_CLK	Receive Clock
RXD<3:0>	Receive Data
RX_DV	Frames Receive SFD and DATA
RX_ER	Receive Error Indication
MDC	Management Data Clock
MDIO	Management Data

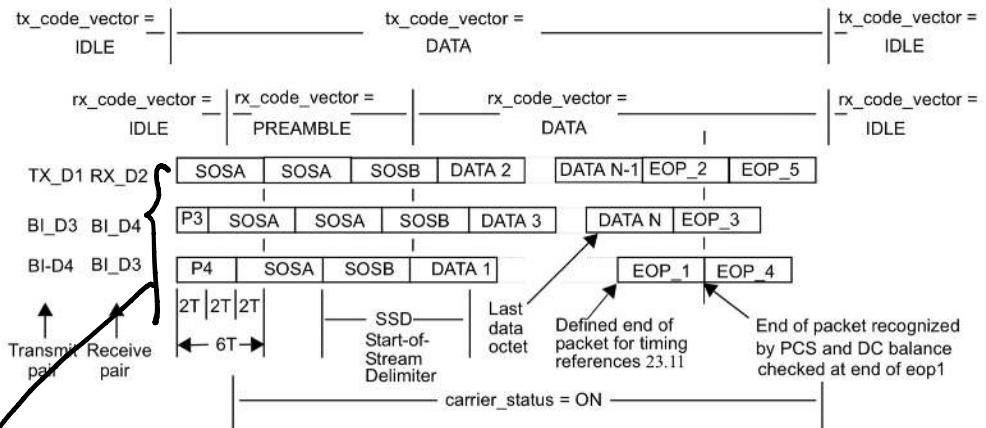
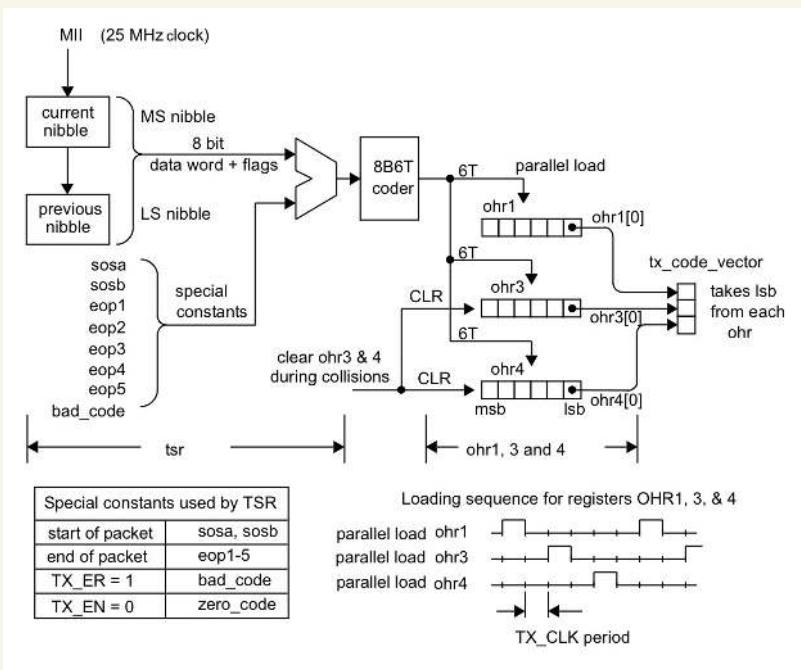


Figure 23-6—PCS sublayer to PMA sublayer frame structure

- SOSA      The succession of six ternary symbols: [ 1 -1 1 -1 1 -1 ], which is the result of encoding the constant sosa.
- SOSB      The succession of six ternary symbols: [ 1 -1 1 -1 -1 1 ], which is the result of encoding the constant sosb.
- P3          The succession of two ternary symbols: [ 1 -1 ].
- P4          The succession of four ternary symbols: [ 1 -1 1 -1 ].
- DATA        A 6T code group that is the result of encoding a data octet in a packet that is not part of the Clause 4 MAC preamble or SFD.
- EOP1-5     A 6T code group that is the result of encoding one of the end-of-packet patterns eop1-5.

在询问发送，因为是8B/1T，所以加载m22 NIBBLE  
需要2T时间。所以三个线，有-1 delay 2i.-T+T。  
加载的话，每个口加载6T。即编码的6T  
1 BYTE。所以是BYTE-INTERLEAVING

sosa	A constant that encodes to: [ 1 -1 1 -1 1 -1].	] $\rightarrow$
sosb	A constant that encodes to: [ 1 -1 1 -1 -1 1].	}
eop1	A constant that encodes to: [ 1 1 1 1 1 1].	
eop2	A constant that encodes to: [ 1 1 1 1 -1 -1].	
eop3	A constant that encodes to: [ 1 1 -1 -1 0 0].	
eop4	A constant that encodes to: [ -1 -1 -1 -1 -1 -1].	
eop5	A constant that encodes to: [ -1 -1 0 0 0 0].	
bad_code	A constant that encodes to: [ -1 -1 -1 1 1 1].	
zero_code	A constant that encodes to: [ 0 0 0 0 0 0].	



100BASE-T4

Table 23-2—MDI signals transmitted by the PMA

Signal	Allowed pair	Meaning
CS1	TX_D1, BI_D3 BI_D4	A waveform that conveys the ternary symbol 1. Nominal voltage level +3.5 V.
CS0	TX_D1, BI_D3 BI_D4	A waveform that conveys the ternary symbol 0. Nominal voltage level 0 V.
CS-1	TX_D1, BI_D3 BI_D4	A waveform that conveys the ternary symbol -1. Nominal voltage level -3.5 V.
TP_IDL_100	TX_D1	Idle signal. Indicates transmitter is currently operating at 100 Mb/s.

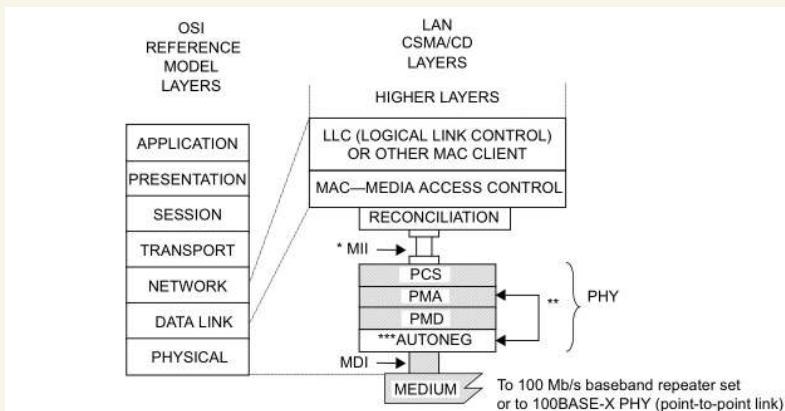
Table 23-3—Signals received at the MDI

Signal	Allowed pair	Meaning
CS1	RX_D2, BI_D3 BI_D4	A waveform that conveys the ternary symbol 1. Nominal transmitted voltage level +3.5 V.
CS0	RX_D2, BI_D3 BI_D4	A waveform that conveys the ternary symbol 0. Nominal transmitted voltage level 0 V.
CS-1	RX_D2, BI_D3 BI_D4	A waveform that conveys the ternary symbol -1. Nominal transmitted voltage level -3.5 V.
TP_IDL_100	RX_D2	Idle signal. Indicates transmitter is currently operating at 100 Mb/s.

TP\_IDL\_100 is defined in 23.4.1.2. The encodings for CS1, CS0, and CS-1 are defined in 23.5.1.2.

Re-timing of CS1, CS0, and CS-1 signals within the PMA is required.

100BASE-T4 ↑



MDI = MEDIUM DEPENDENT INTERFACE

PCS = PHYSICAL CODING SUBLAYER

MII = MEDIA INDEPENDENT INTERFACE

PMA = PHYSICAL MEDIUM ATTACHMENT

PHY = PHYSICAL LAYER DEVICE

PMD = PHYSICAL MEDIUM DEPENDENT

\* MII is optional.  
\*\* AUTONEG communicates with the PMA sublayer through the PMA service interface messages PMA\_LINK.request and PMA\_LINK.indicate.

\*\*\* AUTONEG is mandatory for EEE capability and optional otherwise.

Figure 24-1—Type 100BASE-X PHY relationship to the ISO/IEC Open Systems Interconnection (OSI) reference model and the IEEE 802.3 CSMA/CD LAN model

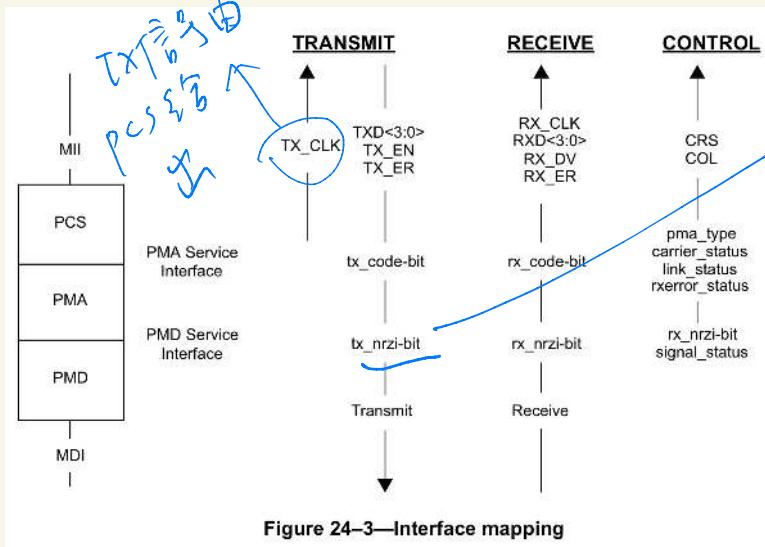


Figure 24-3—Interface mapping

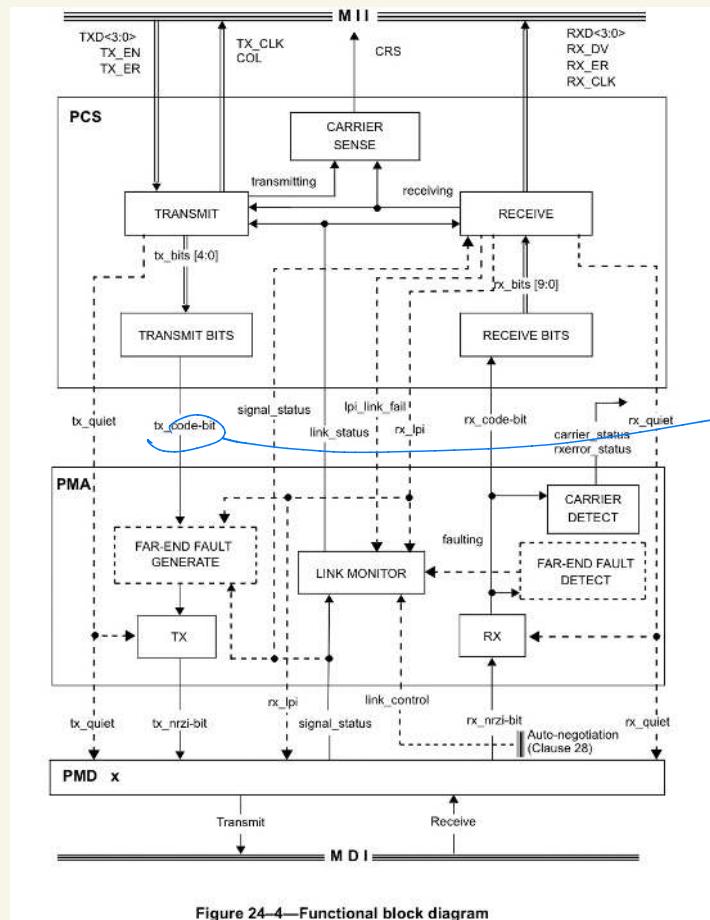


Figure 24-4—Functional block diagram

100BASE-X  
FUNCTION SPEC

EEZ 模式下，会同期  
发送 refresh signal，从而减少  
clock drift

Table 24-1—4B/5B code-groups

	PCS code-group [4:0] 4 3 2 1 0	Name	MII (TXD/RXD) <3:0> 3 2 1 0	Interpretation
D A T A	1 1 1 1 0	0	0 0 0 0	Data 0
	0 1 0 0 1	1	0 0 0 1	Data 1
	1 0 1 0 0	2	0 0 1 0	Data 2
	1 0 1 0 1	3	0 0 1 1	Data 3
	0 1 0 1 0	4	0 1 0 0	Data 4
	0 1 0 1 1	5	0 1 0 1	Data 5
	0 1 1 1 0	6	0 1 1 0	Data 6
	0 1 1 1 1	7	0 1 1 1	Data 7
	1 0 0 1 0	8	1 0 0 0	Data 8
	1 0 0 1 1	9	1 0 0 1	Data 9
	1 0 1 1 0	A	1 0 1 0	Data A
	1 0 1 1 1	B	1 0 1 1	Data B
	1 1 0 1 0	C	1 1 0 0	Data C
	1 1 0 1 1	D	1 1 0 1	Data D
C O N T R O L	1 1 1 0 0	E	1 1 1 0	Data E
	1 1 1 0 1	F	1 1 1 1	Data F
	1 1 1 1 1	I	undefined	IDLE; used as inter-stream fill code
	0 0 0 0 0	P	0 0 0 1	SLEEP; LPI code only for the EEE capability. Otherwise, Invalid code;
	1 1 0 0 0	J	0 1 0 1	Start-of-Stream Delimiter, Part 1 of 2; always used in pairs with K
	1 0 0 0 1	K	0 1 0 1	Start-of-Stream Delimiter, Part 2 of 2; always used in pairs with J
	0 1 1 0 1	T	undefined	End-of-Stream Delimiter, Part 1 of 2; always used in pairs with R
	0 0 1 1 1	R	undefined	End-of-Stream Delimiter, Part 2 of 2; always used in pairs with T
	0 0 1 0 0	H	Undefined	Transmit Error; used to force signaling errors
	0 0 0 0 0	V	Undefined	Invalid code
I N V A L I D	0 0 0 0 1	V	Undefined	Invalid code
	0 0 0 1 0	V	Undefined	Invalid code
	0 0 0 1 1	V	Undefined	Invalid code
	0 0 1 0 1	V	Undefined	Invalid code
	0 0 1 1 0	V	Undefined	Invalid code
	0 1 0 0 0	V	Undefined	Invalid code
	0 1 1 0 0	V	Undefined	Invalid code
	1 0 0 0 0	V	Undefined	Invalid code
	1 1 0 0 1	V	Undefined	Invalid code

→ NRZI (non-return-to-zero-invert) is good for timing recovery

→ bit-order  
'0P' to '0101' =从LSB→msb

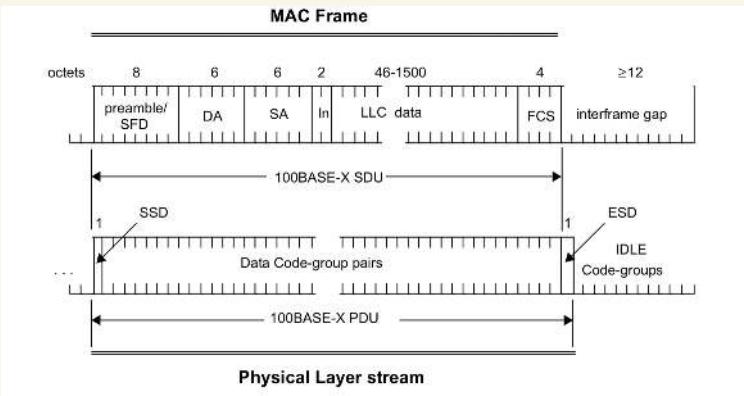


Figure 24-5—PCS encapsulation

SSD 是 code-group 的 boundary, 而 ESD 是 10/10/10.  
第一个 10/10/10 被替换了 SSD.

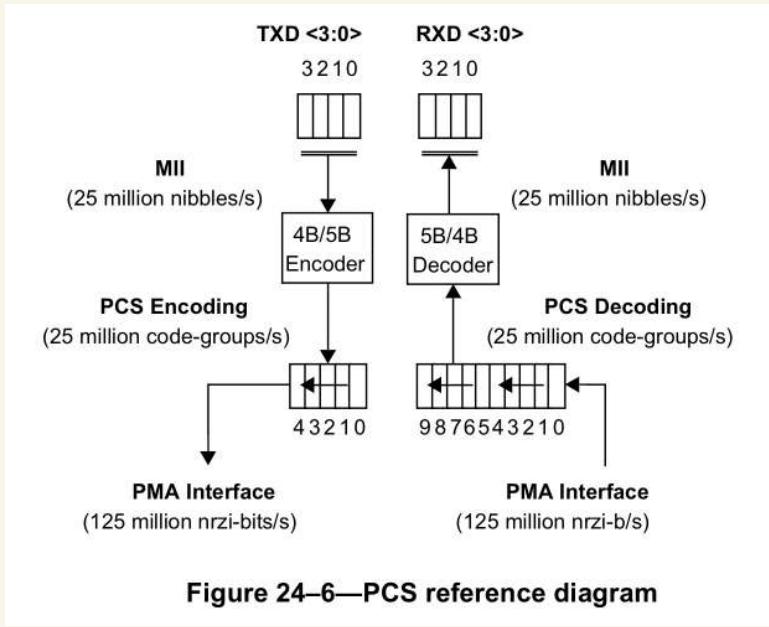


Figure 24-6—PCS reference diagram

发送时从 BIT4 开始,  
接收时从 0 开始一直排列。

# 检测 channel (远端故障) (10T bit time)

generates additional status indications for use by its client.

The following primitives are defined:

PMA\_TYPE.indicate  
PMA\_UNITDATA.request  
PMA\_UNITDATA.indicate  
PMA\_CARRIER.indicate  
PMA\_LINK.indicate  
PMA\_LINK.request

↑  
物理层状态  
↑  
物理层请求  
↑  
物理层指示  
↑  
物理层不活动  
↑  
物理层连接  
↑  
物理层指示

200

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IEEE Std 802.3-2015  
IEEE Standard for Ethernet  
SECTION TWO

PMA\_RXERROR.indicate  
PMA\_LPILINKFAIL.request  
PMA\_RXLPLI.request

↑  
TX-CODE-BIT 是 8VTFB9B-T0

## 24.3.2.1 Far-End fault

Auto-Negotiation provides a Remote Fault capability useful for detection of asymmetric link failures; i.e., channel error conditions detected by the far-end station but not the near-end station. Since Auto-Negotiation is specified only for media supporting eight-pin modular connectors, such as used by 100BASE-TX over twisted pair, Auto-Negotiation's Remote Fault capability is unavailable to other media for which it may be functionally beneficial, such as 100BASE-TX over shielded twisted pair or 100BASE-FX. A remote fault capability for 100BASE-FX is particularly useful due to this medium's applicability over longer distances (making end-station checking inconvenient) and for backbones (in which detection of link failures can trigger redundant systems).

↑  
因为 AUTONEG 不能在光纤里使用，所以不存在。

For these reasons, 100BASE-X provides an optional Far-End Fault facility when Auto-Negotiation cannot be used. Far-End Fault shall not be implemented for media capable of supporting Auto-Negotiation.

When no signal is being received, as indicated by the PMD's signal detect function, the Far-End Fault feature permits the station to transmit a special Far-End Fault Indication to its far-end peer. The Far-End Fault Indication is sent only when a physical error condition is sensed on the receive channel. In all other situations, including reception of the Far-End Fault Indication itself, the PMA passes through tx\_code-bit. (Note that the Far-End Fault architecture is such that IDLEs are automatically transmitted when the Far-End Fault Indication is detected. This is necessary to re-establish communication when the link is repaired.)

#### 24.4.1 PMD service interface

The following specifies the services provided by the PMD. The PMD is a sublayer within 100BASE-X and may not be present in other 100BASE-T PHY specifications. PMD services are described in an abstract manner and do not imply any particular implementation. It should be noted that these services are functionally identical to those defined in the FDDI standards, such as ISO/IEC 9314-3:1990 and ANSI X3.263-1995, with the following three exceptions:

- a) 100BASE-X does not include a Station Management (SMT) function; therefore the PMD-to-SMT interface defined in ISO/IEC 9314-3:1990 and ANSI X3.263-1995.
- b) 100BASE-X does not support multiple instances of a PMD in service to a single PMA; therefore, no qualifiers are needed to identify the unique PMD being referenced.
- c) 100BASE-X may support LPI for the EEE capability.

There are also *editorial* differences between the interfaces specified here and in the referenced standards, as required by the context of 100BASE-X.

The PMD Service Interface supports the exchange of nrzi-bits between PMA entities. The PMD translates the nrzi-bits to and from signals suitable for the specified medium.

The following primitives are defined:

```
PMD_UNITDATA.request  
PMD_UNITDATA.indicate  
PMD_SIGNAL.indicate
```

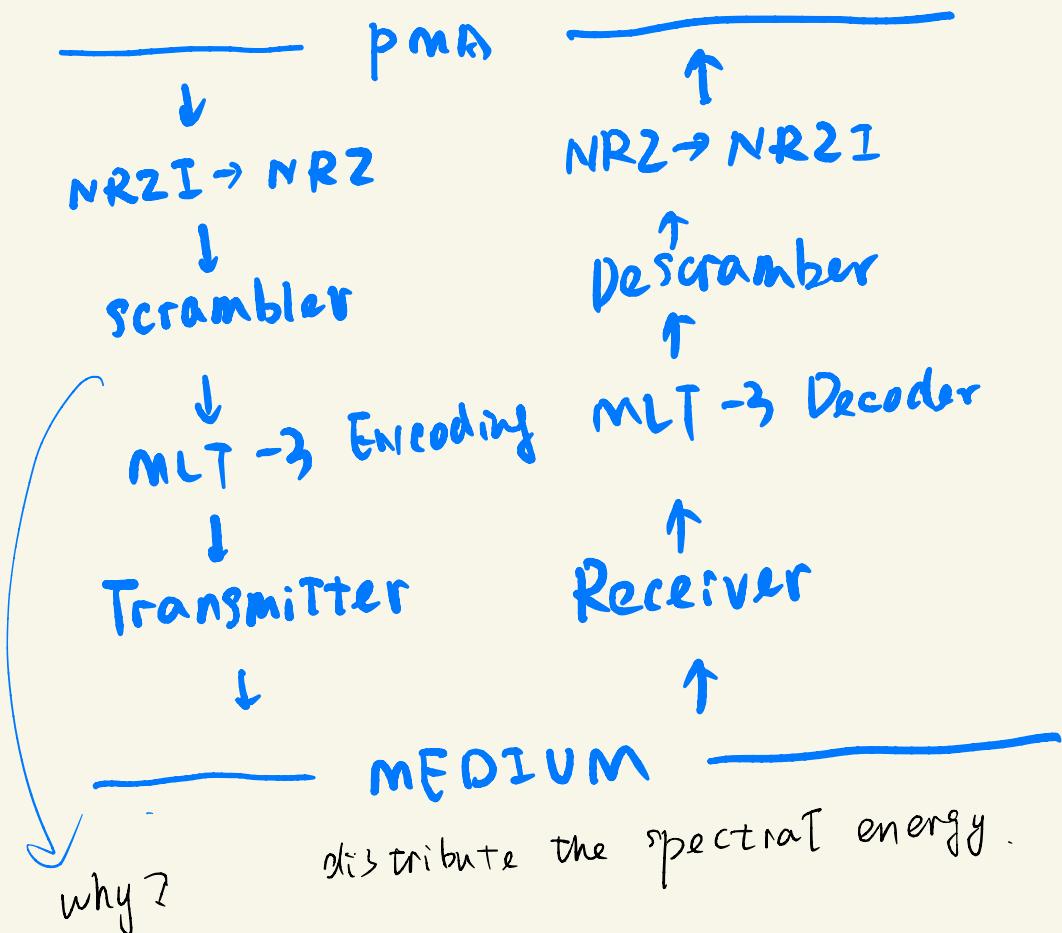
**Table 25–2—Twisted-pair MDI contact assignments**

Contact	PHY without internal crossover MDI SIGNAL	PHY with internal crossover MDI SIGNAL
1	Transmit +	Receive +
2	Transmit –	Receive –
3	Receive +	Transmit +
4		
5		
6	Receive –	Transmit –
7		
8		

100BASE-TX, 100BASE-FX, 100 BASE-FX  
medium, plus PMA layer -> 100Base-TX

PMD

100BASE-TX (TP-PMD)

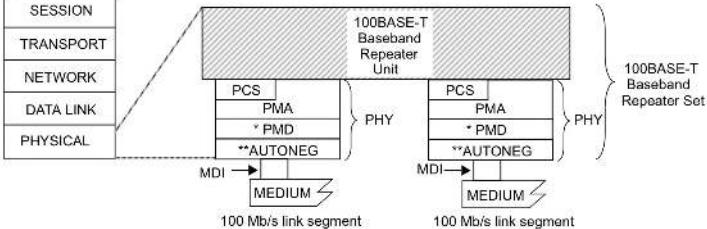


100BASE-PX 遵守 FDDI fibre-MDI

802.3 打包中沒有序號及校驗

OSI  
REFERENCE  
MODEL  
LAYERS

APPLICATION  
PRESENTATION  
SESSION  
TRANSPORT  
NETWORK  
DATA LINK  
PHYSICAL



MDI = MEDIUM DEPENDENT INTERFACE  
MII = MEDIA INDEPENDENT INTERFACE

PCS = PHYSICAL CODING SUBLAYER  
PMA = PHYSICAL MEDIUM ATTACHMENT  
PHY = PHYSICAL LAYER DEVICE  
PMD = PHYSICAL MEDIUM DEPENDENT

- \* PMD is specified for 100BASE-TX and -FX only; 100BASE-T4 does not use this layer.  
Use of MII between PCS and baseband repeater unit is optional.
- \*\* AUTONEG is optional.

Figure 27-1—100BASE-T repeater set relationship to the ISO/IEC OSI reference model

repeater set baseband Repeater Unit 和 position from MII

1. 有且只有一个 broken port for 100M
2. potentially likely cause of this condition
3. block 100M

可能原因：

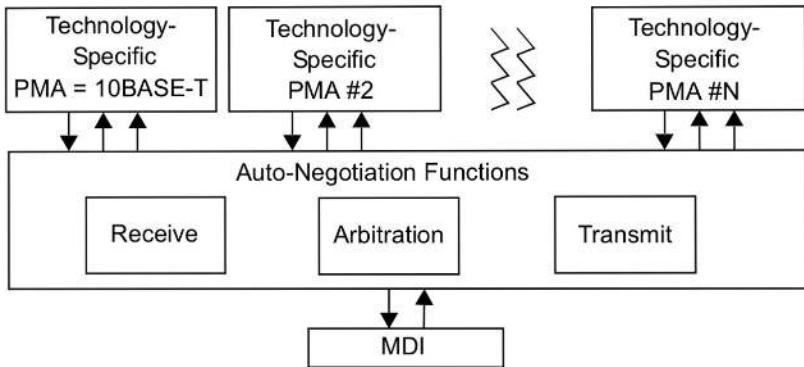
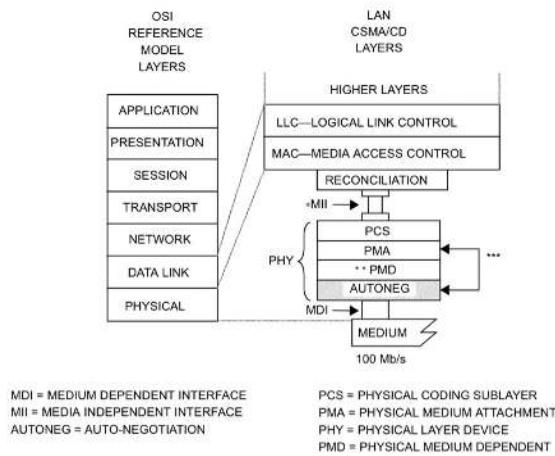


Figure 28–1—High-level model

1. 通过 FLP (fast link pulse) + 方向
  2. 要和 10BASE-T 保持兼容
  3. 由 MAX-NP override
  4. peer-peer 模式，并不走 master-slave 模式
- 支持 100BASE-TX  
100BASE-T4  
10BASE-T

兩方协商



\* MII is optional for 10 Mb/s DTEs and for 100 Mb/s systems and is not specified for 1 Mb/s systems.

\*\* PMD is specified for 100BASE-X only; 100BASE-T4 does not use this layer.

\*\*\* AUTONEG communicates with the PMA sublayer through the PMA service interface messages PMA\_LINK.request and PMA\_LINK.indication.

Figure 28-2—Location of Auto-Negotiation function within the ISO/IEC OSI reference model

1. 双方协商发生在 MDI，AUT & MDI 并不感知，但配置 AN 可通过 MDI-MANAGEMENT 接口
2. 向后兼容 10BASE-T, 100BASE-TX, 100BASE-T4
3. 通过 FLP 协商
4. FLP bursts separated by  $16\text{ms} \pm 8\text{ms}$
5. FLP 包  $62.5\mu\text{s} \pm 7\mu\text{s}$
6. FLP 支持 NLP，但是如果超过了 NLP 自己的 timeout，将自动 disable 它
7. AN 不支持 NLP，但是可以通过 enable 它

# 7. 通过检测线缆类型来 ads cap.

## 28.2.1.1 Link pulse transmission

Auto-Negotiation's method of communication builds upon the link pulse mechanism employed by 10BASE-T MAUs to detect the status of the link. Compliant 10BASE-T MAUs transmit link integrity test pulses as a mechanism to determine if the link segment is operational in the absence of packet data. The 10BASE-T NLP sequence is a pulse (Figure 14–13) transmitted every 16 ms  $\pm$  8 ms while the data transmitter is idle.

Auto-Negotiation substitutes the FLP Burst in place of the single 10BASE-T link integrity test pulse within the NLP sequence (Figure 28–3). The FLP Burst encodes the data that is used to control the Auto-Negotiation function. FLP Bursts shall not be transmitted when Auto-Negotiation is complete and the highest common denominator PMA has been enabled.

FLP Bursts were designed to allow use beyond initial link Auto-Negotiation, such as for a link monitor type function. However, use of FLP Bursts beyond the current definition for link startup shall be prohibited. Definition of the use of FLP Bursts while in the FLP LINK GOOD state is reserved.

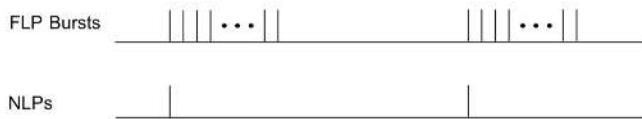
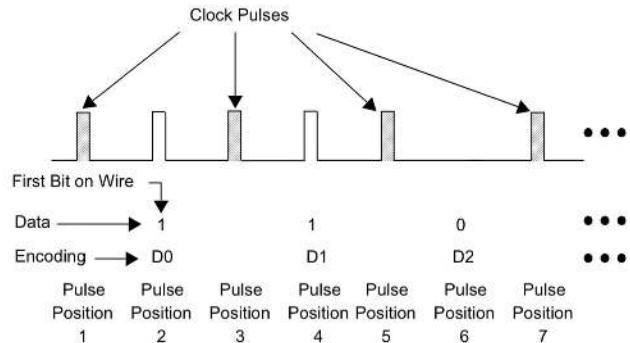


Figure 28–3—FLP Burst sequence to NLP sequence mapping

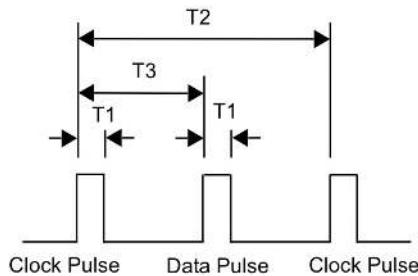
- FLP 里有 33 个脉冲，其中前 7 个是正常的脉冲，  
中间的 16 个是 FLP 周期脉冲，后面是 FLP 97T 脉冲。  
包含 49 个正常的脉冲和 48 个 FLP 脉冲。

脉冲  
脉冲宽度 - 指的是一个脉冲的持续时间。  
从一个脉冲的开始到下一个脉冲的开始的时间间隔。  
从一个脉冲的开始到下一个脉冲的开始的时间间隔 = 2ms.  
从一个脉冲的开始到下一个脉冲的开始的时间间隔 = 2ms.

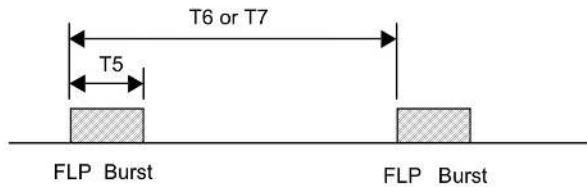
The encoding of data using pulses in an FLP Burst is illustrated in Figure 28–4.



**Figure 28–4—Data bit encoding within FLP Bursts**

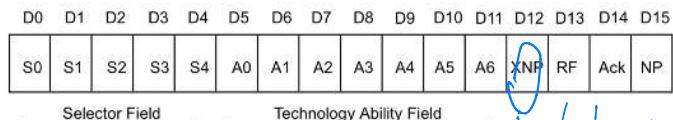


**Figure 28–5—FLP Burst pulse-to-pulse timing**



**Figure 28–6—FLP Burst to FLP Burst timing**

The base link codeword (Base Page) transmitted within an FLP Burst shall convey the encoding shown in Figure 28-7. The Auto-Negotiation function may support additional pages using the Next Page function. Encodings for the link codeword(s) used in Next Page exchange are defined in 28.2.3.4. In an FLP Burst, D0 shall be the first bit transmitted.



**Figure 28–7—Base Page encoding**

The diagram illustrates a memory hierarchy and associated fault handling mechanisms:

- Main Memory:** At the top level.
- Page Frame:** The next level down, containing pages.
- Page Frame Block:** The lowest level shown, containing multiple pages.

Annotations provide additional context:

- extend next + page**: An arrow pointing to the transition between Main Memory and Page Frame.
- remote fault**: An arrow pointing to a fault occurring in a page frame located on a different node.
- next page add additional link - net + page**: An annotation describing a fault that requires adding a link to the network and involves multiple pages.
- register 3/2 3/1 2/0**: An annotation pointing to a specific bit field in a register.
- 42-bit 32-bit 16-bit**: An annotation pointing to bit widths: 42-bit, 32-bit, and 16-bit.
- bit**, **addr**, **adv.**, **reg**, **link**, **net**: A legend defining symbols used in the annotations.

Table 28A-1 Selected Field values

Table 26A-1—Selector Field Value Mappings					
S4	S3	S2	S1	S0	Selector description
0	0	0	0	0	Reserved for future Auto-Negotiation development
0	0	0	0	1	IEEE Std 802.3
0	0	0	1	0	IIEEE Std 802.9u-1995 (withdrawn)
0	0	0	1	1	IIEEE Std 802.3v-2001 (withdrawn)
0	0	1	0	0	IIEEE Std 1394
0	0	1	0	1	INCITS
0	0	1	1	X	Reserved for future Auto-Negotiation development <sup>4</sup>

Table 28B-1—Technology Ability Field bit assignments

Bit	Technology	Minimum cabling requirement
A0	10BASE-T	Two-pair Category 3
A1	10BASE-T full duplex	Two-pair Category 3
A2	100BASE-TX	Two-pair Category 5
A3	100BASE-TX full duplex	Two-pair Category 5
A4	100BASE-T4	Four-pair Category 3
A5	PALSE operation for full duplex links	Not applicable
A6	Asymmetric PALSE operation for full duplex Links	Not applicable

FLP in NT-E tm

1. 第一个脉冲的时钟脉冲  $c_{max}$  ~21
2. 42.5μs Aij 次  $2a_{mix} <$  ~160  
 $\sum b_{max} <$

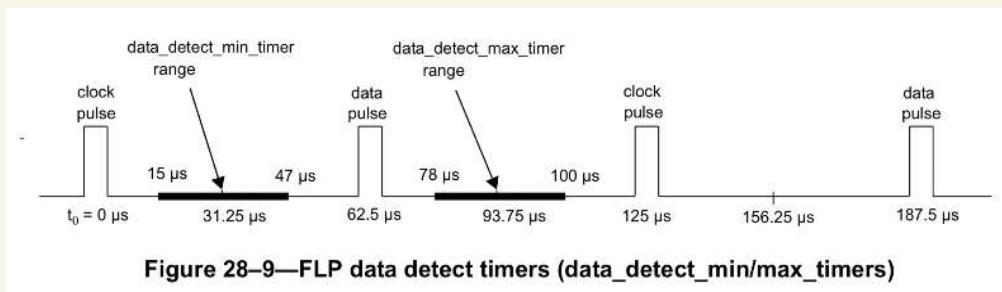


Figure 28-9—FLP data detect timers (data\_detect\_min/max\_timers)

NLP. 相比于10BASE-T来说，发送AN时不带AN帧，  
LINK TEST PASS状态

在AN结束后，MP2的交互会转移到PMA

并行协议

to FLP = by MP2 + 3) 的包向对方发去

(10BASE-T4, IX, PNP  
PMT

AN - PAUSE → pause frame to make all the station  
stop sending frame to the received  
port within the indicated  
period.

# Re-AIX

會 turn down PMA, [16] 附註用 break. timer. 沒有  
SDF 也會感應到，重新切換

D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13	D14	D15
M0	M1	M2	M3	M4	M5	M6	M7	M8	M9	M10	T	Ack2	MP	Ack	NP

Figure 28-11—Message Page encoding

D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13	D14	D15
U0	U1	U2	U3	U4	U5	U6	U7	U8	U9	U10	T	Ack2	MP	Ack	NP

Figure 28-12—Unformatted Page encoding

1. 發完 BASE 后可以 next page }
2. 是否還有下一个 page

EXTEND NEXT PAGE

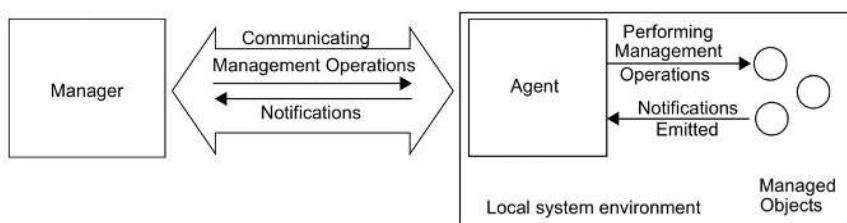
M21 - AN 有存儲 , 0, 1, 4, 5, 6  
7 is next page

## 28.2.6 Technology-Dependent Interface

The Technology-Dependent Interface is the communication mechanism between each technology's PMA and the Auto-Negotiation function. Auto-Negotiation can support multiple technologies, all of which need not be implemented in a given device. Each of these technologies may utilize its own technology-dependent link integrity test function.

当为单双工时，最大帧速率受到冲突检测机制的限制，而为全双工时，只受到信道传输速率的限制。

在 10 Mbit/s 速率 media 由 MAU \ Port  
速率由 PMA & PMD.



NOTE—This figure is drawn from Figure 1 of ISO/IEC 10040:1992, Information technology—Open Systems Interconnection—Systems management overview. In the event of any conflict, the depiction in ISO/IEC 10040:1992 takes precedence.

Figure 30–1—Interaction between manager, agent, and objects

## 31.2 Layer architecture

The MAC Control sublayer is a client of the CSMA/CD MAC. Figure 31-1 depicts the architectural positioning of the MAC Control sublayer with respect to the CSMA/CD MAC and the MAC Control client.

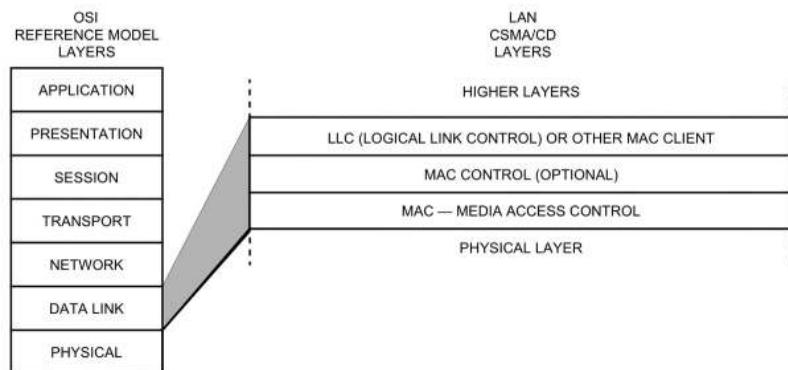


Figure 31-1—Architectural positioning of MAC Control sublayer

MAC control [从 LLC 层 MAC Access 之间, 走到这层]

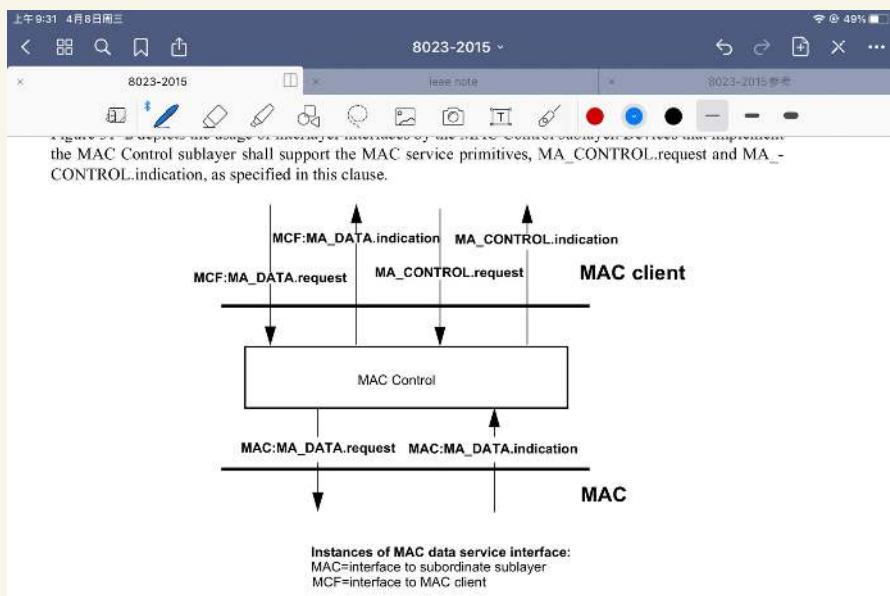


Figure 31-2—MAC Control sublayer support of interlayer service interfaces

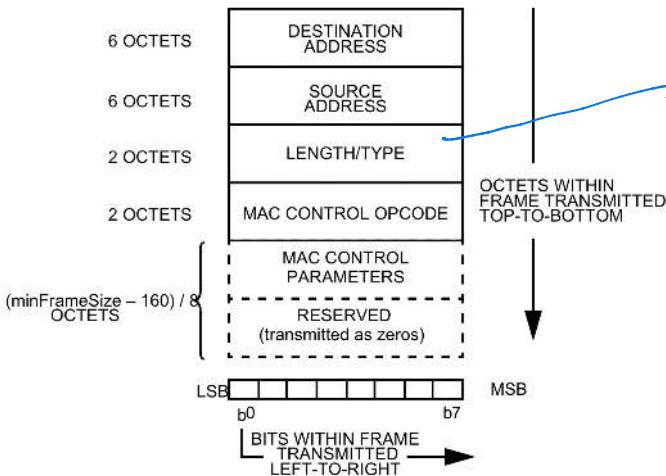
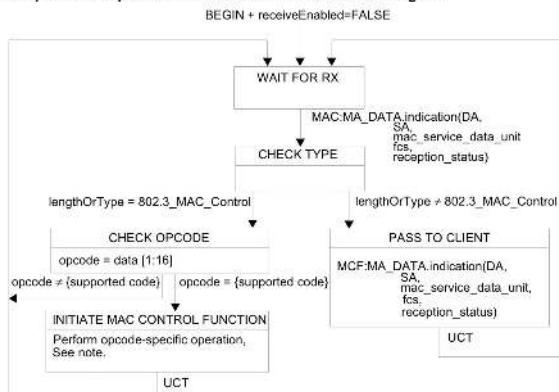


Figure 31-3—MAC Control frame format

固定長度:  $\text{min\_frame\_size} \times 8$   
 $b_0 \dots b_7 = (6 + 6 + 2 + 2 + 4 \times 8) \times 8$

#### 31.5.3.4 Opcode-independent MAC Control Receive state diagram



Instances of MAC data service interface:  
 MAC=interface to subordinate sublayer  
 MCF=interface to MAC client

NOTE—The opcode-specific operation (see Annex 31A) is launched as a parallel process by the MAC Control sublayer, and not as a synchronous function. Progress of the generic MAC Control Receive state diagram (as shown in this figure) is not implicitly impeded by the launching of the opcode-specific function.

Figure 31-4—Generic MAC Control Receive state diagram

具体到 opcode 参见 Annex 31A . s2-731

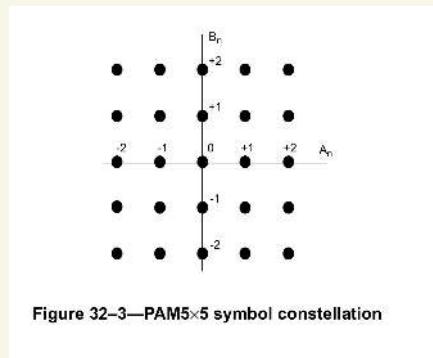
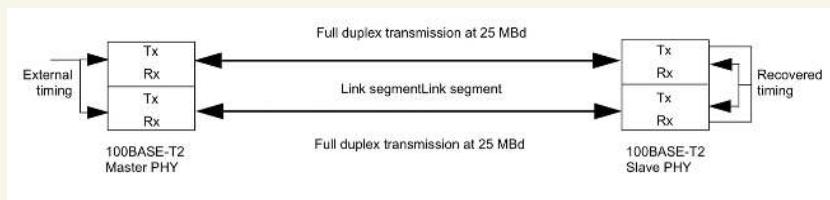
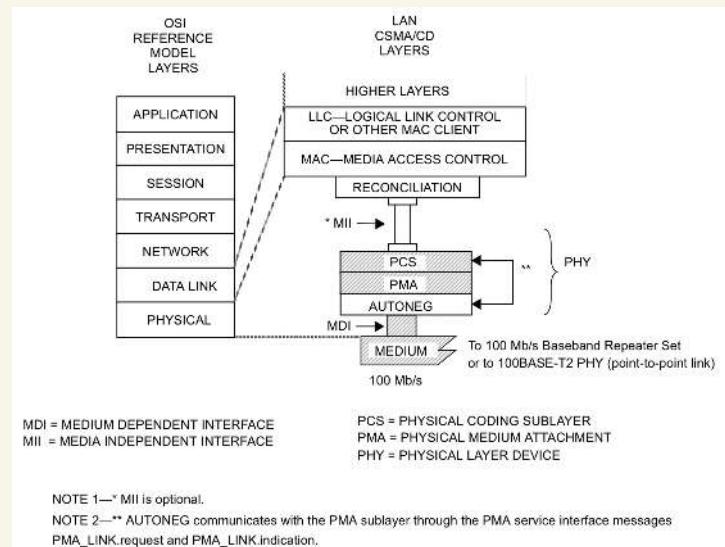


Figure 32-3—PAM5x5 symbol constellation

↑-↑ phy control service.

The following primitives are defined:

PHYC\_CONFIG.indication  
PHYC\_TXMODE.indication  
PHYC\_RXSTATUS.request  
PHYC\_REMRXSTATUS.request

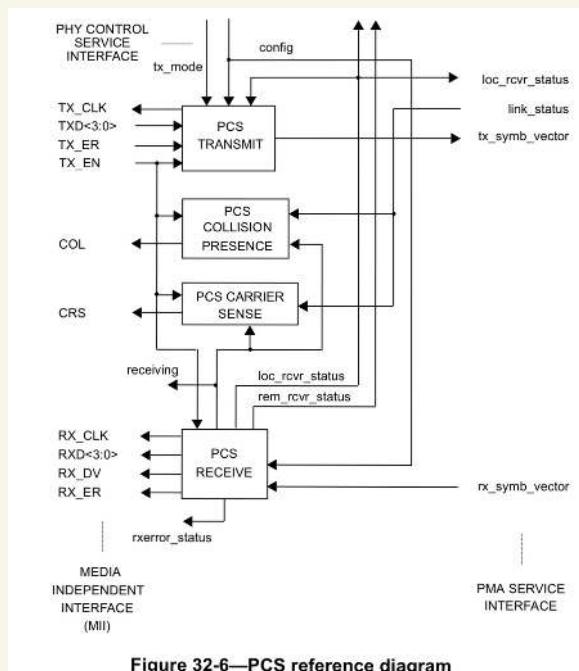
這是時鐘 跟 master 這裏 slave

是 IDLE 還是 DATA

MDI 到 有線傳輸就OK

這端 PHY for T2

PCS [2]: Transmit, Receive, Carrier Sense, PCS collision



### 1. Reset

Figure 32-6—PCS reference diagram

PATH MODE [0, Sa[1] @ TXDn[3], San[0] @ TXDn[2] @ 1]  
VOLT MUTE [1, 0, 0]

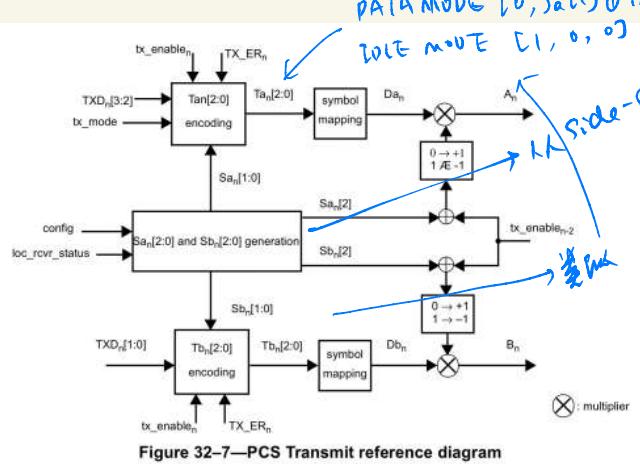


Figure 32-7—PCS Transmit reference diagram

MAC算法：master PHY :  $1T \times 13 + X^{23}$   $\rightarrow$  68K-2

slave PHY :  $1T \times 20 + X^{23}$

Symbol mapping	
Ts/Tb	Ds/Db
000	0
001	+1
010	-1
011	-2
100 (ESC)	+2

	Idle or data
Da <sub>n</sub> :	0, +1, -1, or -2
Db <sub>n</sub> :	0, +1, -1, or -2

Data stream delimiters

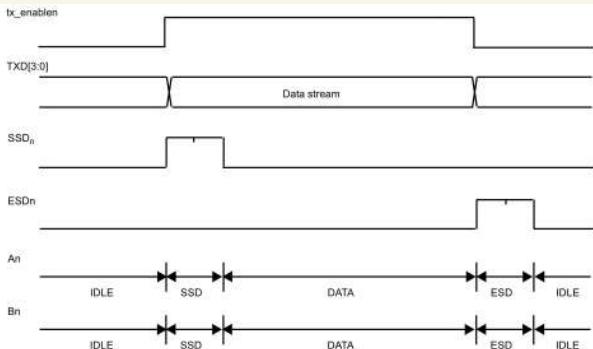
Error indication

100BASE-T2 for AN IN THE NEXT PAGE

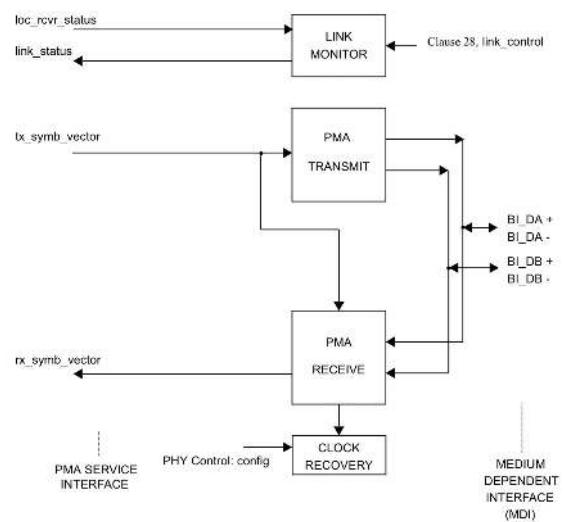
Figure 32–9—Symbol mapping and encoding rule summary

$$A_n = \begin{cases} Da_n & \text{if } \text{Sa}_n[2] \oplus \text{tx\_enable}_{n-2} = 0 \\ -Da_n & \text{else} \end{cases}$$

$$B_n = \begin{cases} Db_n & \text{if } Sb_n[2] \oplus tx\_enable_{n-2} = 0 \\ -Db_n & \text{else} \end{cases}$$



**Figure 32–11—PCS sublayer to PMA sublayer frame structure**



**Figure 32–15—PMA reference diagram**

### 32.5.1 100BASE-T2 Use of Auto-Negotiation and MII Registers 8, 9, and 10

On power-up, before Auto-Negotiation starts, the Auto-Negotiation Advertisement register shall have the following configuration: The Selector Field (4:4:0) is set to an appropriate code as specified in Annex 28A. The Acknowledge bit (4:14) is set to logic zero. The Technology Ability Field (4:9:5) is set based on the values set in the MII Status Register (Register 1) (1:15:11) or equivalent and (4:11:10) is set based on the values set in the MII Status Register (Register 1) (1:10:9) or equivalent.

When Auto-Negotiation begins, 100BASE-T2 implementations send an Auto-Negotiation Base Page with bit D15 set to logical one to indicate that a Next Page follows (see 28.2.1.2.)

The Base Page is followed by a formatted Next Page containing the 100BASL-T2 Technology Ability Message Code (7), which indicates that two Unformatted Next Pages containing the 100BASF-T2 Technology Ability fields follow (see Table 28C-1.)

Two Unformatted Next Pages are sent using the 100BASE-T2 Technology Ability fields shown in Table 32-6. Register 8 will be used to store the transmitted information while it is being processed as described below.

Bit U0 of page 1 shall be copied from MII Register 4.10 to indicate 100BASE-T2FD advertised ability.

Bit U1 of page 1 shall be copied from MII Register 4.11 to indicate 100BASE-T2HD advertised ability.

Bit U2 of page 1 shall be copied from MASTER-SLAVE control register 9.10 to indicate that the PHY device is a repeater port or DTE for 100BASL-T2.

Table 32-14—Assignment of PMA signals to MDI pin-outs

Contact	PHY without internal crossover (100BASE-T2 operation)	PHY with internal crossover (Auto-Negotiation operation)	MDI labeling requirement
1	BI_DA+	BI_DB+	BI_DA+
2	BI_DA-	BI_DB-	BI_DA-
3	BI_DB+	BI_DA+	BI_DB+
4	Not used	Not used	
5	Not used	Not used	
6	BI_DB-	BI_DA-	BI_DB-
7	Not used	Not used	
8	Not used	Not used	

## 22D.2 Read operation

To read a Clause 45 register using the Clause 22 access mechanism, perform the following accesses using the appropriate PHY address for the PHY of interest:

- a) To Register 13, write the Function field to 00 (address) and DEVAD field to the device address value for the desired MMD;
- b) To Register 14, write the desired address value to the MMD's address register;
- c) To Register 13, write the Function field to 01 (Data, no post increment) and DEVAD field to the same device address value for the desired MMD;
- d) From Register 14, read the content of the MMD's selected register.

Step a) and Step b) can be skipped if the MMD's address register was previously configured.

## 22D.1 Write operation

To write a Clause 45 register using the Clause 22 access mechanism, perform the following accesses using the appropriate PHY address for the PHY of interest:

- a) To Register 13, write the Function field to 00 (address) and DEVAD field to the device address value for the desired MMD;
- b) To Register 14, write the desired address value to the MMD's address register;
- c) To Register 13, write the Function field to 01 (Data, no post increment) and DEVAD field to the same device address value for the desired MMD;
- d) To Register 14, write the content of the MMD's selected register.

Step a) and Step b) can be skipped if the MMD's address register was previously configured.

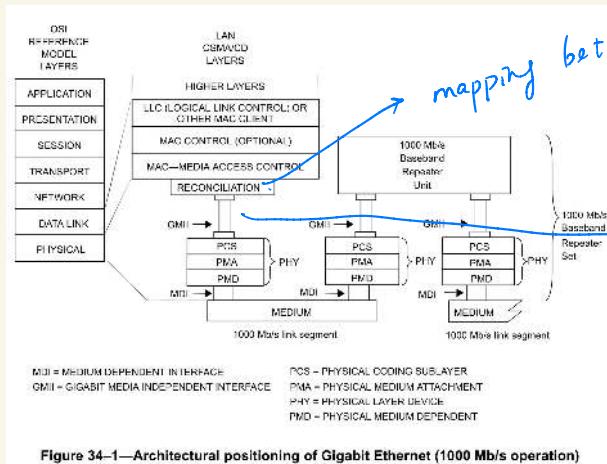


Figure 34–1—Architectural positioning of Gigabit Ethernet (1000 Mb/s operation)

mapping between the signals provided at the GMII and the MAC/PLS service def.   
 PLS & MAC  $\rightarrow$  CMOS  
 compatible with common CMOS  
 $\downarrow$   
 CMOS  
 (EN)  $\rightarrow$  GMII  $\rightarrow$  RS  $\rightarrow$  PLS  
 $\rightarrow$  MAC

#### 34.1.4 Auto-Negotiation, type 1000BASE-X

Auto-Negotiation (Clause 37) provides a 1000BASE-X device with the capability to detect the abilities (modes of operation) supported by the device at the other end of a link segment, determine common abilities, and configure for joint operation. Auto-Negotiation is performed upon link startup through the use of a special sequence of reserved link codewords. Clause 37 adopts the basic architecture and algorithms from Clause 28, but not the use of fast link pulses. Auto-Negotiation for 1000BASE-KX is defined in Clause 73.

#### 34.1.5 Auto-Negotiation, type 1000BASE-T

Auto-Negotiation (Clause 28) is used by 1000BASE-T devices to detect the abilities (modes of operation) supported by the device at the other end of a link segment, determine common abilities, and configure for joint operation. Auto-Negotiation is performed upon link startup through the use of a special sequence of fast link pulses.

1G BASE-T  $\rightarrow$  1G BASE-X  
 同的信号类型不一样。

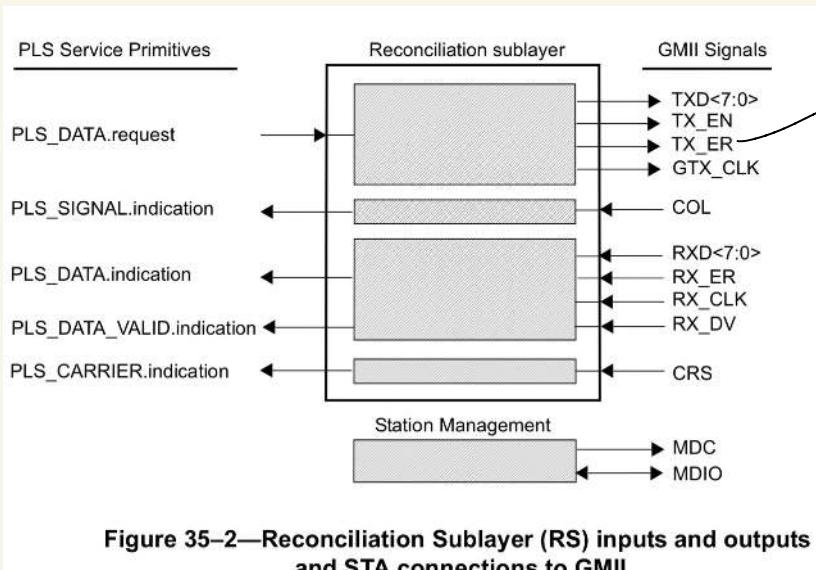


Figure 35–2—Reconciliation Sublayer (RS) inputs and outputs and STA connections to GMII

$\text{GTX\_CLK}$  是不間斷的 MIPI 時鐘是  $\text{TxD}$ ,  $125\text{MHz}$   
 $\text{RX\_CLK}$  可以是  $\text{GTX\_CLK}$ , 但有接收時鐘

Figure 35–3 depicts TX\_EN behavior during a frame transmission with no collisions and without carrier extension or errors.

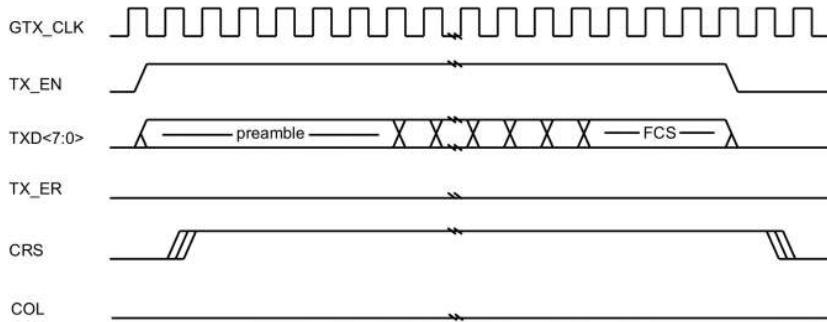


Figure 35–3—Basic frame transmission

↳ TX 和 RX 的 sample 都走上升沿

$\text{TX\_EN} = 0$ ,  $\text{TX\_ER} = 1$ , LPI, carrier extend,  
carrier error extend.

Table 35-1—Permissible encodings of TXD<7:0>, TX\_EN, and TX\_ER

TX_EN	TX_ER	TXD<7:0>	Description	PLS_DATA.request parameter
0	0	00 through FF	Normal inter-frame	TRANSMIT_COMPLETE
0	1	00	Reserved	—
0	1	01	Assert LPI	—
0	1	02 through 0E	Reserved	—
0	1	0F	Carrier Extend	EXTEND (eight bits)
0	1	10 through 1E	Reserved	—
0	1	1F	Carrier Extend Error	EXTEND_ERROR (eight bits)
0	1	20 through FF	Reserved	—
1	0	00 through FF	Normal data transmission	ZERO, ONE (eight bits)
1	1	00 through FF	Transmit error propagation	No applicable parameter

NOTE—Values in TXD<7:0> column are in hexadecimal.

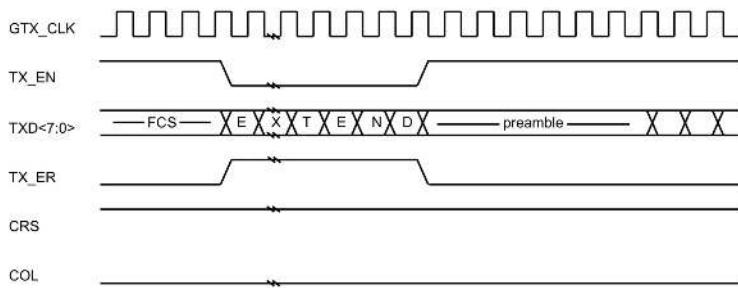


Figure 35-7—Burst transmission

burst [传输] 同样有 extend

进 LPI :  $\text{TX\_EN} = 0$ ,  $\text{TXD} = 1$ ,  $\text{TX\_ER} = 1$

退出 LPI :  $\text{TX\_EN} = 0/1$ ,  $\text{TXD} = 0$ ,  $\text{TX\_ER} = 0$

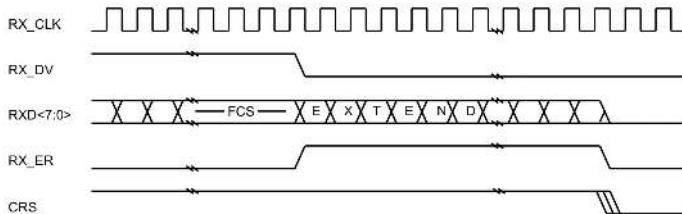


Figure 35–10—Frame reception with carrier extension

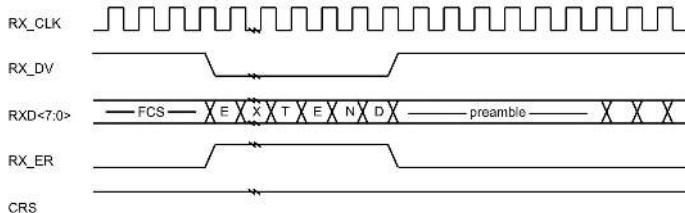


Figure 35–11—Burst reception

Table 35–2—Permissible encoding of RXD<7:0>, RX\_ER, and RX\_DV (continued)

RX_DV	RX_ER	RXD<7:0>	Description	PLS_DATA.indication parameter
0	1	01	Assert LPI	No applicable parameter
0	1	02 through 0D	Reserved	—
0	1	0E	False Carrier indication	No applicable parameter
0	1	0F	Carrier Extend	EXTEND (eight bits)
0	1	10 through 1E	Reserved	—
0	1	1F	Carrier Extend Error	ZERO, ONE (eight bits)
0	1	20 through FF	Reserved	—
1	0	00 through FF	Normal data reception	ZERO, ONE (eight bits)
1	1	00 through FF	Data reception error	ZERO, ONE (eight bits)

NOTE—Values in RXD<7:0> column are in hexadecimal.

Packets transmitted through the GMII shall be transferred within the data stream shown in Figure 35–17.

<inter-frame><preamble><sfd><data><efd><extend>

Figure 35–17—GMII data stream

For the GMII, transmission and reception of each octet of data shall be as shown in Figure 35–18.

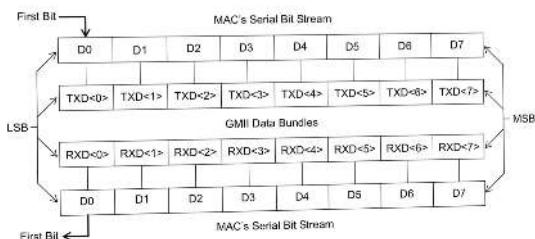


Figure 35–18—Relationship of data bundles to MAC serial bit stream

Table 35–3—Start of receive with no preamble preceding SFD

Signal	Bit values of octets received through GMII <sup>a</sup>			
RXD0	X	X	I <sup>b</sup>	D0 <sup>c</sup>
RXD1	X	X	0	D1
RXD2	X	X	1	D2
RXD3	X	X	0	D3
RXD4	X	X	1	D4
RXD5	X	X	0	D5
RXD6	X	X	1	D6
RXD7	X	X	I	D7
RX_DV	0	0	I	I

<sup>a</sup>Leftmost octet is the first received.

<sup>b</sup>Start Frame Delimiter octet.

<sup>c</sup>D0 through D7 is the first octet of the PDU (first octet of the Destination Address).

Frame 由 IEEE 定义的前导码和 SFD 组成，但没有前导码。但是必须得有 SFD。因为当接收到 SFD 时，RX-DV = 1，并且会触发 carrier sense。并且在发送时，TBI 会将 TX\_PUS 与 CRS 连接。

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Table 35–6—Signal mapping

GMII	MII	TBI
TX_ER	TX_ER	TX<9>
TX_EN	TX_EN	TX<8>
TXD<7>		TX<7>
TXD<6>		TX<6>
TXD<5>		TX<5>
TXD<4>		TX<4>
TXD<3>	TXD<3>	TX<3>
TXD<2>	TXD<2>	TX<2>
TXD<1>	TXD<1>	TX<1>
TXD<0>	TXD<0>	TX<0>
COL	COL	

GMII	MII	TBI
RX_ER	RX_ER	RX<9>
RX_DV	RX_DV	RX<8>
RXD<7>		RX<7>
RXD<6>		RX<6>
RXD<5>		RX<5>
RXD<4>		RX<4>
RXD<3>	RXD<3>	RX<3>
RXD<2>	RXD<2>	RX<2>
RXD<1>	RXD<1>	RX<1>
RXD<0>	RXD<0>	RX<0>
CRS	CRS	

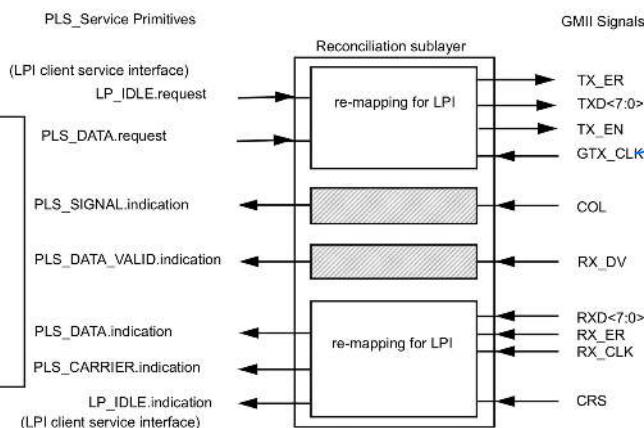


Figure 35–19—LPI assertion and detection mechanism

The 1000BASE-X PCS provides all services required by the GMII, including

- Encoding (decoding) of GMII data octets to (from) ten-bit code-groups (8B/10B) for communication with the underlying PMA
- Generating Carrier Sense and Collision Detect indications for use by PHY's half duplex clients
- Managing the Auto-Negotiation process, and informing the management entity via the GMII when the PHY is ready for use

### 36.1.4.2 Physical Medium Attachment (PMA) sublayer

The PMA provides a medium-independent means for the PCS to support the use of a range of serial-bit-oriented physical media. The 1000BASE-X PMA performs the following functions:

- Mapping of transmit and receive code-groups between the PCS and PMA via the PMA Service Interface
- Serialization (deserialization) of code-groups for transmission (reception) on the underlying serial PMD
- Recovery of clock from the 8B/10B-coded data supplied by the PMD
- Mapping of transmit and receive bits between the PMA and PMD via the PMD Service Interface
- Data loopback at the PMD Service Interface

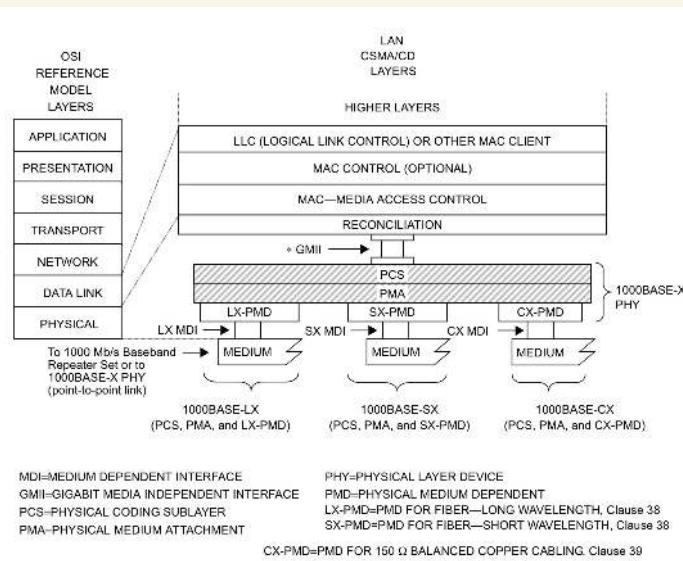


Figure 36–1—Relationship of 1000BASE-X and the PMDs

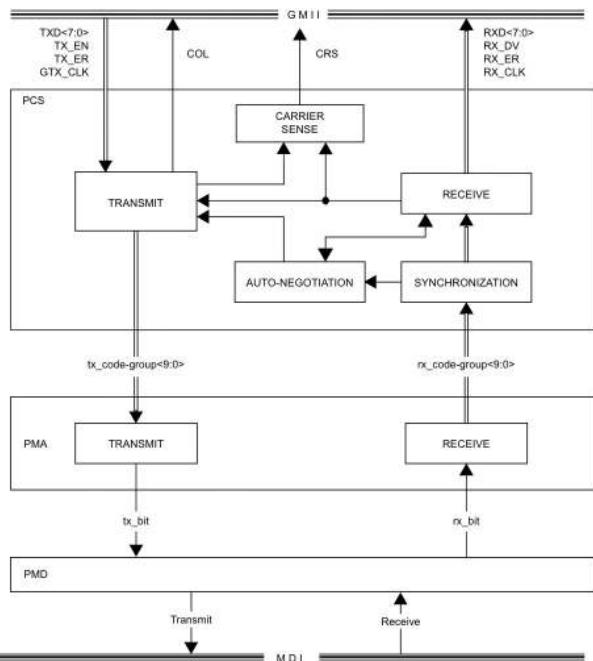


Figure 36–2—Functional block diagram

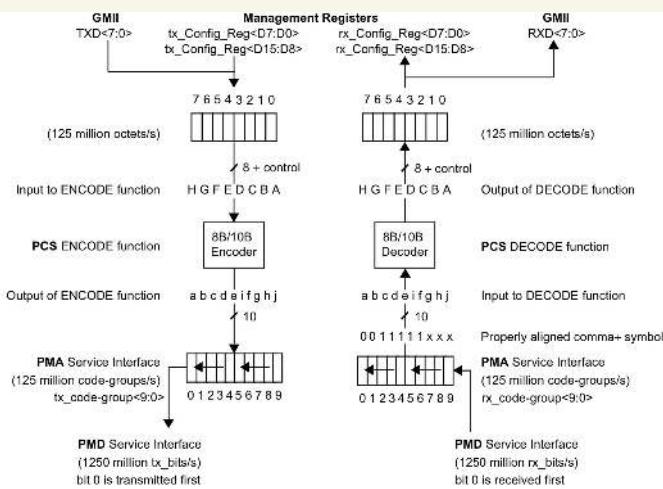


Figure 36–3—PCS reference diagram

Table 36-1a—Valid data code-groups

Code Group Name	Octet Value	Octet Bits HGF EDCBA	Current RD - abedei fghj	Current RD + abedei fghj
D0.0	00	000 000000	100100 1000	011000 1011
D1.0	01	000 000001	011100 0100	001000 1011
D2.0	02	000 000001	101100 0100	010000 1011
D3.0	03	000 000011	110000 1011	000000 1000
D4.0	04	000 000011	100100 1000	011000 1011
D5.0	05	000 000101	010000 1011	101000 0100
D6.0	06	000 000110	011000 1011	001000 1000
D7.0	07	000 000111	110000 1011	000111 0100
D8.0	08	000 001000	110000 1011	000110 0101
D9.0	09	000 001001	100100 1011	101010 0100
D10.0	0A	000 001010	010100 1011	010100 0100
D11.0	0B	000 001011	110100 1011	110100 0100
D12.0	0C	000 001100	001100 1011	000100 0100
D13.0	0D	000 001101	101100 1011	101000 0100
D14.0	0E	000 001110	011000 1011	011000 0100
D15.0	0F	000 001111	010100 1011	101000 1011
D16.0	10	000 100000	010100 1010	100100 1011
D17.0	11	000 100001	100011 1011	100011 0100
D18.0	12	000 100010	010011 1011	010011 0100
D19.0	13	000 100011	110011 1011	110010 0100
D20.0	14	000 100100	001011 1011	000100 0100
D21.0	15	000 100101	101010 1011	101010 0100
D22.0	16	000 100110	011010 1011	011010 0100
D23.0	17	000 100111	111010 0100	000101 1011
D24.0	18	000 110000	110011 0100	001100 1011
D25.0	19	000 110001	100110 1011	100110 0100
D26.0	1A	000 110010	010110 1011	010110 0100
D27.0	1B	000 110011	110110 0100	001101 1011
D28.0	1C	000 111000	001110 0100	001110 0000
D29.0	1D	000 111001	101110 0100	010000 1011
D30.0	1E	000 111010	011110 0100	100000 1011
D31.0	1F	000 111011	101011 0100	010100 1011
D0.1	20	001 000000	100111 1001	011000 1001
D1.1	21	001 000001	011100 1001	100010 1001
D2.1	22	001 000010	101101 1001	010010 1001
D3.1	23	001 000011	110001 1001	110001 1001
D4.1	24	001 000100	110101 1001	101001 1001
D5.1	25	001 000101	101001 1001	101001 1001
D6.1	26	001 000110	011001 1001	010001 1001
D7.1	27	001 000111	110000 1001	000111 1001
D8.1	28	001 001000	110001 1001	000110 1001
D9.1	29	001 001001	100101 1001	100101 1001
D10.1	2A	001 001010	010101 1001	010101 1001
D11.1	2B	001 001011	110100 1001	110100 1001
D12.1	2C	001 001100	001100 1001	001100 1001
D13.1	2D	001 001101	101100 1001	010100 1001
D14.1	2E	001 001110	011100 1001	011100 1001
D15.1	2F	001 001111	010111 1001	101000 1001
D16.1	30	001 100000	010101 1001	100100 1001
D17.1	31	001 100001	100011 1001	100011 1001
D18.1	32	001 100010	010001 1001	010001 1001
D19.1	33	001 100011	110000 1001	110000 1001
D20.1	34	001 100100	001010 1001	001010 1001
D21.1	35	001 100101	101010 1001	101010 1001
D22.1	36	001 100110	010100 1001	010100 1001
D23.1	37	001 100111	110100 1001	000101 1001
D24.1	38	001 110000	110011 1001	001100 1001
D25.1	39	001 110001	100110 1001	100110 1001
D26.1	3A	001 110010	010110 1001	010110 1001
D27.1	3B	001 110011	110110 1001	001001 1001

(continued)

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Table 36-2—Valid special code-groups

Code Group Name	Octet Value	Octet Bits HGF EDCBA	Current RD - abedei fghj	Current RD + abedei fghj	Notes
K28.0	1C	000 111000	001111 0100	110000 1011	1
K28.1	3C	001 111000	001111 0101	110000 0110	1,2
K28.2	5C	010 111000	001111 0101	110000 1010	1
K28.3	7C	011 111000	001111 0011	110000 1100	1
K28.4	9C	100 111000	001111 0010	110000 1101	1
K28.5	BC	101 111000	001111 1010	110000 0101	2
K28.6	DC	110 111000	001111 0110	110000 1001	1
K28.7	FC	111 111000	001111 1000	110000 0111	1,2
K23.7	F7	111 101111	110100 1000	000101 0111	
K27.7	FB	111 111011	101100 1000	001001 01111	
K29.7	FD	111 111011	101110 1000	010001 01111	
K30.7	FE	111 111010	011110 1000	100001 01111	
NOTE 1—Reserved.					
NOTE 2—Contains a comma.					

所有信号都以 K28.5 开头，用于 RECV、SYNC 时序流

1. DATA coding 太长，只看一部分  
 2. 选择 RD- 和 RD+，取决于当前是 running parity。这三组根 CPs 1>0 时偶校验，1<0 时奇校验

由 code group 组成，一个字节  
 ↑

Table 36-3—Defined ordered sets

Code	Ordered Set	Number of Code-Groups	Envelope
JU	Configuration	Alternating X1 and X2	
JCU	Configuration 1	2	K28.3:D2.5:Config_Reg <sup>1</sup>
JC2	Configuration 2	2	K28.5:D2.5:Config_Reg <sup>2</sup>
IDL	IDLE	1	Correcting X1; Preserving X2
ID1	IDLE 1	2	K28.3:D5.6
ID2	IDLE 2	2	K28.5:D6.2
Encapsulation			
IE	Carrier Extend	1	K33.7
IS	Start_of_Packet	1	K25.7
AI	End_of_Packet	1	K29.7
AE	Error Propagation	1	K30.7
LP	LPI	1	Correcting X1; Preserving X2
LP1	LPI 1	2	K28.5:D6.6
LP2	LPI 2	2	K28.5:D5.6

\* Two data code-groups representing the Config\_Reg value.

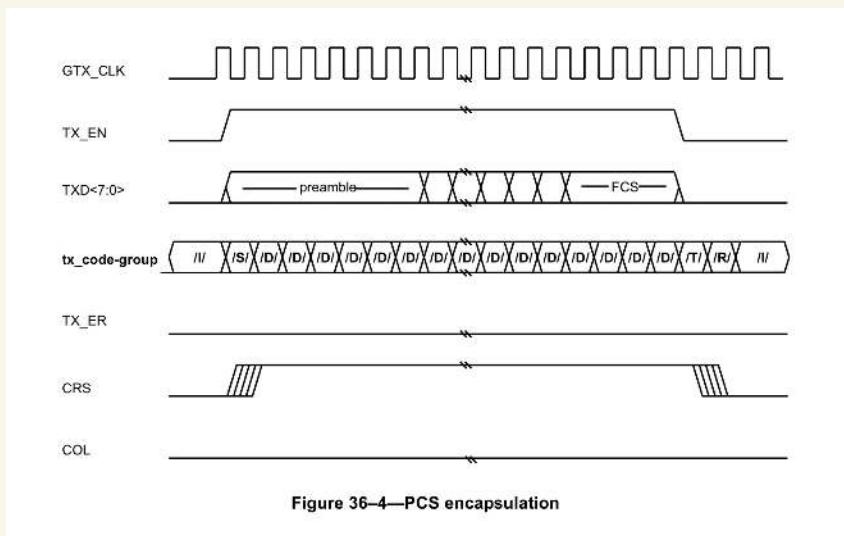
KX.Y - x - EDCBA  
 Y - HGF

LPI 和 PCS 陰陽碼和 持續发送和 IDLE 等价

- packet 由 RIB 产生 PLS 表达 ITR

-↑ packet to burst. MAC Puts to carrier extend. & TX-EN160.  
当 packet to burst时. MAC Puts to carrier extend. & TX-EN160.  
当 packet to burst时. MAC Puts to carrier extend. & TX-EN160.

IDE 定 align 屬性為 code group



对于 PMA 层 42 方向来说，只要收到 10 Bits 就送给 PCS 层，而  
PCS 层进行 alignment 由 PCS 层处理，但是也有办法 pma 会去  
detect comment，来协助 group alignment。不过不会超过 4 T  
BITS

**Table 36–11—TBI required signals**

Symbol	Signal Name	Signal Type	Active Level
tx_code_group<9:0>	Transmit Data	Input	H
PMA_TX_CLK	Transmit Clock	Input	↑
EWRAP	Enable Wrap	Input	H
-LCK_REF	Receive Data	Output	H
PMA_RX_CLK<0:1>	Receive Clock 0	Output	↑
PMA_RX_CLK<1>	Receive Clock 1	Output	↑
COM_DET	Comma Detect	Output	H
-LCK_REF	Lock to Reference	Input	L
EN_CDET	Enable Comma Detect	Input	H

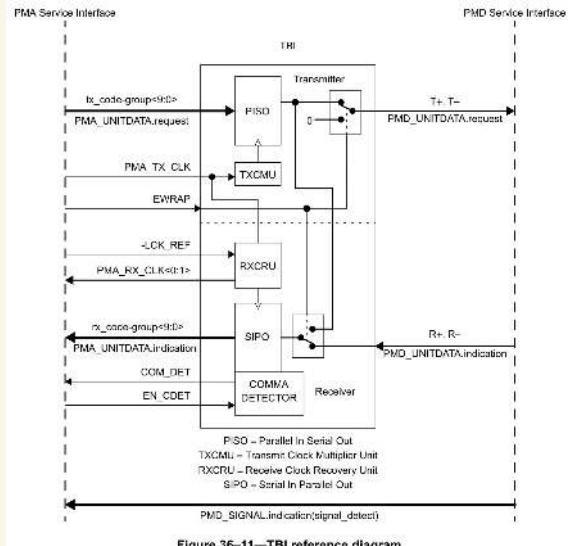
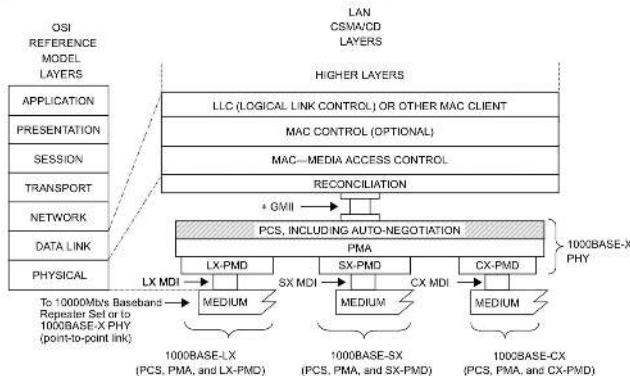


Figure 36–11—TBI reference diagram

# 1000BASE-X AN [更用] 1C) → FLP

## 37.1.3 Relationship to architectural layering

The Auto-Negotiation function is provided at the PCS sublayer of the Physical Layer of the OSI reference model as shown in Figure 36-1. Devices that support multiple modes of operation may advertise this fact using this function. The transfer of information is observable only at the MDI or on the medium.



虽然 Clause 37 AN 是位于 PLS 层, 但 m2 可以管理层分配 AN 参数。

当某个 device 的物理链路固定一种模式时, 仍可以使用 AN

→ 42 行的 3/4 matched to config-reg

SECTION THREE



Table 37-1—Config\_Reg Base Page to management register mapping

Config_Reg Base Page bits	Management register bits
Full Duplex (FD)	4.5 Full Duplex
Half Duplex (HD)	4.6 Half Duplex
PAUSE (PS1)	7 PAUSE
ASM DIR (PS2)	4.8 ASM DIR
Remote Fault (RF2, RF1)	4.13:12 Remote Fault

Table 37-3—Remote Fault encoding

RF1	RF2	Description
0	0	No error, link OK (default)
0	1	Offline
1	0	Link Failure
1	1	Auto-Negotiation_Error

在 RAN 中的  
错误

错误

next page

→ 42 行的 3/4 matched to config-reg

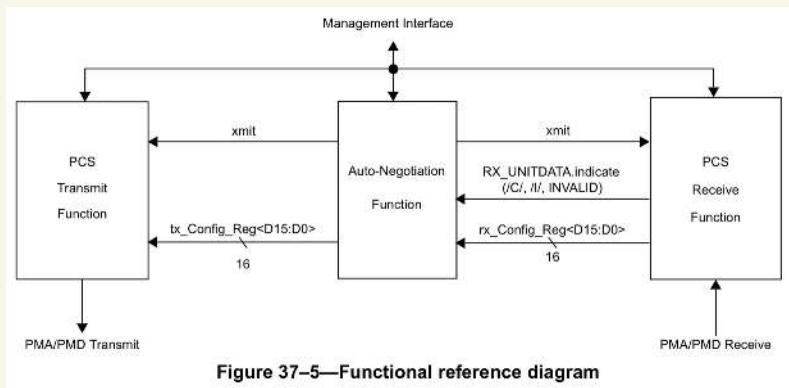
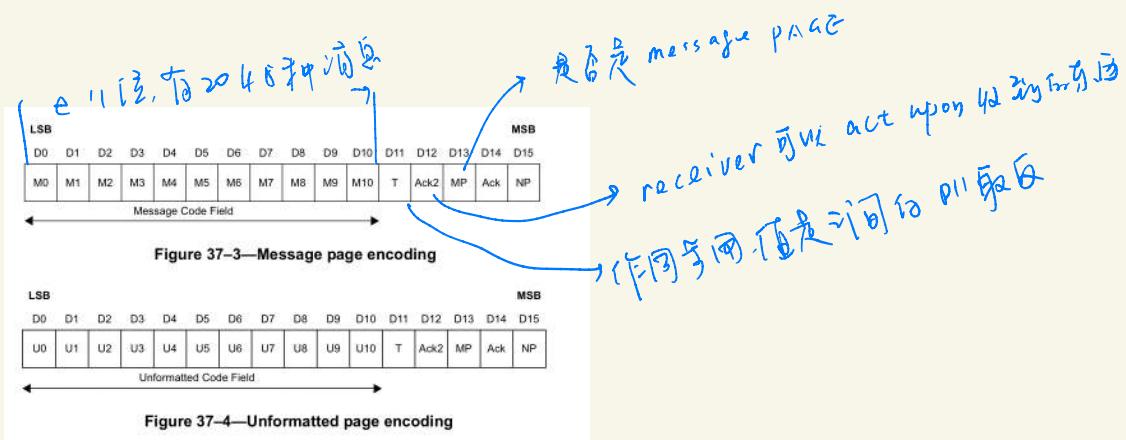
in partner暫停空包的狀態

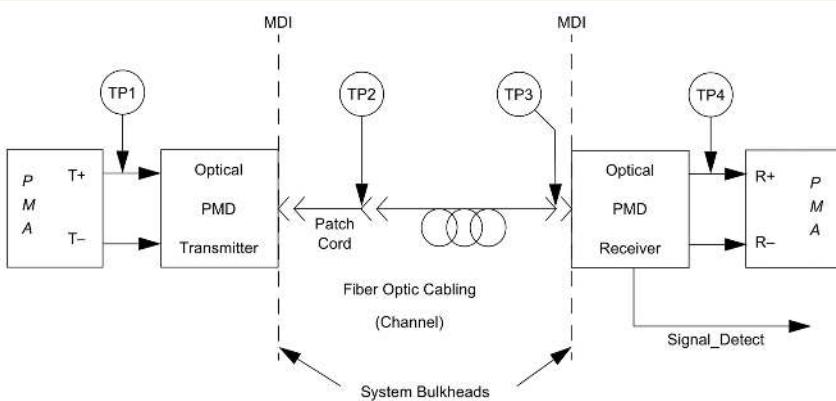
→ 通过 PLS 层的 encode 到 1C1 order list

1. AN 功能基于 1000M 的速率。

2. AN Functionalities 有规定的优先级。

3. next page 延迟在 BASE PAGE 之后, 且双方都设置上 NP\_Bm, RP [图 -> 先 next page L 希望对齐 next page ]





**Figure 38–1—1000BASE-X block diagram**

**Table 38–1—SIGNAL\_DETECT value definition**

Receive conditions	Signal detect value
Input_optical_power ≤ -30 dBm	FAIL
Input_optical_power ≥ Receive sensitivity AND compliant 1000BASE-X signal input	OK
All other conditions	Unspecified

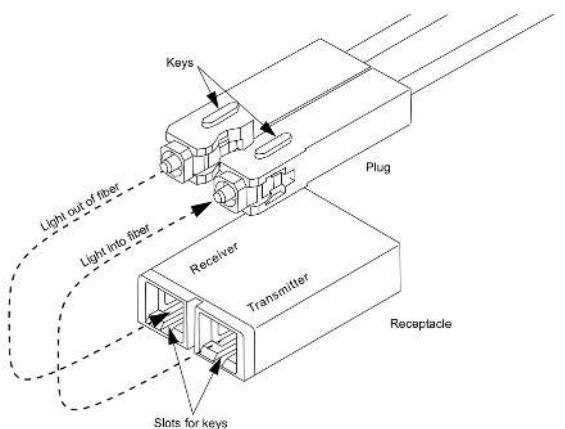
Table 38-10—1000BASE-SX and 1000BASE-LX jitter budget

Compliance point	Total jitter <sup>a</sup>		Deterministic jitter	
	UI	ps	UI	ps
<b>TP1</b>	<b>0.240</b>	<b>192</b>	0.100	80
TP1 to TP2	0.284	227	0.100	80
<b>TP2</b>	<b>0.431</b>	<b>345</b>	0.200	160
TP2 to TP3	0.170	136	0.050	40
<b>TP3</b>	<b>0.510</b>	<b>408</b>	0.250	200
TP3 to TP4	0.332	266	0.212	170
<b>TP4<sup>b</sup></b>	<b>0.749</b>	<b>599</b>	0.462	370

<sup>a</sup> Total jitter is composed of both deterministic and random components. The allowed random jitter equals the allowed total jitter minus the actual deterministic jitter at that point.

<sup>b</sup>Measured with a conformance test signal at TP3 (see 38.6.11) set to an average optical power 0.5 dB greater than the stressed receive sensitivity from Table 38-4 for 1000BASE-SX and Table 38-8 for 1000BASE-LX.

TP1 - TP4 Tr  
1000 BASE - SX  
1000 BASE - LY  
1000 BASE - CX  
中規 common ED



NOTE—Connector keys are used for transmit/receive polarity only. The connector keys do not differentiate between single-mode and multimode connectors.

**Figure 38–8—Duplex SC connector and receptacle (informative)**

1000BASE-CX, RT = R- 为高, RP 为低

Table 39-1—SIGNAL\_DETECT value definition

Receive Conditions	Signal Detect Value
$V_{\text{input}} < (\text{receiver sensitivity} + \text{worst-case local system noise})^b$	FAIL
Minimum differential sensitivity $\leq V_{\text{input}}$ , Receiver $\leq$ Maximum differential input AND compliant 1000BASE-X signal input	OK
All other conditions	Unspecified

<sup>a</sup>Worst-case local system noise includes all receiver coupled noise sources (NEXT, power supply noise, and any reflected signals). Receive sensitivity is the actual sensitivity of the specific port (as imposed to the minimum differential sensitivity).

由手太低也不行  
TX: peak - peak, 1100 mV - 2000 mV  
 $R^+ = 400 \text{ mV} \rightarrow$

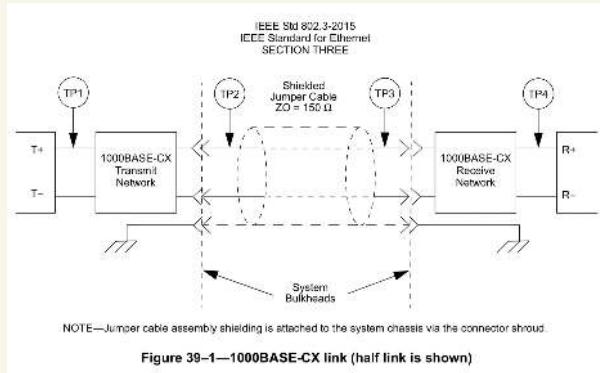


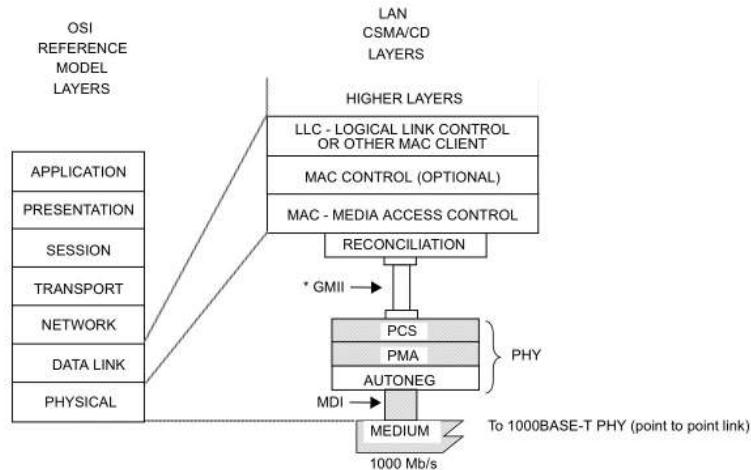
Figure 39-1—1000BASE-CX link (half link is shown)

PCS 层用的是 4D-PAM5, 8bit 转换成 4T5 制  
 $IDLE \rightarrow \{2, 0, -2\}$

PCS-RX - 解扰码 和解编码

PMA - BI-PA & DB & DC & DD

三种模式 - normal & training & LPI



MDI = MEDIUM DEPENDENT INTERFACE

GMII = GIGABIT MEDIA INDEPENDENT INTERFACE

PCS = PHYSICAL CODING SUBLAYER

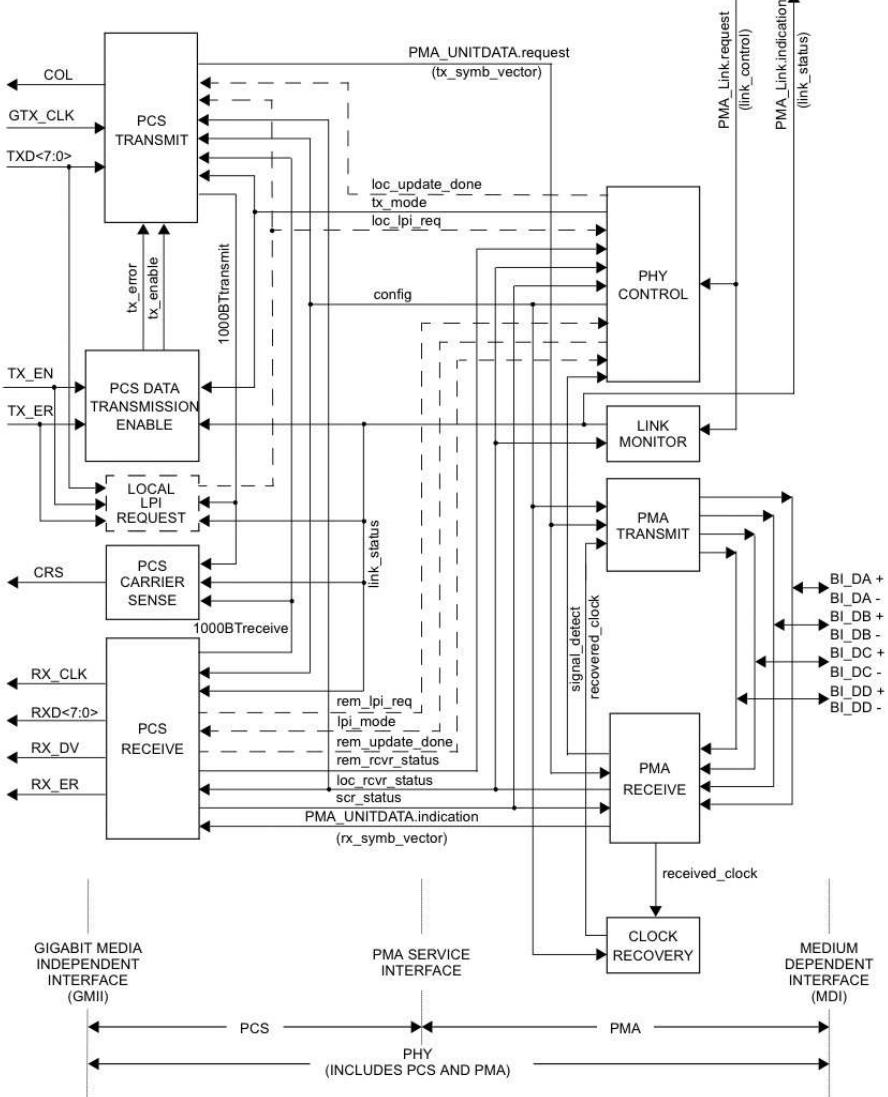
PMA = PHYSICAL MEDIUM ATTACHMENT

PHY = PHYSICAL LAYER DEVICE

\*GMII is optional.

Figure 40-1—Type 1000BASE-T PHY relationship to the ISO Open Systems Interconnection (OSI) Reference Model and the IEEE 802.3 CSMA/CD LAN Model

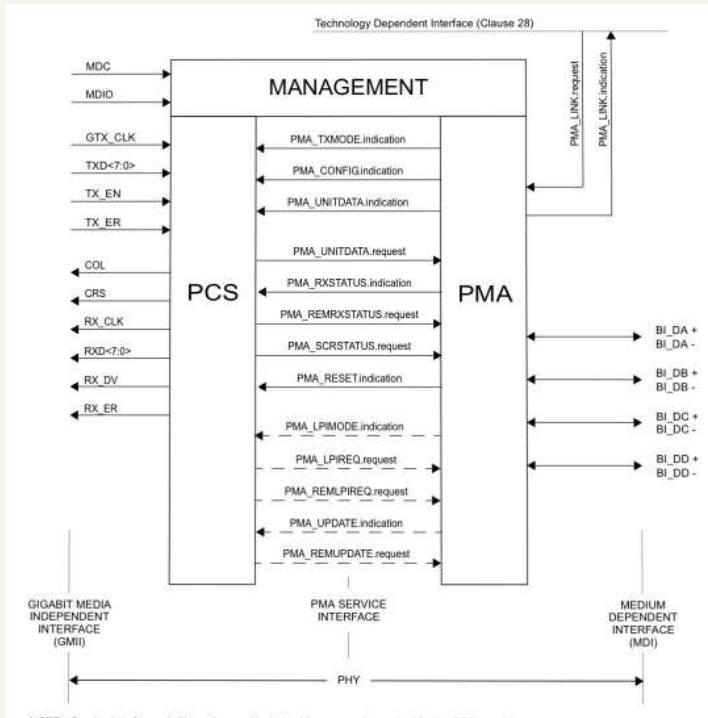
1. PCS层每8个bit从GMII接口过来，转换成4个{-2,-1,0,+,+v} (回)
  2. PCS层在encoding之前会做scrambling。
  3. MVE, SSP, carrier extend 和其他消息编码方式不一样。
  4. 编码书中，数据会填入  $S_{Xn}[3:0]$ ,  $S_{Yn}[3:0]$ ,  $S_{gn}[3:0]$ , 而以上这些会填入 quinary symbols
  5. 护码初始化状态不等于10
  6. master 和 slave 有差异，护码的模式不一样
- $$\left\{ \begin{array}{l} q(x) \text{ 表示} \\ H + x^{13} + x^{33} \text{ master} \\ 1 + x^{20} + x^{33} \text{ slave} \end{array} \right.$$



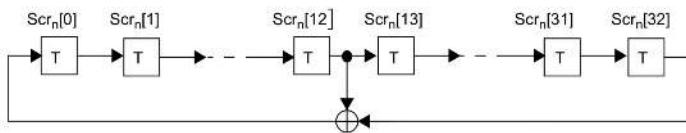
NOTE—The recovered\_clock arc is shown to indicate delivery of the received clock signal back the PMA TRANSMIT for loop timing

NOTE—Signals and functions shown with dashed lines are only required for the EEE capability.

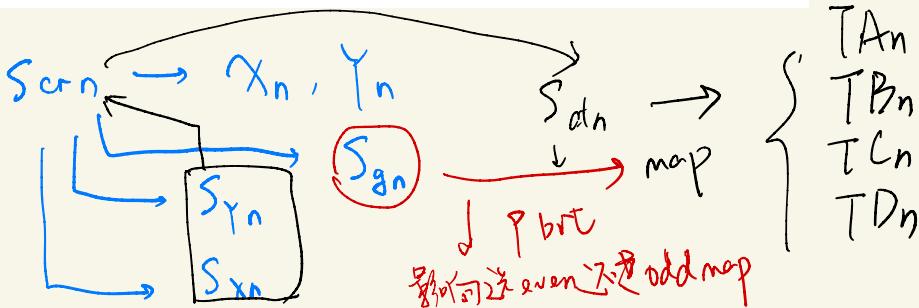
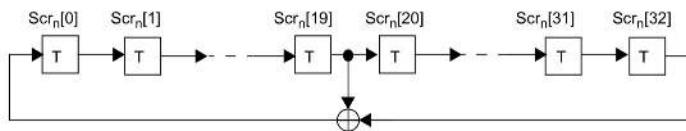
Figure 40–3—Functional block diagram



Side-stream scrambler employed by the MASTER PHY



Side-stream scrambler employed by the SLAVE PHY



SSD 为 1 时 Tx\_enable<sub>n</sub> & !Tx-enable<sub>n-2</sub>

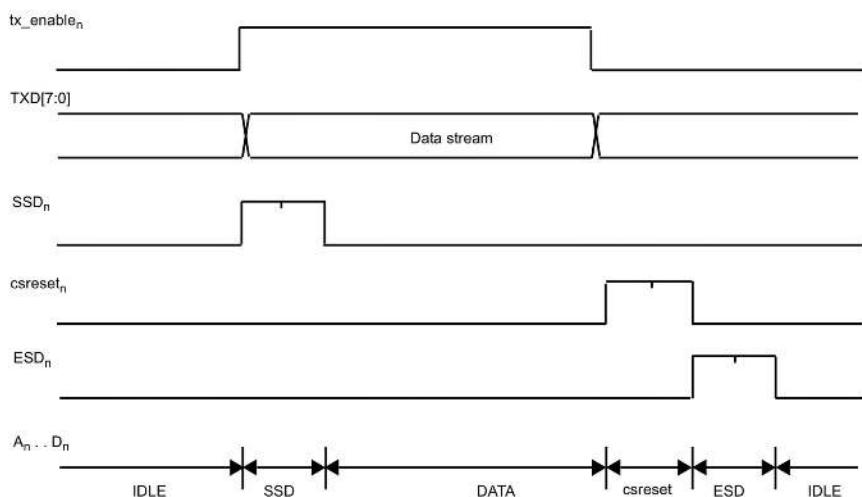


Figure 40-13—PCS sublayer to PMA timing

pMIX

1. 1000BASE-T 中 PMA 层面并没有 PMP，直接与物理层相连。

MDI.

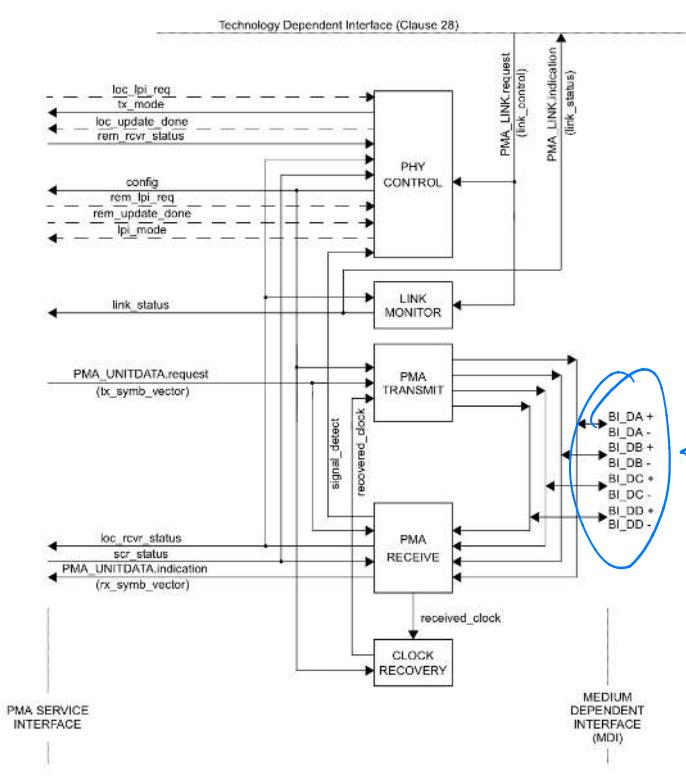
2. pMA: PHY control, pMA transmit, pMA receive,  
link monitor, clock recovery.

3. 1000BASE-T 不要求 error-free.  $e^{-10}$

4. TRAINING 在发送的是 IDLE

5. 必须将消息到 remote 并且必须 OK. 则可以到 IDLE

b. UPS 的 SEND-Z, 从 UPD 拿到的值不是这个  
重新 training



NOTE 1—The recovered clock arc is shown to indicate delivery of the received clock signal back the PMA TRANSMIT for loop timing.

**NOTE 2—**Signals and functions shown with dashed lines are only required for the FFF capability.

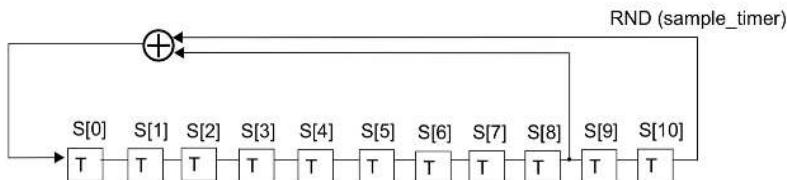


Table 40-4—1000BASE-T Base and Next Pages bit assignments

Bit	Bit definition	Register location
<b>Base Page</b>		
D15	1 (to indicate that Next Pages follow)	
D14:D1	As specified in 28.2.1.2	Management register 4
<b>PAGE 0 (Message Next Page)</b>		
M10:M0	8	
<b>PAGE 1 (Unformatted Next Page)</b>		
U10:U5	Reserved transmit as 0	
U4	1000BASE-T half duplex (1 = half duplex and 0 = no half duplex)	GMII register 9.8 (MASTER-SLAVE Control register)
U3	1000BASE-T full duplex (1 = full duplex and 0 = no full duplex)	GMII register 9.9 (MASTER-SLAVE Control register)
U2	1000BASE-T port type bit (1 = multiport device and 0 = single-port device)	GMII register 9.10 (MASTER-SLAVE Control register)
U1	1000BASE-T MASTER-SLAVE Manual Configuration value (1 = MASTER and 0 = SLAVE.) This bit is ignored if 9.12 = 0.	GMII register 9.11 (MASTER-SLAVE Control register)
U0	1000BASE-T MASTER-SLAVE Manual Configuration Enable (1 = Manual Configuration Enable.) This bit is intended to be used for manual selection in a particular MASTER-SLAVE mode and is to be used in conjunction with bit 9.11.	GMII register 9.12 (MASTER-SLAVE Control register)
<b>PAGE 2 (Unformatted Next Page)</b>		
U10	1000BASE-T MASTER-SLAVE Seed Bit 10 (SB10) (MSB)	MASTER-SLAVE Seed Value (10:0)
U9	1000BASE-T MASTER-SLAVE Seed Bit 9 (SB9)	
U8	1000BASE-T MASTER-SLAVE Seed Bit 8 (SB8)	
U7	1000BASE-T MASTER-SLAVE Seed Bit 7 (SB7)	
U6	1000BASE-T MASTER-SLAVE Seed Bit 6 (SB6)	
U5	1000BASE-T MASTER-SLAVE Seed Bit 5 (SB5)	
U4	1000BASE-T MASTER-SLAVE Seed Bit 4 (SB4)	
U3	1000BASE-T MASTER-SLAVE Seed Bit 3 (SB3)	
U2	1000BASE-T MASTER-SLAVE Seed Bit 2 (SB2)	
U1	1000BASE-T MASTER-SLAVE Seed Bit 1 (SB1)	
U0	1000BASE-T MASTER-SLAVE Seed Bit 0 (SB0)	
<b>PAGE 3 (Message page)</b>		
M10:M0	10	
<b>PAGE 4 (Unformatted Next Page)</b>		
U10:U3	As specified in 45.2.7.13.	
U2	1000BASE-T EEE (1 = EEE is supported for 1000BASE-T, 0 = EEE is not supported for 1000BASE-T.)	Management register 7.60. <sup>24</sup>
U1:U0	As specified in 45.2.7.13.	

1. 正常 BASE-PAGE + Formatted next PAGE + 17T unformatted next PAGE

2. master-store-and-forward - 3T  
softWare (Section 3.27)

1000BASE-X 的 T 周期  
而為 17T 而

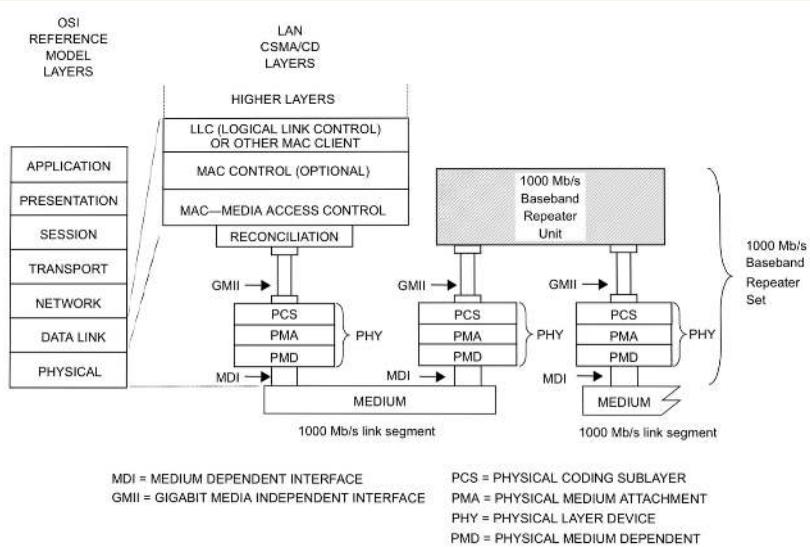
$$TX \text{ jitter } \rightarrow 125 \text{ MHz} \pm 0.01\%, \quad 0.01\% = 1 \times 10^{-4} = \frac{100}{10^6}$$

$$= 100 \text{ ppm.}$$

Table 40-12—Assignment of PMA signal to MDI and MDI-X pin-outs

Contact	MDI	MDI-X
1	BI_DA+	BI_DB+
2	BI_DA-	BI_DB-
3	BI_DB+	BI_DA+
4	BI_DC+	BI_DD+
5	BI_DC-	BI_DD-
6	BI_DB-	BI_DA-
7	BI_DD+	BI_DC+
8	BI_DD-	BI_DC-

MDI  $\Rightarrow$  GMII bit by bit line  
delay, not 3T, not 17T  
下圖



1. repeater 收到的包会转发至所有口(除收到的口)

1. 10G 及以后的速率只支持全双工。  
 2. 使用 XGMII  
 3. 只要是对称的接口，帧都要有带标记。

4. RJ45 端口看作是中继端，即甲  
 标准的 MAC / PLU 映射逻辑与  
 对称的 MII 接口做 Mapping.

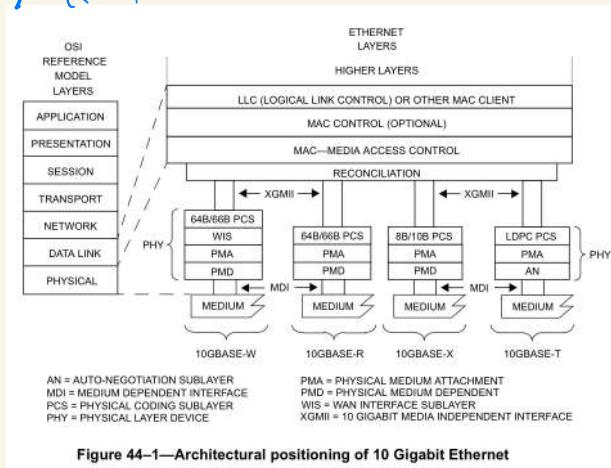


Figure 44-1—Architectural positioning of 10 Gigabit Ethernet

Table 44-1—Nomenclature and clause correlation

Nomenclature	Clause										
	48	49	50	51	52	53	54	55	68		
8B/10B PCS & PMA	M <sup>a</sup>										
64B/66B PCS			WIS	Serial PMA	850 nm Serial PMD	1310 nm Serial PMD	1550 nm Serial PMD	1310 nm WDM PMD	4-4 lane electrical PMD	Twisted-pair PCS & PMA	1310 nm Serial MMF PMD
10GBASE-SR	M										
10GBASE-SW	M	M	M	M							
10GBASE-LX4	M										
10GBASE-CX4	M										
10GBASE-LR	M		M		M						
10GBASE-LW	M	M	M		M						
10GBASE-ER	M		M			M					
10GBASE-ERW	M	M	M			M					
10GBASE-T							M				
10GBASE-LRM	M		M							M	

<sup>a</sup>M = Mandatory

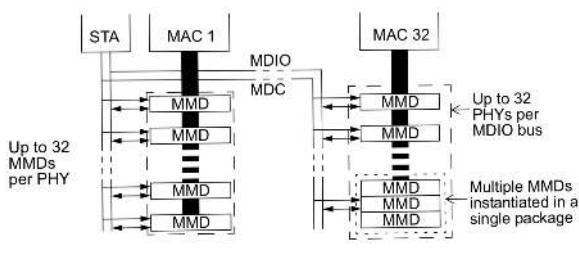


Figure 45-1—DTE and MMD devices

clause 22 - ST=1  
clause 45 - ST=0

Table 45-1—MDIO Manageable Device addresses

Device address	MMD name
0	Reserved
1	PMA/PMD
2	WIS
3	PCS
4	PHY XS
5	DTE XS
6	TC

Table 45-1—MDIO Manageable Device addresses (continued)

Device address	MMD name
7	Auto-Negotiation
8	Separated PMA (1)
9	Separated PMA (2)
10	Separated PMA (3)
11	Separated PMA (4)
12 through 28	Reserved
29	Clause 22 extension
30	Vendor specific 1
31	Vendor specific 2

Table 45-3—PMA/PMD registers

Register address	Register name	Subclause
1.0	PMA/PMD control 1	45.2.1.1
1.1	PMA/PMD status 1	45.2.1.2
1.2, 1.3	PMA/PMD device identifier	45.2.1.3
1.4	PMA/PMD speed ability	45.2.1.4
1.5, 1.6	PMA/PMD devices in package	45.2.1.5
1.7	PMA/PMD control 2	45.2.1.6
1.8	PMA/PMD status 2	45.2.1.7
1.9	PMA/PMD transmit disable	45.2.1.8
1.10	PMD receive signal detect	45.2.1.9
1.11	PMA/PMD extended ability	45.2.1.10
1.12	10G-EPON PMA/PMD ability	45.2.1.11
1.13	40GbE(RJ45) PMA/PMD extended ability	45.2.1.12
1.14, 1.15	PMA/PMD package identifier	45.2.1.13
1.16	FEC capability	45.2.1.14
1.17 through 1.29	Reserved	
1.30	10P2B PMA/PMD control	45.2.1.15
1.31	10P2B PMA/PMD status	45.2.1.16
1.32	10P2B link partner PMA/PMD control <sup>a</sup>	45.2.1.17
1.33	10P2B link partner PMA/PMD status <sup>a</sup>	45.2.1.18
1.34, 1.35	Reserved	
1.36	10P2B link loss counter	45.2.1.19
1.37	10P2B RX SNR margin	45.2.1.20
1.38	10P2B link partner RX SNR margin <sup>b</sup>	45.2.1.21
1.39	10P2B line attenuation	45.2.1.22
1.40	10P2B link partner line attenuation <sup>b</sup>	45.2.1.23
1.41	10P2B line quality thresholds	45.2.1.24
1.42	38 link partner line quality threshold <sup>b</sup>	45.2.1.25
1.43	10P FEC correctable errors counter	45.2.1.26
1.44	10P FEC uncorrectable errors counter	45.2.1.27
1.45	10P link partner FEC correctable errors <sup>c</sup>	45.2.1.28
1.46	10P link partner FEC uncorrectable errors <sup>c</sup>	45.2.1.29
1.47	10P electrical length	45.2.1.30
1.48	10P link partner electrical length <sup>c</sup>	45.2.1.31

↓  
1.48 的意思為 MMD 1 (P device addr)  
for register 48

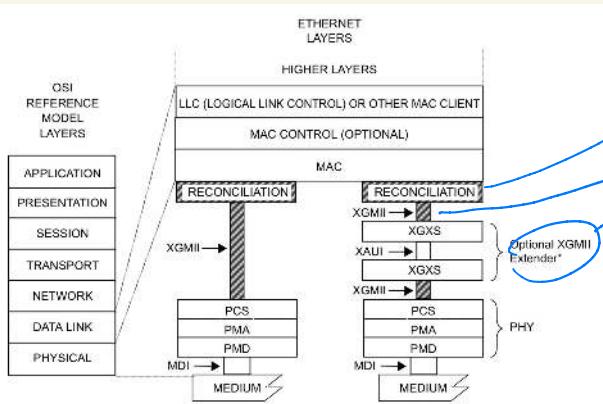


Figure 46-1—XGMII relationship to the ISO/IEC Open Systems Interconnection (OSI) reference model and the IEEE 802.3 Ethernet model

1. XGMII, bit<sup>10</sup> chip to chip 间距离, 可以通过插入到ASIC内部来增加  
上层模块的带宽
2. 只支持10G
3. 10 BASE-X, -R 为 MAC 层 10G, -L 为 MAC 层 P. PJ328.

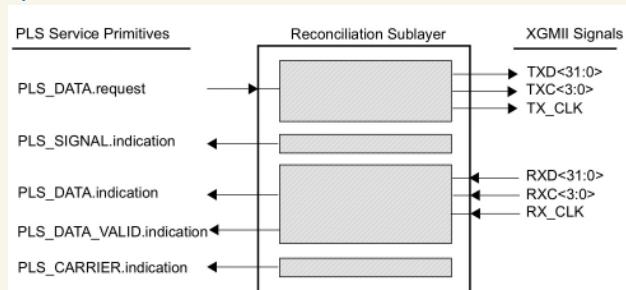


Figure 46-2—Reconciliation Sublayer (RS) inputs and outputs

Table 46-2—Transmit and receive lane associations

TXD RXD	TXC RXC	Lane
<7:0>	<0>	0
<15:8>	<1>	1
<23:16>	<2>	2
<31:24>	<3>	3

Frame 从 Lane 0 传输到 Lane 3  
再返回到 Lane 0

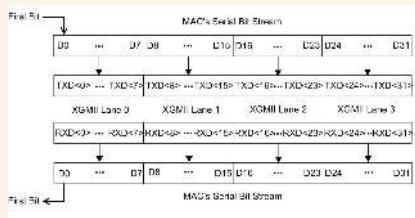
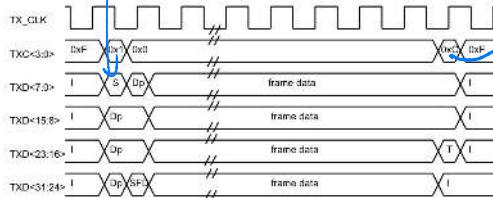


Figure 46-4—Relationship of data lanes to MAC serial bit stream

Table 46-3—Permissible encodings of TXC and TXD

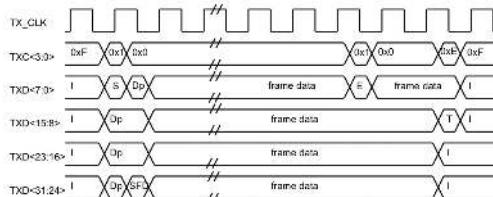
TXC	TXD	Description	PLS_DATA.request parameter
0	00 through FF	Normal data transmission	ZERO, ONE (eight bits)
1	00 through 05	Reserved	—
1	06	Only valid on all four lanes simultaneously in request LPI	No applicable parameter (normal interframe)
1	07	Idle	No applicable parameter (Normal after-frame)
1	08 through 9B	Reserved	—
1	9C	Sequence (only valid in lane 0)	No applicable parameter (inter-frame status signal)
1	9D through FA	Reserved	—
1	FB	Start (only valid in lane 0)	No applicable parameter, replaces first eight ZERO, ONE of a frame (preamble octet)
1	FC	Reserved	—
1	FD	Terminate	DATA_COMPLETE
1	FE	Transmit error propagation	No applicable parameter
1	FF	Reserved	—

NOTE—Values in TXD column are in hexadecimal, most significant bit to least significant bit (i.e., <2><0>).



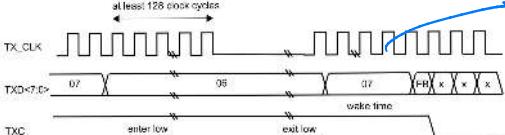
I: Idle control character, S: Start control character, Dp: preamble Data octet, T: Terminate control character.

Figure 46-5—Normal frame transmission



I: Idle control character, S: Start control character, Dp: preamble Data octet, T: Terminate control character, E: Error control character.

Figure 46-6—Transmit Error Propagation



NOTE—TXC and TXD are shown for one lane, all four lanes behave identically during LPI.

Figure 46-7—LPI transition

1. 不同于前段 MII 撇加，XGMII 是上开沿和下降沿采样

2. CLK 频率为 156.25 MHz

$$(156.25 \times 2 \times 32) = 1G$$

3. MII, GMII 同 TX-BN，且只同半发 DATA，XGMII 增加了主动探查，TXC 探测到 TXD<31:0> 变化后会调整 TX\_FRAME。图 4-7  
4. RS 会调整 TX\_FRAME，图 4-8  
preamble assignment Lane 0

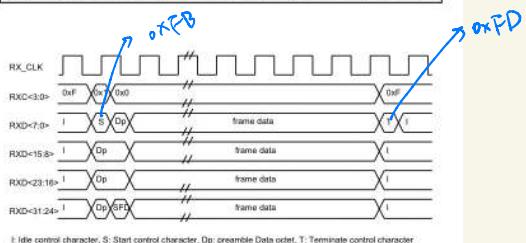
→ TXC = 1100 表示 TXD<31:16> 是 control，  
TXD<15:0> 是数据

Table 46-4—Permissible lane encodings of RXD and RXC

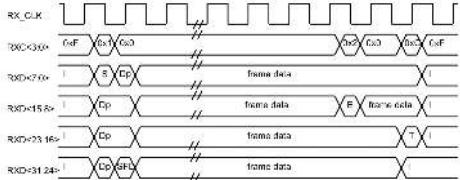
RXC	RXD	Description	PLS_DATA.indication parameter
0	00 through FF	Normal data reception	ZERO, ONE (eight bits)
1	00 through 05	Reserved	—
1	06	Only valid on all four lanes simultaneously to indicate LP_IDLE is asserted	No applicable parameter (Nominal interface)
1	07	Idle	No applicable parameter (Nominal inter-frame)
1	08 through 9B	Reserved	—
1	9C	Sequence (only valid in lane 0)	No applicable parameter (Inter-frame status signal)
1	9D through FA	Reserved	—
1	FB	Start (only valid in lane 0)	No applicable parameter, first eight ZERO, ONE of a frame (a preamble octet)
1	FC	Reserved	—
1	FD	Terminate	No applicable parameter (Start of inter-frame)
1	FE	Receive error	No applicable parameter
1	FF	Reserved	—

NOTE—Values in RXD column are in hexadecimal, most significant bit is least significant bit (i.e., <7>0<).

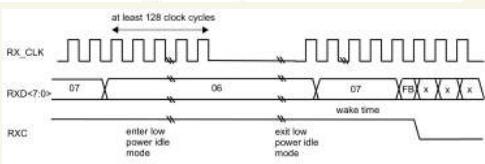
NOTE.—Values in RXD column are in hexadecimal, most significant bit to least significant bit (e.g., <7>(0)).



**Figure 46-8—Basic frame reception**



**Figure 46-9—** Reception with error



NOTE 1—RXC and RXD are shown for one lane; all 4 lanes behave identically during LP1.

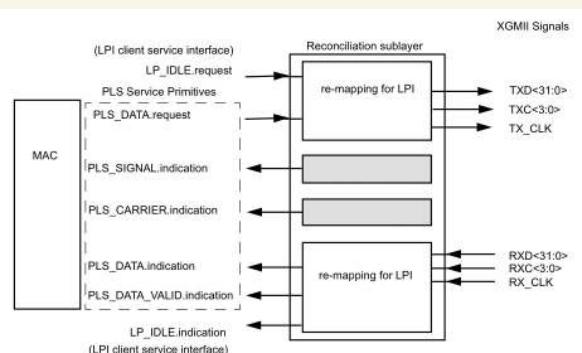
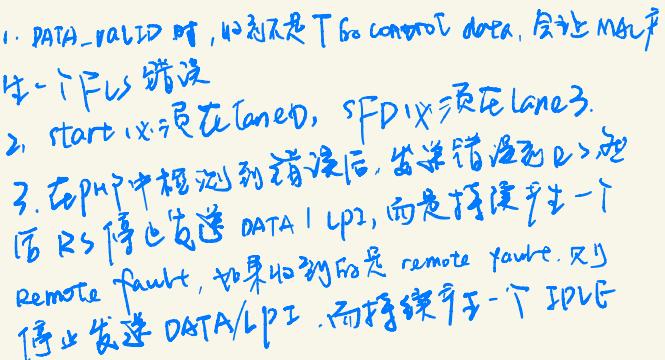
NOTE 2.—In some instances, LPI may be followed by characters other than IDLE during wake time.

Figure 46-10—LPI transition

Table 46-5—Sequence ordered sets

Lane 0	Lane 1	Lane 2	Lane 3	Description
Sequence	0x00	0x00	0x00	Reserved
Sequence	0x00	0x00	0x01	Local Fault
Sequence	0x00	0x00	0x02	Remote Fault
Sequence	0x00	0x00	0x03	Link Interruption
Sequence	≥ 0x00	≥ 0x00	≥ 0x04	Reserved

**NOTE**—Values in Lane 1, Lane 2, and Lane 3 columns are in hexadecimal, most significant bit to least significant bit (i.e., <0:0>). The link fault signaling state diagram allows future standardization of reserved Sequence ordered sets for functions other than link fault indications.



**Figure 46–12—LPI assertion and detection mechanism**

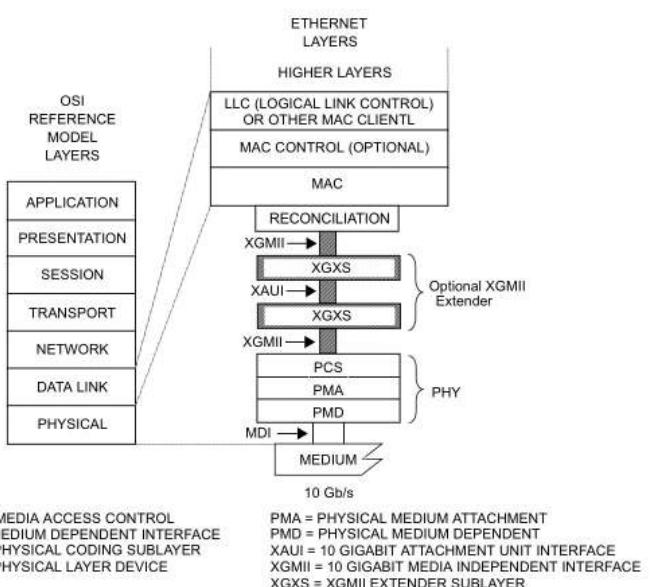


Figure 47-1—XAUI and XGXS relationship to the ISO/IEC Open Systems Interconnection (OSI) reference model and the IEEE 802.3 Ethernet model

1. 主要给 chip-to-chip 使用。XAUI 的距离为 7cm，扩展后为 50cm。
2. XGMII 由 8Tbit 组成 1 channel。每个 XGXS 有 8B/10B 编码组成串行流，只有 4T Lane，8T Lane  $(2.5G \times 10 / 8 = 3.125G)$
3. 共有 16T 速率：

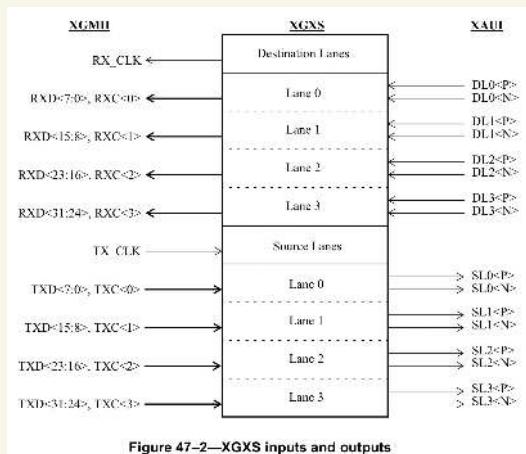


Figure 47-2—XGXS inputs and outputs

10G BASE-X 包括 10GBASE-CX4, KX4, LX4

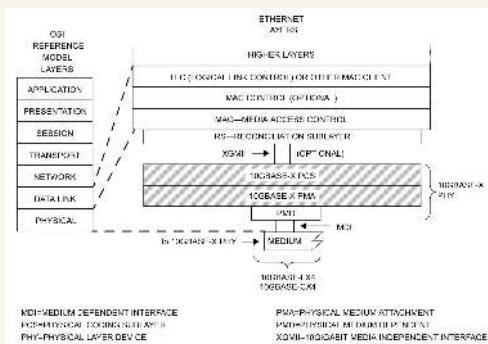


Figure 48-1—10GBASE-X PCS and PMA relationship to the ISO/IEC Open Systems Interconnection (OSI) reference model and the IEEE Ethernet Model

1. XGMII 10GBASE-X

2. PCS 层 — XGMII 32 bus + Y control → 10 Port group per

4 lanes.

3. PMA 层 — 速率化和解串

4. PMD 层 — 发送数据

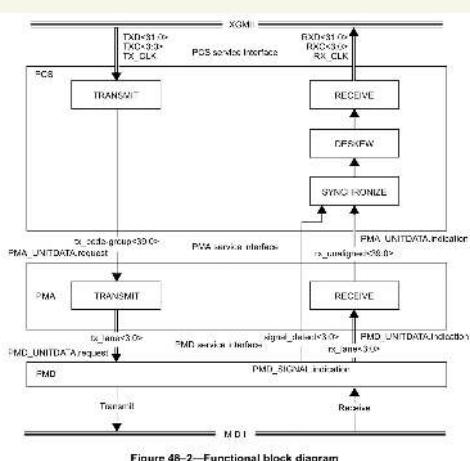


Figure 48-2—Functional block diagram

5. 从 PMA 来的数据是 unaligned, PCS 同步进 4 线 Time

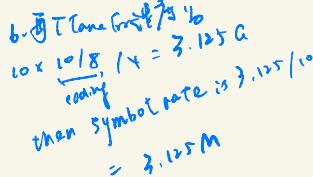
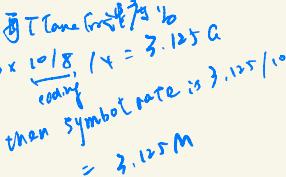
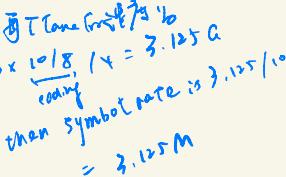
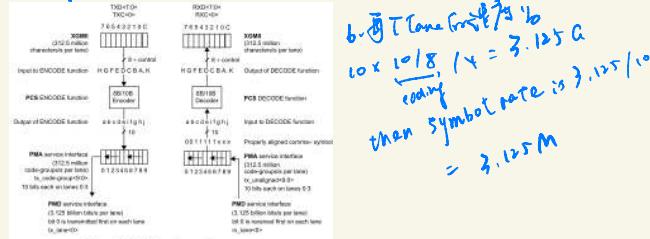
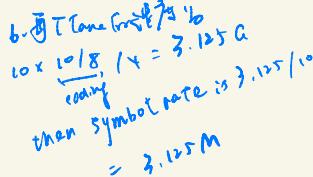


Figure 48-3—PCS reference diagram



#### 4.8.1 Special symbols

- The code-groups x is represented by preceding and following slash characters.  
 Four code groups, one exit in lines 0 through 3 inclusive, synonymous to each other and arranged in a column identified by the value x, is represented by preceding and following double bar characters.

Table 48-2—XGMII character to PCS code-group mapping

XGMII TSC	XGMII TDX	PCS code-group	Description
0	00 through FF	Discard	Normal idle transmission
1	00	K24 # 0 or K23.3 or K23.5 or K23.7	Asset ID#
1	07	K24 # or K23.3 or K23.5	Idle in [0]
1	0F	K23.5	Idle in [1]
1	3C	K23.4	Separate
1	FF	K23.3	Start
1	FD	K23.7	Terminate
1	FE	K23.8	Final
1	Other value in Table 48-3	See Table 48-3	Received XGMII character
1	Any other value	K23.7	Invalid XGMII character
NOTE—Values in XGMII scheme are as described in 4.8.2.2.			

NOTE—Values in PCS scheme are as described in 4.8.2.2.

Table 48-3—PCS code-group to XGMII character mapping

XGMII TSC	XGMII TDX	PCS code-group	Description
0	00 through FF	Discard	Normal data reception
1	00	K24 # or K23.3 or K23.5 or K23.7	Asset ID#
1	0F	K24 # or K23.3 or K23.5	Idle in [0]
1	07	K23.5	Idle in [1]
1	3C	K23.4	Separate
1	FF	K23.3	Start
1	FD	K23.7	Terminate
1	FE	K23.8	Final
1	Other value in Table 48-3	See Table 48-3	Received XGMII character
1	Any other value	K23.7	Invalid XGMII character
NOTE—Values in PCS scheme are as described in 4.8.2.2.			

NOTE—Values in XGMII scheme are as described in 4.8.2.2.

Table 48-4—Defined ordered sets and special code-groups

Code	Ordered set	Number of code-groups	Encoding
[R]	idle	4	Substitute for XGMII idle
[S]	Sync column	4	K23.3/K23.5/K23.5/K23.5
[S]	Sync row	4	K23.3/K23.5/K23.5/K23.5
[S]	Align column	4	K23.3/K23.5/K23.5/K23.5
[E]	Start column	4	K23.2/K23.6/K23.6/K23.6
[T]	Transmit current	4	Terminate code-group by timer
[T]	Transmit in Line 0	4	K23.2/K23.6/K23.6/K23.6
[T]	Transmit in Line 1	4	K23.2/K23.6/K23.6/K23.6
[T]	Transmit in Line 2	4	K23.2/K23.6/K23.6/K23.6
[T]	Transmit in Line 3	4	K23.2/K23.6/K23.6/K23.6
[C]	Control	1	
[P]	Proceed random	1	K23.2
[L]	Link status	1	
[Q]	Sync once (fixed set)	4	K23.4/K23.5/K23.5/K23.5
[U]	Loss Full status	4	K23.4/K23.6/K23.6/K23.6
[R]	Remote Fault signal	4	K23.4/K23.6/K23.6/K23.6
[LNT]	Link Interruption signal	4	K23.4/K23.6/K23.6/K23.6
[Rwd]	Reserved	4	[idle] and [T1] and [LNT]
[Fwd]	Start ordered set	4	K23.2/K23.6/K23.6/K23.6

NOTE—Values in PCS scheme are as described in 4.8.2.2.  
 Reserved for XGMII TSC.

NOTE—Values in XGMII scheme are as described in 4.8.2.2.

1. IDLE pattern —  $\overline{A_3 A_2 A_1 A_0}$ , K, R, A

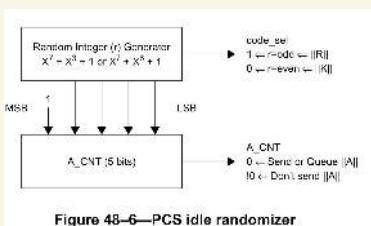


Figure 48-6—PCS idle randomizer

4. R 向下时钟补偿

通过插入/删除 IDLE，当低于时钟插入 IDLE

5. PLS 变到 [IT] 时认为是 PCS 的开销

b. PLS-RX 有两种模式：DATA mode 和 IPDV mode

$42.3^\circ \text{ ! } [IT]$

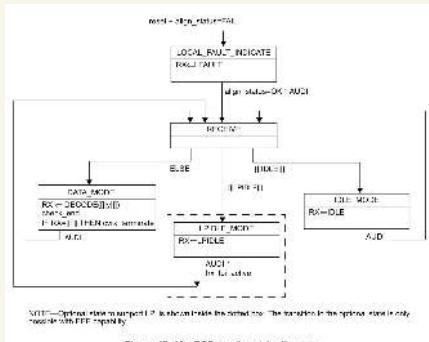


Figure 48-10—PCS receive state diagram

2. K 固定同步 code-group

边界

3. A/R/T/F desktop tones, 音频  
 rtwk 是 41.01.27.255.16  
 $10^{-10} \times 3 \times 10^8 \times 0.6 = 0.018\%$   
 >1.8 cm

$42.3^\circ \text{ ! }$

7. PLS 指示要 VLP-SYNC 和 ALIAN

AN

4.2.3.1. 会议控制  
 XGMII IPDV control  
 从 XGMII 到 XGMII

8. 10Gb BASE-KX4 PMD 要求有

P. LOGBASE-X 的 PMA 不负责对  $\exists$  code-group.

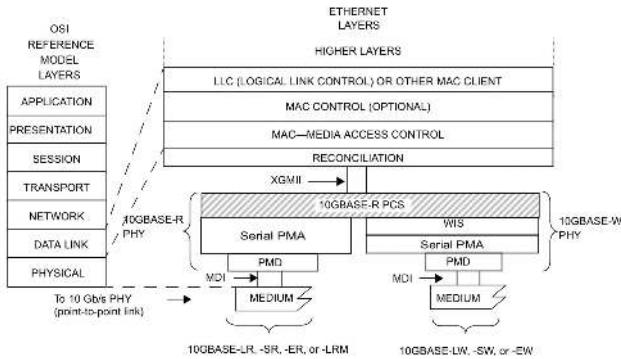
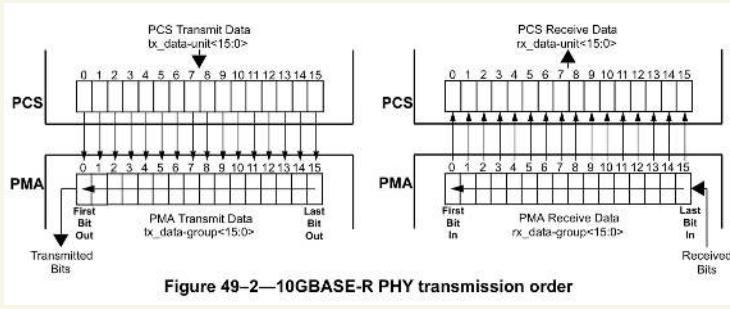


Figure 49-1—10GBASE-R PCS relationship to the ISO/IEC Open Systems Interconnection (OSI) reference model and IEEE 802.3 Ethernet model

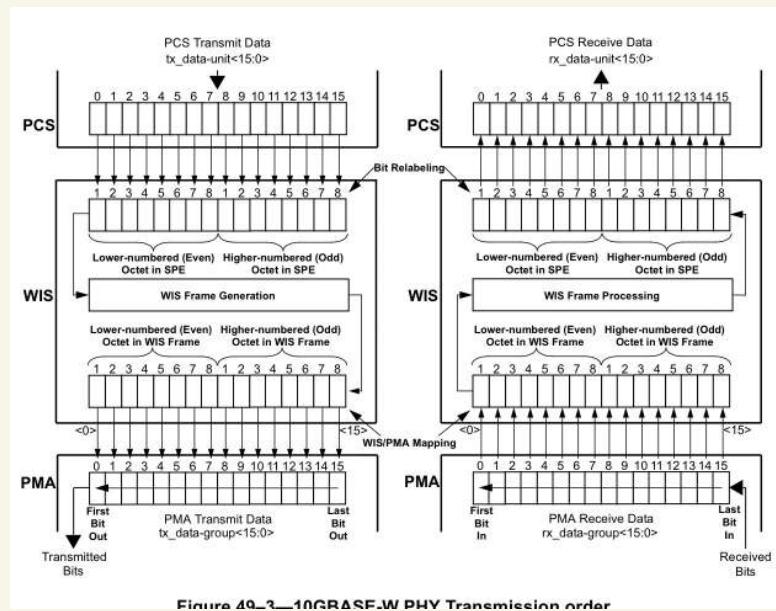
10G BASE - SR  
 10G BASE - LR  
 10G BASE - ER  
 10G BASE - W  
 10G BASE - SW  
 10G BASE - LW  
 10G BASE - EW

1. 64/66 编码
  2. → (from PMA, 16 Tbit)
  3. 通过 WDM, MMF 译码
  4. trunk status
- } → PCS

1. PCS → PMA
  2. 串行化
  3. 光纤收发
  4. PMA → PMD
  5. 环回接收
- } → PMD



SONET网的比特序列为大端 (MSB → LSB)，以太网的字节序为小端 (LSB → MSB)



$$\begin{aligned}
 \text{PMA 速率} &= \\
 10G \times 6b / 64 &\quad 1/b \\
 &= b(40.5) M
 \end{aligned}$$

PUS层可提供PBM的功能（直接连PMA）

#### 49.1.6 Functional block diagram

Figure 49-4 provides a functional block diagram of the 10GBASE-R PHY.

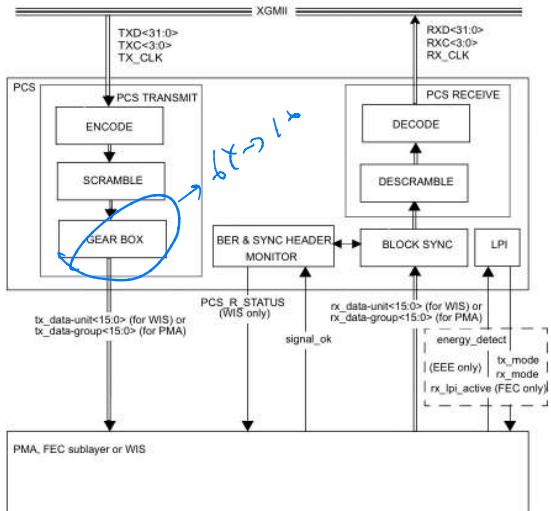


Figure 49-4—Functional block diagram

b416b 在 R 中，头两个 bit 表示数据包 (01) 或者数据包 (10)，中间部分为帧同步。

Input Data	Sync	Block Payload									
Bit Position:	0 1	2									65
Data Block Format:	D <sub>0</sub> D <sub>1</sub> D <sub>2</sub> D <sub>3</sub> /D <sub>4</sub> D <sub>5</sub> D <sub>6</sub> D <sub>7</sub>	01	D <sub>0</sub>	D <sub>1</sub>	D <sub>2</sub>	D <sub>3</sub>	D <sub>4</sub>	D <sub>5</sub>	D <sub>6</sub>	D <sub>7</sub>	
Control Block Formats:	C <sub>0</sub> C <sub>1</sub> C <sub>2</sub> C <sub>3</sub> /C <sub>4</sub> C <sub>5</sub> C <sub>6</sub> C <sub>7</sub>	10	0x1e	C <sub>0</sub>	C <sub>1</sub>	C <sub>2</sub>	C <sub>3</sub>	C <sub>4</sub>	C <sub>5</sub>	C <sub>6</sub>	C <sub>7</sub>
	C <sub>0</sub> C <sub>1</sub> C <sub>2</sub> C <sub>3</sub> /O <sub>4</sub> D <sub>5</sub> D <sub>6</sub> D <sub>7</sub>	10	0x2d	C <sub>0</sub>	C <sub>1</sub>	C <sub>2</sub>	C <sub>3</sub>	O <sub>4</sub>	D <sub>5</sub>	D <sub>6</sub>	D <sub>7</sub>
	C <sub>0</sub> C <sub>1</sub> C <sub>2</sub> C <sub>3</sub> /S <sub>4</sub> D <sub>5</sub> D <sub>6</sub> D <sub>7</sub>	10	0x33	C <sub>0</sub>	C <sub>1</sub>	C <sub>2</sub>	C <sub>3</sub>		D <sub>5</sub>	D <sub>6</sub>	D <sub>7</sub>
	O <sub>0</sub> D <sub>1</sub> D <sub>2</sub> D <sub>3</sub> /S <sub>4</sub> D <sub>5</sub> D <sub>6</sub> D <sub>7</sub>	10	0x66	D <sub>1</sub>	D <sub>2</sub>	D <sub>3</sub>	O <sub>0</sub>		D <sub>5</sub>	D <sub>6</sub>	D <sub>7</sub>
	O <sub>0</sub> D <sub>1</sub> D <sub>2</sub> D <sub>3</sub> /O <sub>4</sub> D <sub>5</sub> D <sub>6</sub> D <sub>7</sub>	10	0x55	D <sub>1</sub>	D <sub>2</sub>	D <sub>3</sub>	O <sub>0</sub>	O <sub>4</sub>	D <sub>5</sub>	D <sub>6</sub>	D <sub>7</sub>
	S <sub>0</sub> D <sub>1</sub> D <sub>2</sub> D <sub>3</sub> /D <sub>4</sub> D <sub>5</sub> D <sub>6</sub> D <sub>7</sub>	10	0x78	D <sub>1</sub>	D <sub>2</sub>	D <sub>3</sub>	D <sub>4</sub>		D <sub>5</sub>	D <sub>6</sub>	D <sub>7</sub>
	O <sub>0</sub> D <sub>1</sub> D <sub>2</sub> D <sub>3</sub> /C <sub>4</sub> C <sub>5</sub> C <sub>6</sub> C <sub>7</sub>	10	0x4b	D <sub>1</sub>	D <sub>2</sub>	D <sub>3</sub>	O <sub>0</sub>	C <sub>4</sub>	C <sub>5</sub>	C <sub>6</sub>	C <sub>7</sub>
	T <sub>0</sub> C <sub>1</sub> C <sub>2</sub> C <sub>3</sub> /C <sub>4</sub> C <sub>5</sub> C <sub>6</sub> C <sub>7</sub>	10	0x87		C <sub>1</sub>	C <sub>2</sub>	C <sub>3</sub>	C <sub>4</sub>	C <sub>5</sub>	C <sub>6</sub>	C <sub>7</sub>
	D <sub>0</sub> T <sub>1</sub> C <sub>2</sub> C <sub>3</sub> /C <sub>4</sub> C <sub>5</sub> C <sub>6</sub> C <sub>7</sub>	10	0x99	D <sub>0</sub>		C <sub>2</sub>	C <sub>3</sub>	C <sub>4</sub>	C <sub>5</sub>	C <sub>6</sub>	C <sub>7</sub>
	D <sub>0</sub> D <sub>1</sub> T <sub>2</sub> C <sub>3</sub> /C <sub>4</sub> C <sub>5</sub> C <sub>6</sub> C <sub>7</sub>	10	0xaa	D <sub>0</sub>	D <sub>1</sub>		C <sub>3</sub>	C <sub>4</sub>	C <sub>5</sub>	C <sub>6</sub>	C <sub>7</sub>
	D <sub>0</sub> D <sub>1</sub> D <sub>2</sub> T <sub>3</sub> /C <sub>4</sub> C <sub>5</sub> C <sub>6</sub> C <sub>7</sub>	10	0xb4	D <sub>0</sub>	D <sub>1</sub>	D <sub>2</sub>		C <sub>4</sub>	C <sub>5</sub>	C <sub>6</sub>	C <sub>7</sub>
	D <sub>0</sub> D <sub>1</sub> D <sub>2</sub> D <sub>3</sub> /T <sub>4</sub> C <sub>5</sub> C <sub>6</sub> C <sub>7</sub>	10	0xcc	D <sub>0</sub>	D <sub>1</sub>	D <sub>2</sub>	D <sub>3</sub>		C <sub>5</sub>	C <sub>6</sub>	C <sub>7</sub>
	D <sub>0</sub> D <sub>1</sub> D <sub>2</sub> D <sub>3</sub> /D <sub>4</sub> D <sub>5</sub> C <sub>6</sub> C <sub>7</sub>	10	0xd2	D <sub>0</sub>	D <sub>1</sub>	D <sub>2</sub>	D <sub>3</sub>	D <sub>4</sub>		C <sub>6</sub>	C <sub>7</sub>
	D <sub>0</sub> D <sub>1</sub> D <sub>2</sub> D <sub>3</sub> /D <sub>4</sub> D <sub>5</sub> T <sub>6</sub> C <sub>7</sub>	10	0xe1	D <sub>0</sub>	D <sub>1</sub>	D <sub>2</sub>	D <sub>3</sub>	D <sub>4</sub>	D <sub>5</sub>		C <sub>7</sub>
	D <sub>0</sub> D <sub>1</sub> D <sub>2</sub> D <sub>3</sub> /D <sub>4</sub> D <sub>5</sub> D <sub>6</sub> D <sub>7</sub>	10	0xff	D <sub>0</sub>	D <sub>1</sub>	D <sub>2</sub>	D <sub>3</sub>	D <sub>4</sub>	D <sub>5</sub>	D <sub>6</sub>	

Figure 49-7—64B/66B block formats

Control character	Notation	XGMII Control Code	10GBASE-R Control Code	10GBASE-R O Code	8B/10B Code <sup>a</sup>
idle	/U/	0x07	0x00		K28.0 or K28.3 or K28.5
LPI	/L/	0x06	0x06		K28.0 with D20.4 in same row or K28.3 or K28.5 with D20.5 in same row <sup>b</sup>
start	/S/	0x0b	Encoded by block type field		K27.7
terminate	/T/	0x0d	Encoded by block type field		K29.7
error	/E/	0x0e	0x1e		K30.7
Sequence ordered set	/Q/	0x9c	Encoded by block type field plus O code	0x0	K28.4
reserved0	/R/ <sup>c</sup>	0x1c	0x2d		K28.0
reserved1		0x3c	0x33		K28.1
reserved2	/A/	0x7c	0x6b		K28.3
reserved3	/K/	0xbc	0x55		K28.5

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IEEE Std 802.3-2015  
IEEE Standard for Ethernet  
SECTION FOUR

Table 49-1—Control codes (continued)

Control character	Notation	XGMII Control Code	10GBASE-R Control Code	10GBASE-R O Code	8B/10B Code <sup>a</sup>
reserved4		0xd6			K28.6
reserved5		0x7f	0x78		K23.7
Signal ordered set	/Fsig/	0x5c	Encoded by block type field plus O code	0xF	K28.2

<sup>a</sup>For information only. The 8B/10B code is specified in Clause 36. Usage of the 8B/10B code for 10 Gb/s operation is specified in Clause 48.

<sup>b</sup>See 48.2.4.1.

<sup>c</sup>The codes for /A/, /K/, and /R/ are used on the XAU1 interface to signal idle. They are not present on the XGMII when no errors have occurred, but certain bit errors cause the XGXS to send them on the XGMII.

<sup>d</sup>Reserved for INCITS T11 Fibre Channel use.

PCs 在 IDLE 时以  
组为 - 4 group of 4, 也  
就是 XGMII 4 bytes  
一起

1. 经过 b4/b6 编码后会变成码字 (头两个会直接 skip)  
PC 产生的 PRBS 是带 control header. 估计经过也会在  
PC (实际遇到的还是不带的)

2. 如果 PC 通过 loopback 了, 那么 loopback XGMII 的端口  
报文, 还会发送 0x00FF 到 PMA

3. 10GBASE-KR 支持 AN

10GBASE-SW, 10GBASE-LW, 10GBASE-EW

達 P.95328 Gb/s DWIS [2]

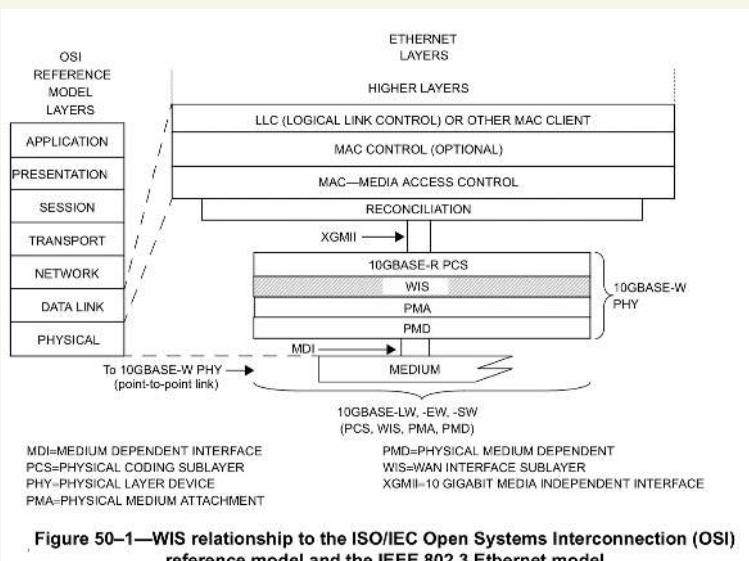


Figure 50-1—WIS relationship to the ISO/IEC Open Systems Interconnection (OSI) reference model and the IEEE 802.3 Ethernet model

#### 50.1.6 Functional block diagram

Figure 50-2 provides a functional block diagram of the WIS.

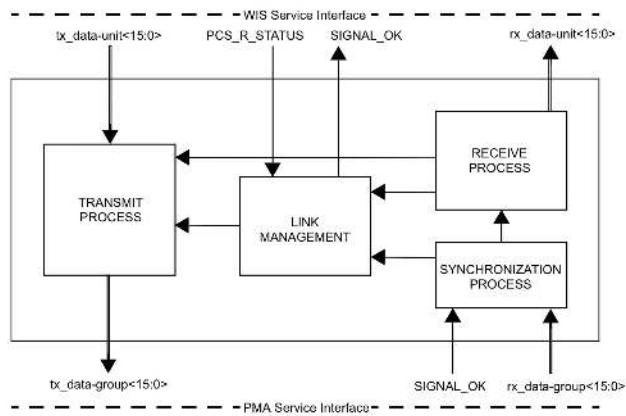


Figure 50-2—Functional block diagram

主要走大小端的流換

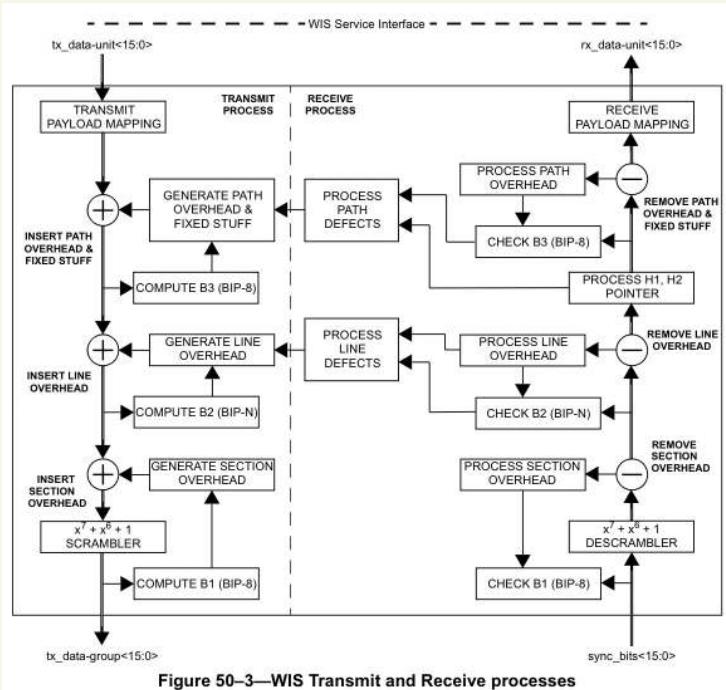
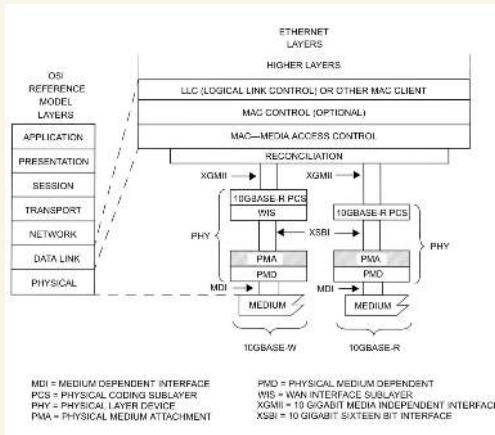


Figure 50–3—WIS Transmit and Receive processes



只在上升沿界线。

1. TX 方向:
    - a. 给 pma client 提供时钟.
    - b. 16bit 并口读行机
    - c. 发送行数据 PWD.
  2. RX 方向:
    - a. 时钟恢复
    - b. 42 古时钟给 pma client
    - c. 并行数据经 16bit 并口
    - d. 并口读取数据 pma client.
    - e. 提供 link status.

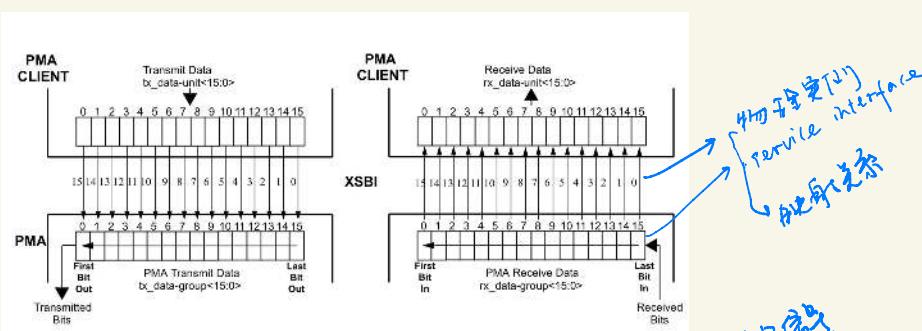


Figure 51–2—XSBI physical interface mapping into PMA service interface

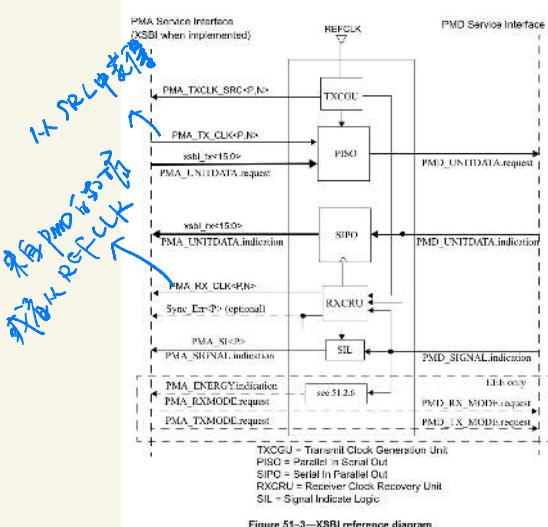
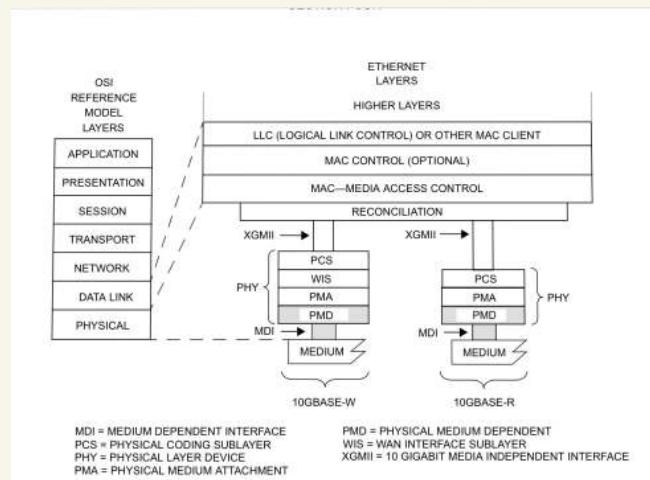


Figure 51-3—XSB1 reference diagram

**Table 52-1—10GBASE serial PHYs**

Name	Description
10GBASE-SR	850 nm serial LAN PHY
10GBASE-LR	1310 nm serial LAN PHY
10GBASE-ER	1550 nm serial LAN PHY
10GBASE-SW	850 nm serial WAN PHY
10GBASE-LW	1310 nm serial WAN PHY
10GBASE-EW	1550 nm serial WAN PHY



S → 多模光纤  
 L → 单模光纤 1310 nm  
 G → 单模光纤 1550 nm

Table 52–20—Pattern segments

Segments	Seed[57:0] <sup>a</sup>
$A_n$	0x3C8B44DCAB6804F
$B_n$	0x34906BD85A38884

<sup>a</sup>The “invert” segments  $A_i$  and  $B_i$  are generated using the inverted seeds for  $A_n$  and  $B_n$ , respectively.

Table 52–21—Test patterns

Pattern	Pattern for 10GBASE-R	Pattern for 10GBASE-W
1	$B_n B_i B_n B_i$	Mixed <sup>a</sup>
2	$A_n A_i A_n A_i$	
3	PRBS31 <sup>b</sup>	PRBS31 <sup>c</sup>

<sup>a</sup>The patterns for 10GBASE-W are defined in 50.3.8.

<sup>b</sup>This is the test-pattern checker defined in 49.2.12.

<sup>c</sup>This is the test-pattern checker defined in 50.3.8.2.

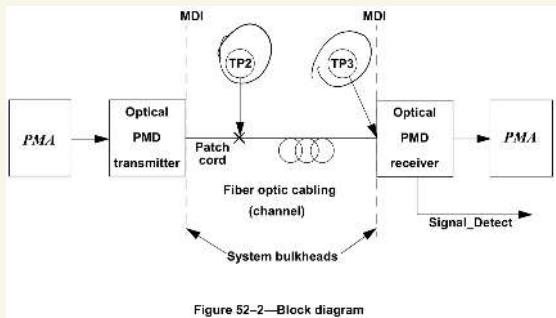


Figure 52–2—Block diagram

TP2: 发送端布线段测试点  
TP3: 接收端布线段测试点

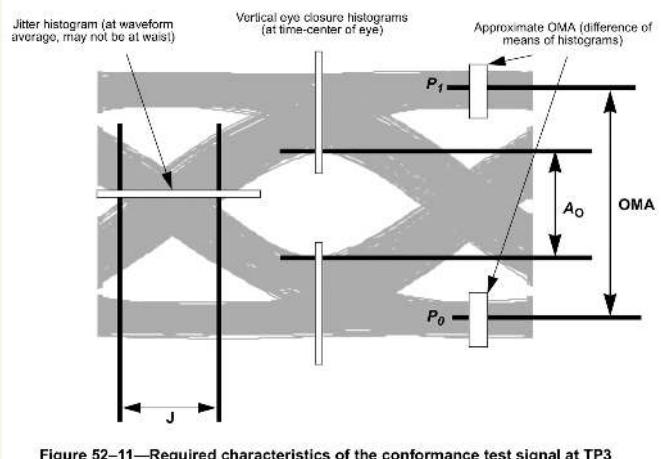
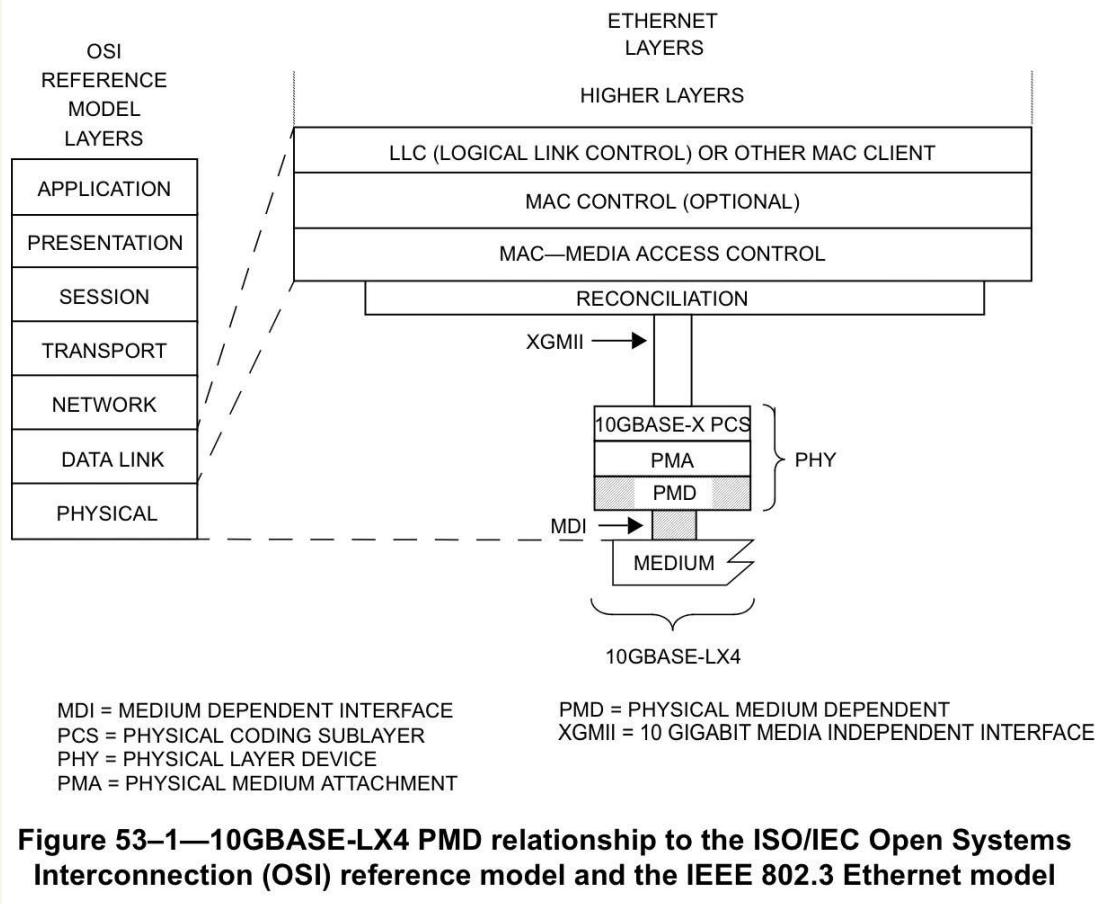
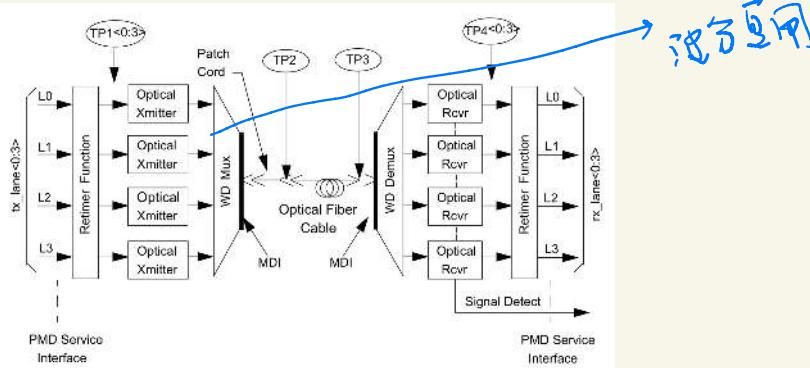


Figure 52–11—Required characteristics of the conformance test signal at TP3

10BASE-LX4 PMD 支持的模及單模光傳。



**Figure 53–1—10GBASE-LX4 PMD relationship to the ISO/IEC Open Systems Interconnection (OSI) reference model and the IEEE 802.3 Ethernet model**



WD = Wavelength Division

NOTE—Specification of the retimer function is beyond the scope of this standard; however, a retimer may be required to ensure compliance at test points TP2 and TP3.

Table 53–5—Wavelength-division-multiplexed lane assignments

Lane	Wavelength ranges	PMD Service Interface transmit bit stream	PMD Service Interface receive bit stream
L <sub>0</sub>	1269.0 – 1282.4 nm	tx_lane<0>	rx_lane<0>
L <sub>1</sub>	1293.5 – 1306.9 nm	tx_lane<1>	rx_lane<1>
L <sub>2</sub>	1318.0 – 1331.4 nm	tx_lane<2>	rx_lane<2>
L <sub>3</sub>	1342.5 – 1355.9 nm	tx_lane<3>	rx_lane<3>

10 µm single-mode fiber) according to the specifications defined in 53.14. A transceiver that exceeds the operational range requirement while meeting all other optical specifications is considered compliant (e.g., a single-mode solution operating at 10 500 m meets the minimum range requirement of 2 m to 10 000 m).

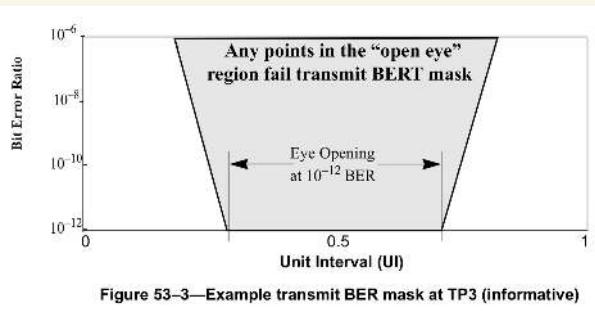
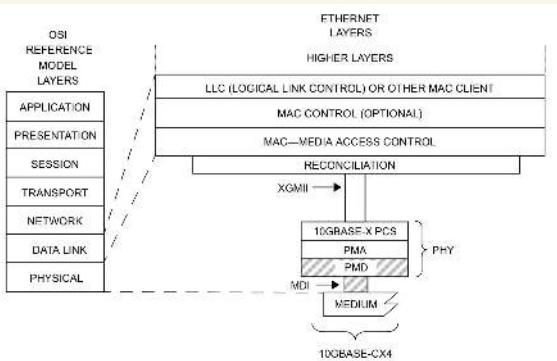


Figure 53–3—Example transmit BER mask at TP3 (informative)



MDI = MEDIUM DEPENDENT INTERFACE  
PCS = PHYSICAL CODING SUBLAYER  
PHY = PHYSICAL LAYER DEVICE  
PMA = PHYSICAL MEDIUM ATTACHMENT

Figure 54-1—10GBASE-CX4 PMD relationship to the ISO/IEC Open Systems Interconnection (OSI) reference model and the IEEE 802.3 Ethernet model

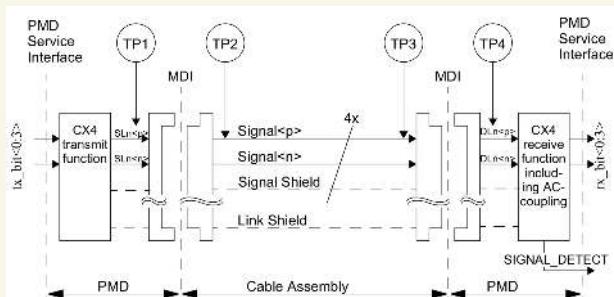


Figure 54-2—10GBASE-CX4 link (half link is shown)

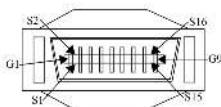


Figure 54-12—Example cable assembly plug (informative)

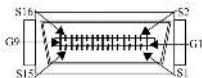


Figure 54-13—Example MDI board receptacle (informative)

4 組雙向信道，差分线

$$P - N > 0 \quad = = 1$$

AC-couple

点到点连接

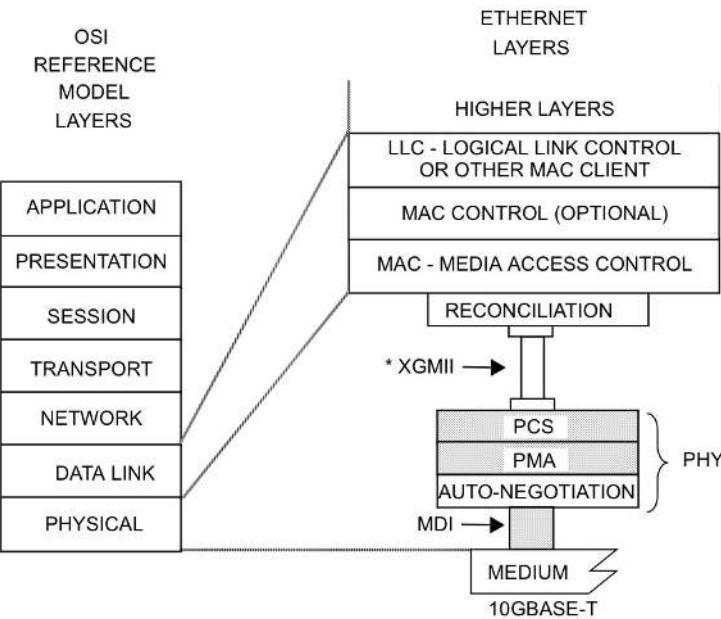
每个 lane 都是物理层

共 4 个 pairs x 2 个 lanes

2 点合 = 16 个连接

cross-over → 1 为 TX 1 为 RX

到 RX



MDI = MEDIUM DEPENDENT INTERFACE

XGMII = TEN GIGABIT MEDIA INDEPENDENT INTERFACE

PCS = PHYSICAL CODING SUBLAYER

PMA = PHYSICAL MEDIUM ATTACHMENT

PHY = PHYSICAL LAYER DEVICE

\*XGMII is optional.

**Figure 55-1—Type 10GBASE-T PHY relationship to the ISO Open Systems Interconnection (OSI) reference model and the IEEE 802.3 Ethernet model**

4条Lane，每条Lane 2500m，向PAM16编码码，每个PAM16  
含有3.125 bit信息。

正常retrans需要2秒，但有可选的fast retrans。  
10GBASE-T中的PCS层并不是8B/10B或者64/66B，而是2次XGMII共64bits，加上DATA/CONTROL[位移位]  
65B。每50个TR会加上CRL，即一大块为 $50 \times 65 + 8 = 3258$  bits，最后加上一个填充位，最后得到3259 bits  
(经过校验)

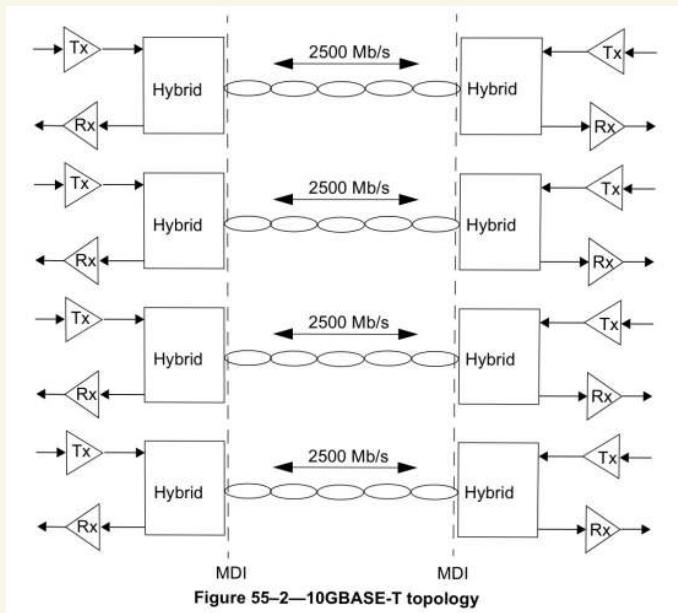


Figure 55-2—10GBASE-T topology

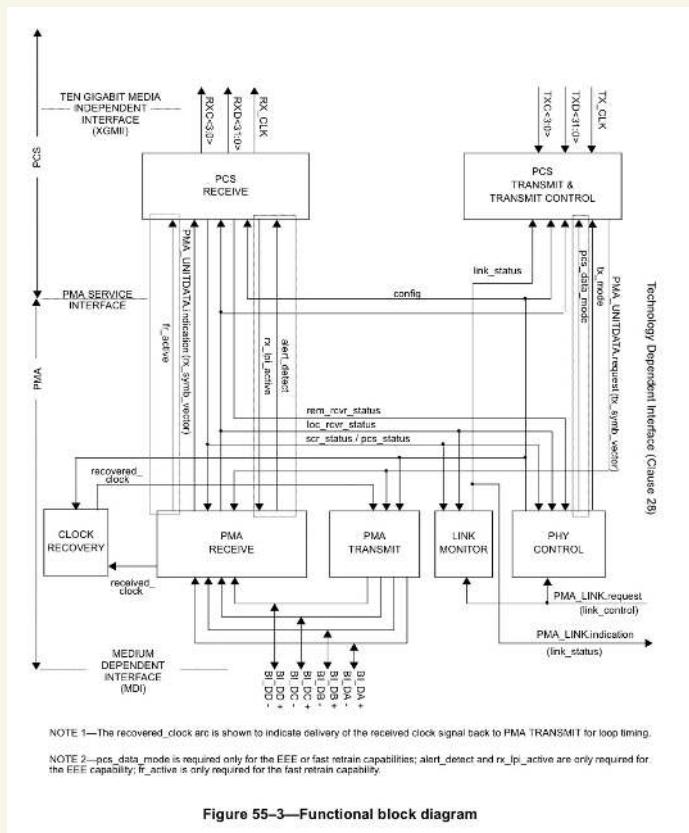
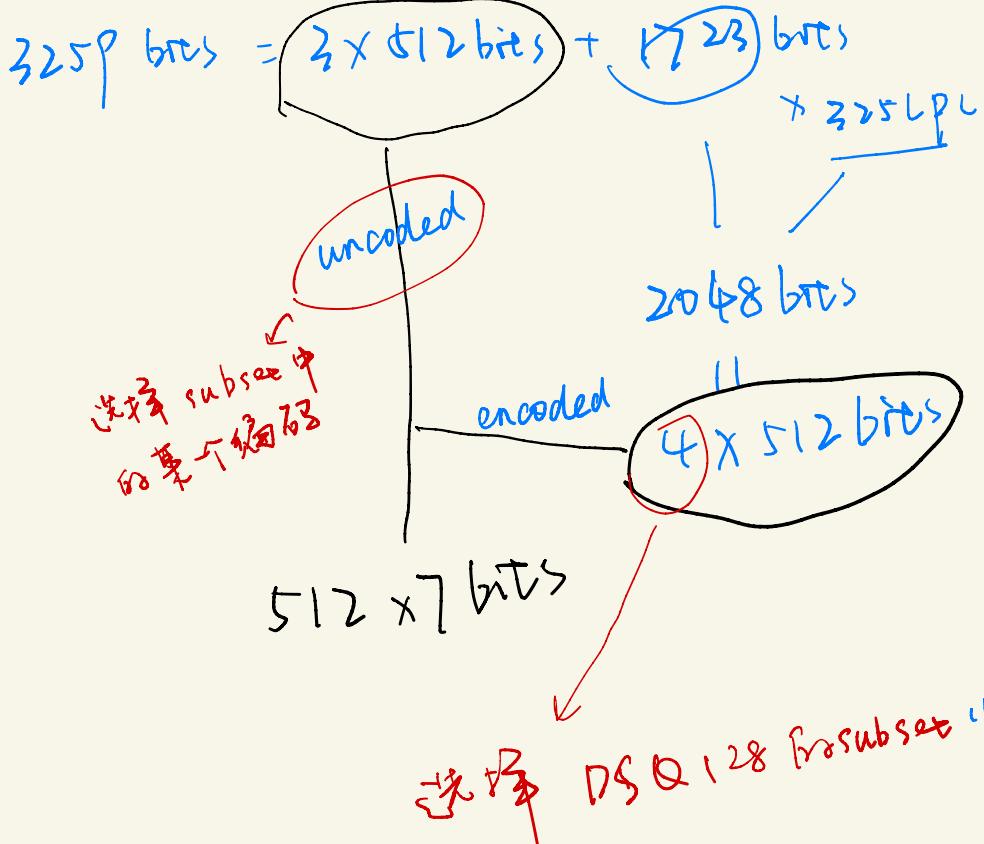


Figure 55-3—Functional block diagram



如大 100m.

虽然 bus 里有 DSQ128 编码及 PAM 及概念，但是这也  
是字域。

1000sE-T 有成功通过 remote, local RX 通过 T

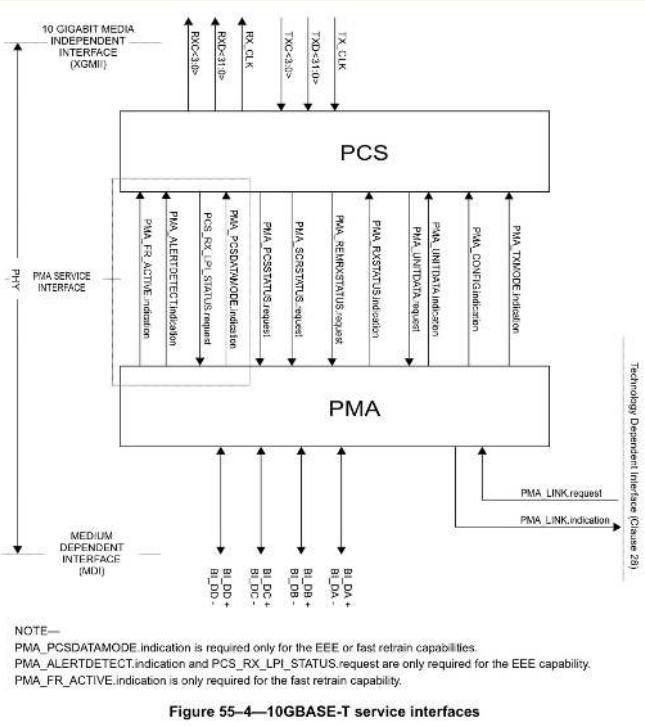


Figure 55-4—10GBASE-T service interfaces

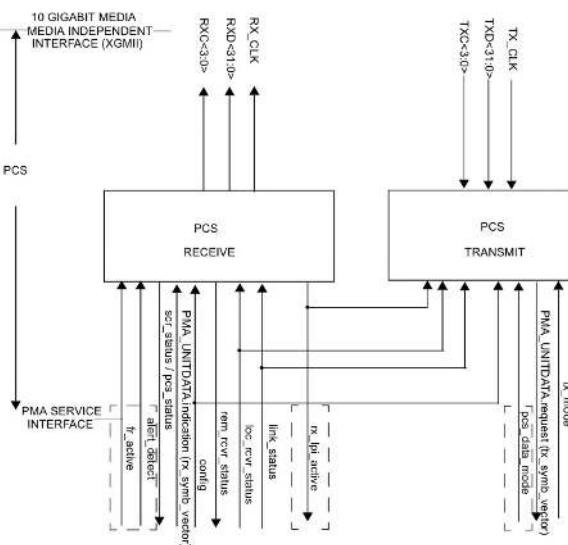


Figure 55-5—PCS reference diagram

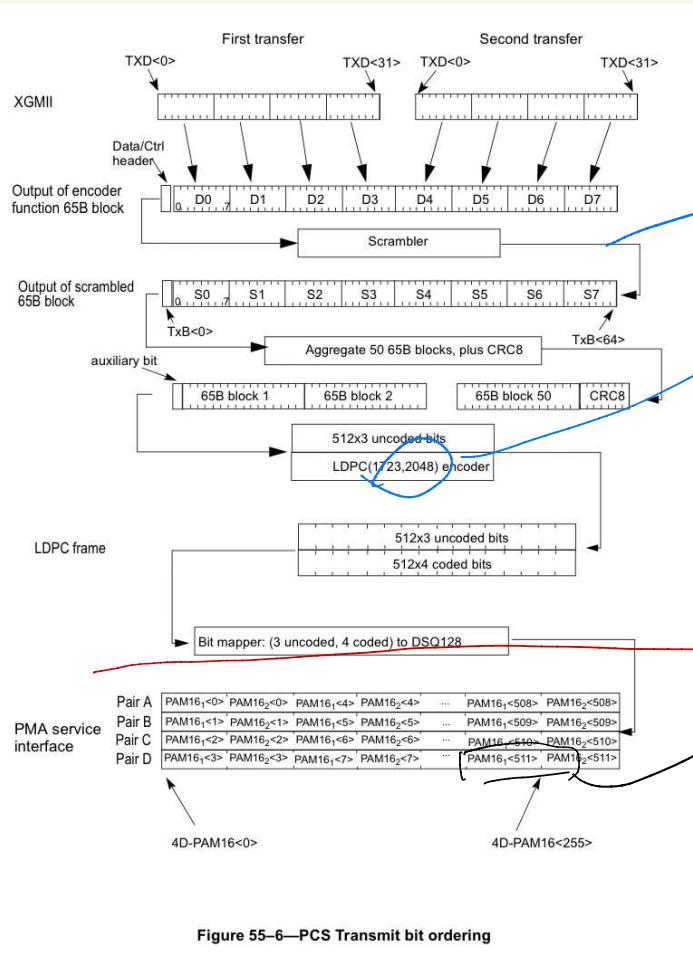


Figure 55–6—PCS Transmit bit ordering

Input Data	cate ctrl header	Block Payload							
Bit Position	0	1	2	3	4	5	6	7	84
Data Block Format:	D <sub>0</sub> D <sub>1</sub> D <sub>2</sub> D <sub>3</sub> D <sub>4</sub> D <sub>5</sub> D <sub>6</sub> D <sub>7</sub>	D <sub>0</sub>	D <sub>1</sub>	D <sub>2</sub>	D <sub>3</sub>	D <sub>4</sub>	D <sub>5</sub>	D <sub>6</sub>	D <sub>7</sub>
Control Block Formats:		Block	C <sub>0</sub>	C <sub>1</sub>	C <sub>2</sub>	C <sub>3</sub>	C <sub>4</sub>	C <sub>5</sub>	C <sub>6</sub>
	C <sub>0</sub> C <sub>1</sub> C <sub>2</sub> C <sub>3</sub> C <sub>4</sub> C <sub>5</sub> C <sub>6</sub> C <sub>7</sub>	0x1E	C <sub>0</sub>	C <sub>1</sub>	C <sub>2</sub>	C <sub>3</sub>	C <sub>4</sub>	C <sub>5</sub>	C <sub>6</sub>
	C <sub>0</sub> C <sub>1</sub> C <sub>2</sub> C <sub>3</sub> O <sub>4</sub> O <sub>5</sub> O <sub>6</sub> O <sub>7</sub>	0x2D	C <sub>0</sub>	C <sub>1</sub>	C <sub>2</sub>	C <sub>3</sub>	O <sub>4</sub>	D <sub>5</sub>	O <sub>6</sub>
	C <sub>0</sub> C <sub>1</sub> C <sub>2</sub> C <sub>3</sub> S <sub>4</sub> S <sub>5</sub> S <sub>6</sub> S <sub>7</sub>	0x33	C <sub>0</sub>	C <sub>1</sub>	C <sub>2</sub>	C <sub>3</sub>	S <sub>4</sub>	D <sub>5</sub>	D <sub>6</sub>
	O <sub>0</sub> D <sub>1</sub> D <sub>2</sub> D <sub>3</sub> S <sub>4</sub> D <sub>5</sub> D <sub>6</sub> D <sub>7</sub>	0x86	D <sub>1</sub>	D <sub>2</sub>	D <sub>3</sub>	O <sub>0</sub>	S <sub>4</sub>	D <sub>5</sub>	D <sub>6</sub>
	O <sub>0</sub> D <sub>1</sub> D <sub>2</sub> D <sub>3</sub> D <sub>4</sub> O <sub>5</sub> D <sub>6</sub> D <sub>7</sub>	0x55	D <sub>1</sub>	D <sub>2</sub>	D <sub>3</sub>	O <sub>0</sub>	O <sub>5</sub>	D <sub>6</sub>	D <sub>7</sub>
	S <sub>0</sub> D <sub>1</sub> D <sub>2</sub> D <sub>3</sub> D <sub>4</sub> D <sub>5</sub> D <sub>6</sub> D <sub>7</sub>	0x78	D <sub>1</sub>	D <sub>2</sub>	D <sub>3</sub>	D <sub>4</sub>	D <sub>5</sub>	D <sub>6</sub>	D <sub>7</sub>
	O <sub>0</sub> D <sub>1</sub> D <sub>2</sub> D <sub>3</sub> C <sub>4</sub> C <sub>5</sub> C <sub>6</sub> C <sub>7</sub>	0x4B	D <sub>1</sub>	D <sub>2</sub>	D <sub>3</sub>	O <sub>0</sub>	C <sub>5</sub>	C <sub>6</sub>	C <sub>7</sub>
	T <sub>0</sub> C <sub>1</sub> C <sub>2</sub> C <sub>3</sub> C <sub>4</sub> C <sub>5</sub> C <sub>6</sub> C <sub>7</sub>	0x87	T <sub>0</sub>	C <sub>1</sub>	C <sub>2</sub>	C <sub>3</sub>	C <sub>4</sub>	C <sub>5</sub>	C <sub>6</sub>
	D <sub>0</sub> T <sub>1</sub> C <sub>2</sub> C <sub>3</sub> C <sub>4</sub> C <sub>5</sub> C <sub>6</sub> C <sub>7</sub>	0x99	D <sub>0</sub>	T <sub>1</sub>	C <sub>2</sub>	C <sub>3</sub>	C <sub>4</sub>	C <sub>5</sub>	C <sub>6</sub>
	D <sub>0</sub> T <sub>1</sub> T <sub>2</sub> C <sub>3</sub> C <sub>4</sub> C <sub>5</sub> C <sub>6</sub> C <sub>7</sub>	0xAA	D <sub>0</sub>	T <sub>1</sub>	T <sub>2</sub>	C <sub>3</sub>	C <sub>4</sub>	C <sub>5</sub>	C <sub>6</sub>
	D <sub>0</sub> D <sub>1</sub> D <sub>2</sub> T <sub>3</sub> C <sub>4</sub> C <sub>5</sub> C <sub>6</sub> C <sub>7</sub>	0xB4	D <sub>0</sub>	D <sub>1</sub>	T <sub>3</sub>	C <sub>4</sub>	C <sub>5</sub>	C <sub>6</sub>	C <sub>7</sub>
	D <sub>0</sub> D <sub>1</sub> D <sub>2</sub> D <sub>3</sub> T <sub>4</sub> C <sub>5</sub> C <sub>6</sub> C <sub>7</sub>	0xCC	D <sub>0</sub>	D <sub>1</sub>	D <sub>2</sub>	D <sub>3</sub>	T <sub>4</sub>	C <sub>5</sub>	C <sub>6</sub>
	D <sub>0</sub> D <sub>1</sub> D <sub>2</sub> D <sub>3</sub> D <sub>4</sub> O <sub>5</sub> C <sub>6</sub> C <sub>7</sub>	0xD2	D <sub>0</sub>	D <sub>1</sub>	D <sub>2</sub>	D <sub>3</sub>	D <sub>4</sub>	O <sub>5</sub>	C <sub>6</sub>
	D <sub>0</sub> D <sub>1</sub> D <sub>2</sub> D <sub>3</sub> D <sub>4</sub> D <sub>5</sub> T <sub>6</sub> C <sub>7</sub>	0xE1	D <sub>0</sub>	D <sub>1</sub>	D <sub>2</sub>	D <sub>3</sub>	D <sub>4</sub>	D <sub>5</sub>	T <sub>6</sub>
	D <sub>0</sub> D <sub>1</sub> D <sub>2</sub> D <sub>3</sub> D <sub>4</sub> D <sub>5</sub> D <sub>6</sub> T <sub>7</sub>	0xFF	D <sub>0</sub>	D <sub>1</sub>	D <sub>2</sub>	D <sub>3</sub>	D <sub>4</sub>	D <sub>5</sub>	D <sub>6</sub>

Figure 55–9—64B/65B block formats

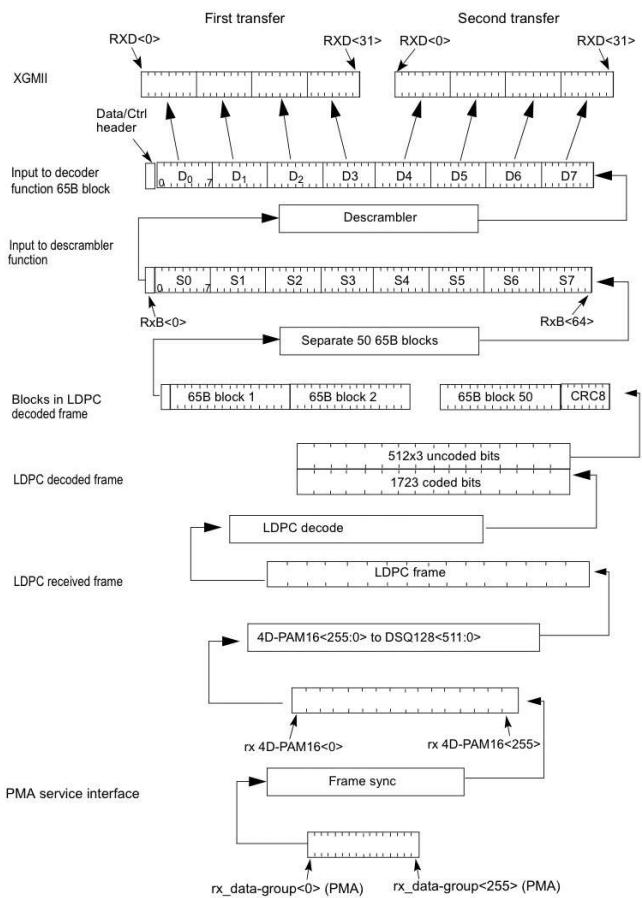


Figure 55-7—PCS Receive bit ordering

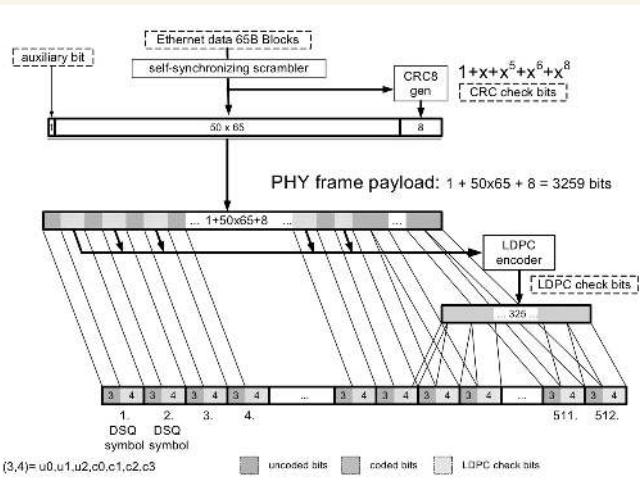


Figure 55-8—PCS detailed transmit bit ordering

Table 55-1—Control codes

Control character	Notation	XGMII control codes	10GBASE-T control codes	10GBASE-T O code	8B/10B code <sup>a</sup>
idle	/I/	0x07	0x00		K28.0 or K28.3 or K28.5 without D20.5 <sup>b</sup>
LPI	/LI/	0x06	0x06		K28.0 or K28.3 or K28.5 with D20.5 <sup>b</sup>
start	/S/	0xFB	Encoded by block type field		K27.7
terminate	/T/	0xFD	Encoded by block type field		K29.7
error	/E/	0xFE	0x1E		K30.7
Sequence ordered set	/Q/	0x9C	Encoded by block type field plus O code	0x0	K28.4
reserved0	/R/ <sup>c</sup>	0x1C	0x2D		K28.0
reserved1		0x3C	0x33		K28.1
reserved2	/A/	0x7C	0x4B		K28.3
reserved3	/K/	0xBC	0x55		K28.5
reserved4		0xDC	0x66		K28.6
reserved5		0xF7	0x78		K23.7
Signal ordered set <sup>d</sup>	/Fsig/	0x5C	Encoded by block type field plus O code	0xF	K28.2

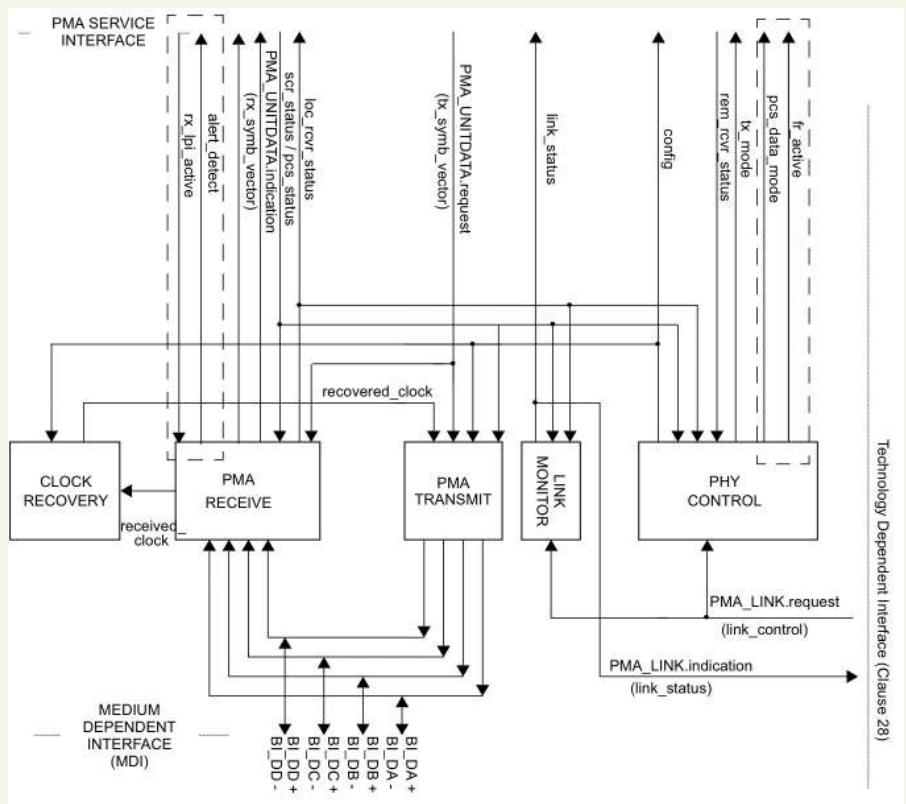
<sup>a</sup>For information only. The 8B/10B code is specified in Clause 36. Usage of the 8B/10B code for 10 Gb/s operation is specified in Clause 48.

<sup>b</sup>Use of idle and LPI ordered sets per 48.2.4.2.

<sup>c</sup>The codes for /A/, /K/, and /R/ are used on the XAUI interface to signal idle. They are not present on the XGMII when no errors have occurred, but certain bit errors cause the XGXS to send them on the XGMII.

<sup>d</sup>Reserved for INCITS T11 Fibre Channel use.

loop timing: 有时候并不想走快点的话，比如 10ms 读一下温度，这时候控制温度没有读时间长  
24 [t] Loop timing,



1. train for symbol 10 -9 和 +9.
2. fast-retrain 之前会发送 link failure. 4T LPPC Frame
3. 10GBASE-T 并行的 PMD
4. PHY control 为 pair A 16284 和 B 128 bit 9
5. PHY control 有 16.5 octet
6. PHY control 有 16.5 octet 通过 PCS 和 PMD 共同协商到物理层
7. fast-retrain. 每 30ms 重新完成

Start of Frame Delimiter 0xBBA70000	3 Transmitter Settings	Message Field	SNR Margin	Message Field Dependent	Message Field Dependent	CRC16
4 octets	3 octets	1 octet	4 bits	1.5 octets	4 octets	2 octets

Figure 55–22—InfoField format

8. 10GBASE-T for  $\Delta$   
 ↗ master-pre<sup>†</sup> in pair  
 for symbol - note  $\Delta$   
 800 m ± 50 ppm.  
 9. 支持 AN-28

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649  
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 IEEE Std 802.3-2015  
 IEEE Standard for Ethernet  
 SECTION FOUR

Start of Frame Delimiter 0xBBA70000	3 Transmitter Settings	Message Field	SNR Margin	Reser- ved	Transition Counter	Reser- ved	Vendor Specific	CRC16
4 octets	3 octets	1 octet	4 bits	2 bits	10 bits	2 octets	2 octets	2 octets

Figure 55–23—InfoField transition counter format

10. 从 XAMII 到 MDI 口  
 的时间不超过 25600 BT.

Start of Frame Delimiter 0xBBA70000	3 Transmitter Settings	Message Field	SNR Margin	Coefficient Exchange	Coefficient Field	CRC16
4 octets	3 octets	1 octet	4 bits	1.5 octets	4 octets	2 octets

Figure 55–24—InfoField coefficient exchange format

Start of Frame Delimiter 0xBBA70000	3 Transmitter Settings	Message Field	SNR Margin	Reserved	Reserved	Vendor Specific	CRC16
4 octets	3 octets	1 octet	4 bits	1.5 octets	2 octets	2 octets	2 octets

Figure 55–25—InfoField not transition counter and not coefficient exchange format

- a) Echo from the local transmitter on the same duplex channel (cable pair). Echo is caused by the hybrid function used to achieve simultaneous bi-directional transmission of data and by impedance mismatches in the link segment. It is impractical to achieve the objective BER without using echo cancellation. Since the symbols transmitted by the local disturbing transmitter are available to the cancellation processor, echo interference can be reduced to a small residual noise using echo cancellation methods.
- b) Near-end crosstalk (NEXT) interference from the local transmitters on the duplex channels (cable pairs) of the link segment. Each receiver experiences NEXT interference from three adjacent transmitters. NEXT cancellers are used to reduce the interference from each of the three disturbing transmitters to a small residual noise. NEXT cancellation is possible since the symbols transmitted by the three disturbing local transmitters are available to the cancellation processor.
- c) Far-end crosstalk (FEXT) noise at a receiver is from three disturbing transmitters at the far end of the duplex channel (cable pairs) of the link segment. FEXT noise can be reduced through cross coupled equalizers although the symbols from the remote transmitters are not immediately available.
- d) Intersymbol interference (ISI). ISI is the extraneous energy from one signaling symbol that interferes with the reception of another symbol on the same channel. 10GBASE-T supports the use of Tomlinson-Harashima Precoding as a mechanism to reduce the effects of ISI.
- e) Noise from non-idealities in the duplex channel, transmitters, and receivers; for example, DAC/ADC non-linearity, electrical noise (shot and thermal), and non-linear channel characteristics. 10GBASE-T limits the effects of some of these non-idealities by a variety of PMA electrical specifications.
- f) Noise coupled between link segments. Noise coupled between the disturbed duplex channel in a link segment and the disturbing duplex channels in other link segments is referred to as alien crosstalk noise. Since the transmitted symbols from the alien crosstalk noise sources are not available to the cancellation processor (they are in another cable), it is very difficult to cancel the alien crosstalk noise. To ensure robust operation the alien crosstalk is specified in 55.7.3.
- g) The background noise for 10GBASE-T is expected not to exceed  $-150$  dBm/Hz. A background noise limit of  $-150$  dBm/Hz was assumed for determining the minimum signal-to-noise ratio.

jitter test pattern .

1. high freq  $\rightarrow$  1010 ...

2. low freq  $\rightarrow$  1111 00000 ...

3. mix freq  $\rightarrow$  (1111 0101 100000 10100 ...)

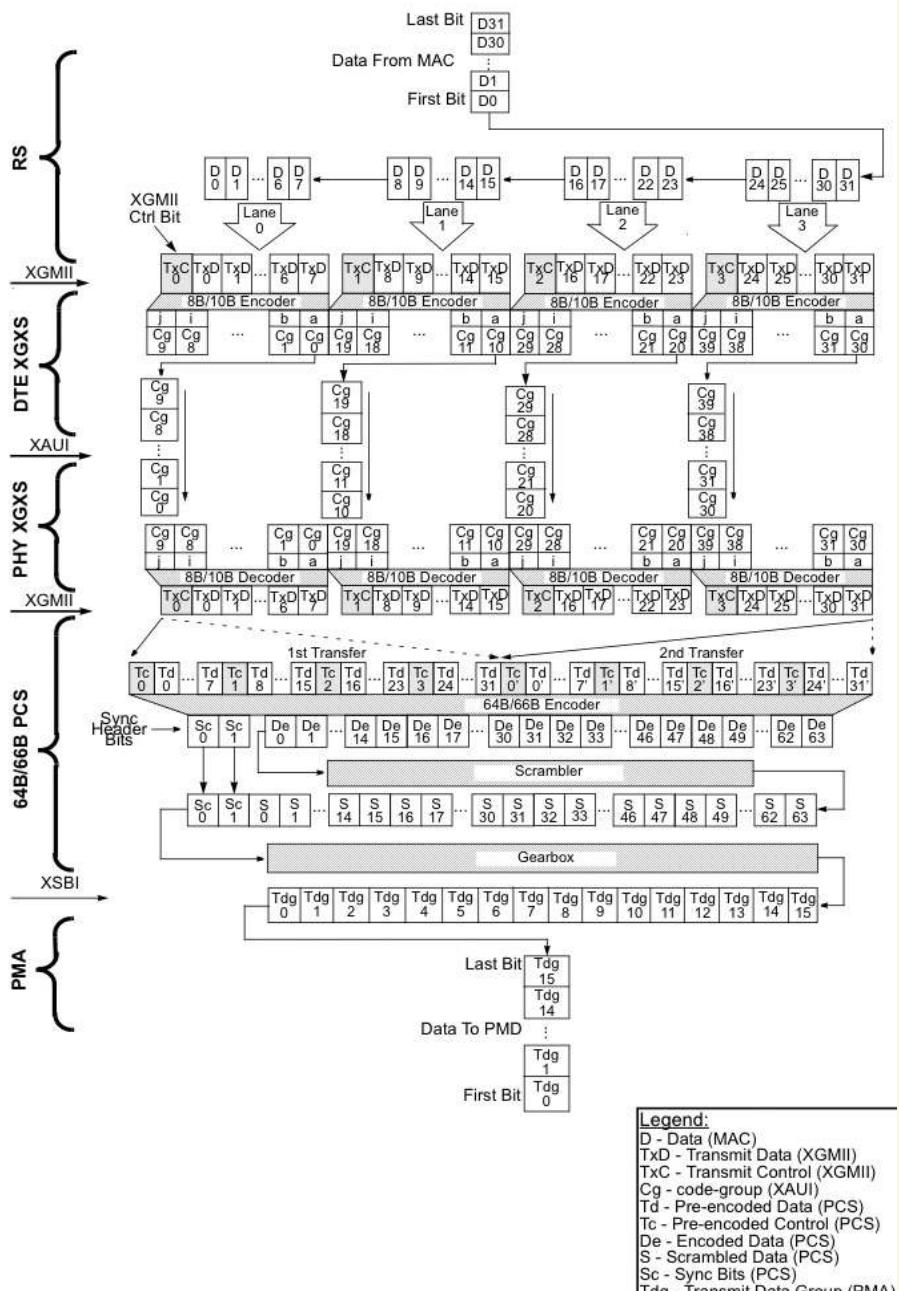


Figure 44A-1—10GBASE-R transmit data path bit ordering

# Ethernet in the first mile

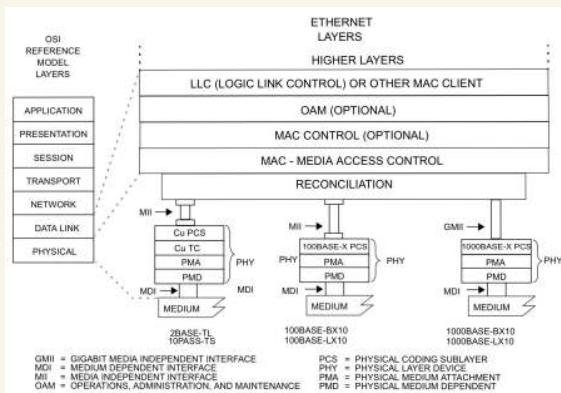
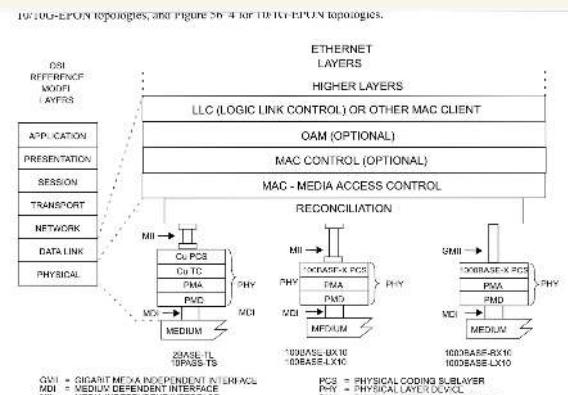


Figure 56-1—Architectural positioning of EFM: P2P Topologies

*OAM = operation, administration, maintenance.*



Bx-D → downstream

Bx-U → upstream

OLT, 分光器, ONU 组成了 PON 端口  
的关键部分

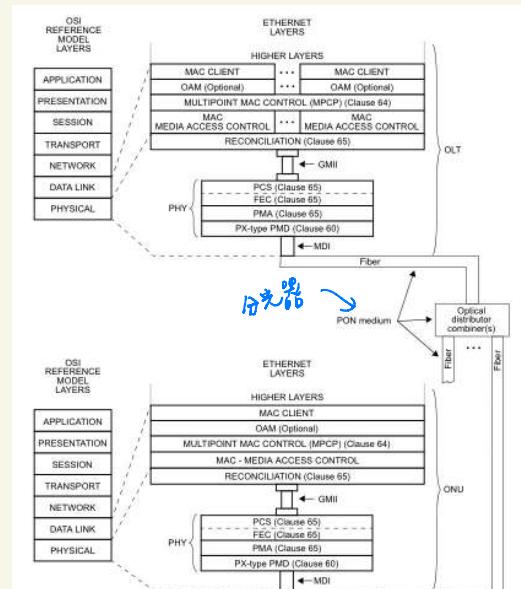


Figure 56-2—Architectural positioning of EFM:  
P2MP 1G-EPON architecture (1 Gb/s downstream, 1 Gb/s upstream)

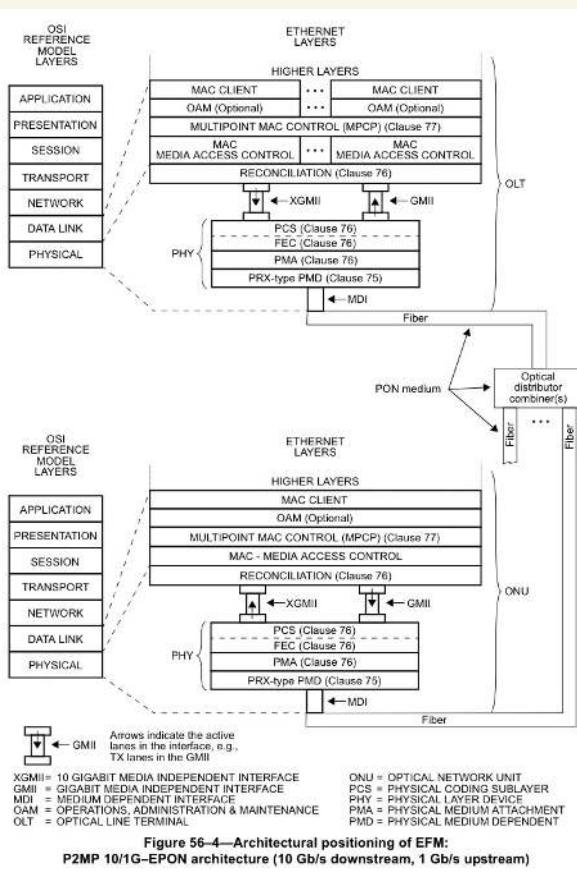


Figure 56-4—Architectural positioning of EFM:  
P2MP 10/1G-EPON architecture (10 Gb/s downstream, 1 Gb/s upstream)

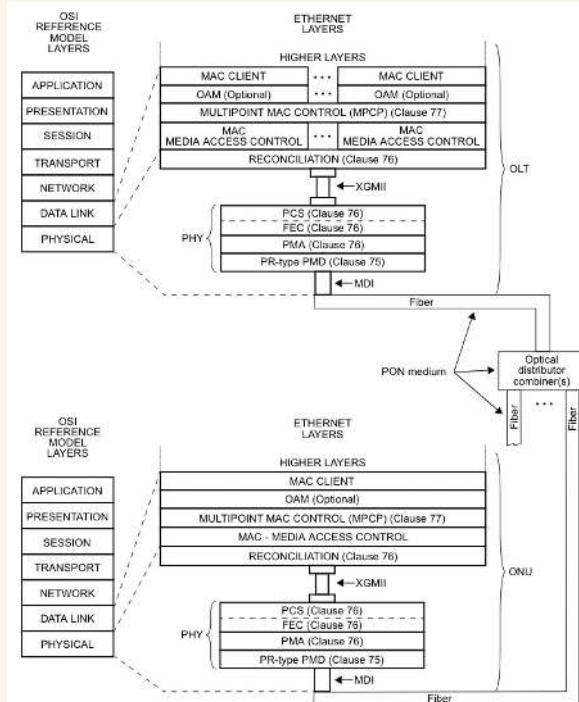


Figure 56-3—Architectural positioning of EFM:  
P2MP 10/10G-EPON architecture (10 Gb/s downstream, 10 Gb/s upstream)

Table 56-2—Nomenclature and clause correlation for P2P systems

Nomenclature	Clause							
	57	58	59	61	62	63	66	
OAM	100BASE-LX10 PMD	100BASE-BX10 PMD	100BASE-LX10 PMD	100BASE-BX10 PMD	Cu PCS	10PASS-TS PMA & PMD	2BASE-TL PMA & PMD	100BASE-X PCS, PMA
2BASE-TL	O <sup>a</sup>			M	M			
10PASS-TS	O			M	M			
100BASE-LX10	O	M				M		
100BASE-BX10	O		M			M		
1000BASE-LX10	O		M				M	
1000BASE-BX10	O			M			M	

<sup>a</sup>O = Optional, M = Mandatory

在 p2p 成為 p2mp 的情況下，  
可以將 RX 份之一 ready 下去並 TX

### 57.2.1 Interlayer service interfaces

Figure 57–2 depicts the usage of interlayer interfaces by the OAM sublayer.

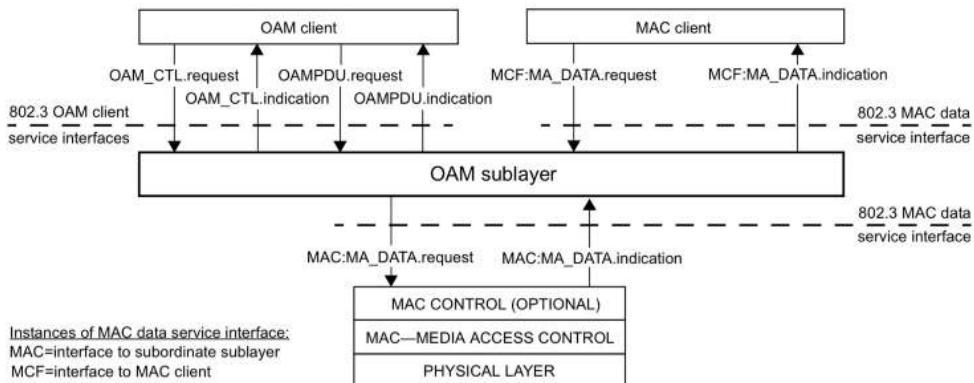
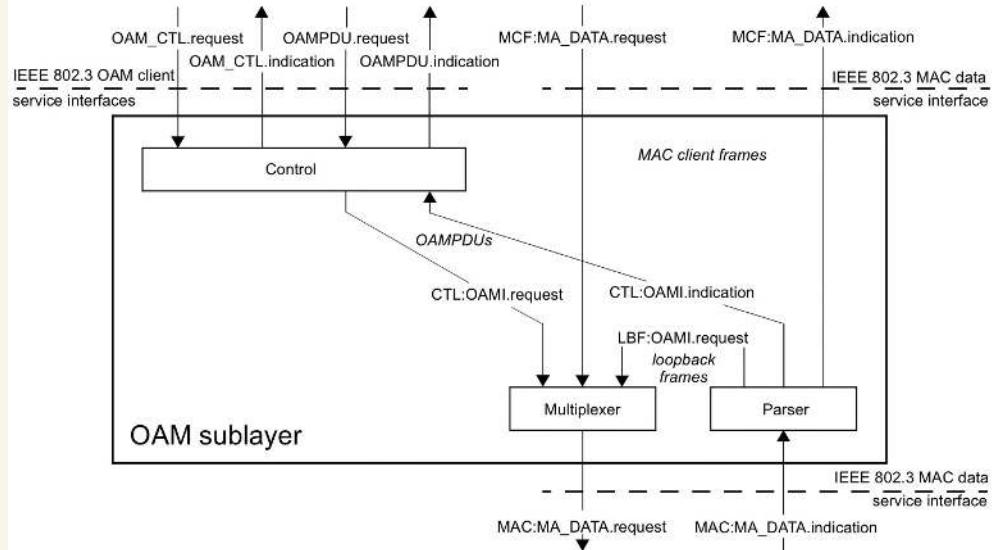


Figure 57–2—OAM sublayer support of interlayer service interfaces

Figure 57–3 depicts the major blocks within the OAM sublayer and their interrelationships.



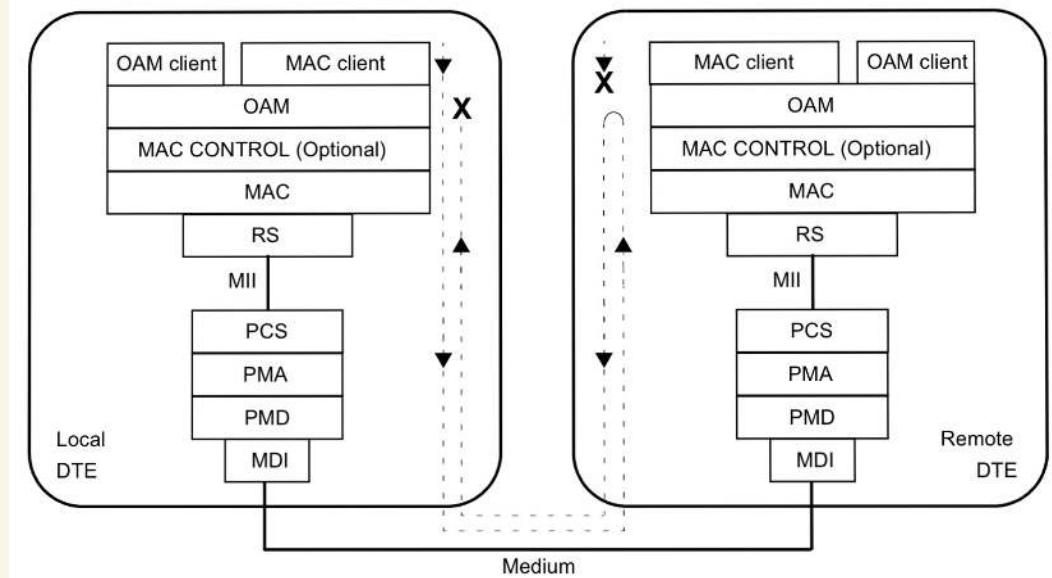
**Instances of OAM internal service interfaces:**

- CTL:OAMI.indication = Passes OAMPDUs to OAM Control
- CTL:OAMI.request = Passes OAMPDUs to Multiplexer
- LBF:OAMI.request = Passes loopback frames to Multiplexer

**Instances of MAC data service interface:**

- MAC=interface to subordinate sublayer
- MCF=interface to MAC client

Figure 57–3—OAM sublayer block diagram



remote loopback at first ND - OAMPDU 会報  
loopback.

- Multiplexer.** This function is responsible for passing frames received from the superior sublayer (e.g., MAC client sublayer), OAMPDUs from the Control function and loopback frames from the Parser, to the subordinate sublayer (e.g., MAC sublayer).
- Parser.** This function distinguishes among OAMPDUs, MAC client frames and loopback frames and passes each to the appropriate entity (Control, superior sublayer and Multiplexer, respectively).
- Control.** This function is responsible for providing the interface between the OAM client entity and the functions internal to the OAM sublayer. It incorporates the Discovery process which detects the existence and capabilities of OAM at the remote DTE. Also, it includes the Transmit process, which governs the transmission of OAMPDUs to the Multiplexer function and a set of Receive rules, which govern the reception of OAMPDUs.

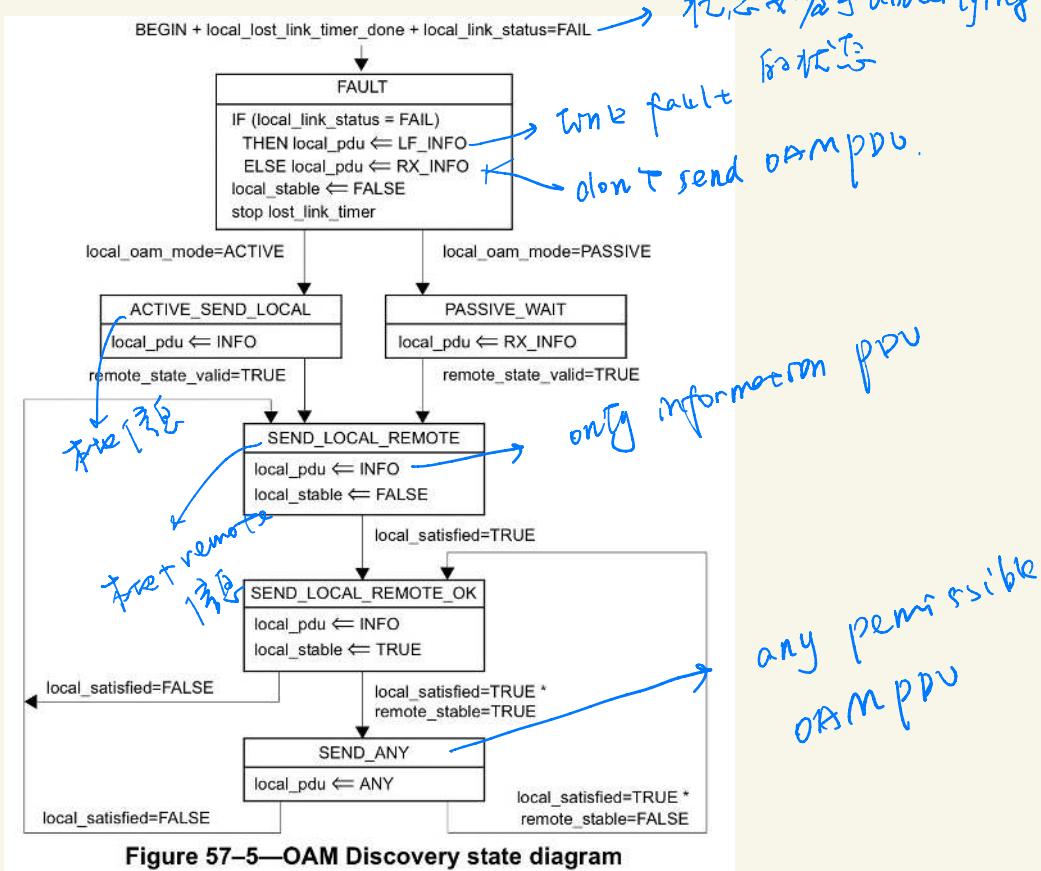
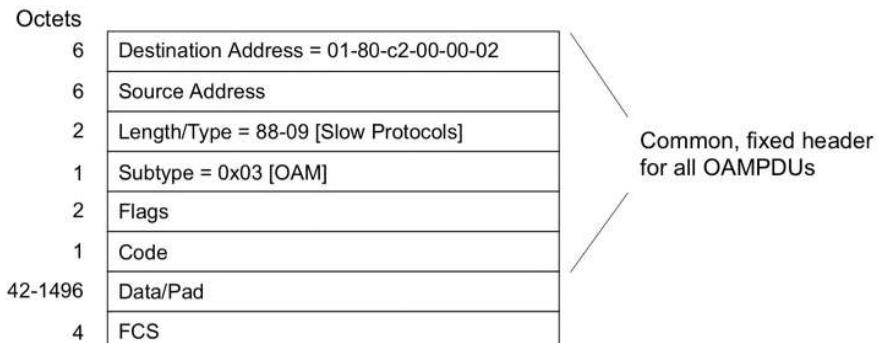


Figure 57-5—OAM Discovery state diagram

1. 序列图，transmit，multiplexer，parser.

2. parser → { context  
superior  
loopback }

The OAMPDU structure shall be as shown in Figure 57–9.



**Figure 57–9—OAMPDU frame structure**

**Table 57–3—Flags field**

Bit(s)	Name	Description
15:7	<i>Reserved</i>	Reserved bits shall be set to zero when sending an OAMPDU, and should be ignored on reception for compatibility with future use of reserved bits.
6	Remote Stable	When remote_state_valid is set to TRUE, the Remote Stable and Remote Evaluating values shall be a copy of the last valid received Local Stable and Local Evaluating values from the remote OAM peer.
5	Remote Evaluating	Otherwise, the Remote Stable and Remote Evaluating bits shall be set to 0.

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**Table 57–3—Flags field (continued)**

Bit(s)	Name	Description
4	Local Stable	Local Stable and Local Evaluating form a two-bit encoding shown below: 4:3 0x0 = Local DTE Unsatisfied, Discovery can not complete 0x1 = Local DTE Discovery process has not completed 0x2 = Local DTE Discovery process has completed 0x3 = Reserved. This value shall not be sent. If the value 0x3 is received, it should be ignored and not change the last received value.
3	Local Evaluating	
2	Critical Event	1 = A critical event has occurred. 0 = A critical event has not occurred.
1	Dying Gasp	1 = An unrecoverable local failure condition has occurred. 0 = An unrecoverable local failure condition has not occurred.
0	Link Fault	The PHY has detected a fault has occurred in the receive direction of the local DTE (e.g., link, Physical Layer). 1 = Local device's receive path has detected a fault. 0 = Local device's receive path has not detected a fault.

Table 57–4—OAMPDU codes

Code	OAMPDU	Comment	Source
00	Information	Communicates local and remote OAM information.	OAM client / OAM sublayer
01	Event Notification	Alerts remote DTE of link event(s).	OAM client
02	Variable Request	Requests one or more specific MIB variables.	OAM client
03	Variable Response	Returns one or more specific MIB variables.	OAM client
04	Loopback Control	Enables/disables OAM remote loopback.	OAM client
05-FD	Reserved	Reserved	OAM client
FE	Organization Specific	Reserved for Organization Specific Extensions, distinguished by Organizationally Unique Identifier.	OAM client
FF	Reserved	Reserved	OAM client

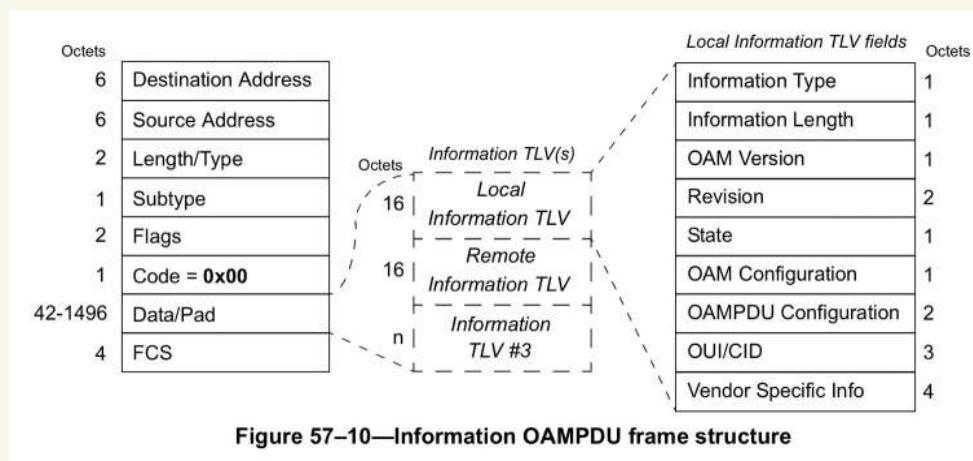
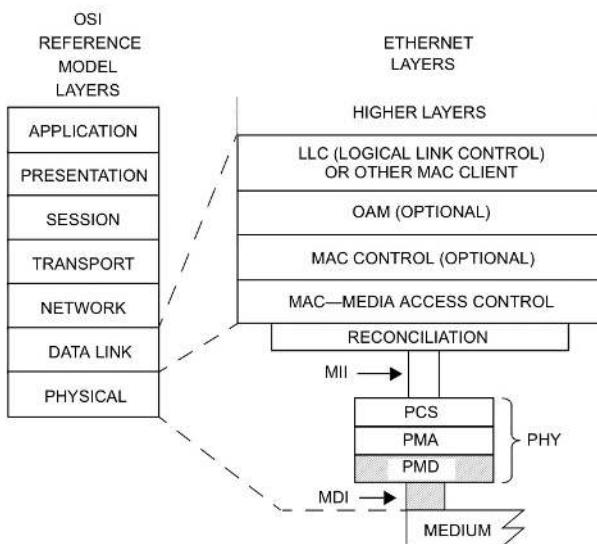


Figure 57–10—Information OAMPDU frame structure

MIB → object ⇒ packages ⇒ { attr  
action }

Table 58–1—Classification of 100BASE-LX10 and 100BASE-BX10

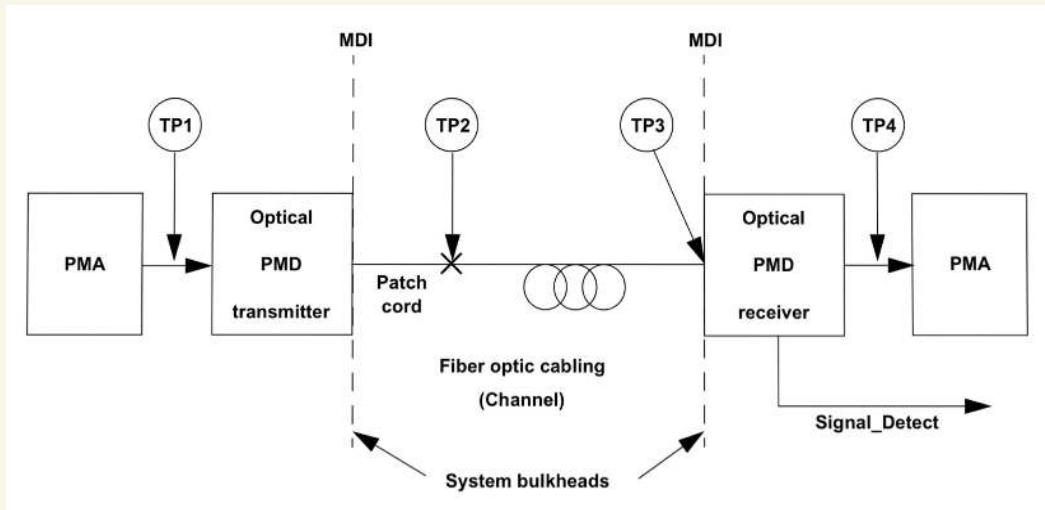
Description	100BASE-LX10	100BASE-BX10-D	100BASE-BX10-U	Unit
Fiber type	B1.1, B1.3 SMF <sup>a</sup>			
Number of fibers	2	1		
Typical transmit direction	Any	Downstream	Upstream	
Nominal transmit wavelength	1310	1550	1310	nm
Minimum range	0.5 m to 10 km			
Maximum channel insertion loss <sup>b</sup>	6.0	5.5	6.0	dB

<sup>a</sup>Specified in IEC 60793-2.<sup>b</sup>At the nominal wavelength.

MDI = MEDIUM DEPENDENT INTERFACE  
MII = MEDIUM INDEPENDENT INTERFACE

PCS = PHYSICAL CODING SUBLAYER  
PHY = PHYSICAL LAYER DEVICE  
PMA = PHYSICAL MEDIUM ATTACHMENT  
PMD = PHYSICAL MEDIUM DEPENDENT

Figure 58–1—100BASE-LX10 and 100BASE-BX10 PMDs relationship to the ISO/IEC Open Systems Interconnection (OSI) reference model and the IEEE 802.3 Ethernet model



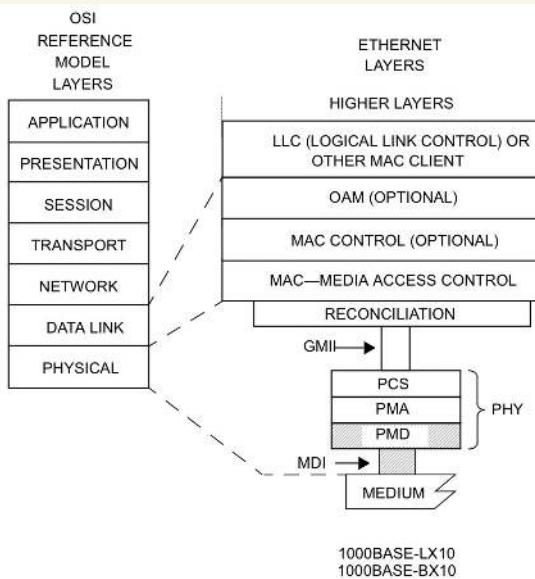
**Table 59–1—Classification of 1000BASE-LX10 and 1000BASE-BX10 PMDs**

Description	1000BASE-LX10		1000BASE-BX10-D	1000BASE-BX10-U	Unit
Fiber type <sup>a</sup>	B1.1, B1.3 SMF		50, 62.5 µm MMF		
Number of fibers	2		2		1
Typical transmit direction	N/A		Downstream	Upstream	
Nominal transmit wavelength	1310		1310	1490	1310
Minimum range	0.5 m to 10 km		0.5 m to 550 m <sup>b</sup>	0.5 m to 10 km	
Maximum channel insertion loss <sup>c</sup>	6.0		2.4	5.5	6.0
					dB

<sup>a</sup>Per IEC 60793-2.

<sup>b</sup>See Table 59–16 for fiber and cable characteristics.

<sup>c</sup>At the nominal operating wavelength



MDI = MEDIUM DEPENDENT INTERFACE  
GMII = GIGABIT MEDIUM INDEPENDENT INTERFACE

PCS = PHYSICAL CODING SUBLAYER  
PHY = PHYSICAL LAYER DEVICE  
PMA = PHYSICAL MEDIUM ATTACHMENT  
PMD = PHYSICAL MEDIUM DEPENDENT

**Figure 59–1—1000BASE-LX10 and 1000BASE-BX10 PMDs relationship to the ISO/IEC Open Systems Interconnection (OSI) reference model and the IEEE 802.3 Ethernet model**

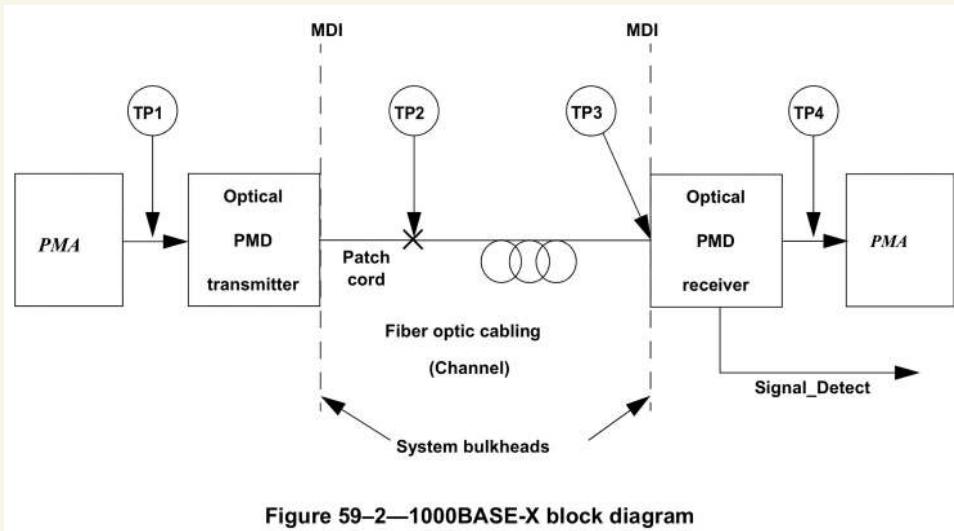


Figure 59-2—1000BASE-X block diagram

Table 59-1—Classification of 1000BASE-LX10 and 1000BASE-BX10 PMDs

Description	1000BASE-LX10		1000BASE-BX10-D	1000BASE-BX10-U	Unit
Fiber type <sup>a</sup>	B1.1, B1.3 SMF		50, 62.5 µm MMF		B1.1, B1.3 SMF
Number of fibers	2		2		1
Typical transmit direction	N/A		Downstream	Upstream	
Nominal transmit wavelength	1310	1310	1490	1310	nm
Minimum range	0.5 m to 10 km	0.5 m to 550 m <sup>b</sup>	0.5 m to 10 km		
Maximum channel insertion loss <sup>c</sup>	6.0	2.4	5.5	6.0	dB

<sup>a</sup>Per IEC 60793-2.

<sup>b</sup>See Table 59-16 for fiber and cable characteristics.

<sup>c</sup>At the nominal operating wavelength

术语：TP → transmitter and dispersion  
penalty 色散损失

P2MP : point-to-multipoint

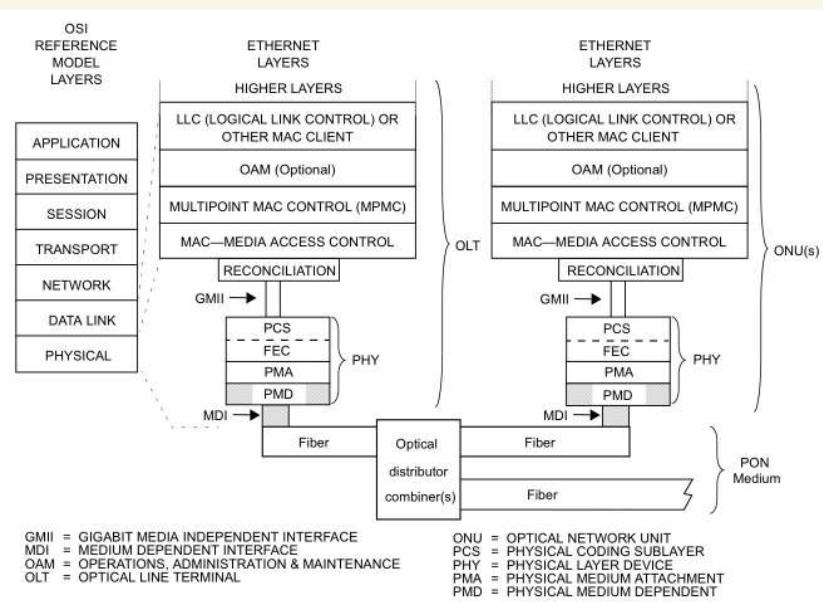
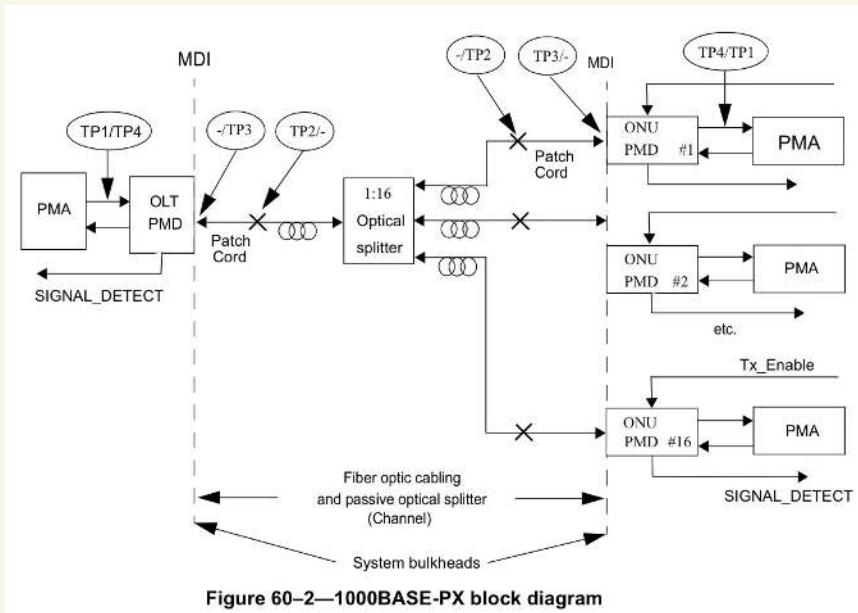


Figure 60–1—P2MP PMDs relationship to the ISO/IEC Open Systems Interconnection (OSI) reference model and the IEEE 802.3 Ethernet model

Table 60–1—PMD types specified in this clause

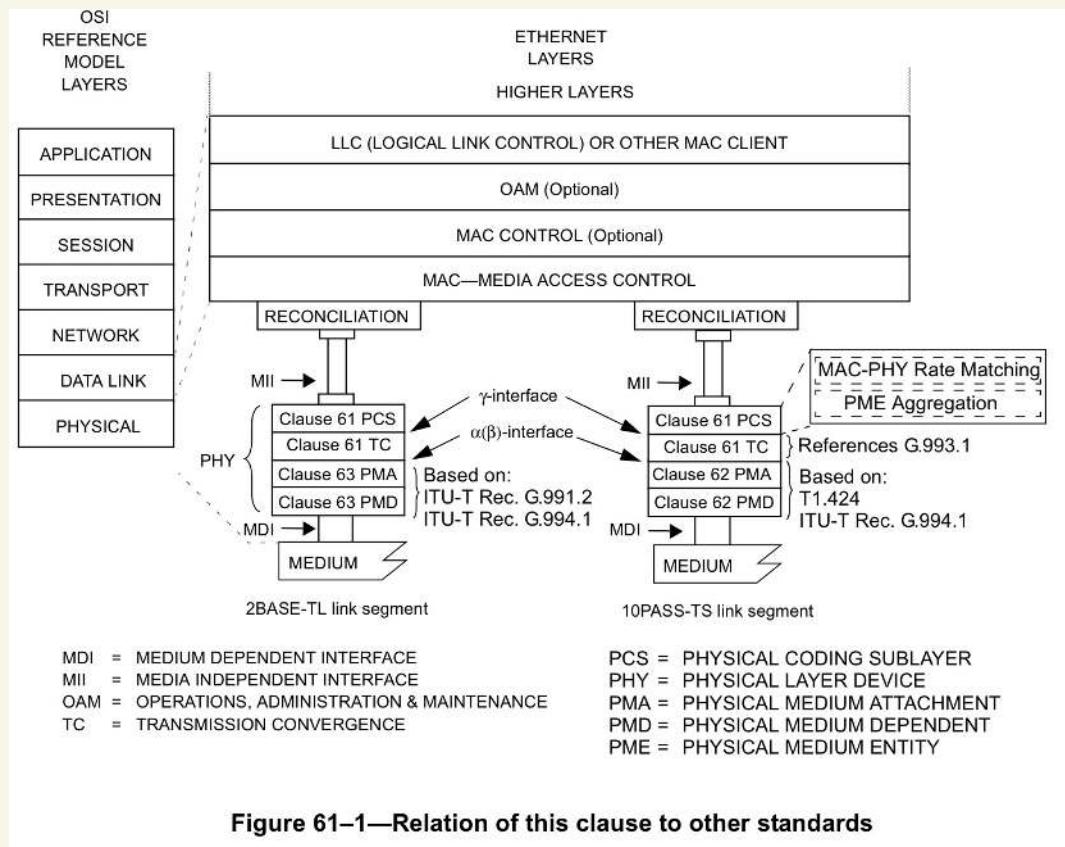
Description	100BASE-PX10-U	100BASE-PX10-D	100BASE-PX20-L	100BASE-PX20-D	100BASE-PX30-L	100BASE-PX30-D	100BASE-PX40-U	100BASE-PX40-D	Unit	
Fiber type	IEC 60793–2 B1.1, B1.3 SMF					IEC 60793–2 B1.1, B1.3 SMF ITU-T G.652, G.657 SMF				
Number of fibers	1					1				
Nominal transmit wavelength	1310	1490	1310	1490	1310	1490	1310	1490	nm	
Transmit direction <sup>a</sup>	US	DS	US	DS	US	DS	US	DS		
Minimum range <sup>b</sup>	0.5 m to 10 km					0.5 m to 20 km				
Maximum channel insertion loss <sup>c</sup>	20	19.5	24	23.5	29	33	33	33	dB	
Minimum channel insertion loss <sup>d</sup>	5		10		15		18		dB	



**Figure 60–2—1000BASE-PX block diagram**

10PASS-TS : 10PASS-TS-D / R

2BASE-TL: 2BASE-TL-D / R



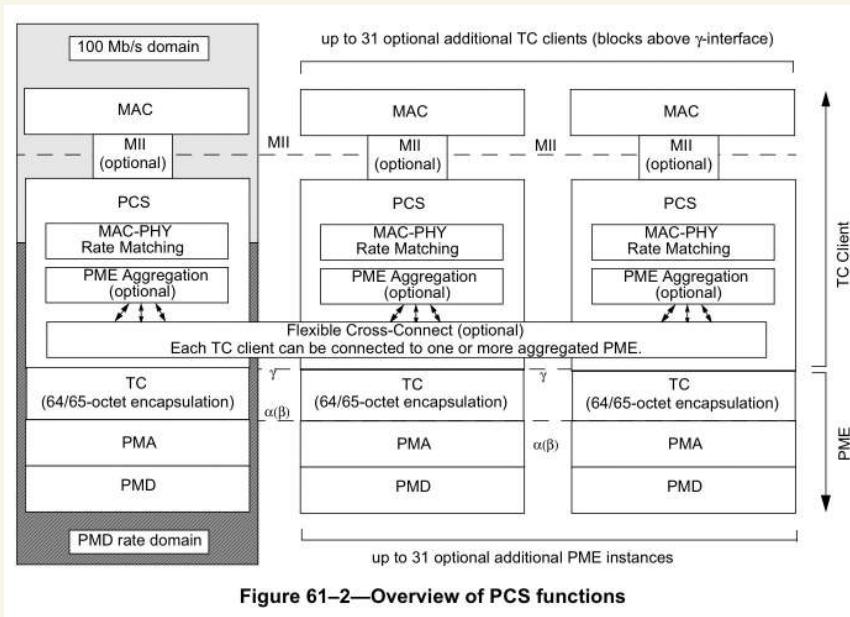


Figure 61–2—Overview of PCS functions

暫時不看 CPE - CO 這種關係

EPON - PON combined with ethernet.

ONU → OLT. 各个ONU 独立

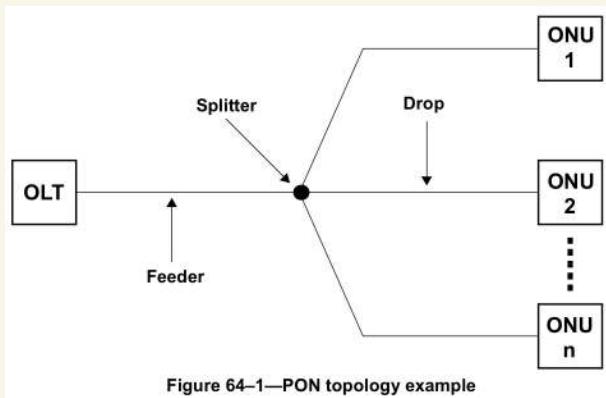
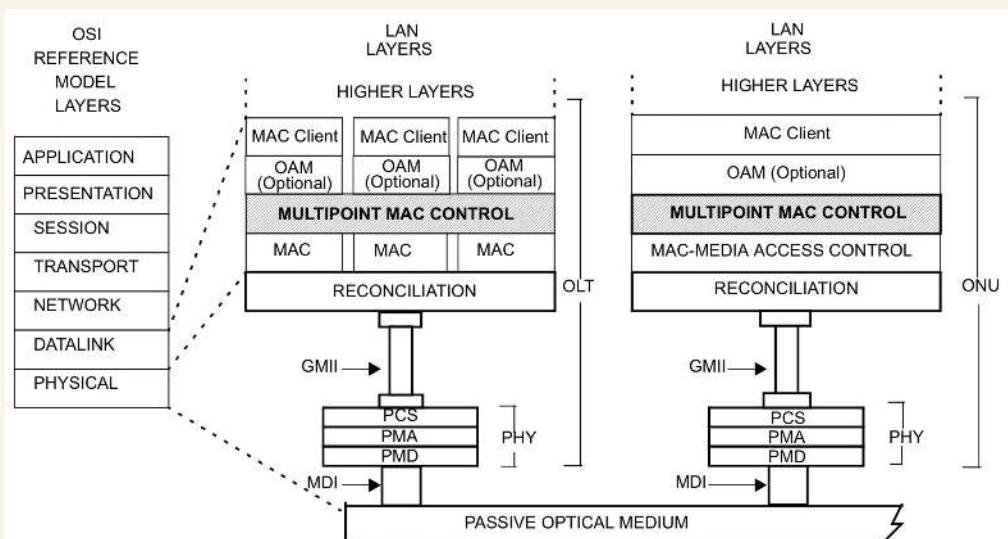


Figure 64-1—PON topology example



GMII = GIGABIT MEDIA INDEPENDENT INTERFACE

MDI = MEDIUM DEPENDENT INTERFACE

OAM = OPERATIONS, ADMINISTRATION & MAINTENANCE

OLT = OPTICAL LINE TERMINAL

ONU = OPTICAL NETWORK UNIT

PCS = PHYSICAL CODING SUBLAYER

PHY = PHYSICAL LAYER DEVICE

PMA = PHYSICAL MEDIUM ATTACHMENT

PMD = PHYSICAL MEDIUM DEPENDENT

Figure 64-2—Relationship of Multipoint MAC Control and the OSI protocol stack

Figure 64–3 provides a functional block diagram of the Multipoint MAC Control architecture.

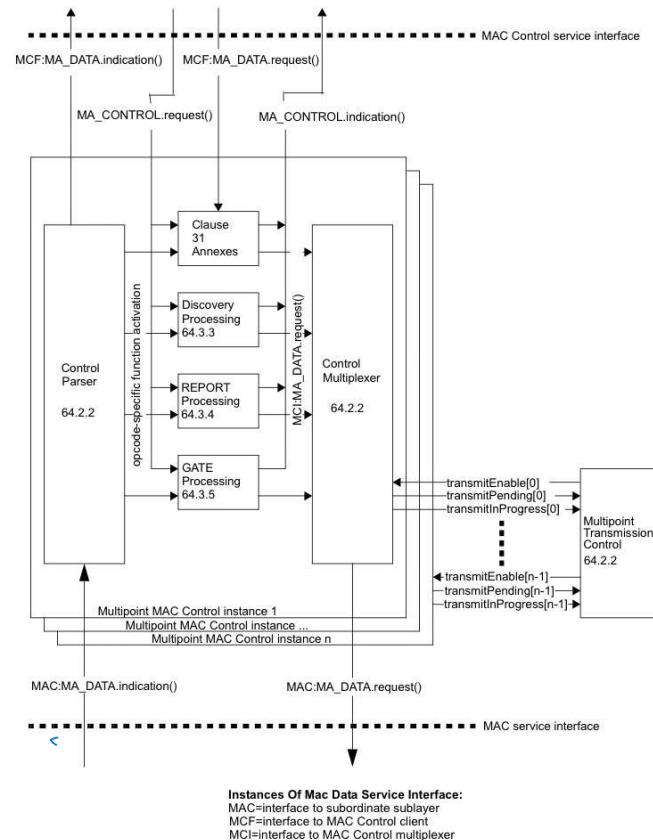


Figure 64–3—Multipoint MAC Control functional block diagram

由哪向哪 control multiplexer  
由哪向哪 control parser

Discovery:

1. OLT → ONU, 指定 discovery 順序
2. ONU → OLT, Register-RQ, LLID
3. OLT → ONU, Register-msg, LLID
4. ONU → OLT, Register-Ack

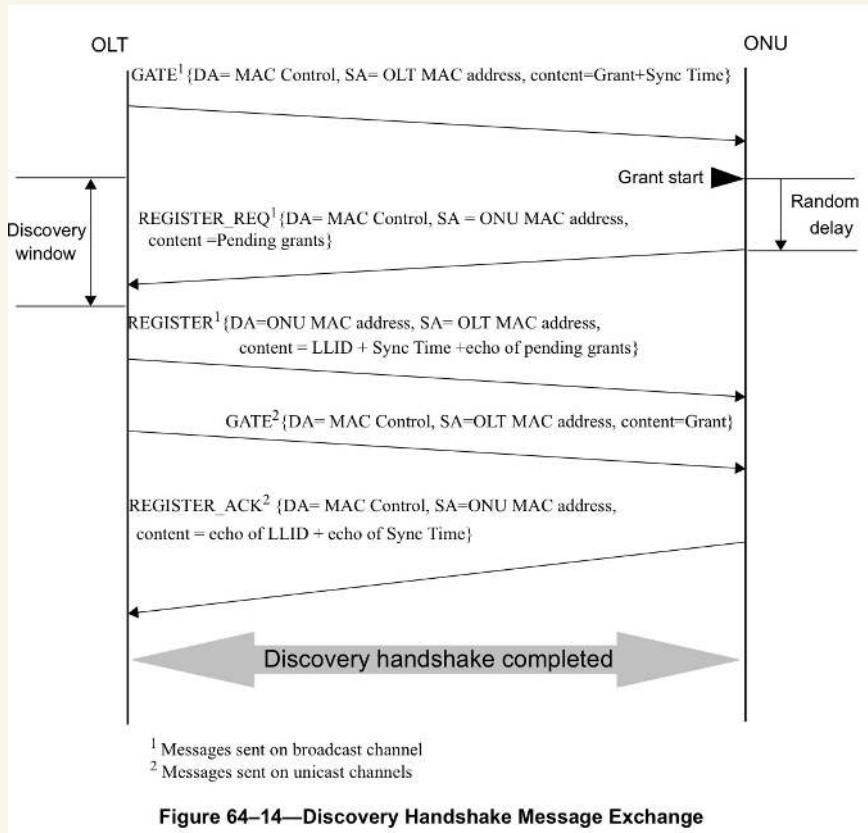
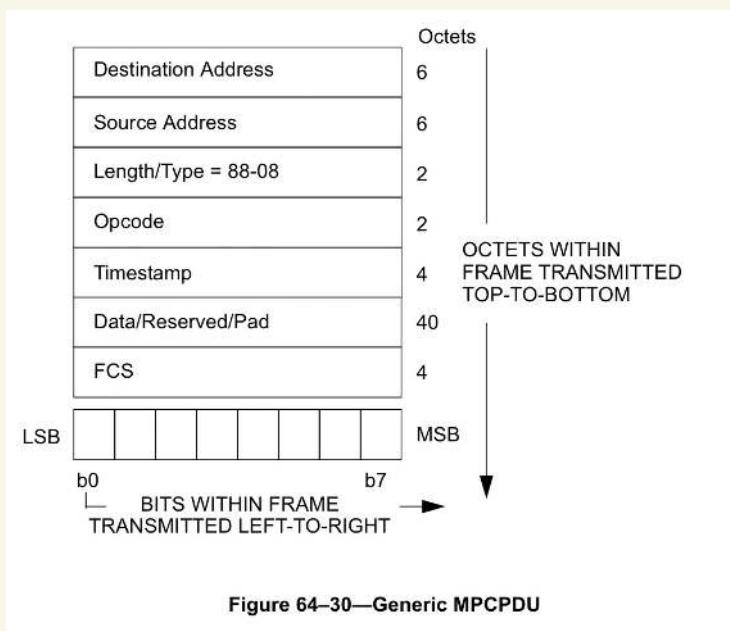


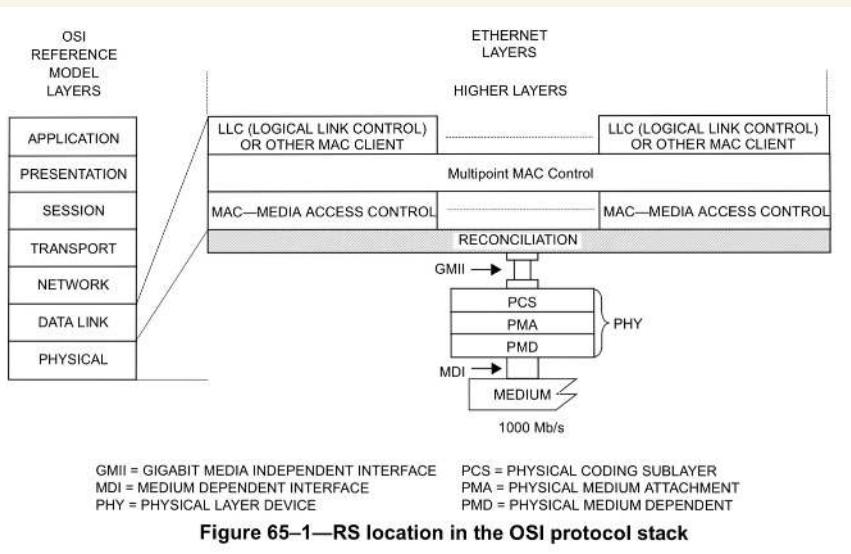
Figure 64–14—Discovery Handshake Message Exchange

GATE MESSAGE - 由 OLT 发给 ONU, 其中包括时间片, 用来控制 ONU 向 OLT 回包的时机



**Figure 64-30—Generic MPCPDU**

以太网帧前导码中，第6、7字节为LLID，先由光  
纤。第1-120 → PUP. 1 → 语音.  
下行 OUT → ONU. 语音 ONU 通过 LLID 选  
自己的帧。  
上行 ONU → OUT. 语音 交换



**Figure 65–1—RS location in the OSI protocol stack**

**Table 65–1—Preamble/SFD replacement mapping**

Offset	Field	Preamble/SFD	Modified preamble/SFD
1	—	0x55	same
2	—	0x55	same
3	SLD	0x55	0xd5
4	—	0x55	same
5	—	0x55	same
6	LLID[15:8]	0x55	<mode, logical_link_id[14:8]> <sup>a</sup>

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**Table 65–1—Preamble/SFD replacement mapping (continued)**

Offset	Field	Preamble/SFD	Modified preamble/SFD
7	LLID[7:0]	0x55	<logical_link_id[7:0]> <sup>b</sup>
8	CRC8	0xd5	The 8-bit CRC calculated over offsets 3 through 7

<sup>a</sup>mode maps to TXD[7], logical\_link\_id[14] maps to TXD[6], logical\_link\_id[8] maps to TXD[0]

<sup>b</sup>logical\_link\_id[7] maps to TXD[7], logical\_link\_id[0] maps to TXD[0]

1000BASE-Tx 禁止使用 FEC

ONU 发送 DATA 间隔减少噪声，会关闭 laser... 這樣子做需要在发送数据前去 lock CDR, SYNC 等。

PMD 需要 DATA detector 在数据到达时，并且 I/I

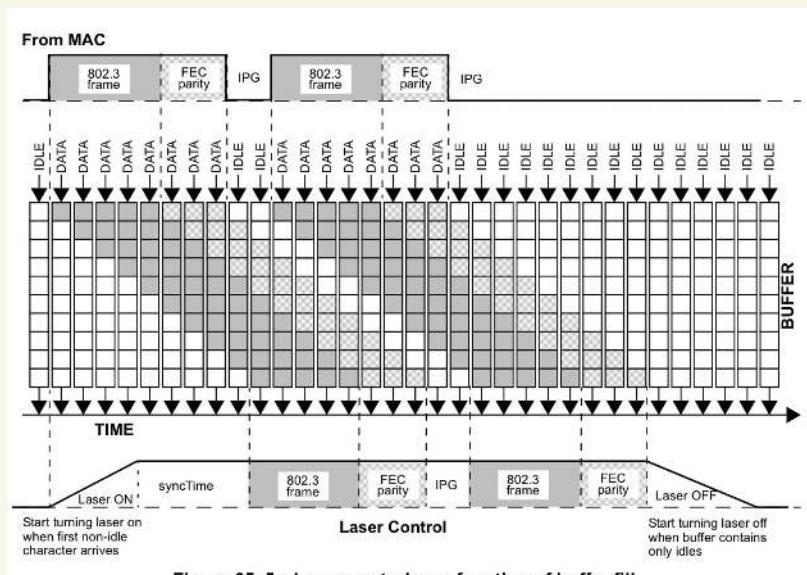
Laser, 而且 laser 有支撑

并且 I/I 充满 buffer.

OLT Laser 永远开 (正常) Phv2 不用

buffer.

ONU  
buffer →



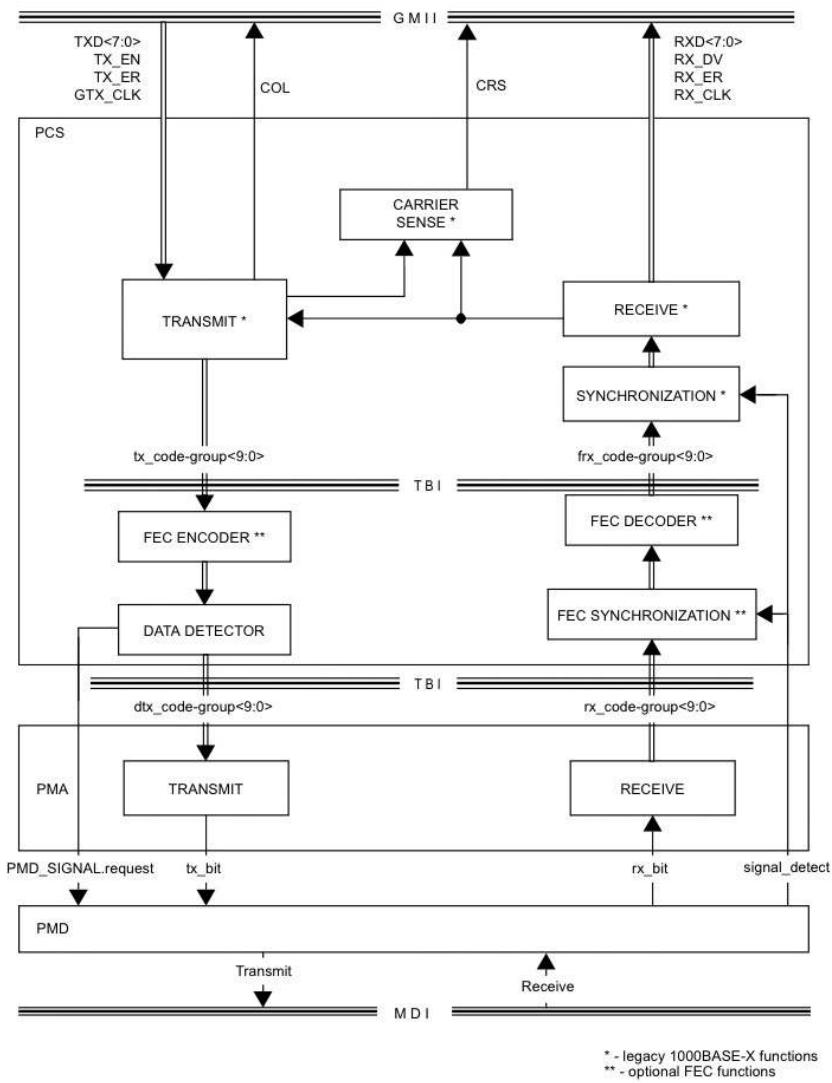


Figure 65–4—PCS Extension functional block diagram

(255, 238, 8) 代表總碼元為 255 symbo[ , 其中有效碼元為 238 symbo[ , 因為  $255 - 238 = 16$  個 symbo[ 为冗余, 故可以有 8 個 symbo[ .

FEC , 239 symbol.  $\rightarrow$  (255, 239, 8)

239 symbol  $\rightarrow$  block.

239 encode for symbol  $\rightarrow$  1S1 FEC 121 131

末端 239 symbol 0.

FEC 的边界  $\rightarrow$  /S-FEC/ 和 /T-FEC/

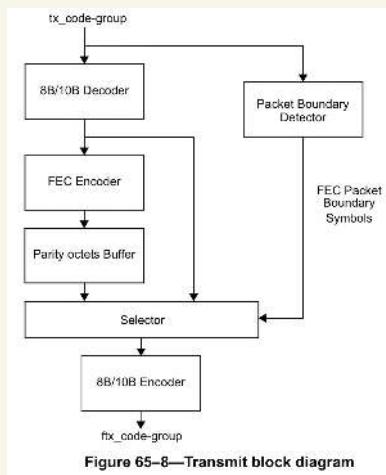
The start and end symbols are constructed from 8B/10B code-groups:

- /S\_FEC/ - start of FEC coded packet - /K28.5/D6.4/K28.5/D6.4/S/
- /T\_FEC\_E/ - end of FEC coded packet with even alignment. If the starting running disparity is positive, the /T\_FEC\_E/ has the following pattern: /T/R/K28.5/D10.1/T/R/. If the starting running disparity is negative, the T\_FEC\_E has the following pattern: /T/R/K28.5/D29.5/T/R/.
- /T\_FEC\_O/ - end of FEC coded packet with odd alignment - /T/R/R/I/T/R/

Figure 65-7 describes the FEC coded Ethernet frame. Between the FCS and PARITY fields, the T\_FEC can be either the /T\_FEC\_E/ or the /T\_FEC\_O/ ordered set. After the PARITY field, the T\_FEC can only be a /T\_FEC\_E/ ordered set.



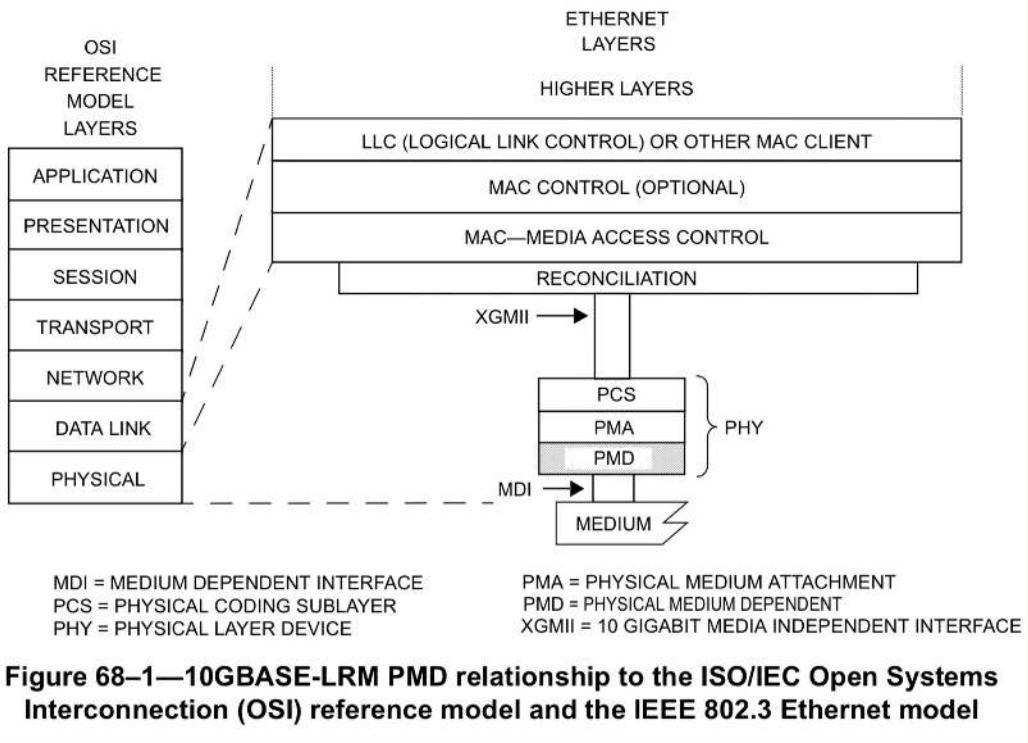
Figure 65-7—FEC coded Ethernet frame



encoded  $\rightarrow$  de encoded  
encoder  
why? 因为要保证 run parity.

另一种是降低 PMA/TBZ 的浓度。

1. 金环工时 RX 状态为 FALSE 时 TX 会切换到 IDLE，但如果不支持单工时，TX 不再需要 RX 驱动。
  2. 单工时，FAR-END fault，也不网管。
  3. 因为 ONU 会不断在 UP & DOWN 端口之间切换，问哪一个是单工？
  4. 单工时，AN 不会将 enable。
  5. R3 层 如果支持单工，如果检测到 local fault，会将 IPA 换成 remote fault，如果对端也是 enable 单工，则无视。
- b. 10h 和 P2MP 类似，支持单工时如果本地设备是单工，发 IDLE 而不是 remote fault，如果便能了单工则无视本地源，继续发送数据。
7. linkspan → 那线长



**Figure 68–1—10GBASE-LRM PMD relationship to the ISO/IEC Open Systems Interconnection (OSI) reference model and the IEEE 802.3 Ethernet model**

**Table 68–2—10GBASE-LRM fiber types and operating ranges**

Multimode fiber type <sup>a</sup>	ISO/IEC 11801:2002 fiber type	Operating range (m)	Maximum channel insertion loss (dB) <sup>b</sup>
62.5 µm 160/500 <sup>c</sup>		0.5 to 220	1.9
62.5 µm 200/500	OM1	0.5 to 220	1.9
50 µm 500/500	OM2	0.5 to 220	1.9
50 µm 400/400		0.5 to 100	1.7
50 µm 1500/500 <sup>d</sup>	OM3	0.5 to 220	1.9

<sup>a</sup>Each fiber type is identified by its core diameter followed by a pair of OFL bandwidth values separated by “/”. The OFL bandwidths are in MHz · km and are for 850 nm and 1300 nm respectively.

<sup>b</sup>Channel insertion loss includes cabled optical fiber attenuation and an allocation of 1.5 dB for connectors.

<sup>c</sup>160/500, 62.5 µm fiber is commonly referred to as “FDDI-grade” fiber.

<sup>d</sup>The OM3 fiber specification includes the 850 nm laser launch bandwidth in addition to the OFL bandwidths.

# Backplane Ethernet – electrical backplane

- 1000BASE-KX for 1 Gb/s operation over a single lane
- 10GBASE-KX4 for 10 Gb/s operation over four lanes
- 10GBASE-KR for 10 Gb/s operation over a single lane
- 40GBASE-KR4 for 40 Gb/s operation over four lanes
- 100GBASE-KR4 and 100GBASE-KP4 for 100 Gb/s operation over four lanes

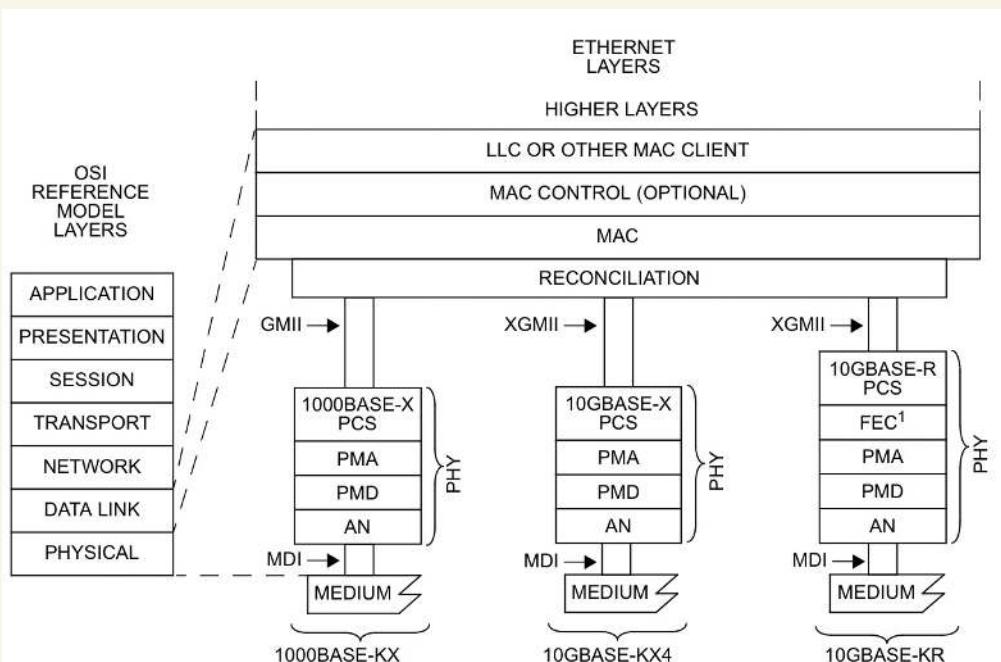
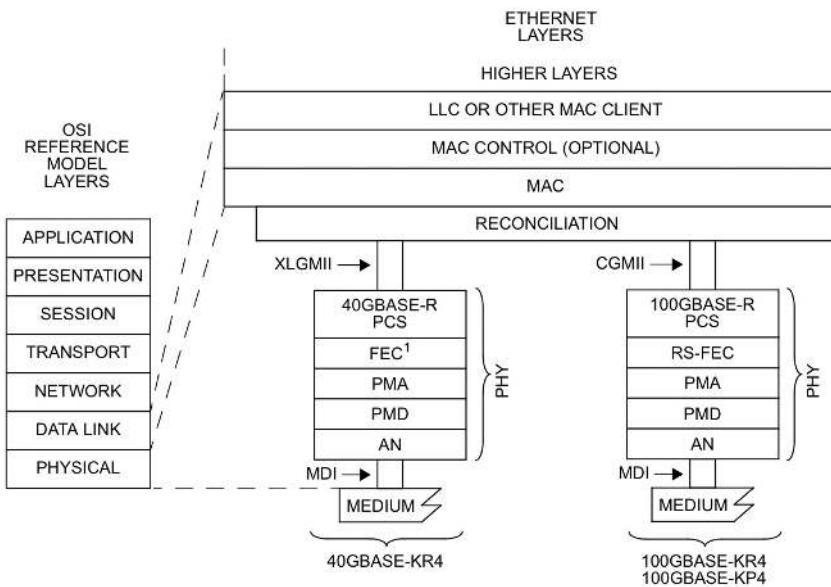


Figure 69–1—Architectural positioning of 1 Gb/s and 10 Gb/s Backplane Ethernet



AN = AUTO-NEGOTIATION

CGMII = 100 Gb/s MEDIA INDEPENDENT INTERFACE

FEC = FORWARD ERROR CORRECTION

LLC = LOGICAL LINK CONTROL

MAC = MEDIA ACCESS CONTROL

MDI = MEDIUM DEPENDENT INTERFACE

PCS = PHYSICAL CODING SUBLAYER

PHY = PHYSICAL LAYER DEVICE

PMA = PHYSICAL MEDIUM ATTACHMENT

PMD = PHYSICAL MEDIUM DEPENDENT

RS-FEC = REED-SOLOMON FEC

XLMII = 40 Gb/s MEDIA INDEPENDENT INTERFACE

NOTE 1—OPTIONAL

Figure 69–2—Architectural positioning of 40 Gb/s and 100 Gb/s Backplane Ethernet

1. 如下下列哪項是暴露出來的？

XGMII - 8位

MOTD - bitwide

XSBII - 16位

CAVI-10 - 10 Tanes

XGMII - 32位

100GBASE-X - 10bie TBI

XLAUI, CAVI-4 - 4 lanes

**Table 69–1—Nomenclature and clause correlation for 1 Gb/s and 10 Gb/s Backplane Ethernet Physical Layers**

Nomenclature	Clause																									
	35		36		46		48		49		51		70		71		72		73		74		78			
	RS	GMII	RS	XGMII	RS	10GBASE-X PCS/PMA	RS	10GBASE-X PCS/PMA	Serial PMA	RS	10GBASE-R PCS	Serial PMA	RS	1000BASE-X PCS/PMA	RS	10GBASE-KR PMD	Auto-Negotiation	RS-FEC	BASE-R FEC	Energy-Efficient Ethernet (EEE)	RS	XGMII	RS	10GBASE-X PCS/PMA		
1000BASE-KX	M <sup>a</sup>	O <sup>a</sup>	M											M										O		
10GBASE-KX4					M	O	M							M		M			M		M		O			
10GBASE-KR					M	O		M	M					M		M	M	O	O				O			

<sup>a</sup>O = Optional, M = Mandatory

**Table 69–2—Nomenclature and clause correlation for 40 Gb/s and 100 Gb/s Backplane Ethernet Physical Layers**

Nomenclature	Clause																	
	73	74	78	81		82		83		83A		83D		84		91	93	94
	Auto-Negotiation	RS	XLGMII	CGMII	40GBASE-R PCS	100GBASE-R PCS	40GBASE-R PMA	100GBASE-R PMA	XLAUI	CAUI-10	CAUI-4	40GBASE-KR4 PMD	RS-FEC	100GBASE-KR4 PMD	Auto-Negotiation	RS-FEC	100GBASE-KR4 PMD	100GBASE-KP4 PMD/PMD
40GBASE-KR4	M <sup>a</sup>	O <sup>a</sup>	O	M	O	M	M	M	O			M						
100GBASE-KR4	M		O	M		O	M	M		O	O			M	M			
100GBASE-KP4	M		O	M		O	M			O	O			M		M		

<sup>a</sup>O = Optional, M = Mandatory

AN 固定 不再是 FLP.

Table 70-1—Physical Layer clauses associated with the 1000BASE-KX PMD

Associated clause	1000BASE-KX
35—GMII <sup>a</sup>	Optional
36—1000BASE-X PCS/PMA	Required
73—Auto-Negotiation for Backplane Ethernet	Required
78—Energy-Efficient Ethernet	Optional

<sup>a</sup>The GMII is an optional interface. However, if the GMII is not implemented, a conforming implementation must behave functionally as though the RS and GMII were present.

只支持背板

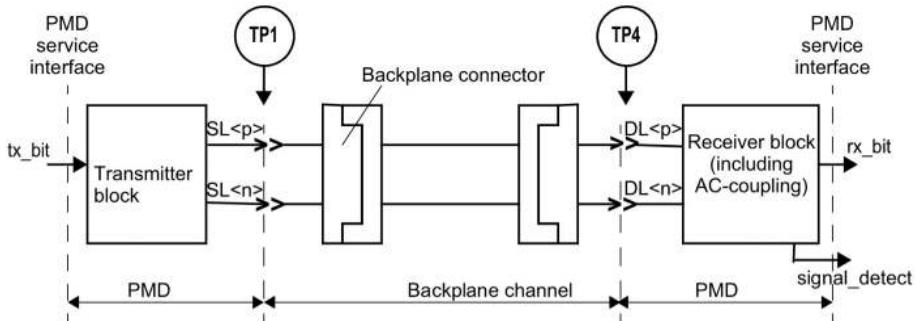


Figure 70-1—Link block diagram

LPI of SIGNAL\_DETECT to FAIL  
 TX shunted to the receiver → Loopback  
 Backplane 需要 AC-couple

$\lambda_{BVI}$   $\leq 0.5\text{m}$ , 10G BASE-KX4  $\leq 1\text{m}$ .

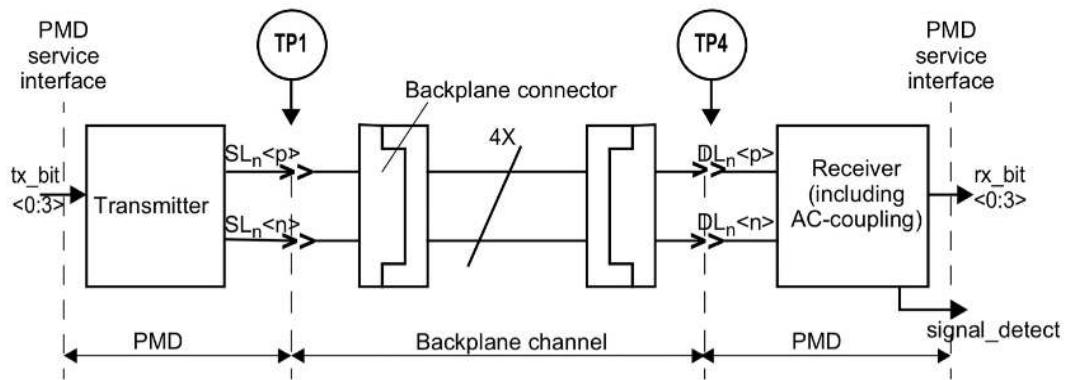


Figure 71-1—Link block diagram

4 定 lane. 由 TX PMD 送  $SL_n < p >$  到 TX-bit (0:3)  
時鐘速率 - 每 2 部份為 100 PPM -

AC-coupling .

Table 72-1—Physical Layer clauses associated with the 10GBASE-KR PMD

Associated clause	10GBASE-KR
46—XGMII <sup>a</sup>	Optional
47—XGXS and XAUI	Optional
49—10GBASE-R PCS	Required
51—10-Gigabit Serial PMA	Required
73—Auto-Negotiation for Backplane Ethernet	Required
74—BASE-R FEC	Optional
78—Energy-Efficient Ethernet	Optional

<sup>a</sup>The XGMII is an optional interface. However, if the XGMII is not implemented, a conforming implementation must behave functionally as though the RS and XGMII were present.

10GBASE-KR 的 模式有3种,

1. DATA .
2. QUIET  $\neq$  ECE
3. ALERT

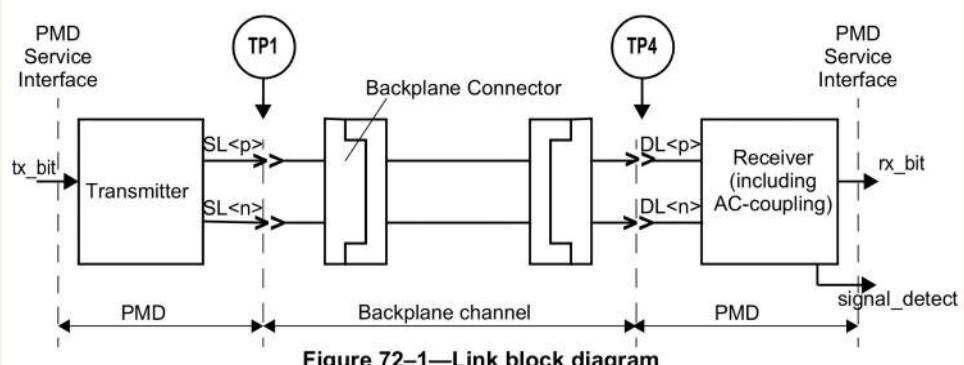


Figure 72-1—Link block diagram

## Octets

4	Frame marker	Control channel
16	Coefficient update	
16	Status report	
512	Training pattern	

Figure 72–2—Training frame structure

1. 使用曼彻斯特编码  $\neg \rightarrow 1 \quad 1 \rightarrow 0$

Table 72–4—Coefficient update field

Cell(s)	Name	Description										
15:14	Reserved	Transmitted as 0, ignored on reception.										
13	Preset	1 = Preset coefficients 0 = Normal operation										
12	Initialize	1 = Initialize coefficients 0 = Normal operation										
11:6	Reserved	Transmitted as 0, ignored on reception.										
5:4	Coefficient (+1) update	<table> <tr><td>5</td><td>4</td></tr> <tr><td>1</td><td>1 = reserved</td></tr> <tr><td>0</td><td>1 = increment</td></tr> <tr><td>1</td><td>0 = decrement</td></tr> <tr><td>0</td><td>0 = hold</td></tr> </table>	5	4	1	1 = reserved	0	1 = increment	1	0 = decrement	0	0 = hold
5	4											
1	1 = reserved											
0	1 = increment											
1	0 = decrement											
0	0 = hold											
3:2	Coefficient (0) update	<table> <tr><td>3</td><td>2</td></tr> <tr><td>1</td><td>1 = reserved</td></tr> <tr><td>0</td><td>1 = increment</td></tr> <tr><td>1</td><td>0 = decrement</td></tr> <tr><td>0</td><td>0 = hold</td></tr> </table>	3	2	1	1 = reserved	0	1 = increment	1	0 = decrement	0	0 = hold
3	2											
1	1 = reserved											
0	1 = increment											
1	0 = decrement											
0	0 = hold											
1:0	Coefficient (-1) update	<table> <tr><td>1</td><td>0</td></tr> <tr><td>1</td><td>1 = reserved</td></tr> <tr><td>0</td><td>1 = increment</td></tr> <tr><td>1</td><td>0 = decrement</td></tr> <tr><td>0</td><td>0 = hold</td></tr> </table>	1	0	1	1 = reserved	0	1 = increment	1	0 = decrement	0	0 = hold
1	0											
1	1 = reserved											
0	1 = increment											
1	0 = decrement											
0	0 = hold											

**Table 72-5—Status report field**

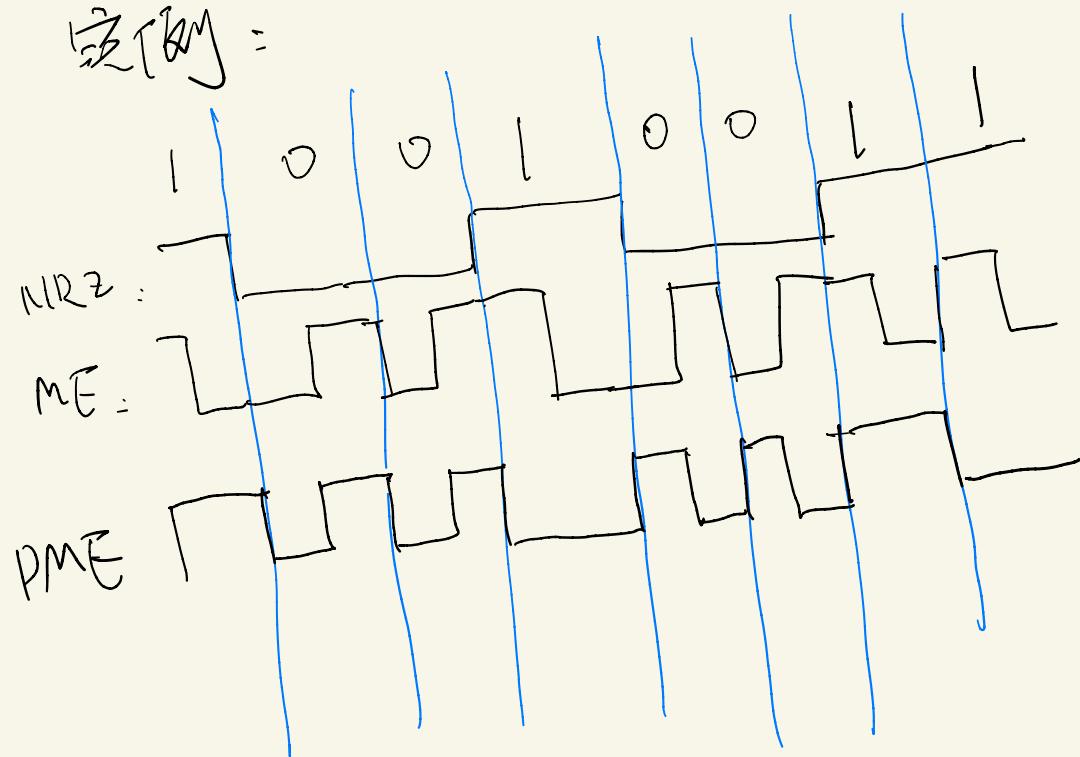
Cell(s)	Name	Description
15	Receiver ready	1 = The local receiver has determined that training is complete and is prepared to receive data. 0 = The local receiver is requesting that training continue.
14:6	Reserved	Transmitted as 0, ignored on reception.
5:4	Coefficient (+1) status	5    4 1    1 = maximum 1    0 = minimum 0    1 = updated 0    0 = not_updated
3:2	Coefficient (0) status	3    2 1    1 = maximum 1    0 = minimum 0    1 = updated 0    0 = not_updated
1:0	Coefficient (-1) status	1    0 1    1 = maximum 1    0 = minimum 0    1 = updated 0    0 = not_updated

差分曼彻斯特编码:

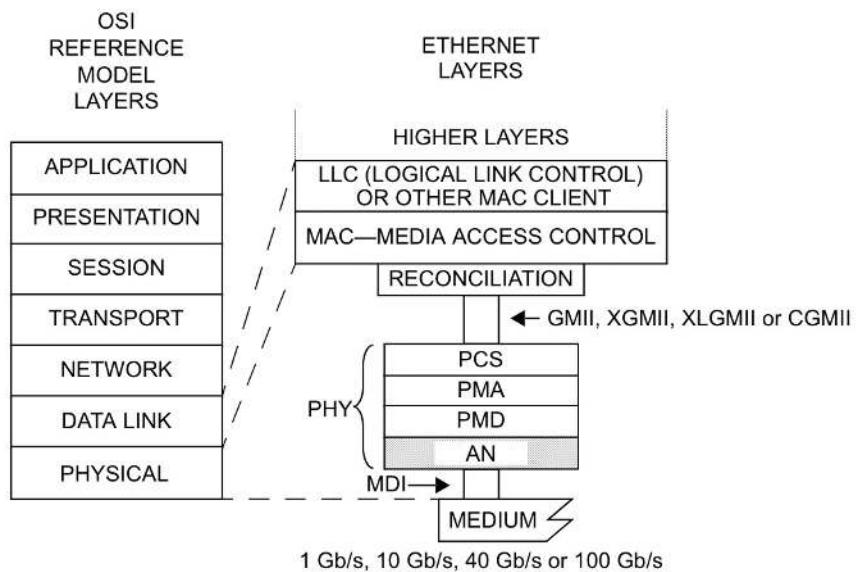
1. 带标边界肯定有跳变，下加时钟
2. 时钟边界内的带标有变化为0.

否则为1

波形图：



1. 支持 AN 的设备也有检测机制去支持非 AN 的设备
2. 1000BASE-KX AN 和 Flow 37 不兼容（需要特殊实现）



AN = AUTO-NEGOTIATION

CGMII = 100 Gb/s MEDIA INDEPENDENT INTERFACE

GMII = GIGABIT MEDIA INDEPENDENT INTERFACE

MDI = MEDIUM DEPENDENT INTERFACE

PCS = PHYSICAL CODING SUBLAYER

PHY = PHYSICAL LAYER DEVICE

PMA = PHYSICAL MEDIUM ATTACHMENT

PMD = PHYSICAL MEDIUM DEPENDENT

XGMII = 10 Gb/s MEDIA INDEPENDENT INTERFACE

XLGMII = 40 Gb/s MEDIA INDEPENDENT INTERFACE

**Figure 73–1—Location of Auto-Negotiation function within the ISO/IEC OSI reference model**

3. 支持 1000BASE-KX, 10GBASE-KX4, 10GBASE-KR, 40GBASE-KR4, 40GBASE-CR4, 100GBASE-CR10, 100GBASE-KP4, 100GBASE-KR4, 100GBASE-CR4.

4. 由 Tone 的速度，AIN 同 Come 0. (實際實現可配置非Tone)
5. 传输曼彻斯特特碼，有 violation delimiter，即  
在两个 transmission 间有 T interval.

## 6. PAGE ENCODING

10b transitions = 8 分隔符

$$\begin{array}{c}
 + \quad \text{49 位元} \\
 \text{P8} \quad \swarrow \quad \text{49 數字} \\
 \downarrow \\
 48 + 1
 \end{array}$$

### 73.5.3.1 Manchester violation delimiter

A violation is signaled as shown in Figure 73-5.

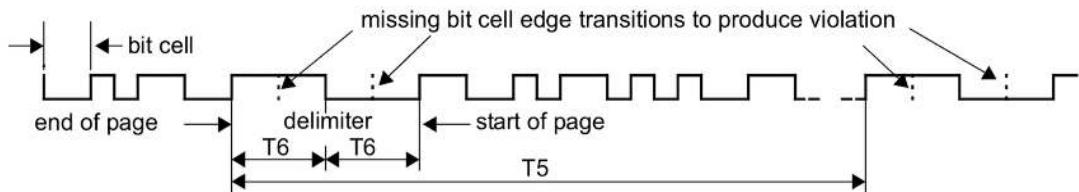


Figure 73-5—Manchester violation

D 0	D 1	D 2	D 3	D 4	D 5	D 6	D 7	D 8	D 9	D 10	D 11	D 12	D 13	D 14	D 15
S 0	S 1	S 2	S 3	S 4	E 0	E 1	E 2	E 3	E 4	C 0	C 1	C 2	RF	Ack	NP

D 16	D 17	D 18	D 19	D 20	D 21	D 22	D 23	D 24	D 25	D 26	D 27	D 28	D 45	D 46	D 47
T 0	T 1	T 2	T 3	T 4	A 0	A 1	A 2	A 3	A 4	A 5	A 6	A 7	A 24	F 0	F 1

Figure 73–6—Link codeword Base Page

D[4:0] contains the Selector Field. D[9:5] contains the EchoedNonce field. D[12:10] contains capability bits to advertise capabilities not related to the PHY. C[1:0] is used to advertise pause capability. The remaining capability bit C[2] is reserved. D[15:13] contains the RF, Ack, and NP bits. These bits shall function as specified in 28.2.1.2. D[20:16] contains the TransmittedNonce field. D[45:21] contains the Technology Ability Field. D[47:46] contains FEC capability (see 73.6.5).

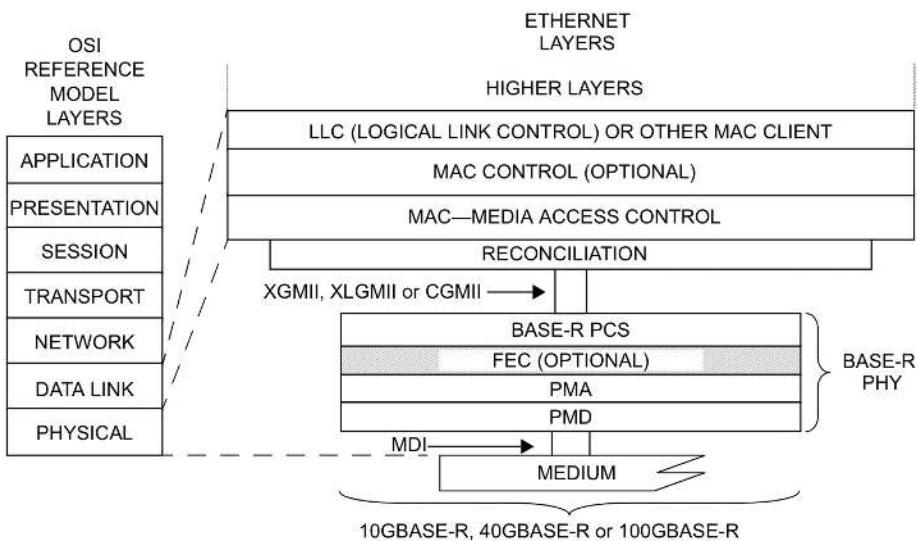
Link-control = TRUE. 代表 AIN 指令  
 這個字號

Table 73–5—Priority Resolution

Priority	Technology	Capability
1	100GBASE-CR4	100 Gb/s 4 lane, highest priority
2	100GBASE-KR4	100 Gb/s 4 lane
3	100GBASE-KP4	100 Gb/s 4 lane
4	100GBASE-CR10	100 Gb/s 10 lane
5	40GBASE-CR4	40 Gb/s 4 lane
6	40GBASE-KR4	40 Gb/s 4 lane
7	10GBASE-KR	10 Gb/s 1 lane
8	10GBASE-KX4	10 Gb/s 4 lane
9	1000BASE-KX	1 Gb/s 1 lane, lowest priority

HCD - highest common denominator

对于 Ethernet for pos. 编译Tame for pos 简单一Tfec



CGMII = 100 Gb/s MEDIA INDEPENDENT INTERFACE

FEC = FORWARD ERROR CORRECTION

MDI = MEDIUM DEPENDENT INTERFACE

PCS = PHYSICAL CODING SUBLAYER

PHY = PHYSICAL LAYER DEVICE

PMA = PHYSICAL MEDIUM ATTACHMENT

PMD = PHYSICAL MEDIUM DEPENDENT

XGMII = 10 Gb/s MEDIA INDEPENDENT INTERFACE

XLGMII = 40 Gb/s MEDIA INDEPENDENT INTERFACE

**Figure 74–1—BASE-R FEC relationship to ISO/IEC Open Systems Interconnection (OSI) reference model and the IEEE 802.3 Ethernet model**

Figure 74-2 shows the functional block diagram of FEC for 10GBASE-R PHY and the relationship between PCS and PMA sublayers.

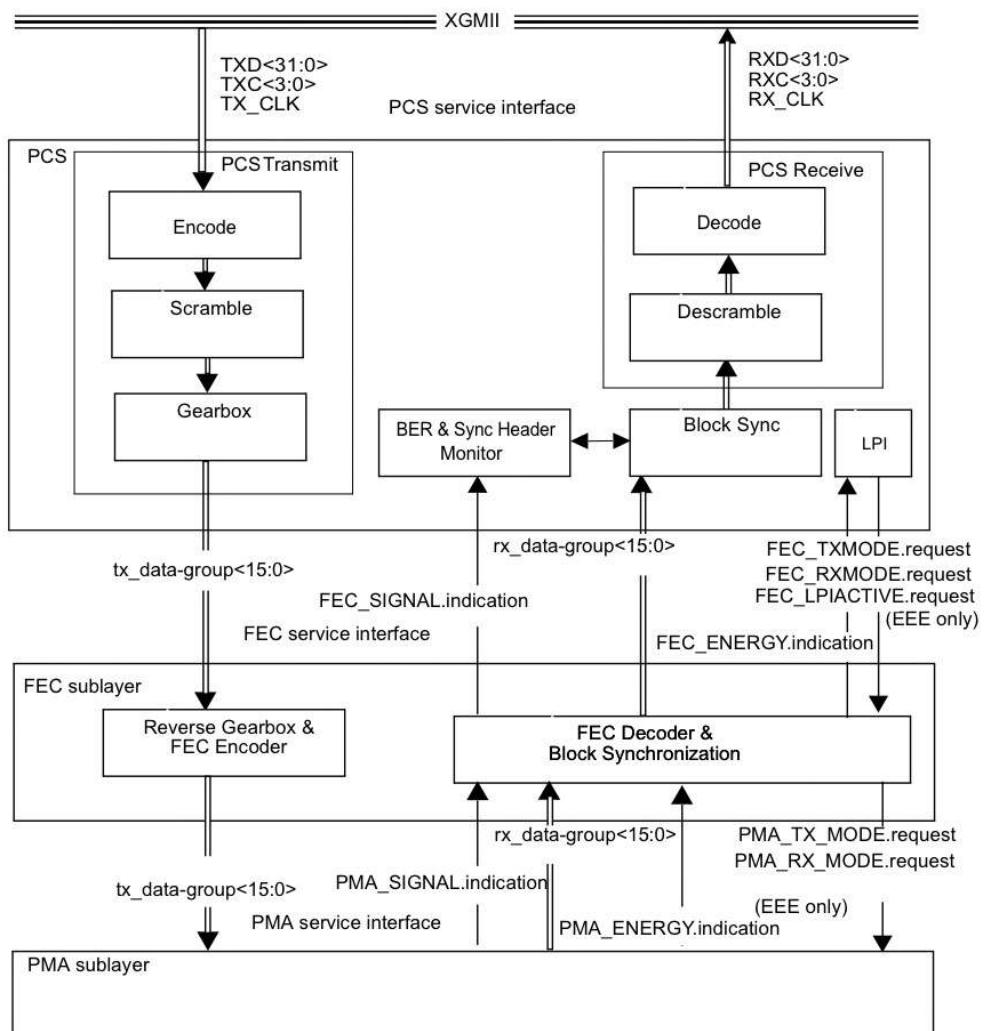


Figure 74-2—Functional block diagram for 10GBASE-R PHYs

1. 2080 bits 轉換成 2112 bits, 和之前 FEC  
相比, 不同於 PCS 的映射圖。

Figure 74-3 shows the functional block diagram of FEC for 40GBASE-R PHYs and the relationships between the PCS and PMA sublayers.

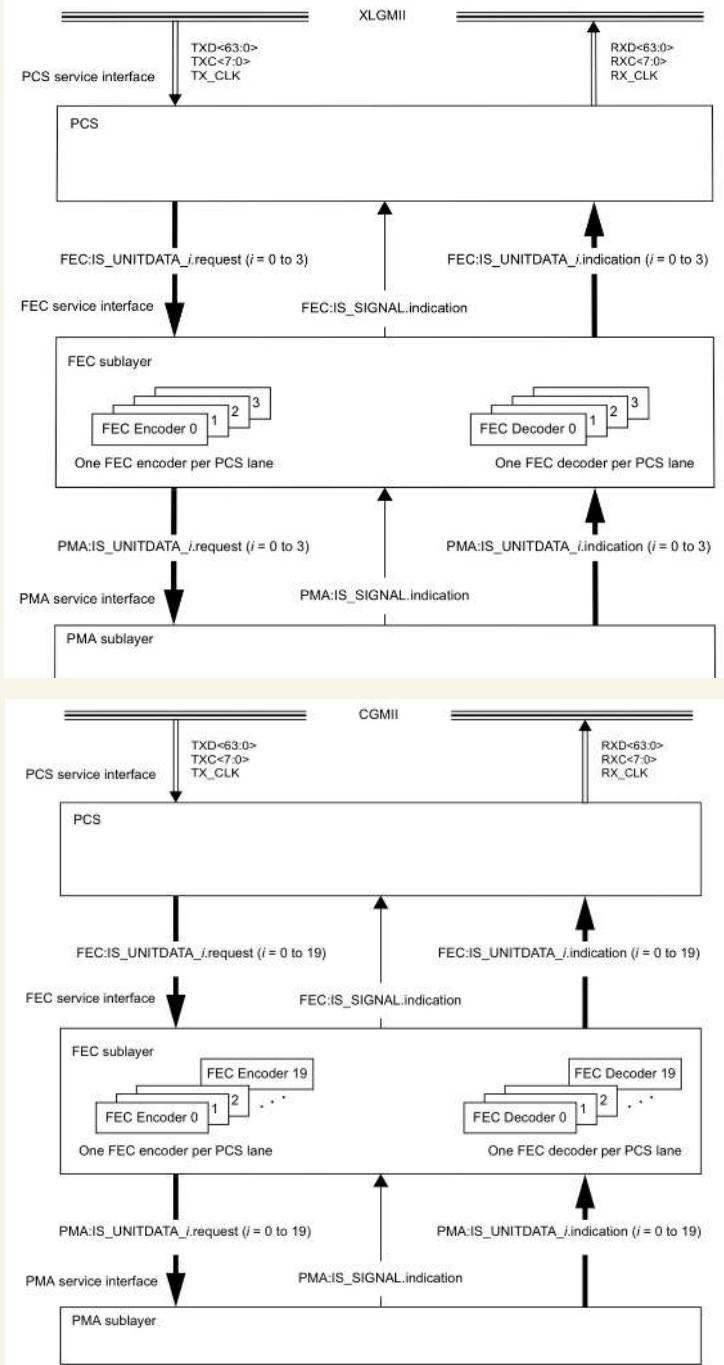


Figure 74-4—Functional block diagram for 100GBASE-R PHY

2. 每字节 11 bit  $\frac{11}{12} \times 2080 + 32$
3. 格式 - 由 64 payload  $\xrightarrow{\text{+32}} 1$  bit overhead,  $\xrightarrow{\text{+32}}$   
后会加上 32 为 parity bits.

Table 74-1—FEC block format

T <sub>0</sub>	64 bit payload Word 0	T <sub>1</sub>	64 bit payload Word 1	T <sub>2</sub>	64 bit payload Word 2	T <sub>3</sub>	64 bit payload Word 3
T <sub>4</sub>	64 bit payload Word 4	T <sub>5</sub>	64 bit payload Word 5	T <sub>6</sub>	64 bit payload Word 6	T <sub>7</sub>	64 bit payload Word 7
T <sub>8</sub>	64 bit payload Word 8	T <sub>9</sub>	64 bit payload Word 9	T <sub>10</sub>	64 bit payload Word 10	T <sub>11</sub>	64 bit payload Word 11
T <sub>12</sub>	64 bit payload Word 12	T <sub>13</sub>	64 bit payload Word 13	T <sub>14</sub>	64 bit payload Word 14	T <sub>15</sub>	64 bit payload Word 15
T <sub>16</sub>	64 bit payload Word 16	T <sub>17</sub>	64 bit payload Word 17	T <sub>18</sub>	64 bit payload Word 18	T <sub>19</sub>	64 bit payload Word 19
T <sub>20</sub>	64 bit payload Word 20	T <sub>21</sub>	64 bit payload Word 21	T <sub>22</sub>	64 bit payload Word 22	T <sub>23</sub>	64 bit payload Word 23
T <sub>24</sub>	64 bit payload Word 24	T <sub>25</sub>	64 bit payload Word 25	T <sub>26</sub>	64 bit payload Word 26	T <sub>27</sub>	64 bit payload Word 27
T <sub>28</sub>	64 bit payload Word 28	T <sub>29</sub>	64 bit payload Word 29	T <sub>30</sub>	64 bit payload Word 30	T <sub>31</sub>	64 bit payload Word 31
32 parity bits							

4. FEC 会压缩  $11 \times 64 / 166$  的前两个字节 (去掉第一个 bit), 这两个字节会  
上圆弧 T, 这两个字节会被拆碎以  
维持 DC BALANCE.

5. reverse gearbox, 从向下反转到  
 16 bits, FEC将其转回为 66 bits, [是吗?]  
 从 PMA 反转为 16 bits, 则由  
 16 bits → PMA 不是直接用的 16 bits, 而是由  
 需此功能 ← 拆分是 10G.  
 由 16, 100G BASE-R 的是 1 bit width.

## b. FEC Encoder

The format of the FEC block and the transmit bit ordering is shown in Figure 74-5.

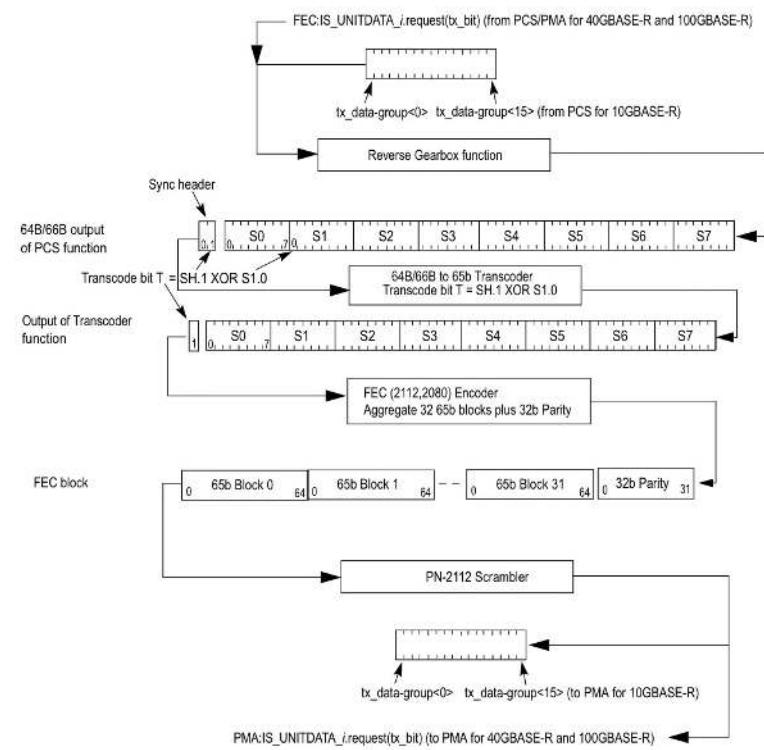


Figure 74-5—FEC Transmit bit ordering

7. DECODER - 發現錯誤後，由解出  
位 6bit 與兩個 bit, (1, 9, 17, 25, 32).  
若 8,100 GBASE-R 會設滿 32 個 symbol

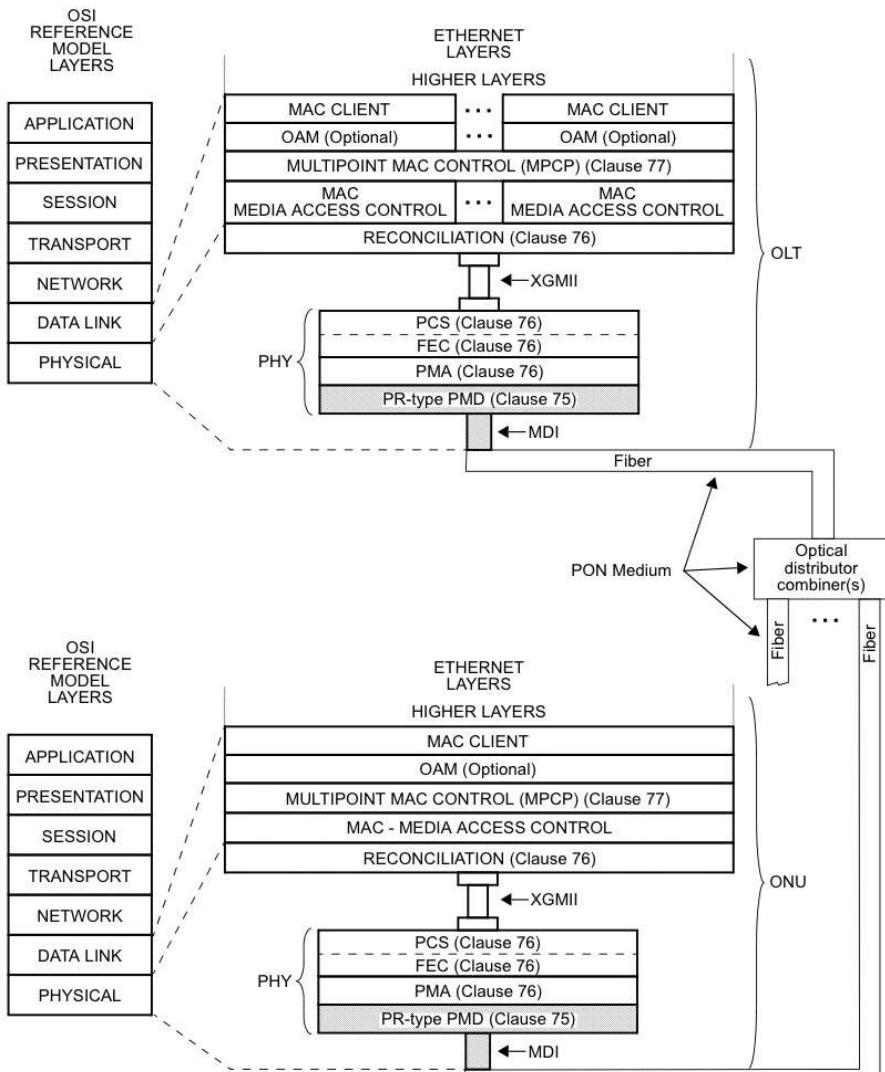
8. FEC SYNC 的方法，是不斷  
去解 bit 流找到一正確 parity [b]  
題，再持續下去 code word，如果  
一直正確，即 SYNC 上。

Table 75-1—Power budgets

Description	Low Power Budget		Medium Power Budget		High Power Budget		Extended Power Budget		Units
	PRX10	PR10	PRX20	PR20	PRX30	PR30	PRX40	PR40	
Number of fibers	1								—
Nominal downstream line rate	10.3125								GBd
Nominal upstream line rate	1.25	10.3125	1.25	10.3125	1.25	10.3125	1.25	10.3125	GBd
Nominal downstream wavelength	1577								nm
Downstream wavelength tolerance	-2, +3								nm
Nominal upstream wavelength	1310	1270	1310	1270	1310	1270	1310	1270	nm
Upstream wavelength tolerance	±50	±10	±50	±10	±50	±10	±20	±10	nm
Maximum reach <sup>a</sup>	≥10		≥20						km
Maximum channel insertion loss	20		24		29		33		dB
Minimum channel insertion loss	5		10		15		18		dB

<sup>a</sup>A compliant system may exceed the maximum reach designed for given power budget as long as optical power budget and other mandatory optical layer specifications are met.

PR - 非达标速率  
 PRX - 非达标速率.



PR-type PMD and MDI described in this clause

XGMII = 10 GIGABIT MEDIA INDEPENDENT INTERFACE

MDI = MEDIUM DEPENDENT INTERFACE

OAM = OPERATIONS, ADMINISTRATION & MAINTENANCE

OLT = OPTICAL LINE TERMINAL

ONU = OPTICAL NETWORK UNIT

PCS = PHYSICAL CODING SUBLAYER

PHY = PHYSICAL LAYER DEVICE

PMD = PHYSICAL MEDIUM DEPENDENT

**Figure 75-1—Relationship of 10/10G-EPON P2MP PMD to the ISO/IEC OSI reference model and the IEEE 802.3 Ethernet model**

PRX 相關 和 PR 單元

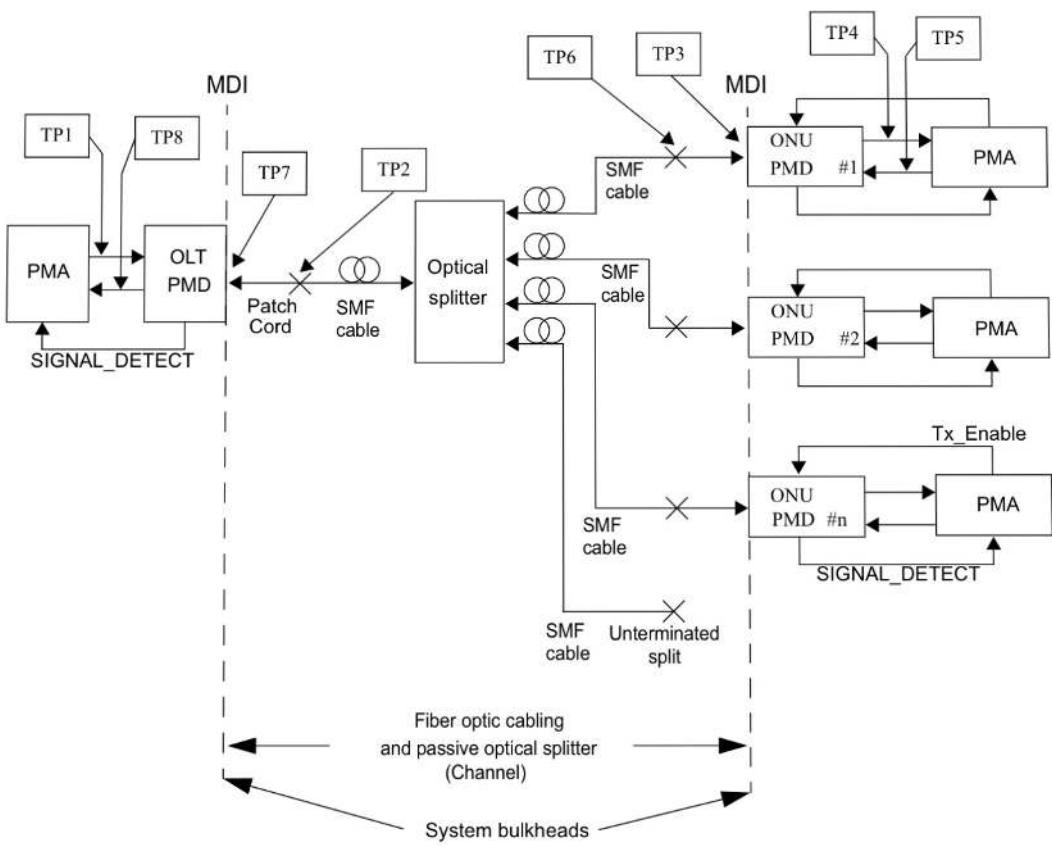
10G PR 同向走 64/66 bit

10G PRX-D

10G PRX-U 同向走 8B/10B, 同向走

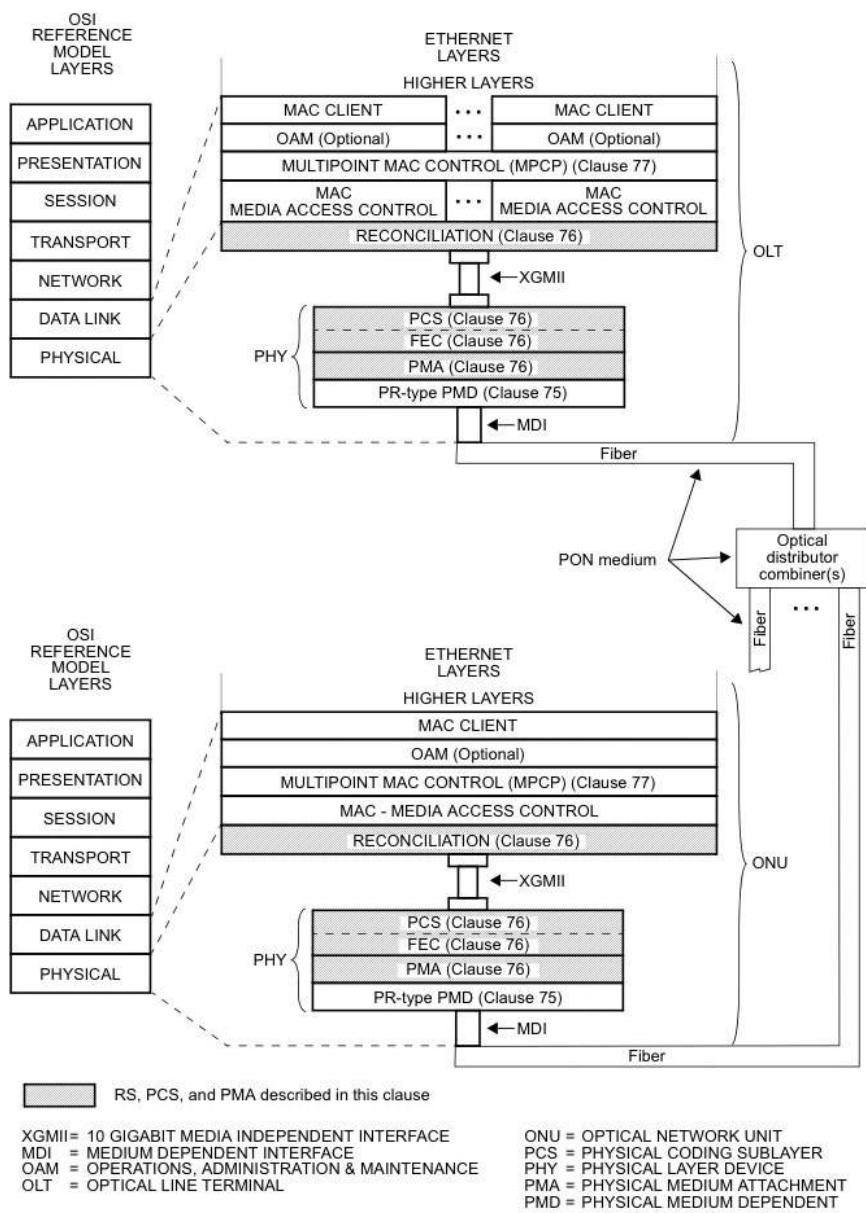
上行同向走 1G

SECTION FIVE

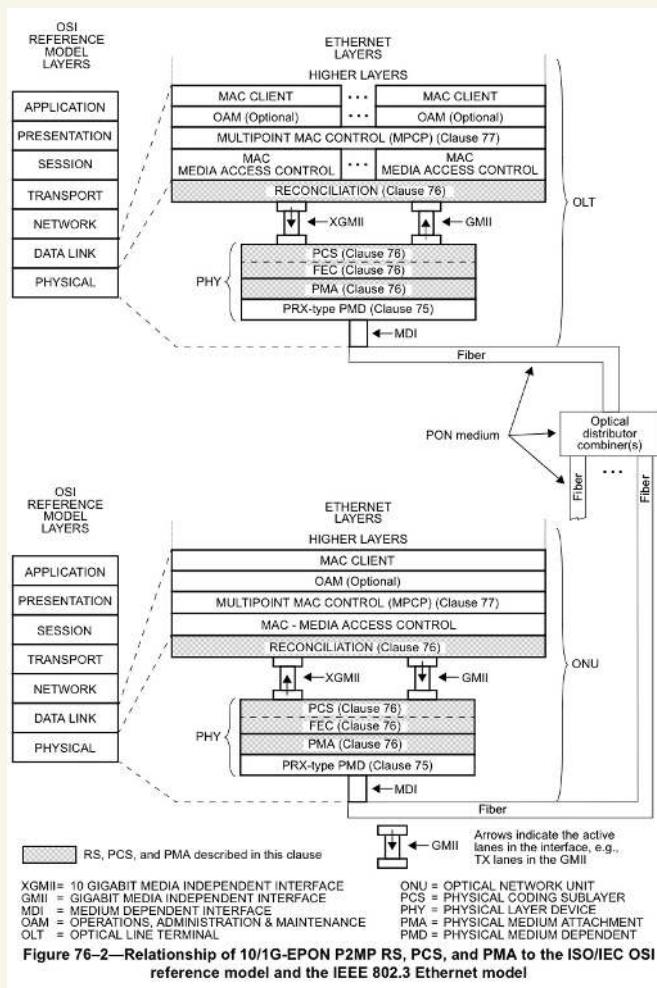


OLT 支持双速率，即同时支持  
10G & 1G，（WDM 波分复用）  
ONU 也支持双速率，因此是

TDMA



**Figure 76-1—Relationship of 10/10G-EPON P2MP RS, PCS, and PMA to the ISO/IEC OSI reference model and the IEEE 802.3 Ethernet model**



**Table 76-3—Preamble/SFD replacement mapping**

Column	Lane	Field	Preamble/SFD	Modified preamble/SFD
0	0	—	0x55	Same
	1	—	0x55	Same
	2	SLD	0x55	0xd5
	3	—	0x55	Same
1	0	—	0x55	Same
	1	LLID[15:8]	0x55	<mode, logical_link_id[14:8]> <sup>a</sup>
	2	LLID[7:0]	0x55	<logical_link_id[7:0]> <sup>b</sup>
	3	CRC8	0xd5	The 8 bit CRC calculated over column 0 lane 2 through column 1 lane 2

<sup>a</sup>mode maps to TXD[15], logical\_link\_id[14] maps to TXD[14], logical\_link\_id[8] maps to TXD[8].

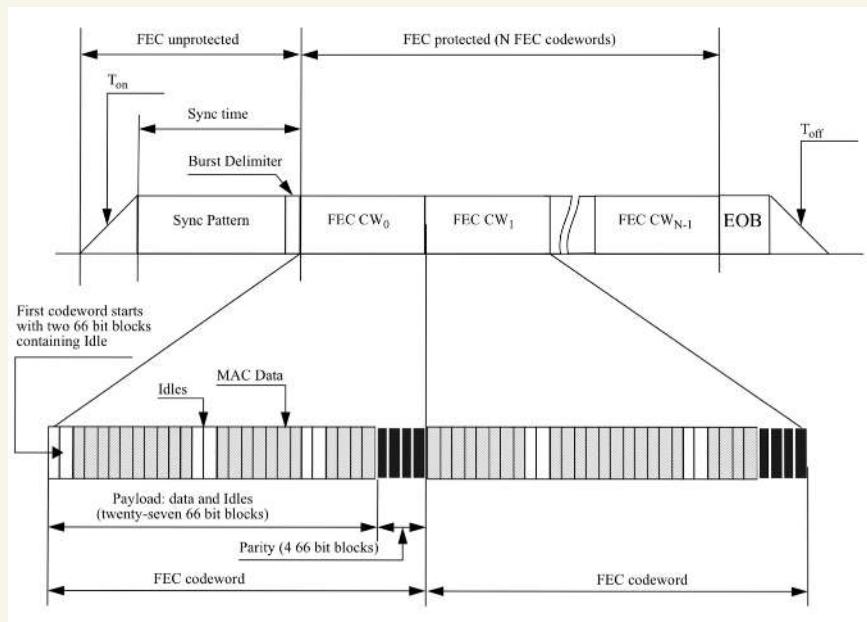
<sup>b</sup>logical\_link\_id[7] maps to TXD[23], logical\_link\_id[0] maps to TXD[16].

Table 76-4—Reserved LLID values

LLID value	Used in RS	Purpose
0x7FFF	1000BASE-PX	Downstream: 1 Gb/s SCB Upstream: ONU registration at 1 Gb/s
0x7FFE	10/1GBASE-PRX	Downstream: 10 Gb/s SCB Upstream: ONU registration at 1 Gb/s
	10GBASE-PR	Downstream: 10 Gb/s SCB Upstream: ONU registration at 10 Gb/s
0x7FFD-0x7F00	—	Reserved for future use

可选 FEC - RS(255,223)

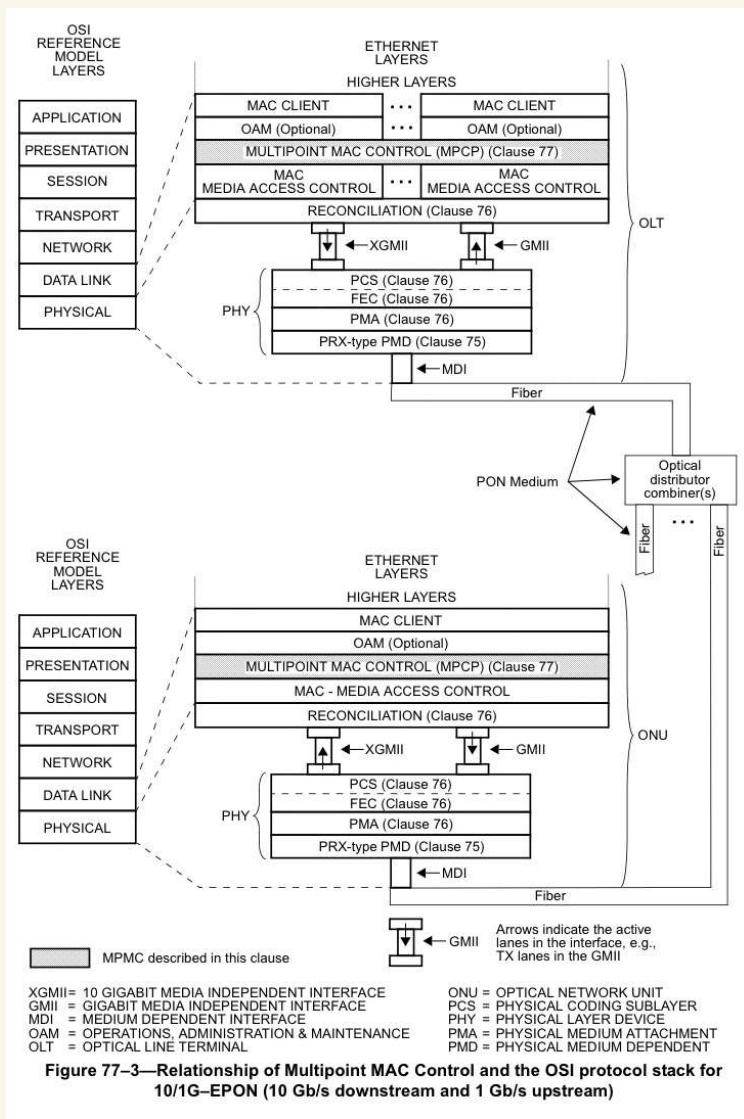
1. 每 66B 压缩成 65B
2. 每 8T bit b ~ T symbol
3. 27 个 66B 压缩成 65B, 加上 29 bits for PDI 以及  $223 \times 8$  parity portion
4.  $223 \times 8 + \underbrace{32 \times 8}_{\text{parity portion}} = 255 \text{ symbol}$



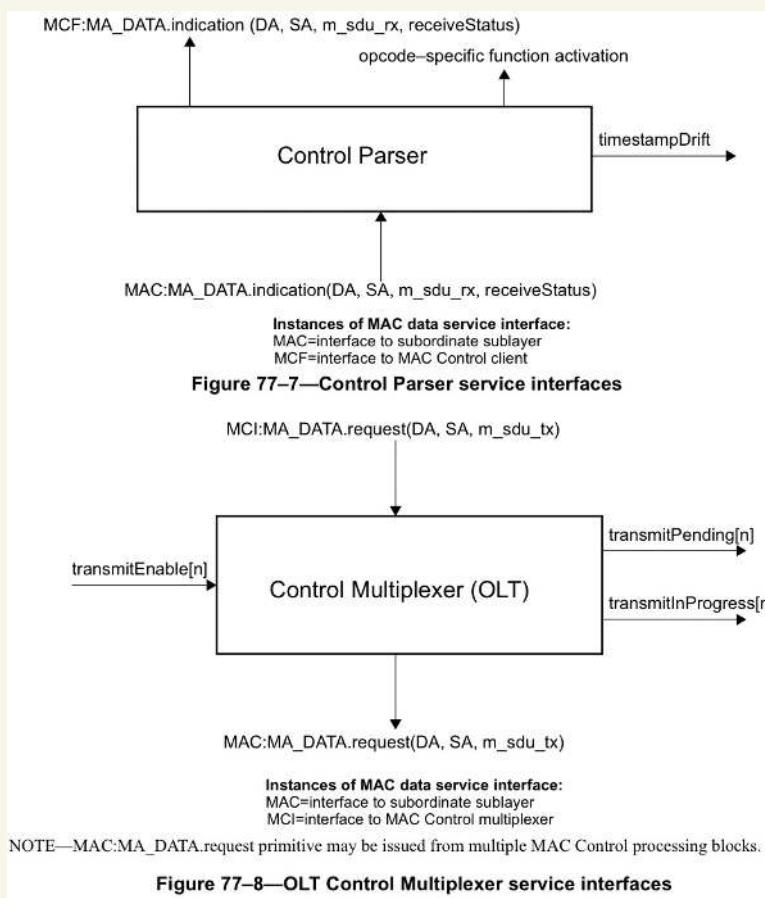
1. 將  $10G/1G$  由 ONU  $\xrightarrow{\text{PMD}}$  RX  $\rightarrow 10.3125 / 16$   
     由光纖  $\leftarrow \begin{cases} \text{PMD} & \text{TX} \rightarrow 1.25 / 10 \end{cases}$
- 2 - PMD 42列  $\rightarrow$  FEC decoder 會移除 parity code.  
     (此時需要插入 IDLE 來保證 MII 同步)

PON = optical fiber, splices, splitters.

接入网前一个明显的特点，就是服务端一分为多模式，多户端之间无法直接通信。



- multiple transmission  
同一时刻只有1个MAC client能传输数据
- OLT 对于 MAC 层是透明的



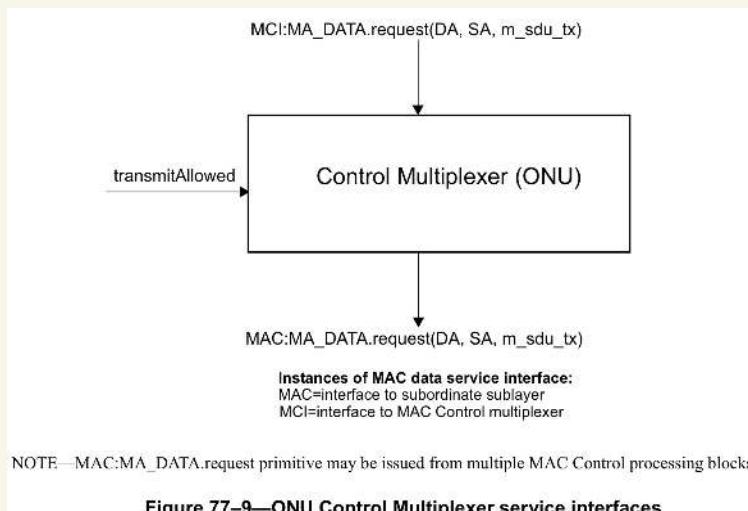


Figure 77–9—ONU Control Multiplexer service interfaces

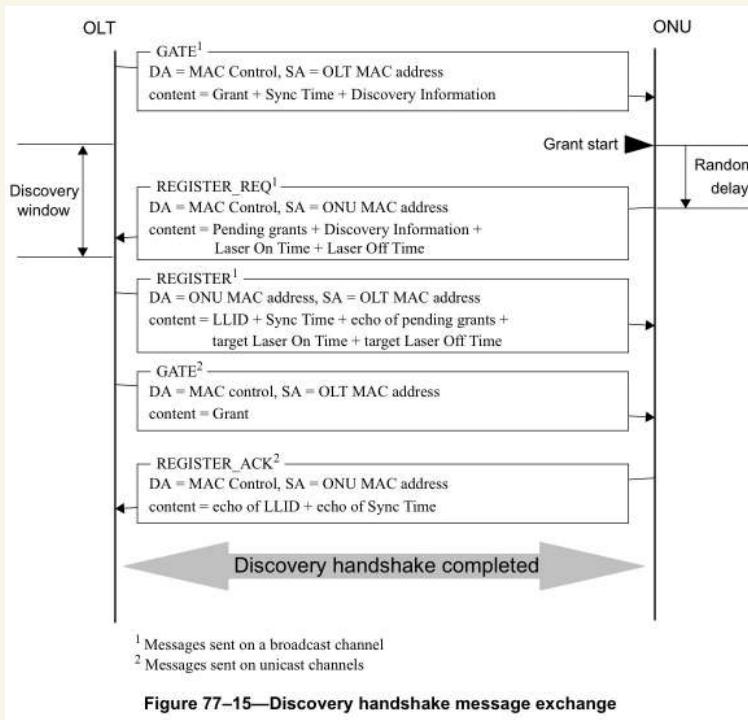


Figure 77–15—Discovery handshake message exchange

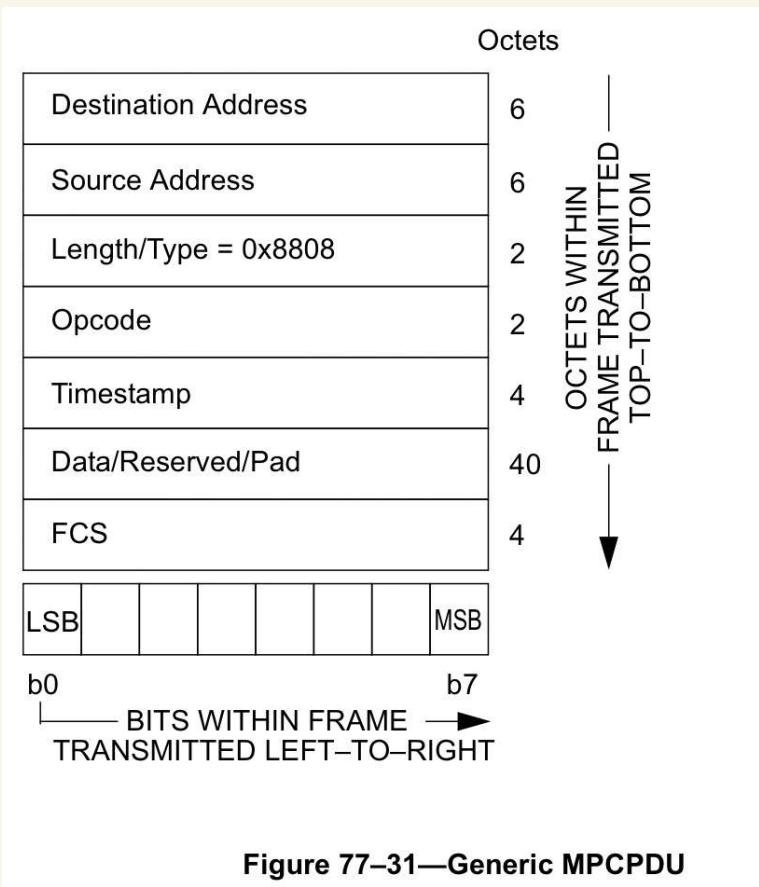
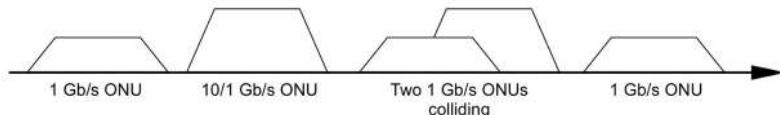


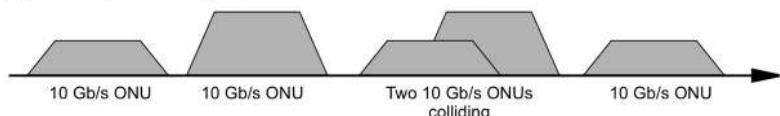
Figure 77-31—Generic MPCPDU

3. GATE Message 由OLT到ONU  
的帧。Report由ONU到OLT  
的帧。
4. Discovery 中由OLT发起  
Request 由ONU应答。

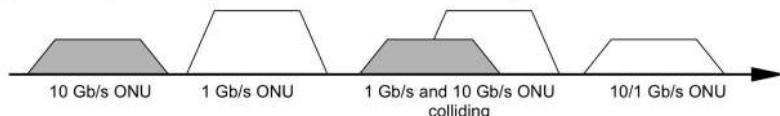
(a) Discovery window opened for 1 Gb/s upstream transmission



(b) Discovery window opened for 10 Gb/s upstream transmission



(c) Discovery window opened for both 1 Gb/s and 10 Gb/s upstream transmission



**Figure 77-37—Combinations of REGISTER\_REQ MPCPDUs during discovery window for 10G-EPON and 1G-EPON coexisting in the same PON**

5. DLT 由同一個向 10G 和 1G 下發  
在 discovery，10G 的消息中有碰撞信息。  
 $0x7FFF \rightarrow 1G$   
 $0x7FFE \rightarrow 10G$

**Table 77-9—Discovery GATE MPCPDUs for all ONU types**

ONU types targeted by discovery GATE MPCPDU	LLID of discovery GATE(s)	Discovery information			
		Upstream capable		Discovery window	
		1G	10G	1G	10G
1G-EPON	0x7FFF	No Discovery Information field present			
10/1G-EPON	0x7FFE	1	0	1	0
1G EPON and 10/1G EPON	0x7FFF <sup>a</sup>	No Discovery Information field present			
10/10G-EPON	0x7FFE	1	0	1	0
10/1G-EPON and 10/10G-EPON	0x7FFE	0	1	0	1
1G-EPON, 10/1G-EPON, and 10/10G-EPON	0x7FFF <sup>a</sup>	No Discovery Information field present			
	0x7FFE <sup>a</sup>	1	1	1	1

<sup>a</sup>Two discovery GATE MPCPDUs are transmitted in two separate downstream broadcast channels: one with the LLID of 0x7FFF transmitted in the 1 Gb/s downstream broadcast channel and another one the LLID of 0x7FFE transmitted in the 10 Gb/s downstream broadcast channel.

Figure 78–1 depicts the LPI Client and the RS interlayer service interfaces.

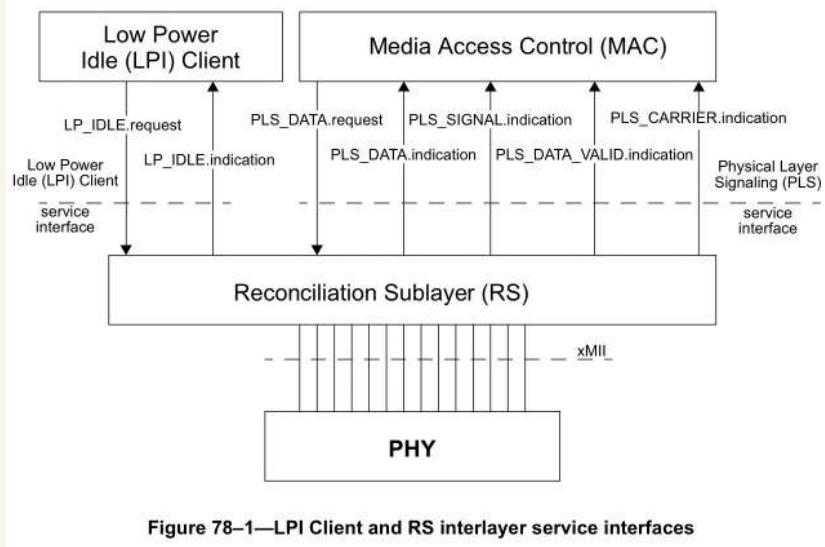


Figure 78–1—LPI Client and RS interlayer service interfaces

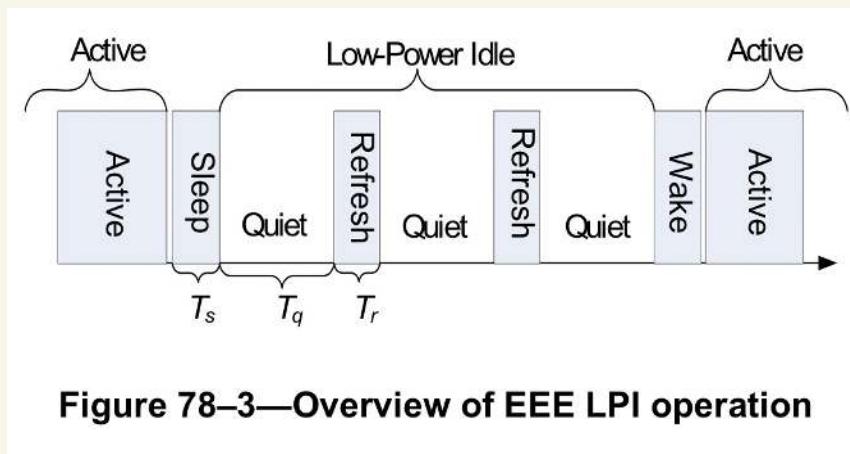
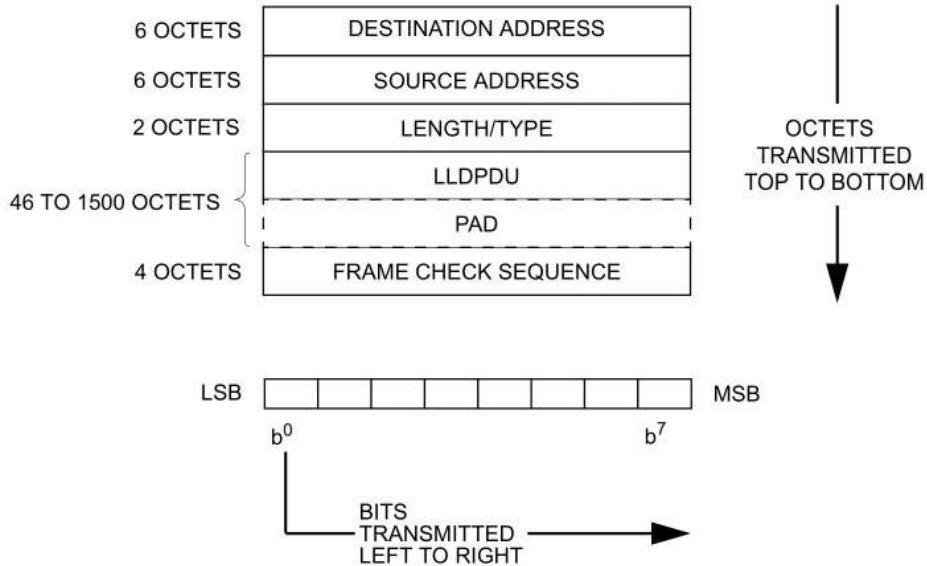


Figure 78–3—Overview of EEE LPI operation

超过40G的EEE有 deep sleep 和 fast wake 两种模式  
通过MAC的LLDP协议来配置EEE PLV.

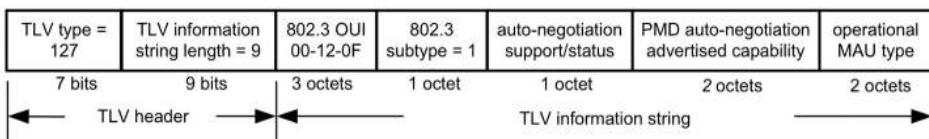


**Figure 79–1—IEEE 802.3 LLDP frame format**

**Table 79–1—IEEE 802.3 Organizationally Specific TLVs**

IEEE 802.3 subtype	TLV name	Subclause reference
1	MAC/PHY Configuration/Status	79.3.1
2	Power Via Medium Dependent Interface (MDI)	79.3.2
3	Link Aggregation (deprecated)	79.3.3
4	Maximum Frame Size	79.3.4
5	Energy-Efficient Ethernet	79.3.5
6	EEE fast wake	79.3.6
7 to 255	Reserved	—

Figure 79–2 shows the format of this TLV.



**Figure 79–2—MAC/PHY configuration/status TLV format**

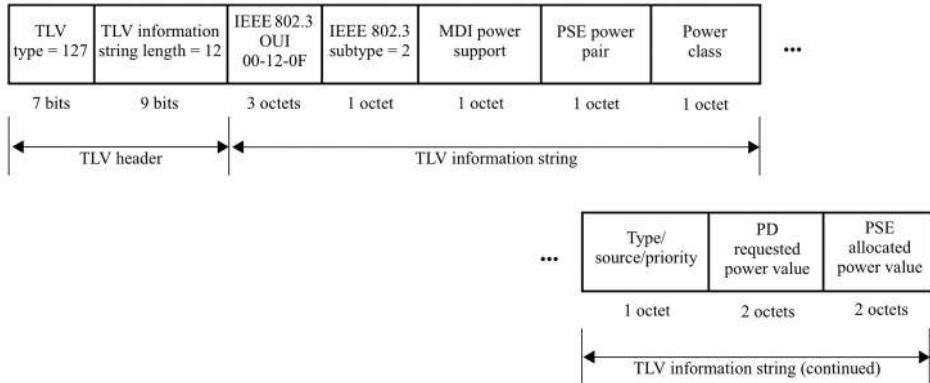


Figure 79–3—Power Via MDI TLV format

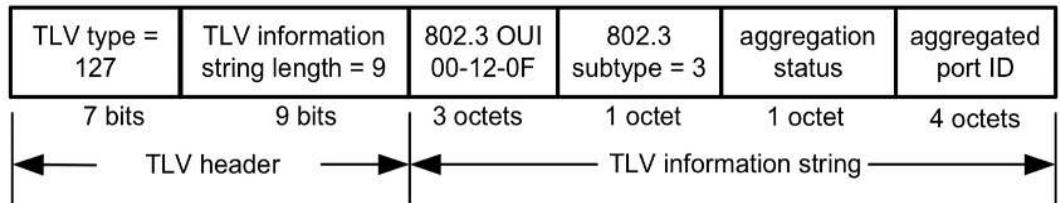


Figure 79–4—Link Aggregation TLV format

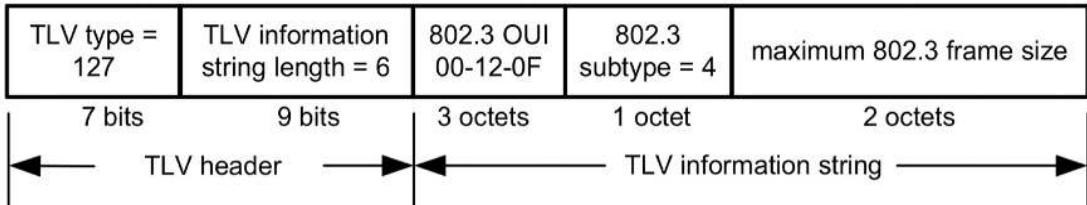


Figure 79–5—Maximum Frame Size TLV format

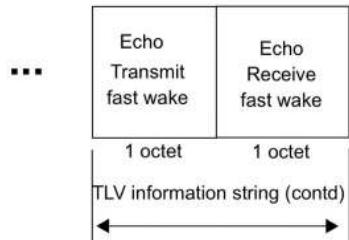
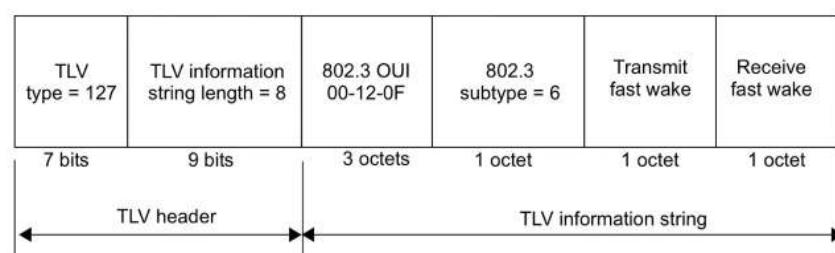
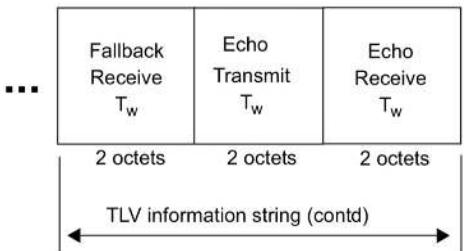
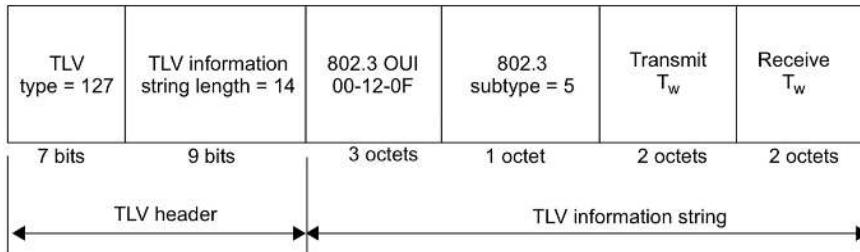
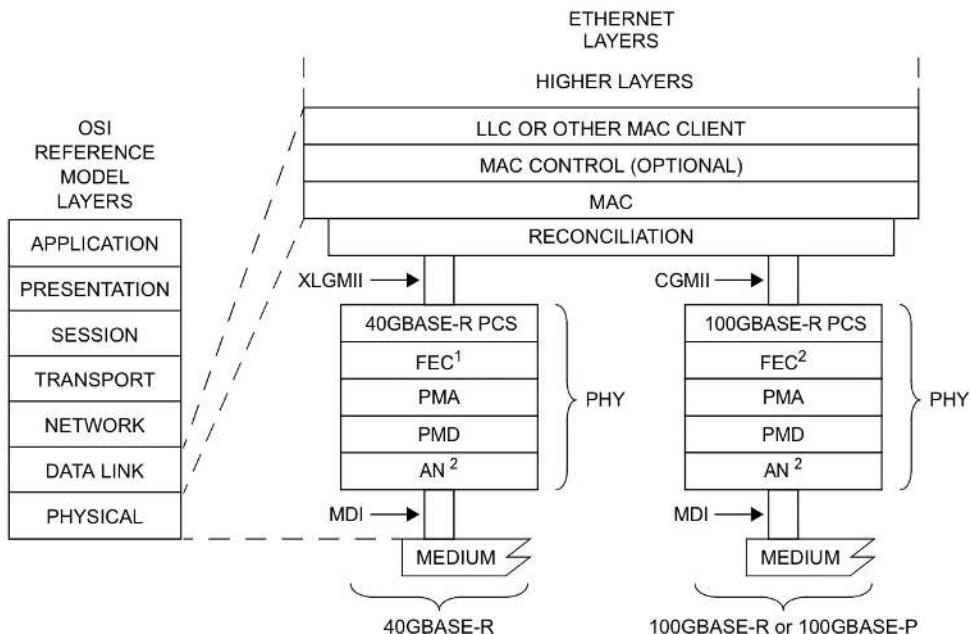


Figure 79-7—EEE Fast Wake TLV format

此章是LLDP 协议行不行



AN = AUTO-NEGOTIATION

CGMII = 100 Gb/s MEDIA INDEPENDENT INTERFACE

FEC = FORWARD ERROR CORRECTION

LLC = LOGICAL LINK CONTROL

MAC = MEDIA ACCESS CONTROL

MDI = MEDIUM DEPENDENT INTERFACE

PCS = PHYSICAL CODING SUBLAYER

PHY = PHYSICAL LAYER DEVICE

PMA = PHYSICAL MEDIUM ATTACHMENT

PMD = PHYSICAL MEDIUM DEPENDENT

XLMII = 40 Gb/s MEDIA INDEPENDENT INTERFACE

NOTE 1—OPTIONAL OR OMITTED DEPENDING ON PHY TYPE

NOTE 2—CONDITIONAL BASED ON PHY TYPE

**Figure 80–1—Architectural positioning of 40 Gigabit and 100 Gigabit Ethernet**

**Table 80–2—Nomenclature and clause correlation (40GBASE)**

Nomenclature	Clause <sup>a</sup>														
	73	74	78	RS	XLGMII	40GBASE-R PCS	83	83A	83B	84	85	86	86A	87	89
40GBASE-KR4	M	O	O	M	O	M	M	O		M				40GBASE-LR4 PMD	
40GBASE-CR4	M	O	O	M	O	M	M	O		M				40GBASE-FR4 PMD	
40GBASE-SR4			O	M	O	M	M	O	O		M	O		40GBASE-SR4 PMD	
40GBASE-FR			O	M	O	M	M	O	O						M
40GBASE-LR4			O	M	O	M	M	O	O			O	M		
40GBASE-ER4			O	M	O	M	M	O	O						M

<sup>a</sup>O = Optional, M = Mandatory.

**Table 80-3—Nomenclature and clause correlation (100GBASE copper)**

Nomenclature	Clause <sup>a</sup>														
	73	74	78	EEE		81	82	83	83A	83D	85	91	92	93	94
	EEE	RS	CGMII	100GBASE-R PCS	100GBASE-R PMMA	CAUI-10	CAUI-10	CAUI-4	CAUI-4	CAUI-4	100GBASE-CR10 PMD	RS-FEC	100GBASE-KR4 PMD	100GBASE-KP4 PMD	100GBASE-KP4 PMD
100GBASE-KR4	M		O	M	O	M	M	M	O	O	M		M		
100GBASE-KP4	M		O	M	O	M	O	O	O		M			M	
100GBASE-CR4	M		O	M	O	M	M	M	O	O	M	M			
100GBASE-CR10	M	O	O	M	O	M	M	O	O	M					

<sup>a</sup>O = Optional, M = Mandatory.

**Table 80-4—Nomenclature and clause correlation (100GBASE optical)**

Nomenclature	Clause <sup>a</sup>														
	78	81	82	83	83A	83B	83D	83E	86	86A	88	91	92	93	95
	EEE	RS	CGMII	100GBASE-R PCS	100GBASE-R PMMA	CAUI-10	CAUI-10	CAUI-4	CAUI-4	100GBASE-SR10 PMD	CPPI	100GBASE-LR4 PMD	100GBASE-ER4 PMD	RS-FEC	100GBASE-SR4 PMD
100GBASE-SR10	O	M	O	M	M	O	O	O	O	M	O				
100GBASE-SR4	O	M	O	M	M	O	O	O	O				M	M	
100GBASE-LR4	O	M	O	M	M	O	O	O	O			M			
100GBASE-ER4	O	M	O	M	M	O	O	O	O			M			

<sup>a</sup>O = Optional, M = Mandatory.

40G 80G 100G 各種規格支持 deep sleep 等  
PCIE 不支持入 EEE, LPI 模式

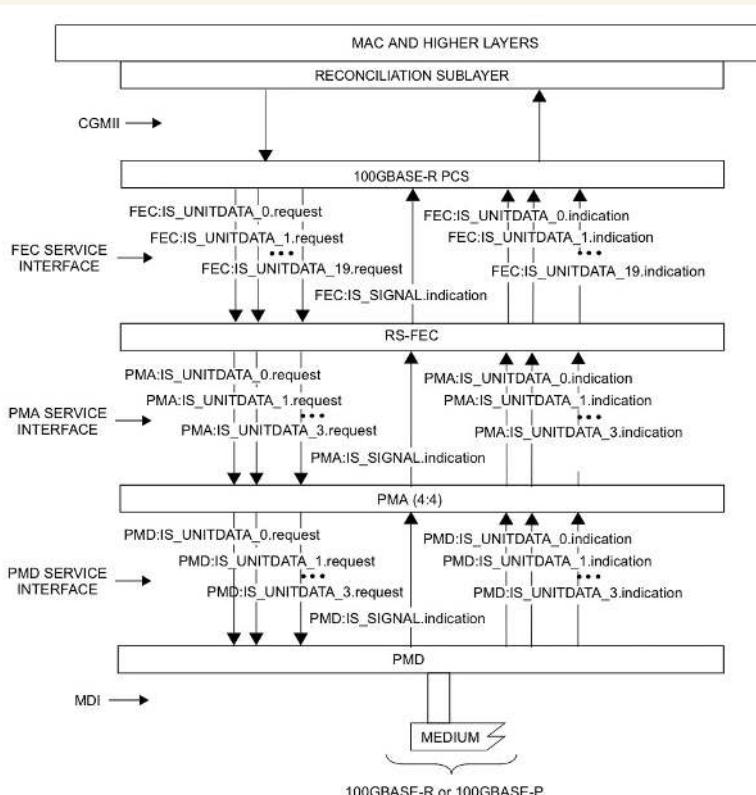
### 80.3.3.1 IS\_UNITDATA\_i.request

The IS\_UNITDATA\_i.request (where  $i = 0$  to  $n - 1$ ) primitive is used to define the transfer of multiple streams of data units from a sublayer N to the next lower sublayer  $N - 1$ , where  $n$  is the number of parallel streams of data units.

#### 80.3.3.1.1 Semantics of the service primitive

```
IS_UNITDATA_0.request(tx_bit)
IS_UNITDATA_1.request(tx_bit)
...
IS_UNITDATA_n-1.request(tx_bit)
```

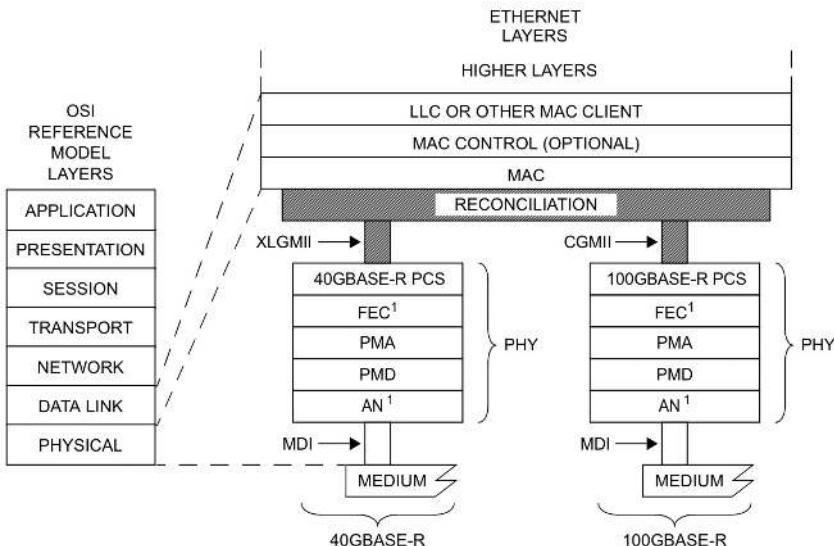
The data conveyed by IS\_UNITDATA\_0.request to IS\_UNITDATA\_n-1.request consists of  $n$  parallel continuous streams of encoded bits, one stream for each lane. Each of the tx\_bit parameters can take one of two values: one or zero.



CGMII = 100 Gb/s MEDIA INDEPENDENT INTERFACE  
RS-FEC = REED-SOLOMON FORWARD  
ERROR CORRECTION  
MAC = MEDIA ACCESS CONTROL

MDI = MEDIUM DEPENDENT INTERFACE  
PCS = PHYSICAL CODING SUBLAYER  
PMA = PHYSICAL MEDIUM ATTACHMENT  
PMD = PHYSICAL MEDIUM DEPENDENT

Figure 80-4—100GBASE-R and 100GBASE-P inter-sublayer service interfaces with RS-FEC



AN = AUTO-NEGOTIATION

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FEC = FORWARD ERROR CORRECTION

LLC = LOGICAL LINK CONTROL

MAC = MEDIA ACCESS CONTROL

MDI = MEDIUM DEPENDENT INTERFACE

PCS = PHYSICAL CODING SUBLAYER

PHY = PHYSICAL LAYER DEVICE

PMA = PHYSICAL MEDIUM ATTACHMENT

PMD = PHYSICAL MEDIUM DEPENDENT

XLGMI = 40 Gb/s MEDIA INDEPENDENT INTERFACE

NOTE 1—CONDITIONAL BASED ON PHY TYPE

Figure 81–1—RS and MII relationship to the ISO/IEC Open Systems Interconnection (OSI) reference model and the IEEE 802.3 Ethernet model

RJ45 之后工作主要支撑 MAC 层进行数据传输  
模拟 MII 并行数据总线

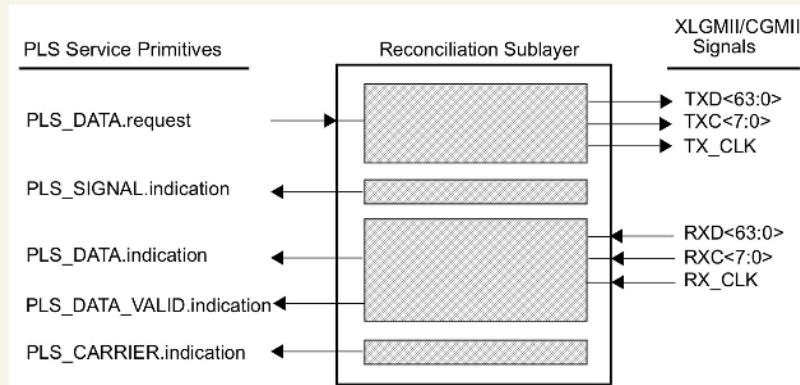


Figure 81–2—Reconciliation Sublayer (RS) inputs and outputs

1. IT control lane 管理 8T bit DATA Lane,  
 2. RS 从收到 64 位 PLS-req. 后向 MII 接口发出。  
 3. INTERFRAME 间隔是两个帧的包之间  
 及 gap. 它由是 IDLE 或小包 IPB - ToCtet.

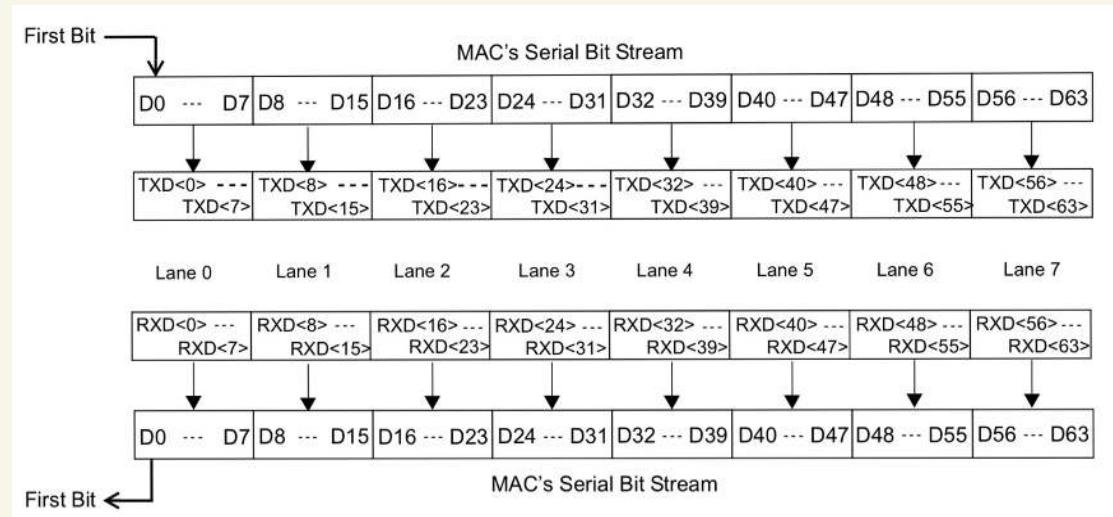


Figure 81-4—Relationship of data lanes to MAC serial bit stream

4. 一標 01101010 01101011

preamble ↑  
 ↓ SFD

↑  
 第一層包 report

control  
 <----> Lane 0

5. Dltex 内小端、cpu 大端

Dltex 间是大端

6. RS 会停在 (S) 在 Lane 0. 没有 RS  
被设计成 MRL 中.

Table 81-3—Permissible encodings of TXC and TXD

TXC	TXD	Description	PLS_DATA.request parameter
0	0x00 through 0xFF	Normal data transmission	Zero, one (eight bits)
1	0x00 through 0x05	Reserved	—
1	0x06	Only valid on all 8 lanes simultaneously to request LPI	No applicable parameter (normal inter-frame)
1	0x07	Idle	No applicable parameter (normal inter-frame)
1	0x08 through 0x9B	Reserved	—
1	0x9C	Sequence (only valid in lane 0)	No applicable parameter (inter-frame status signal)
1	0x9D through 0xFA	Reserved	—
1	0xFB	Start (only valid in lane 0)	No applicable parameter, replaces first eight zero, one of a frame (preamble octet)
1	0xFC	Reserved	—
1	0xFD	Terminate	DATA_COMPLETE
1	0xFE	Error	No applicable parameter
1	0xFF	Reserved	—

7. RX 和 TX permissible - 一样

8. PHY层检测到错误,会产生 local fault 给 RS 层, RS 会向上反送 MDL DATA & LPI, 而且发送 remote fault.  
 ↴ 本地如果由远端引起  
 remote, 则会  
 由 TDL 引起

Table 81-5—Sequence ordered sets

Lane 0	Lane 1	Lane 2	Lane 3	Lane 4	Lane 5	Lane 6	Lane 7	Description
Sequence	0x00	Reserved						
Sequence	0x00	0x00	0x01	0x00	0x00	0x00	0x00	Local Fault
Sequence	0x00	0x00	0x02	0x00	0x00	0x00	0x00	Remote Fault

local fault : local  $\leftarrow$  remote  
 remote fault : local  $\rightarrow$  remote

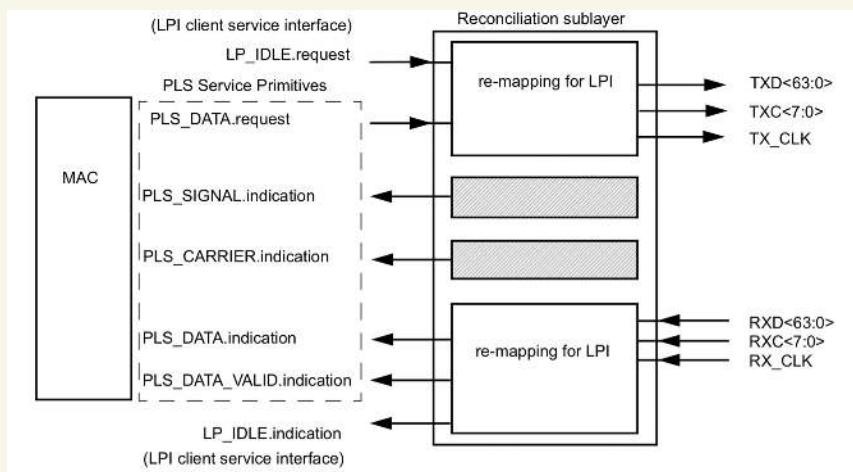
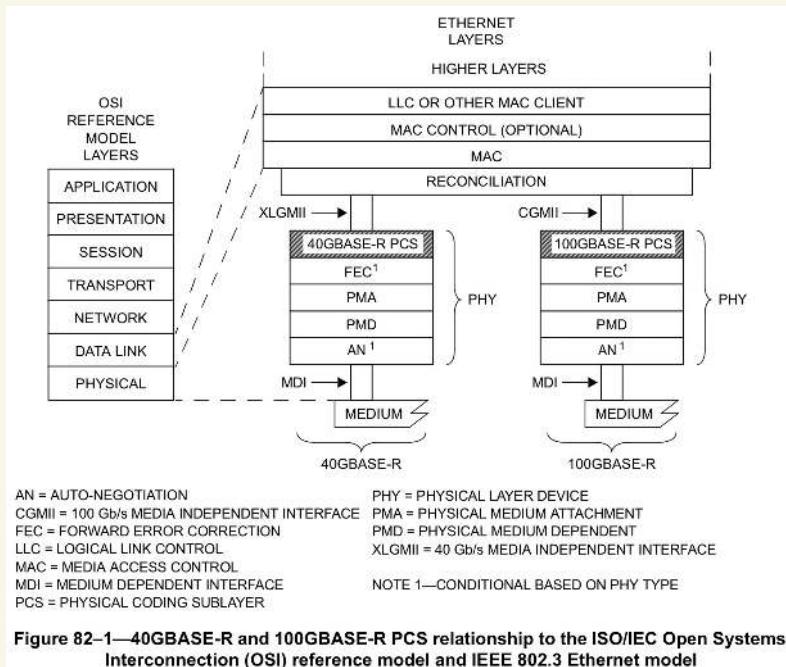


Figure 81-12—LPI assertion and detection mechanism

1. 和4章很类似.

2. 8字节对齐

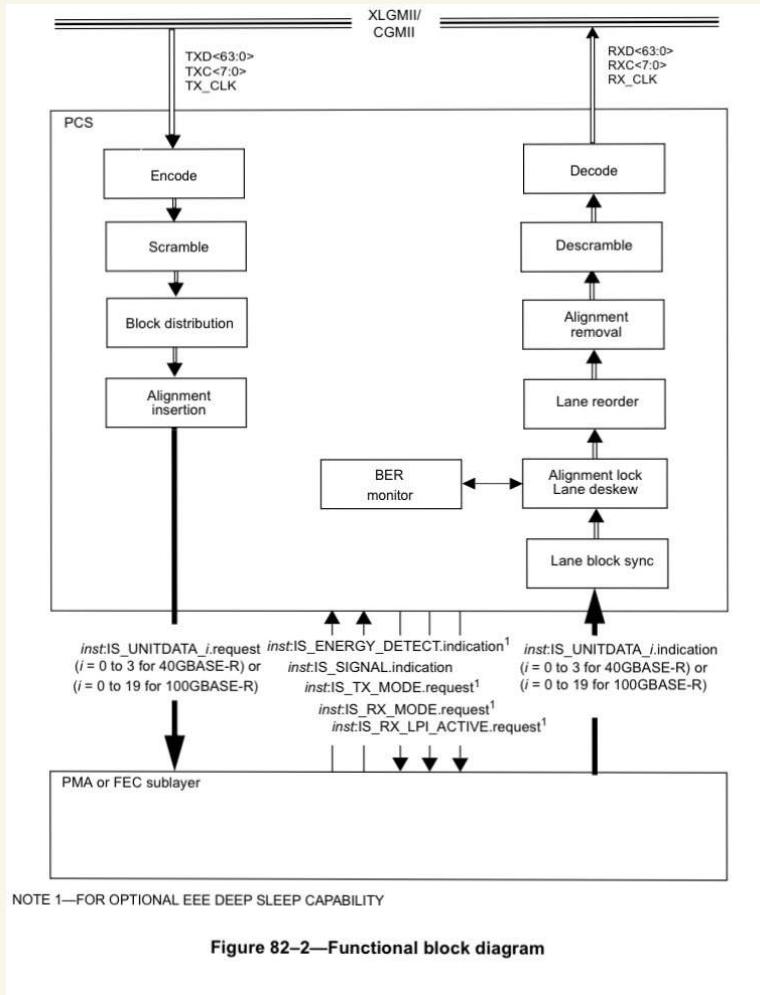
3. 新增 alignment marker.



1. 标注到 PMA 上行 ↗

40G — 4

100G — 20



NOTE 1—FOR OPTIONAL EEE DEEP SLEEP CAPABILITY

Figure 82–2—Functional block diagram

2. PCS负责align 6Y/6b bit

3. PCS会插入AM, → deskew  
PCS lane reorder

4. 6b = 2 + 6Y + 会做scramble.  
Header, 不会scramble

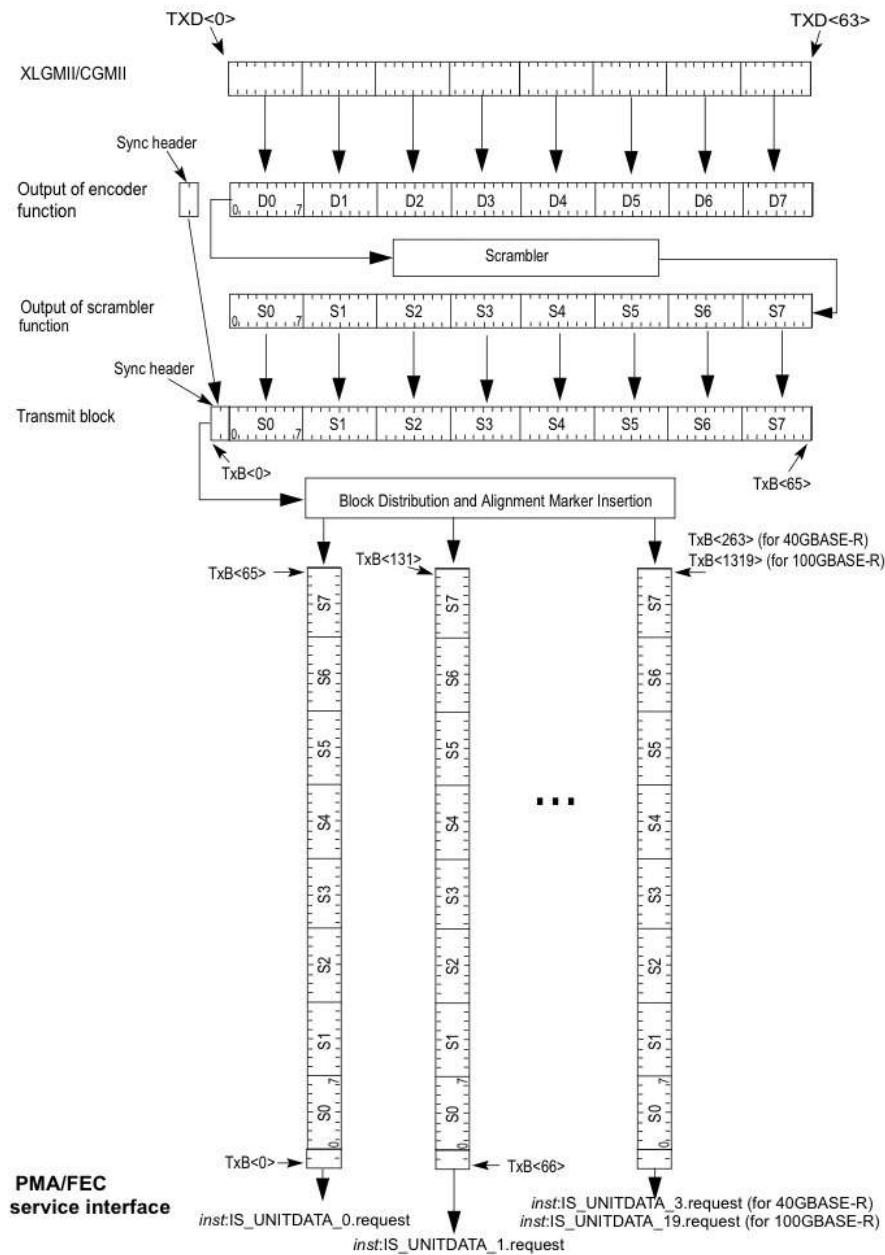


Figure 82–3—PCS Transmit bit ordering

5. Terminal 16 to 64 boundary 12 bit C.

Input Data		Sync	Block Payload									
		Bit Position:	0	1	2							
Data Block Format:		D <sub>0</sub>	D <sub>1</sub>	D <sub>2</sub>	D <sub>3</sub>	D <sub>4</sub>	D <sub>5</sub>	D <sub>6</sub>	D <sub>7</sub>			
Control Block Formats:		Block Type Field										
C <sub>0</sub> C <sub>1</sub> C <sub>2</sub> C <sub>3</sub> C <sub>4</sub> C <sub>5</sub> C <sub>6</sub> C <sub>7</sub>	10	0x1E	C <sub>0</sub>	C <sub>1</sub>	C <sub>2</sub>	C <sub>3</sub>	C <sub>4</sub>	C <sub>5</sub>	C <sub>6</sub>	C <sub>7</sub>		
S <sub>0</sub> D <sub>1</sub> D <sub>2</sub> D <sub>3</sub> D <sub>4</sub> D <sub>5</sub> D <sub>6</sub> D <sub>7</sub>	10	0x7B	D <sub>1</sub>	D <sub>2</sub>	D <sub>3</sub>	D <sub>4</sub>	D <sub>5</sub>	D <sub>6</sub>	D <sub>7</sub>			
O <sub>1</sub> D <sub>1</sub> D <sub>2</sub> D <sub>3</sub> Z <sub>4</sub> Z <sub>5</sub> Z <sub>6</sub> Z <sub>7</sub>	10	0x4B	D <sub>1</sub>	D <sub>2</sub>	D <sub>3</sub>	O <sub>0</sub>				0x000_0000		
T <sub>0</sub> C <sub>1</sub> C <sub>2</sub> C <sub>3</sub> C <sub>4</sub> C <sub>5</sub> C <sub>6</sub> C <sub>7</sub>	10	0x67		C <sub>1</sub>	C <sub>2</sub>	C <sub>3</sub>	C <sub>4</sub>	C <sub>5</sub>	C <sub>6</sub>	C <sub>7</sub>		
D <sub>0</sub> T <sub>1</sub> C <sub>2</sub> C <sub>3</sub> C <sub>4</sub> C <sub>5</sub> C <sub>6</sub> C <sub>7</sub>	10	0x99	D <sub>0</sub>		C <sub>2</sub>	C <sub>3</sub>	C <sub>4</sub>	C <sub>5</sub>	C <sub>6</sub>	C <sub>7</sub>		
D <sub>2</sub> T <sub>1</sub> T <sub>2</sub> C <sub>3</sub> C <sub>4</sub> C <sub>5</sub> C <sub>6</sub> C <sub>7</sub>	10	0x5A	D <sub>0</sub>	D <sub>1</sub>		C <sub>3</sub>	C <sub>4</sub>	C <sub>5</sub>	C <sub>6</sub>	C <sub>7</sub>		
D <sub>0</sub> D <sub>1</sub> D <sub>2</sub> T <sub>3</sub> C <sub>4</sub> C <sub>5</sub> C <sub>6</sub> C <sub>7</sub>	10	0xB4	D <sub>0</sub>	D <sub>1</sub>	D <sub>2</sub>		C <sub>4</sub>	C <sub>5</sub>	C <sub>6</sub>	C <sub>7</sub>		
D <sub>0</sub> D <sub>1</sub> D <sub>2</sub> D <sub>3</sub> T <sub>4</sub> C <sub>5</sub> C <sub>6</sub> C <sub>7</sub>	10	0xCC	D <sub>0</sub>	D <sub>1</sub>	D <sub>2</sub>	D <sub>3</sub>		C <sub>5</sub>	C <sub>6</sub>	C <sub>7</sub>		
D <sub>0</sub> D <sub>1</sub> D <sub>2</sub> D <sub>3</sub> D <sub>4</sub> T <sub>5</sub> C <sub>6</sub> C <sub>7</sub>	10	0xD2	D <sub>0</sub>	D <sub>1</sub>	D <sub>2</sub>	D <sub>3</sub>	D <sub>4</sub>		C <sub>6</sub>	C <sub>7</sub>		
D <sub>0</sub> D <sub>1</sub> D <sub>2</sub> D <sub>3</sub> D <sub>4</sub> D <sub>5</sub> T <sub>6</sub> C <sub>7</sub>	10	0xE1	D <sub>0</sub>	D <sub>1</sub>	D <sub>2</sub>	D <sub>3</sub>	D <sub>4</sub>	D <sub>5</sub>		C <sub>7</sub>		
D <sub>0</sub> D <sub>1</sub> D <sub>2</sub> D <sub>3</sub> D <sub>4</sub> D <sub>5</sub> D <sub>6</sub> T <sub>7</sub>	10	0xFF	D <sub>0</sub>	D <sub>1</sub>	D <sub>2</sub>	D <sub>3</sub>	D <sub>4</sub>	D <sub>5</sub>	D <sub>6</sub>	D <sub>7</sub>		

**Figure 82-5—64B/66B block formats**

Table 82-1—Control codes				
Control character	Notation	XLGMII/ CGMII control code	40/100GBASE-R O code	40GBASE-R and 100GBASE-R control code
idle	3F	0x07		0x00
LPI	4LP	0x06		0x06
start	SS	0xFB		Encoded by block type field
terminal	TE	0xFD		Encoded by block type field
error	AE	0xFE		0x1E
Sequence ordered set	XQ	0x9C	0xd0	Encoded by block type 0x4B plus O code, control codes are set to 0x00
Signal ordered set <sup>10</sup>	FSig	0x5C	0xF	Encoded by block type 0x4B plus O code, control codes are set to 0x00

<sup>9</sup>Reserved for INCTES III Fibre Channel use.

b. order rot. =  $O_2 + 3 \uparrow$  data +  $4 \uparrow$  o. O.  $\xrightarrow{\text{Step 1}}$  Octet.

7. block distribution - 最小單位為 66 bits.

is block.

8. AM. → a. 通常は ITC 中  
b. 在 scramble. [B] は encoding する  
scramble [B]

P. 16383 blocks 抽取一个 AM

The format of the alignment markers is shown in Figure 82-7.

Bit Position:	0	1	2	9	10	17	18	25	26	33	34	41	42	49	50	57	58	65
	10	M <sub>0</sub>		M <sub>1</sub>		M <sub>2</sub>		BIP <sub>3</sub>		M <sub>4</sub>		M <sub>5</sub>		M <sub>6</sub>		BIP <sub>7</sub>		

Table 82-2—100GBASE-R Alignment marker encodings

PCS lane number	Encoding <sup>a</sup> {M <sub>0</sub> , M <sub>1</sub> , M <sub>2</sub> , BIP <sub>3</sub> , M <sub>4</sub> , M <sub>5</sub> , M <sub>6</sub> , BIP <sub>7</sub> }	PCS lane number	Encoding <sup>a</sup> {M <sub>0</sub> , M <sub>1</sub> , M <sub>2</sub> , BIP <sub>3</sub> , M <sub>4</sub> , M <sub>5</sub> , M <sub>6</sub> , BIP <sub>7</sub> }
0	0xC1, 0x68, 0x21, BIP <sub>3</sub> , 0x2E, 0x97, 0xDE, BIP <sub>7</sub>	10	0xFD, 0x6C, 0x99, BIP <sub>3</sub> , 0x02, 0x93, 0x66, BIP <sub>7</sub>
1	0x9D, 0x71, 0x8E, BIP <sub>3</sub> , 0x62, 0x8E, 0x71, BIP <sub>7</sub>	11	0xB9, 0x91, 0x55, BIP <sub>3</sub> , 0x46, 0x6E, 0xAA, BIP <sub>7</sub>
2	0x59, 0x4B, 0x18, BIP <sub>3</sub> , 0xA0, 0xB4, 0x17, BIP <sub>7</sub>	12	0x5C, 0x B9, 0x12, BIP <sub>3</sub> , 0xA3, 0x46, 0x4D, BIP <sub>7</sub>
3	0x4D, 0x95, 0x7B, BIP <sub>3</sub> , 0xB2, 0x6A, 0x84, BIP <sub>7</sub>	13	0x1A, 0xF8, 0xBD, BIP <sub>3</sub> , 0xE5, 0x07, 0x42, BIP <sub>7</sub>
4	0xF5, 0x07, 0x09, BIP <sub>3</sub> , 0x0A, 0xF8, 0xF6, BIP <sub>7</sub>	14	0x83, 0xC7, 0xCA, BIP <sub>3</sub> , 0x7C, 0x38, 0x35, BIP <sub>7</sub>
5	0xDD, 0x14, 0xC2, BIP <sub>3</sub> , 0x22, 0xEB, 0x3D, BIP <sub>7</sub>	15	0x35, 0x36, 0xCD, BIP <sub>3</sub> , 0xCA, 0xC9, 0x32, BIP <sub>7</sub>
6	0x9A, 0x4A, 0x26, BIP <sub>3</sub> , 0x65, 0x85, 0xD9, BIP <sub>7</sub>	16	0xC4, 0x31, 0x4C, BIP <sub>3</sub> , 0x3B, 0xCE, 0xB3, BIP <sub>7</sub>
7	0x7B, 0x45, 0x66, BIP <sub>3</sub> , 0x84, 0xBA, 0x99, BIP <sub>7</sub>	17	0xAD, 0xD6, 0xB7, BIP <sub>3</sub> , 0x52, 0x29, 0x48, BIP <sub>7</sub>
8	0xA0, 0x24, 0x76, BIP <sub>3</sub> , 0x5F, 0xDB, 0x89, BIP <sub>7</sub>	18	0x5F, 0x66, 0x2A, BIP <sub>3</sub> , 0xA0, 0x99, 0xD5, BIP <sub>7</sub>
9	0x68, 0xC9, 0xFB, BIP <sub>3</sub> , 0x97, 0x36, 0x04, BIP <sub>7</sub>	19	0xC0, 0xF0, 0xE5, BIP <sub>3</sub> , 0x3F, 0x0F, 0x1A, BIP <sub>7</sub>

<sup>a</sup>Each octet is transmitted LSB to MSB.

Table 82-3—40GBASE-R Alignment marker encodings

PCS lane number	Encoding <sup>a</sup> {M <sub>0</sub> , M <sub>1</sub> , M <sub>2</sub> , BIP <sub>3</sub> , M <sub>4</sub> , M <sub>5</sub> , M <sub>6</sub> , BIP <sub>7</sub> }
0	0x90, 0x76, 0x47, BIP <sub>3</sub> , 0x6F, 0x89, 0xB8, BIP <sub>7</sub>
1	0xF0, 0xC4, 0xE6, BIP <sub>3</sub> , 0x0F, 0x3B, 0x19, BIP <sub>7</sub>
2	0xC5, 0x65, 0x9B, BIP <sub>3</sub> , 0x3A, 0x9A, 0x64, BIP <sub>7</sub>
3	0xA2, 0x79, 0x3D, BIP <sub>3</sub> , 0x5D, 0x86, 0xC2, BIP <sub>7</sub>

<sup>a</sup>Each octet is transmitted LSB to MSB.

(10. LPI 里还有-种 RAM, 因为有 66bit block

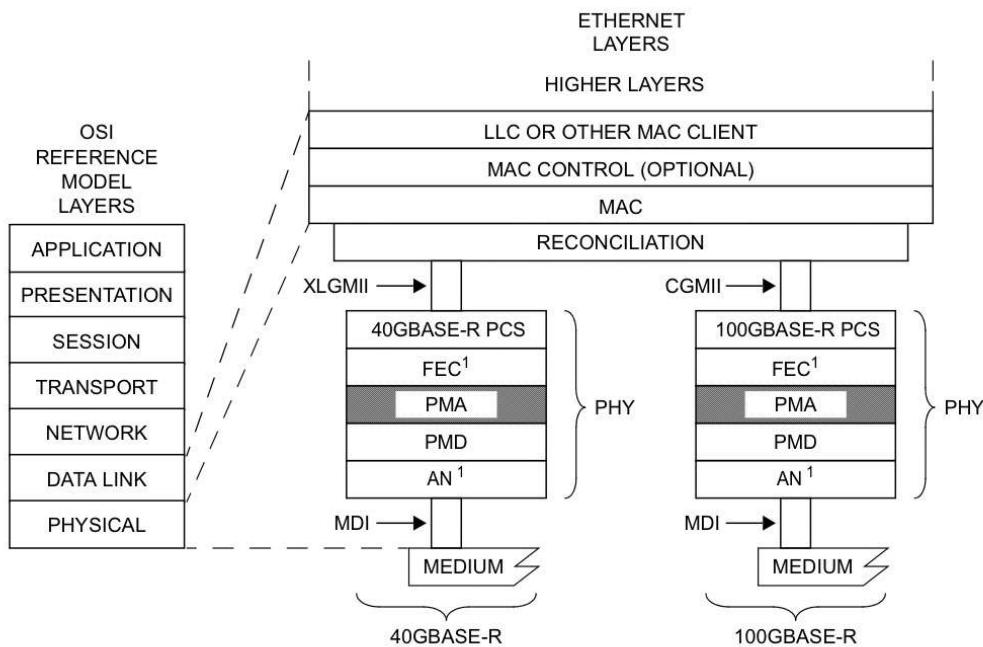
11. 补修操作 AM for removal 带  
来的时钟，会插入到 T

Table 82-7—Skew tolerance requirements

PCS	Maximum Skew	Maximum Skew Variation
40GBASE-R	180 ns (~1856 bits)	4ns (~41 bits)
100GBASE-R	180 ns (~928 bits)	4ns (~21 bits)
100GBASE-R with RS-FEC	49 ns (~253 bits)	0.4 ns (~2 bits)

12. Feedback ps, p13 也属于  
mzi 到 PMA / FEC 之间

40G 和 100G PMA 分別支持 40G 和 100G  
 (T&D) PMD



AN = AUTO-NEGOTIATION

CGMII = 100 Gb/s MEDIA INDEPENDENT INTERFACE

FEC = FORWARD ERROR CORRECTION

LLC = LOGICAL LINK CONTROL

MAC = MEDIA ACCESS CONTROL

MDI = MEDIUM DEPENDENT INTERFACE

PCS = PHYSICAL CODING SUBLAYER

PHY = PHYSICAL LAYER DEVICE

PMA = PHYSICAL MEDIUM ATTACHMENT

PMD = PHYSICAL MEDIUM DEPENDENT

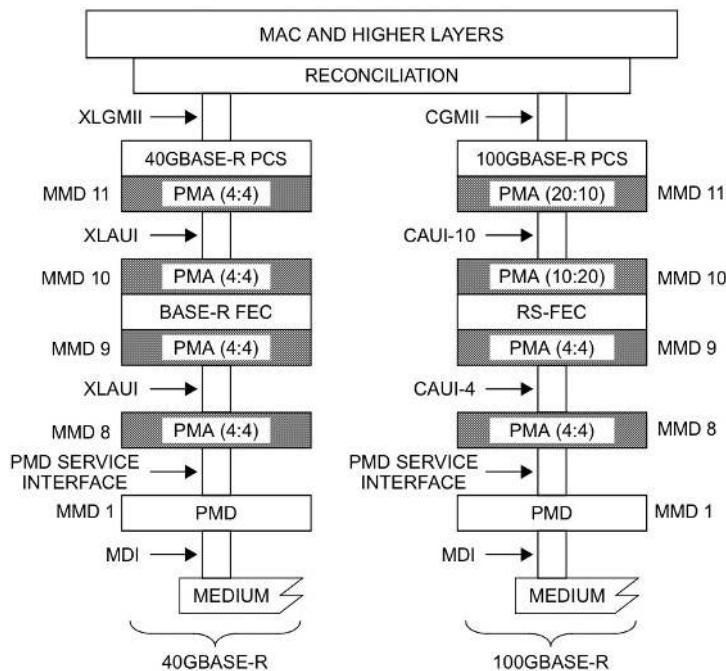
XLGMII = 40 Gb/s MEDIA INDEPENDENT INTERFACE

NOTE 1—CONDITIONAL BASED ON PHY TYPE

Figure 83-1—40GBASE-R and 100GBASE-R PMA relationship to the ISO/IEC Open Systems Interconnection (OSI) reference model and IEEE 802.3 Ethernet model

1. 40G & 100G PMA 開不同。  
 每個光路使用 16x1 bit mux.

每個光路使用 16x1 bit mux.



CAUI-4 = 100 Gb/s FOUR-LANE ATTACHMENT UNIT INTERFACE  
CAUI-10 = 100 Gb/s TEN-LANE ATTACHMENT UNIT INTERFACE

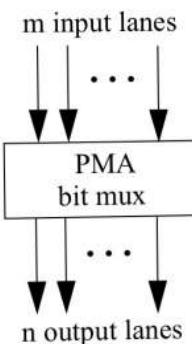
CGMII = 100 Gb/s MEDIA INDEPENDENT INTERFACE  
FEC = FORWARD ERROR CORRECTION

MAC = MEDIA ACCESS CONTROL

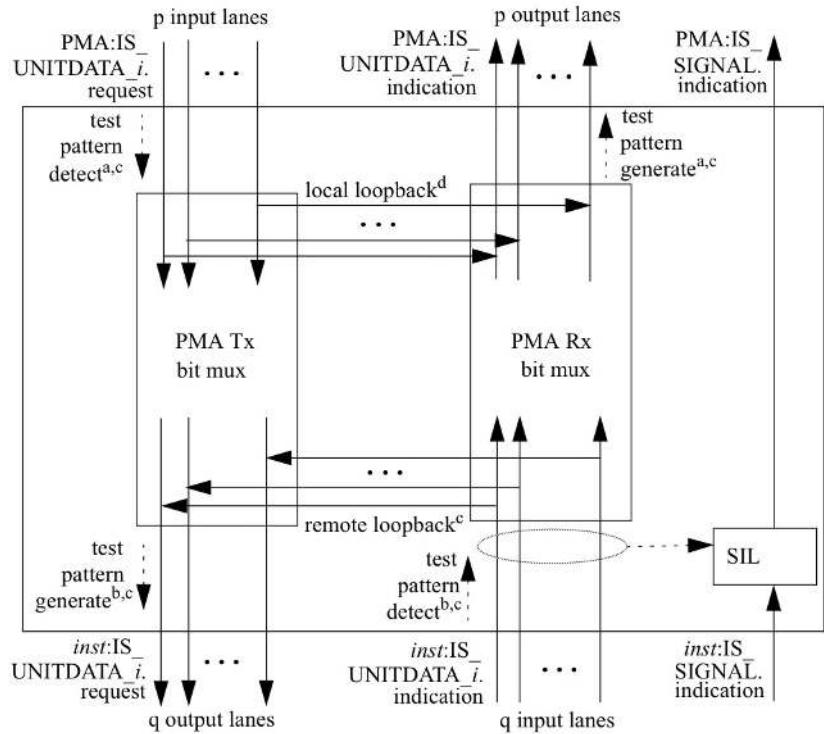
MMD = MDIO MANAGEABLE DEVICE  
PCS = PHYSICAL CODING SUBLAYER  
PMA = PHYSICAL MEDIUM ATTACHMENT  
PMD = PHYSICAL MEDIUM DEPENDENT  
RS-FEC = REED-SOLOMON FORWARD ERROR CORRECTION

XLAUI = 40 Gb/s ATTACHMENT UNIT INTERFACE  
XLGMII = 40 Gb/s MEDIA INDEPENDENT INTERFACE  
MDI = MEDIUM DEPENDENT INTERFACE

**Figure 83–2—Example 40GBASE-R and 100GBASE-R PMA layering**



**Figure 83–3—PMA bit mux used in both Tx and Rx directions**



*inst* PMD, PMA, or FEC, depending on which sublayer is below this PMA  
*SIL* Signal Indication Logic

<sup>a</sup> If physically instantiated interface (XLAUI/CAUI-n) immediately above this PMA.

<sup>b</sup> If physically instantiated interface (XLAUI/CAUI-n or PMD service interface) immediately below this PMA, or if this is the closest PMA to the PMD.

<sup>c</sup> Optional.

<sup>d</sup> Local loopback is required for PMAs adjacent to some PMDs, and optional for other PMAs. See 83.5.8.

Figure 83-5—PMA Functional Block Diagram

2. TX: demultiplex pscl, buffering.

multiplex →

RX: 反过来但是要加上 CPR.

3. P进Q出时. 对于某一条 lane (P)  
Q出的 lane 也是确定的

4. quiet 和 ALERT 信号 (EE)  
会随机 scramble, 如果检测到后  
会在 lane (P) 有 quiet. ALERT 至少  
224 bit 时间, 则认为有 ALERT

或 Quiet

5. EBF 面. Q quiet 发 quiet.  
和 ALERT 在 ALERT  
和 DATA 间

6. 一般 Quiet 和 ALERT  
是 ALERT

7. TX 方向

transmit → aui-tx-mode

receive → tx-mode 受到 42

到上层 [信号帧], v2B

aui-RX-mode

RX 方向

transmit → RX-mode 受到

接收 [信号帧] B

RX-TX-mode

receive → energy-detect

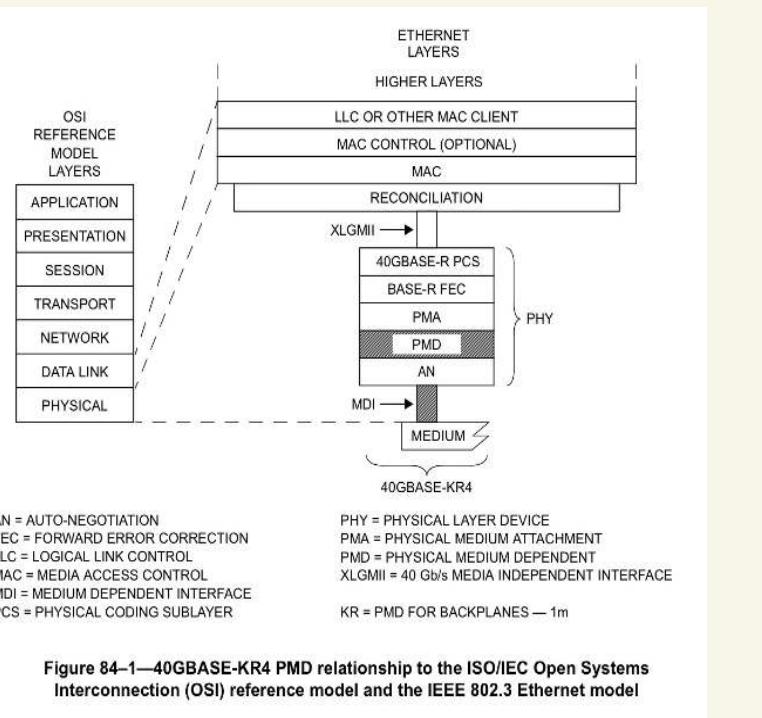
受到 rx-mode 帧 B

aui-RX-mode

**Table 84–1—Physical Layer clauses associated with the 40GBASE-KR4 PMD**

Associated clause	40GBASE-KR4
81—RS	Required
81—XLGMII <sup>a</sup>	Optional
82—PCS for 40GBASE-R	Required
74—BASE-R FEC	Optional
83—PMA for 40GBASE-R	Required
83A—XLAUI	Optional
73—Auto-Negotiation	Required
78—Energy Efficient Ethernet	Optional

<sup>a</sup>The XLGMII is an optional interface. However, if the XLGMII is not implemented, a conforming implementation must behave functionally as though the RS and XLGMII were present.



1. 如果有XLAVI (with interlayer) 且  
支持AN, 那么 AN-link.ind TL  
plus 会沿布到AN节点

2. 签名信号,  $\text{bit1} = \frac{\text{SL}_{\text{cp}} - \text{SL}_{\text{cn}}}{2^0}$

3. EEG:  
tx mode ALERT, 发送 FF00  
tx mode Quiet, 关 transmitter

4. SIGNAL-DETECT  
OK. } start-up protocol completion  
} transp completion  
} transp disabled  
} OUTGT → ALERT

FAIL

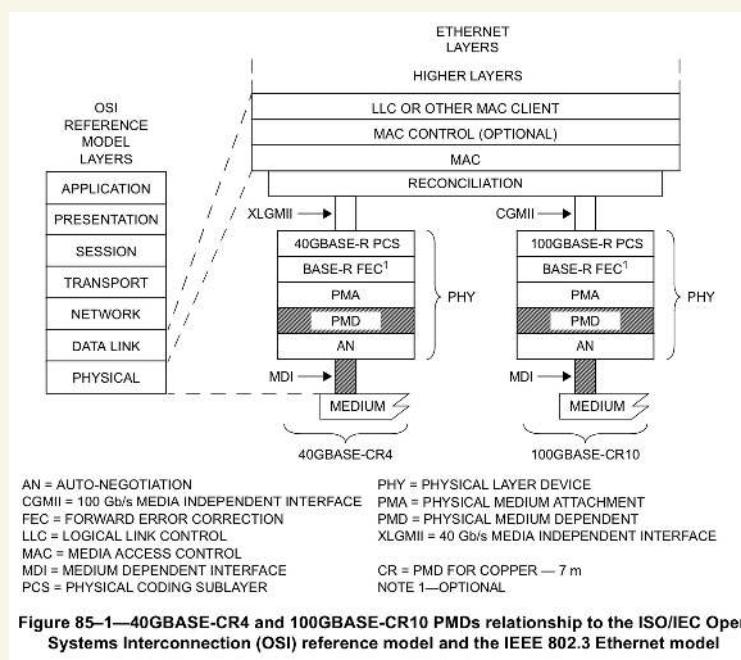
{ DATA → QUIET  
QUIET

**Table 85–1—Physical Layer clauses associated with the 40GBASE-CR4 and 100GBASE-CR10 PMDs**

Associated clause	40GBASE-CR4	100GBASE-CR10
81—RS	Required	Required
81—XLGMII <sup>a</sup>	Optional	Not applicable
81—CGMII <sup>b</sup>	Not applicable	Optional
82—PCS for 40GBASE-R	Required	Not applicable
82—PCS for 100GBASE-R	Not applicable	Required
74—BASE-R FEC	Optional	Optional
83—PMA for 40GBASE-R	Required	Not applicable
83—PMA for 100GBASE-R	Not applicable	Required
83A—XLAUI	Optional	Not applicable
83A—CAUI-10	Not applicable	Optional
83D—CAUI-4	Not applicable	Optional
73—Auto-Negotiation	Required	Required
78—Energy Efficient Ethernet	Optional	Optional

<sup>a</sup>The XLGMII is an optional interface. However, if the XLGMII is not implemented, a conforming implementation must behave functionally as though the RS and XLGMII were present.

<sup>b</sup>The CGMII is an optional interface. However, if the CGMII is not implemented, a conforming implementation must behave functionally as though the RS and CGMII were present.



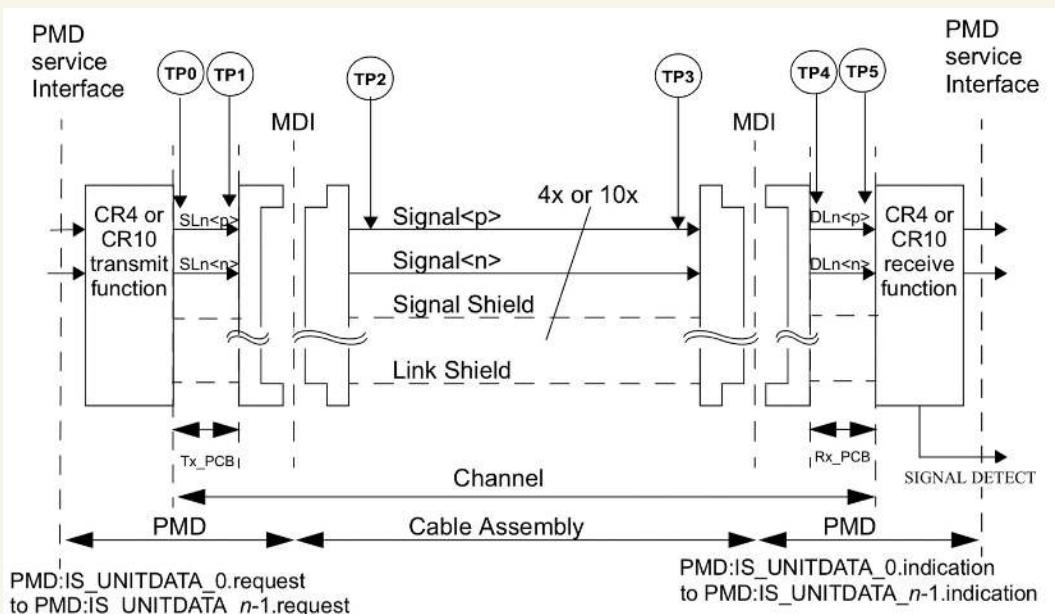


Figure 85–2—40GBASE-CR4 or 100GBASE-CR10 link (half link is illustrated)

1. 40G CR4  $\xrightarrow{\text{Tx}} \text{100G CR10}$  之 AL —  
coupled interface .  
只用 low swing .

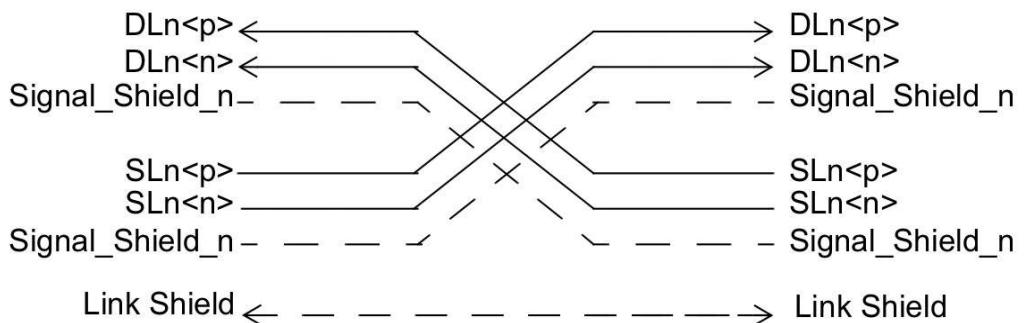
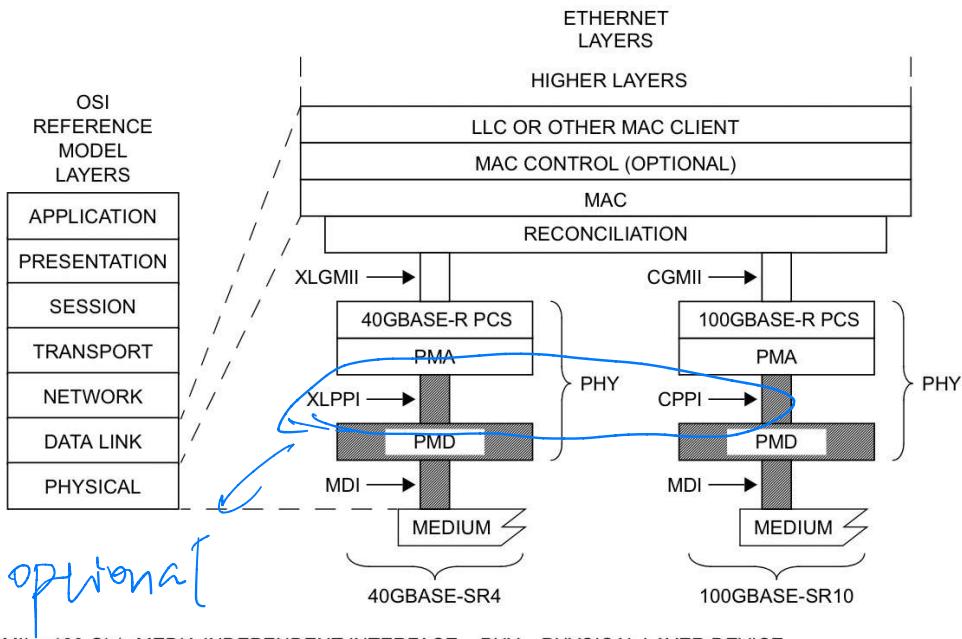


Figure 85–18—Cable assembly wiring



CGMII = 100 Gb/s MEDIA INDEPENDENT INTERFACE  
 CPPI = 100 Gb/s PARALLEL PHYSICAL INTERFACE  
 LLC = LOGICAL LINK CONTROL  
 MAC = MEDIA ACCESS CONTROL  
 MDI = MEDIUM DEPENDENT INTERFACE  
 PCS = PHYSICAL CODING SUBLAYER

PHY = PHYSICAL LAYER DEVICE  
 PMA = PHYSICAL MEDIUM ATTACHMENT  
 PMD = PHYSICAL MEDIUM DEPENDENT  
 XLGMI = 40 Gb/s MEDIA INDEPENDENT INTERFACE  
 XLPPI = 40 Gb/s PARALLEL PHYSICAL INTERFACE  
 SR = PMD FOR MULTIMODE FIBER

Figure 86-1—40GBASE-SR4 and 100GBASE-SR10 PMDs relationship to the ISO/IEC Open Systems Interconnection (OSI) reference model and IEEE 802.3 Ethernet model

1. 支持光纤
2. 只支持 fast wak& up mode, 不支持 deep sleep of EEE
3. 光的 Lane 和 电源 Tone一一对应, 没一个 assign.

Table 86–2—Summary of 40GBASE-SR4 and 100GBASE-SR10

PMD Type	40GBASE-SR4	100GBASE-SR10	Unit
Fiber type	50/125 $\mu\text{m}$ multimode, type A1a.2 <sup>a</sup> (OM3) or A1a.3 <sup>b</sup> (OM4)		
Number of fiber pairs	4	10	
Nominal wavelength	850		nm
Required operating range	0.5 to 100 for OM3		m
	0.5 to 150 for OM4 <sup>c</sup>		
Signaling rate, each lane	$10.3125 \pm 100$ ppm		GBd

<sup>a</sup> Type A1a.2 (OM3) specified in IEC 60793-2-10. See 86.10.2.1.

<sup>b</sup> Type A1a.3 (OM4) specified in IEC 60793-2-10. See 86.10.2.1.

<sup>c</sup> This is an engineered link with maximum 1 dB connection and splice loss.

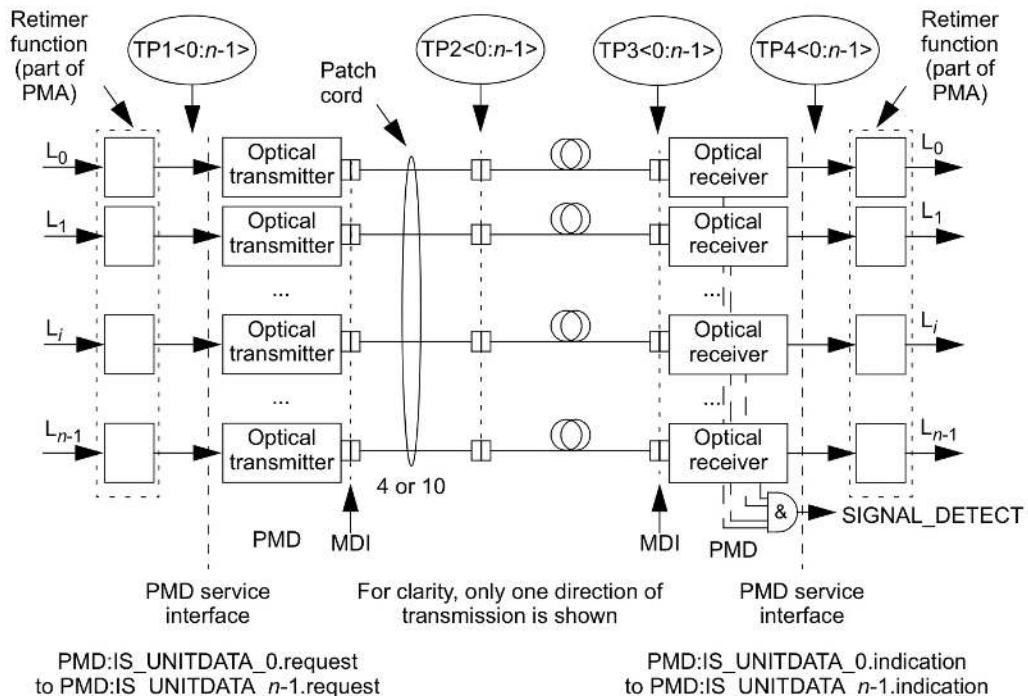
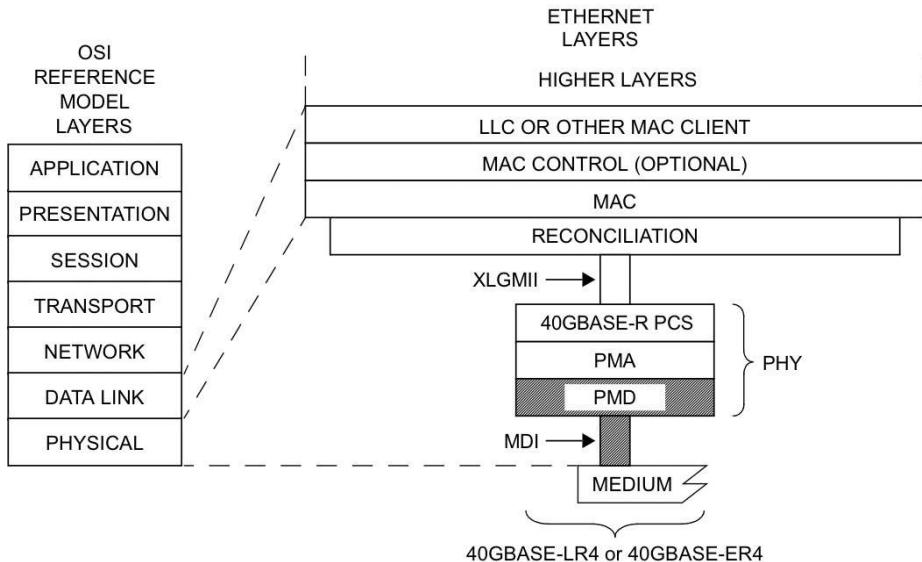


Figure 86–2—Block diagram for 40GBASE-SR4 and 100GBASE-SR10 transmit/receive paths

4. 测 BER 及其是否为 Lane[3] 时  
测还是 Lane-by-Lane 测



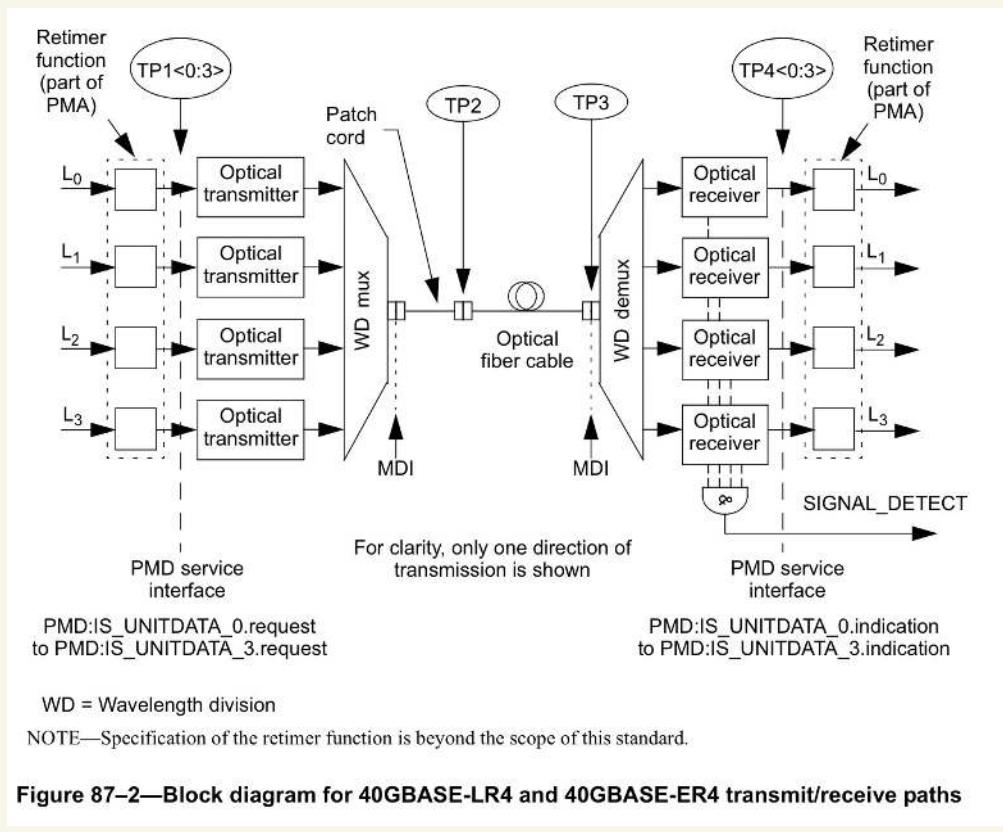
LLC = LOGICAL LINK CONTROL  
 MAC = MEDIA ACCESS CONTROL  
 MDI = MEDIUM DEPENDENT INTERFACE  
 PCS = PHYSICAL CODING SUBLAYER  
 PHY = PHYSICAL LAYER DEVICE  
 PMA = PHYSICAL MEDIUM ATTACHMENT

PMD = PHYSICAL MEDIUM DEPENDENT  
 XLGMII = 40 Gb/s MEDIA INDEPENDENT INTERFACE  
 LR = PMD FOR SINGLE-MODE FIBER — 10 km  
 ER = PMD FOR SINGLE-MODE FIBER — 40 km

Figure 87-1—40GBASE-LR4 and 40GBASE-ER4 PMDs relationship to the ISO/IEC Open Systems Interconnection (OSI) reference model and IEEE 802.3 Ethernet model

1. 单模光纤
2. XLGPI 是 40G 的并行物理口
3. PMD service interface.  
两个传输 PMA 和 PMD 之间
4. 带缓存

4 四个光信号通过 WD mux 后进入 MDI 面层 mux  
在一起，信号复用



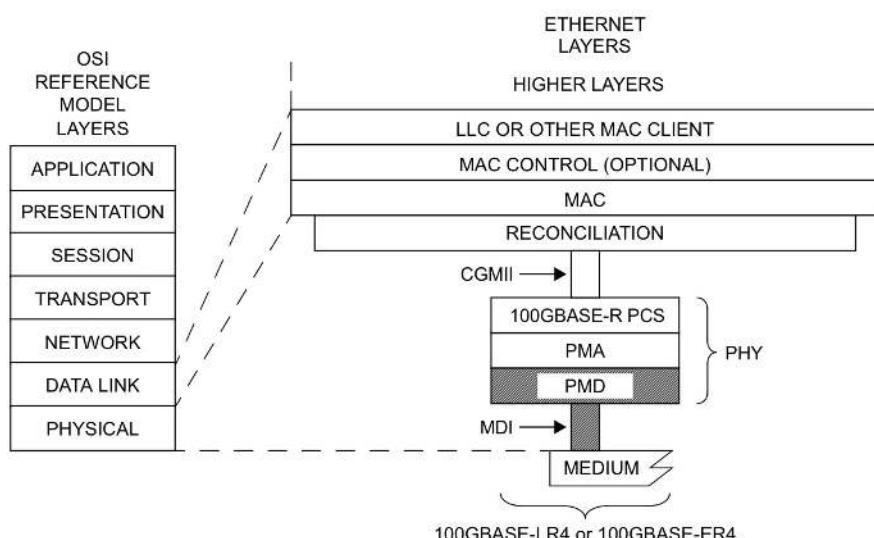
**Table 87–5—Wavelength-division-multiplexed lane assignments**

Lane	Center wavelength	Wavelength range
L <sub>0</sub>	1271 nm	1264.5 to 1277.5 nm
L <sub>1</sub>	1291 nm	1284.5 to 1297.5 nm
L <sub>2</sub>	1311 nm	1304.5 to 1317.5 nm
L <sub>3</sub>	1331 nm	1324.5 to 1337.5 nm

**Table 88-1—Physical Layer clauses associated with the 100GBASE-LR4 and 100GBASE-ER4 PMDs**

Associated clause	100GBASE-LR4	100GBASE-ER4
81—RS	Required	Required
81—CGMII <sup>a</sup>	Optional	Optional
82—PCS for 100GBASE-R	Required	Required
83—PMA for 100GBASE-R	Required	Required
83A—CAUI-10	Optional	Optional
83B—Chip to module CAUI-10	Optional	Optional
83D—CAUI-4	Optional	Optional
83E—Chip-to-module CAUI-4	Optional	Optional
78—Energy Efficient Ethernet	Optional	Optional

<sup>a</sup>The CGMII is an optional interface. However, if the CGMII is not implemented, a conforming implementation must behave functionally as though the RS and CGMII were present.



CGMII = 100 Gb/s MEDIA INDEPENDENT INTERFACE

LLC = LOGICAL LINK CONTROL

MAC = MEDIA ACCESS CONTROL

MDI = MEDIUM DEPENDENT INTERFACE

PCS = PHYSICAL CODING SUBLAYER

PHY = PHYSICAL LAYER DEVICE

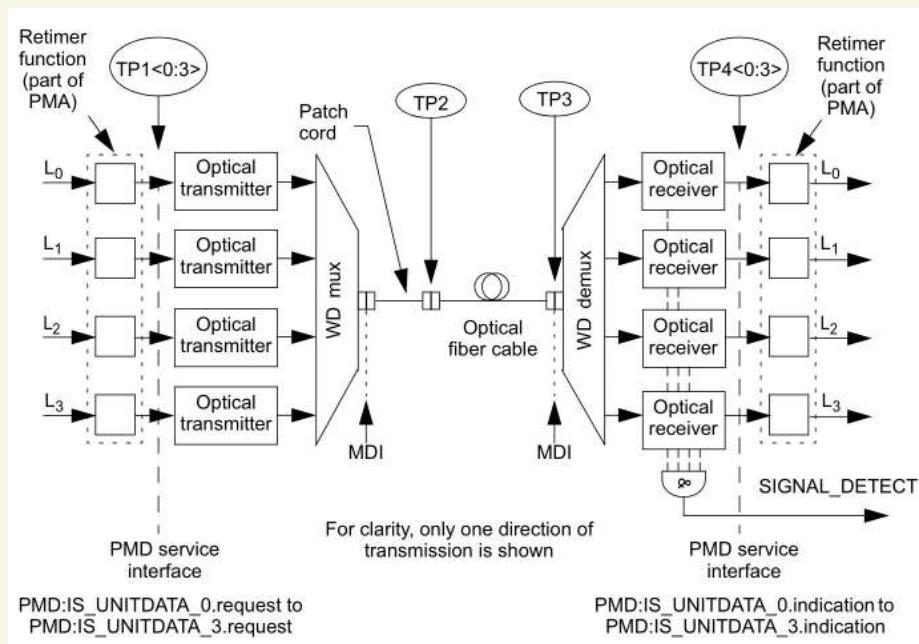
PMA = PHYSICAL MEDIUM ATTACHMENT

PMD = PHYSICAL MEDIUM DEPENDENT

LR = PMD FOR SINGLE-MODE FIBER — 10 km

ER = PMD FOR SINGLE-MODE FIBER — 40 km

**Figure 88-1—100GBASE-LR4 and 100GBASE-ER4 PMDs relationship to the ISO/IEC Open Systems Interconnection (OSI) reference model and IEEE 802.3 Ethernet model**



**Table 88–5—Wavelength-division-multiplexed lane assignments**

Lane	Center frequency	Center wavelength	Wavelength range
L <sub>0</sub>	231.4 THz	1295.56 nm	1294.53 to 1296.59 nm
L <sub>1</sub>	230.6 THz	1300.05 nm	1299.02 to 1301.09 nm
L <sub>2</sub>	229.8 THz	1304.58 nm	1303.54 to 1305.63 nm
L <sub>3</sub>	229 THz	1309.14 nm	1308.09 to 1310.19 nm

**Table 88-6—100GBASE-LR4 and 100GBASE-ER4 operating ranges**

PMD type	Required operating range
100GBASE-LR4	2 m to 10 km
100GBASE-ER4	2 m to 30 km
	2 m to 40 km <sup>a</sup>

<sup>a</sup>Links longer than 30 km for the same link power budget are considered engineered links. Attenuation for such links needs to be less than the worst case specified for B1.1, B1.3, or B6\_a single-mode fiber.

超过 operating range 但仍符合 optical spec 是可以的。

光模块内部有 CRV (clock recovery)

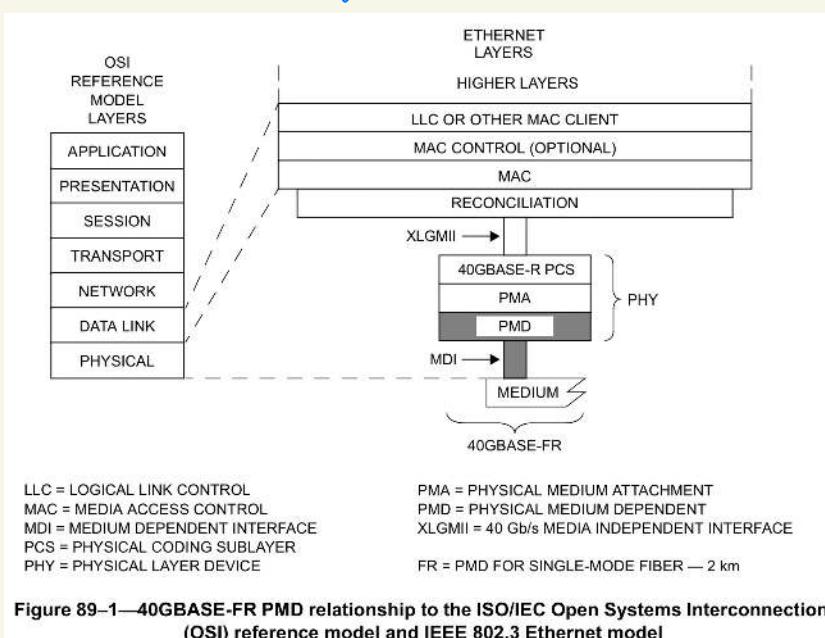
WST?

**Table 89–1—Physical Layer clauses associated with the 40GBASE-FR PMD**

Associated clause	40GBASE-FR
81—RS	Required
81—XLGMII <sup>a</sup>	Optional
82—PCS for 40GBASE-R	Required
83—PMA for 40GBASE-R	Required
83A—XLAUI	Optional
83B—Chip to module XLAUI	Optional
78—Energy Efficient Ethernet	Optional

<sup>a</sup>The XLGMII is an optional interface. However, if the XLGMII is not implemented, a conforming implementation must behave functionally as though the RS and XLGMII were present.

单模光纤，单工 41-25G



1. 時間同步子層 I,

2. RS層子層 II

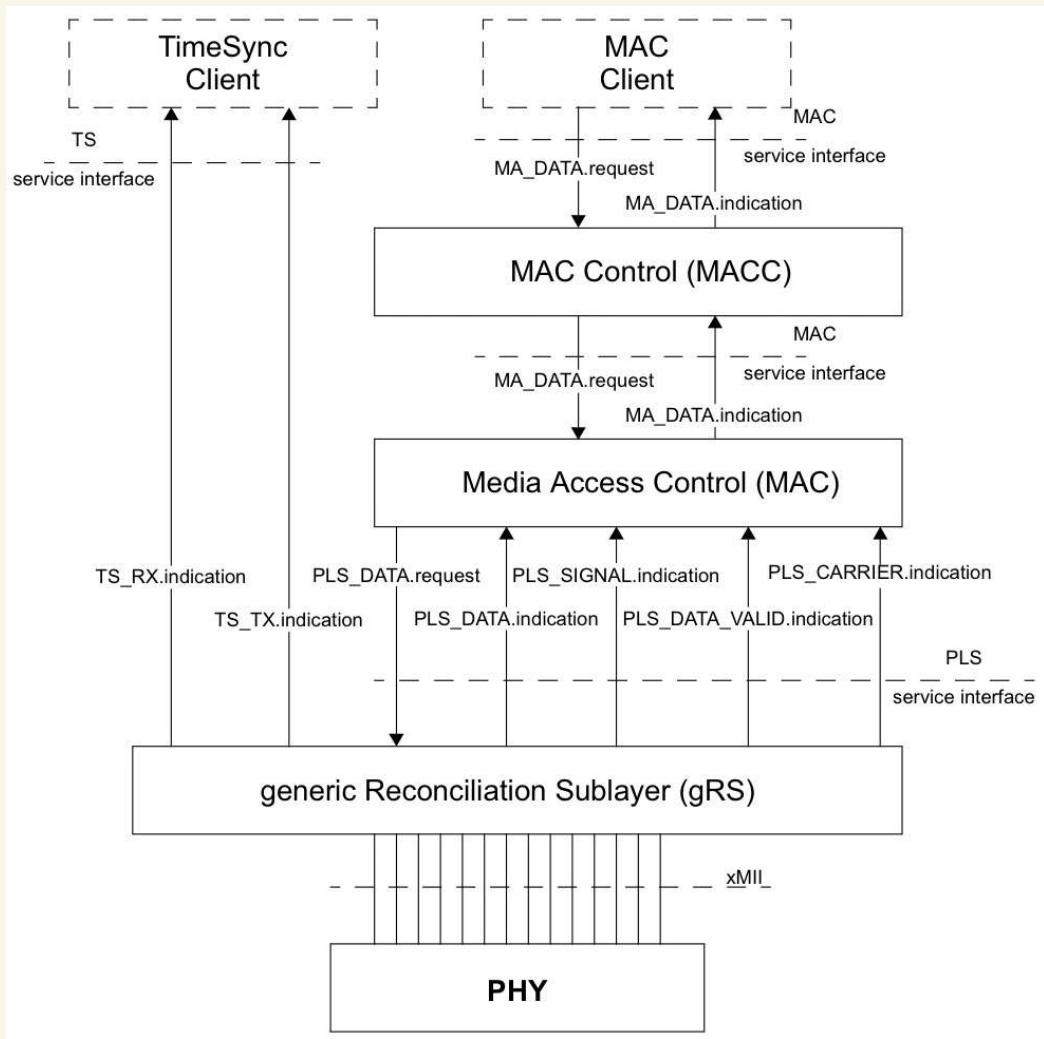


Figure 90–1—Relationship of the TimeSync Client, TSSI and gRS sublayer relative to MAC and MAC Client and associated interfaces

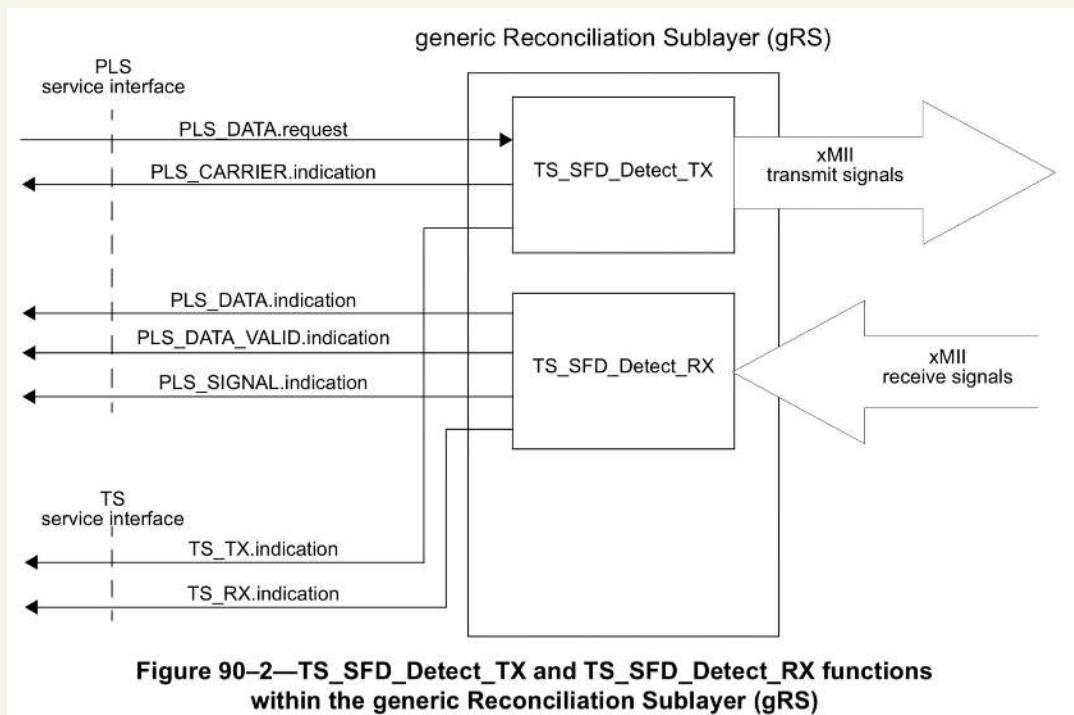
3. TS-TX. IND

TS-RX. IND

分別是檢測到SFD. - TX 是  
RX 是

TX : RS → PLS

RX : PLS → RS



OSI  
REFERENCE  
MODEL  
LAYERS

ETHERNET  
LAYERS

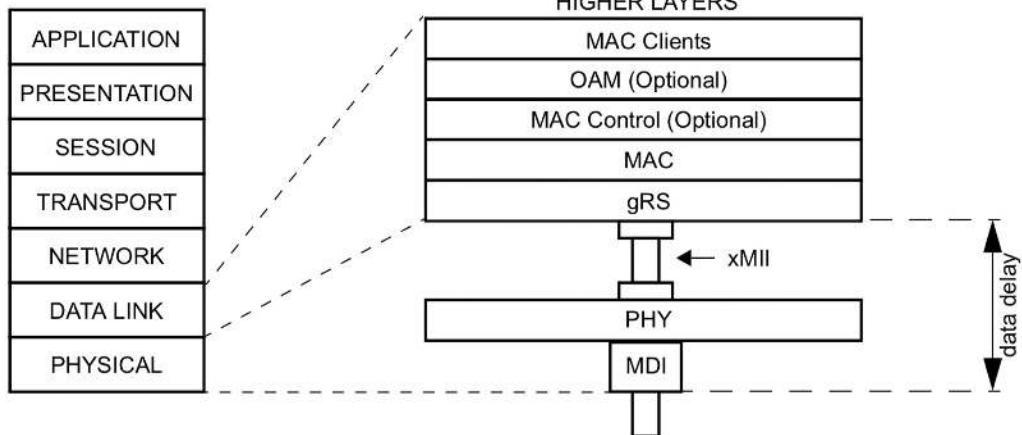
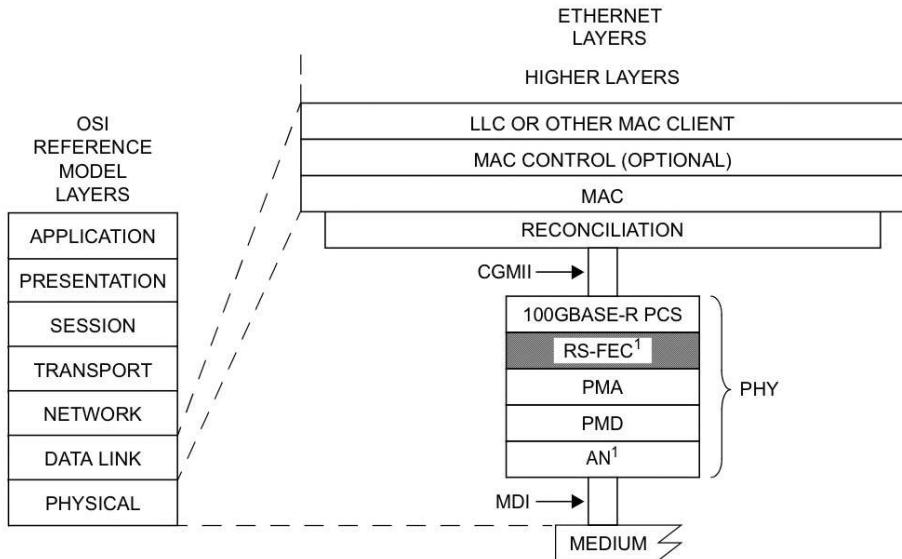


Figure 90-3—Data delay measurement

DATA DELAY : RJ45 線 MDI [ ] 由 延遲



AN = AUTO-NEGOTIATION

CGMII = 100 Gb/s MEDIA INDEPENDENT INTERFACE

LLC = LOGICAL LINK CONTROL

MAC = MEDIA ACCESS CONTROL

MDI = MEDIUM DEPENDENT INTERFACE

PCS = PHYSICAL CODING SUBLAYER

PHY = PHYSICAL LAYER DEVICE

PMA = PHYSICAL MEDIUM ATTACHMENT

PMD = PHYSICAL MEDIUM DEPENDENT

RS-FEC = REED-SOLOMON FORWARD ERROR  
CORRECTION

NOTE 1—CONDITIONAL BASED ON PHY TYPE

**Figure 91–1—RS-FEC relationship to the ISO/IEC Open Systems Interconnection (OSI) reference model and the IEEE 802.3 Ethernet model**

1. FEC, singal 为  
TRUE → 检测到 FEC 错误
2. RS-FEC 要求 pma 是 4 个 Lane  
(lane 和回传 Lane)

3. 索引译码器 FEL 和 PMD [P]

→ PMD 要求是小于等于 4 (one, B)  
CAVI → 不匹配用。

4. 先 lock b6b 再 lock

5. transcode.  $64/66B \rightarrow 257/256$

4 ↑ one 66B 组合 2 - 257

如果 4 ↑ 66B 加 01, 则 组合 2

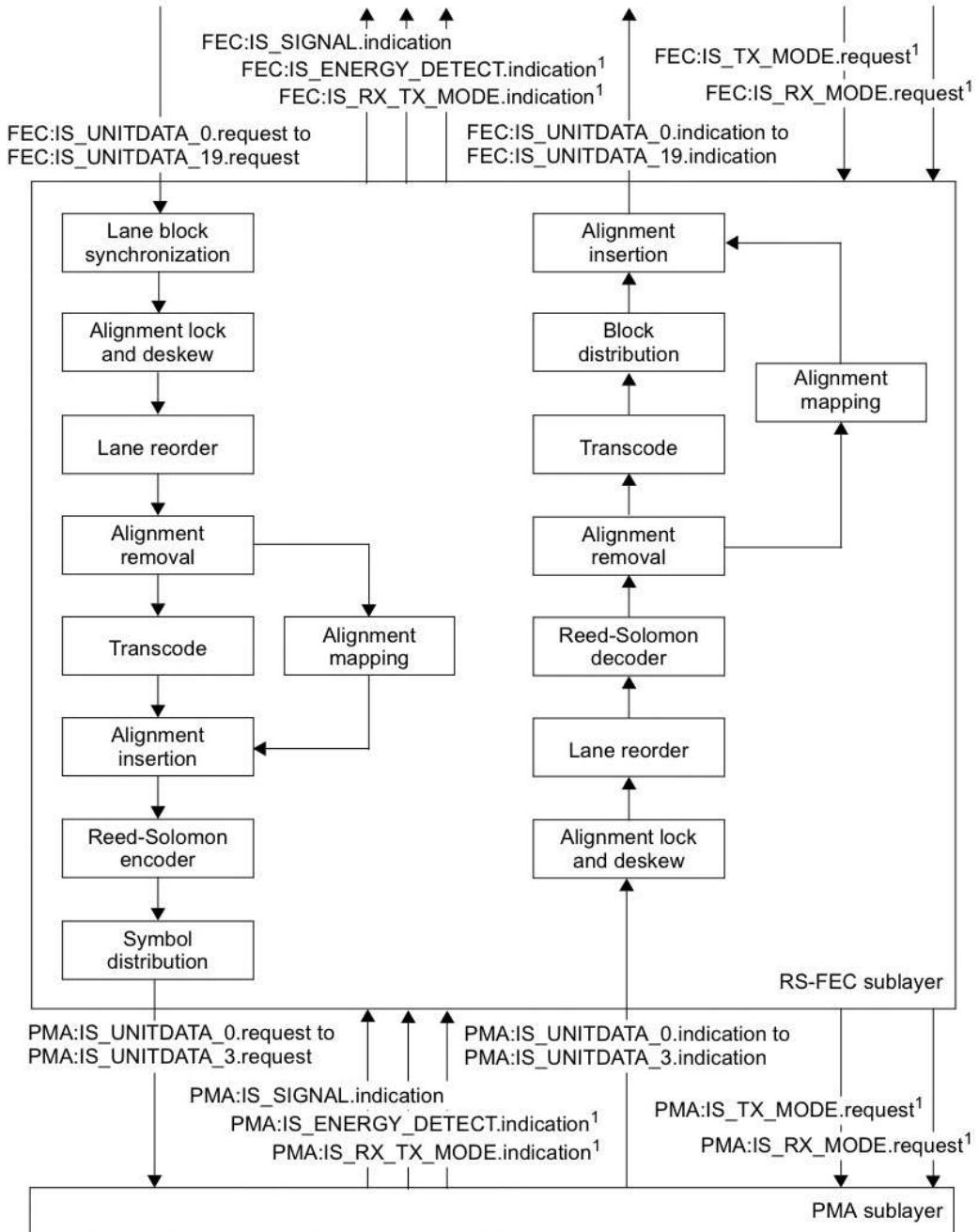
1 + 64B XY

如果 67 66B 中有 10, B 组合 2

0 + 4 个 SYNC HEADER [1]

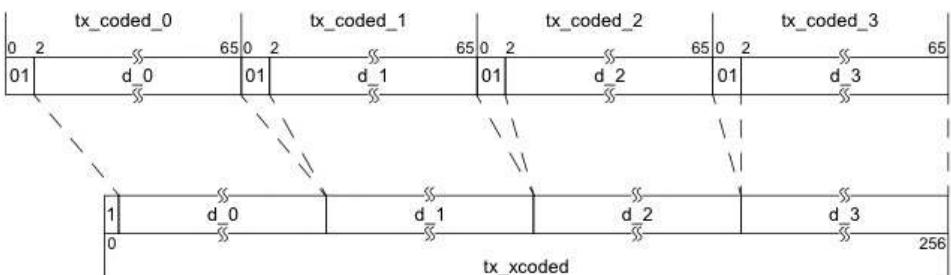
+ 64B XY - 4 (第一 control)

由 第二 nibble)

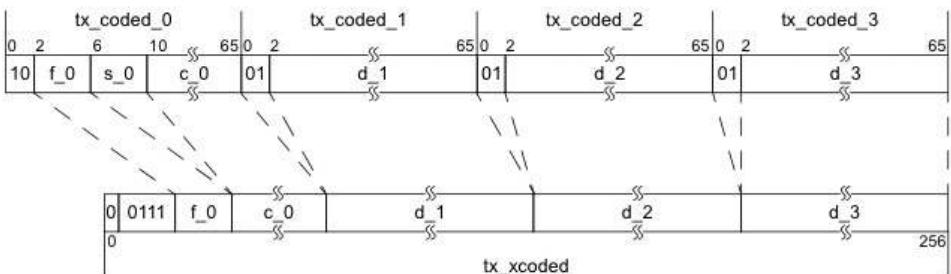


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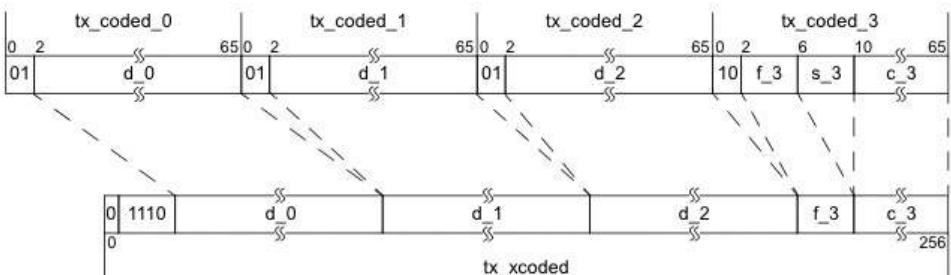
**NOTE 1—FOR OPTIONAL EEE DEEP SLEEP CAPABILITY**



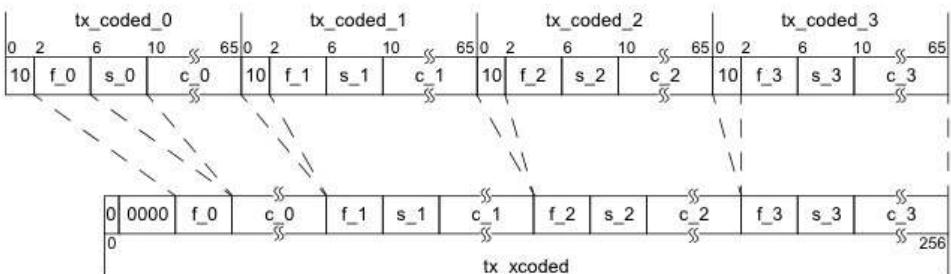
**Example 1: All data blocks**



**Example 2: Control block followed by three data blocks**



**Example 3: Three data blocks followed by a control block**



**Example 4: All control blocks**

b. 257 BTGE 头 5 字节会插入到第 68

$$\langle 4 \geq 0 \rangle = \langle 4 \geq 0 \rangle \text{ or } \langle 12 \geq 8 \rangle$$

$\langle 256 \geq 5 \rangle$  keep

FEC lane, $i$	Reed-Solomon symbol index, $k$ (10-bit symbols)																																	
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33
0	amp_tx_0	63	0	amp_tx_4	63	0	amp_tx_8	63	0	amp_tx_12	63	0	amp_tx_16	63	0																			
1	amp_tx_1	63	0	amp_tx_5	63	0	amp_tx_9	63	0	amp_tx_13	63	0	amp_tx_17	63	0																			
2	amp_tx_2	63	0	amp_tx_6	63	0	amp_tx_10	63	0	amp_tx_14	63	0	amp_tx_18	63	0																			
3	amp_tx_3	63	0	amp_tx_7	63	0	amp_tx_11	63	0	amp_tx_15	63	0	amp_tx_19	63	0																			

= 5-bit pad

tx\_scrambled

Figure 91-4—Alignment marker mapping to FEC lanes

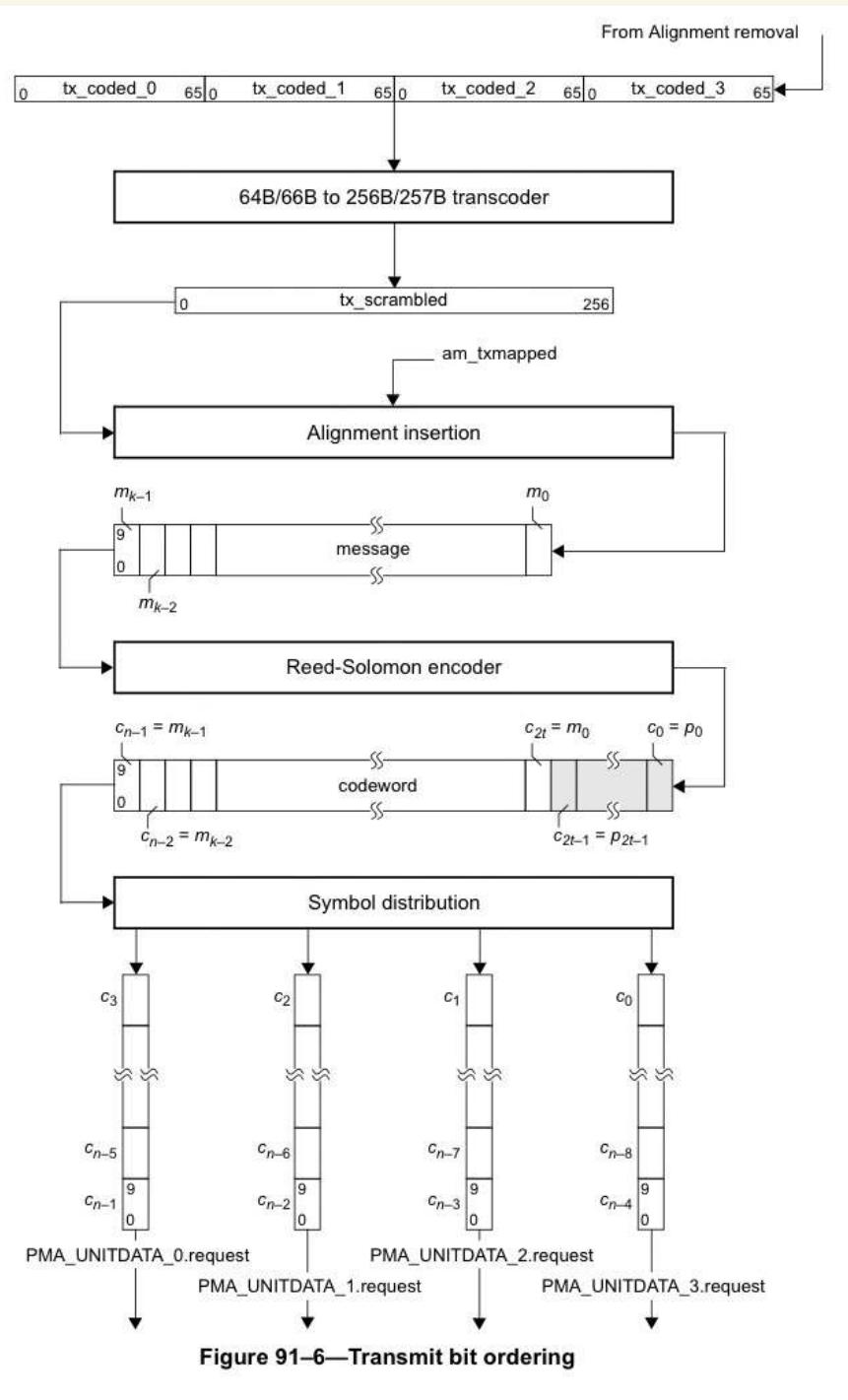
7. AM 会重新插入，原来 6 bbs 改为 64 bits  
<如何映射到 FEC 节点>，然后加上 5 bits 为 PAPD。总字节数  
为 1285，加 PAPD 后总共有 1320 (费 25) 为帧高  
度。

8.  $257 \times 20 = 5140$ , 配为 RS-code 编码

9. 编码完成后，BTG symbol 为 10 bits。按 5 ms/1000

10. 总比特数  $80 \times 64 = 5120$  =  $\frac{64}{65}$  RS28 symbol

在 22.5 ms 内



8. 同時 RX 例也允許 Lane swap.  
這樣 FGE AM 可 reorder.

P. - T codeword 長度 4

CR4, KR4, SR4 - bin 7

KP4 - bin 15

10. 无法纠正错误时，会将前两个  
6 bits 为 SYNC HEADER. 第二个

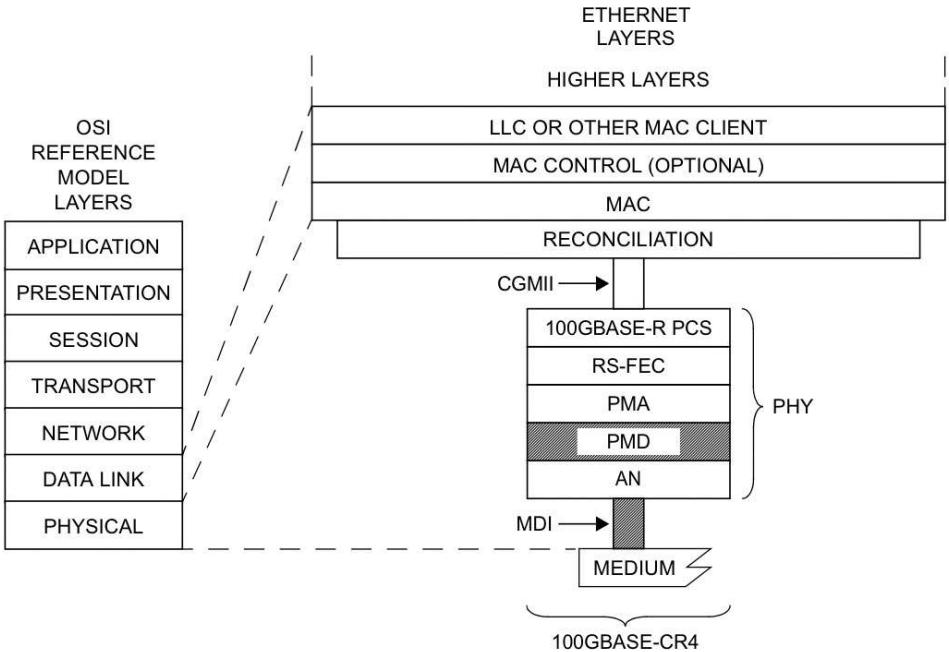
00 00 00 11

Associated clause	100GBASE-CR4
81—RS	Required
81—CGMII <sup>a</sup>	Optional
82—PCS for 100GBASE-R	Required
91—RS-FEC	Required
83—PMA for 100GBASE-R <sup>b</sup>	Required
83A—CAUI-10	Optional
83D—CAUI-4	Optional
73—Auto-Negotiation	Required
78—Energy Efficient Ethernet	Optional

<sup>a</sup>The CGMII is an optional interface. However, if the CGMII is not implemented, a conforming implementation must behave functionally as though the RS and CGMII were present.

<sup>b</sup>There are limitations on the number of PMA lanes that may be used between sublayers, see 83.

1. 4字Tone
2. AIN 完成 training pattern  $\rightarrow$   
40pbit & PRBS 和 TX
3. peak to peak  $\leq 3$  倍  $\rightarrow$  1200mV.  
TX 不得超過 3mm



AN = AUTO-NEGOTIATION

CGMII = 100 Gb/s MEDIA INDEPENDENT INTERFACE

LLC = LOGICAL LINK CONTROL

MAC = MEDIA ACCESS CONTROL

MDI = MEDIUM DEPENDENT INTERFACE

PCS = PHYSICAL CODING SUBLAYER

PHY = PHYSICAL LAYER DEVICE

PMA = PHYSICAL MEDIUM ATTACHMENT

PMD = PHYSICAL MEDIUM DEPENDENT

RS-FEC = REED-SOLOMON FORWARD ERROR CORRECTION

Figure 92-1—100GBASE-CR4 PMD relationship to the ISO/IEC Open Systems Interconnection (OSI) reference model and the IEEE 802.3 Ethernet model

4. 早撲  $\Rightarrow$  0 - 1.9V  
 $\beta_L$ -couple  $\leq 30mV$

5. Sends training by  $\frac{1}{2}$  當量  $\rightarrow$   $\frac{1}{2}$  正負

±0.0083 ~ 0.05 · 正  
 ±0.0083 ~ -0.05

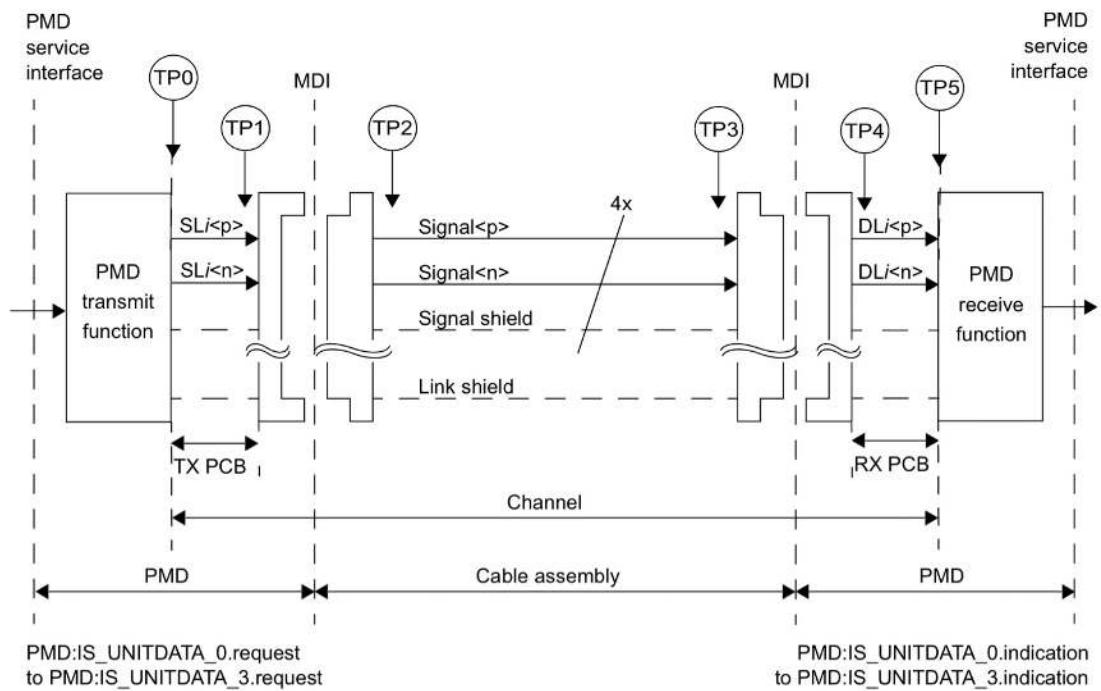


Figure 92-2—100GBASE-CR4 link (one direction is illustrated)

6. 速率 100 ppm  
 7. 有两种 connector, 指向何处都可  
 couple.

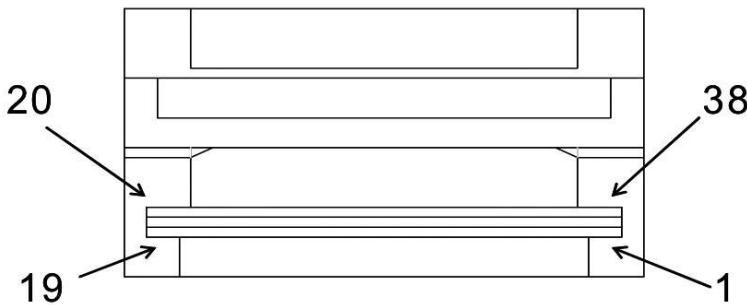


Figure 92-24—Style-1 example cable assembly

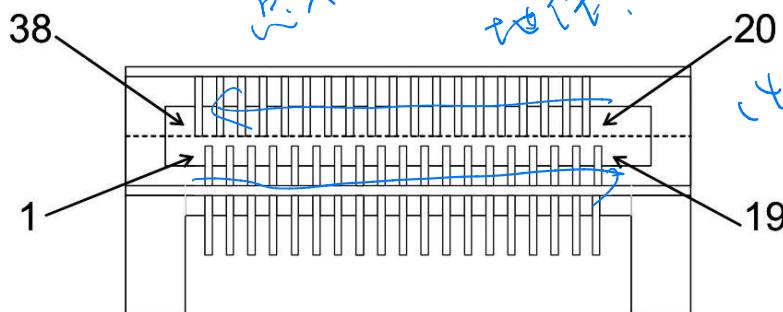


Figure 92-25—Style-1 example MDI board receptacle



Figure 92–26—Style-2 example cable assembly

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(07/27/16) 10:16 AM. 本也沒用

IEEE Std 802.3-2015  
IEEE Standard for Ethernet  
SECTION SIX

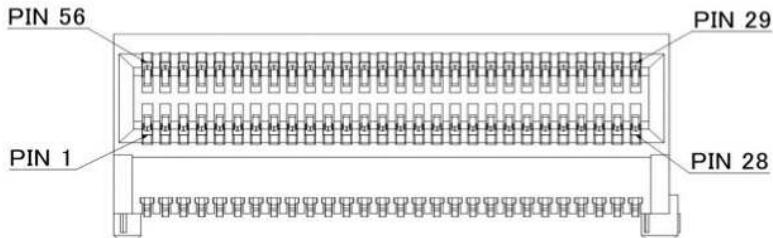


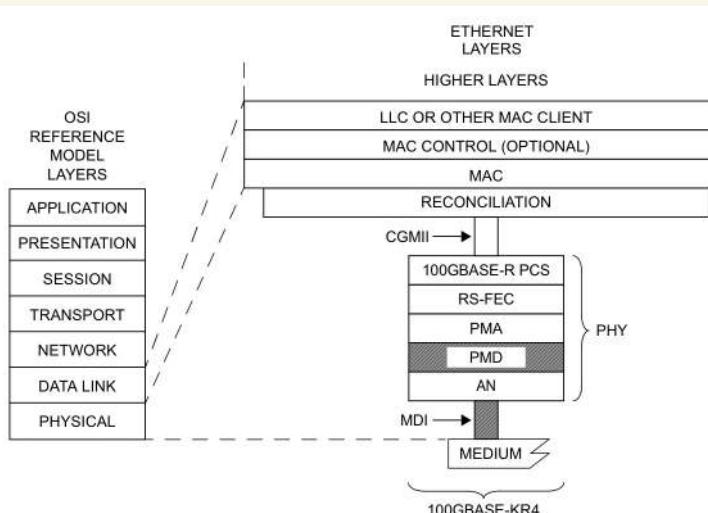
Figure 92–27—Style-2 example MDI board receptacle

**Table 93–1—Physical Layer clauses associated with the 100GBASE-KR4 PMD**

Associated clause	100GBASE-KR4
81—RS	Required
81—CGMII <sup>a</sup>	Optional
82—PCS for 100GBASE-R	Required
91—RS-FEC	Required
83—PMA for 100GBASE-R <sup>b</sup>	Required
83A—CAUI-10	Optional
83D—CAUI-4	Optional
73—Auto-Negotiation	Required
78—Energy-Efficient Ethernet	Optional

<sup>a</sup>The CGMII is an optional interface. However, if the CGMII is not implemented, a conforming implementation must behave functionally as though the RS and CGMII were present.

<sup>b</sup>There are limitations on the number of PMA lanes that may be used between sublayers, see 83.3.



AN = AUTO-NEGOTIATION

CGMII = 100 Gb/s MEDIA INDEPENDENT INTERFACE

LLC = LOGICAL LINK CONTROL

MAC = MEDIA ACCESS CONTROL

MDI = MEDIUM DEPENDENT INTERFACE

PCS = PHYSICAL CODING SUBLAYER

PHY = PHYSICAL LAYER DEVICE

PMA = PHYSICAL MEDIUM ATTACHMENT

PMD = PHYSICAL MEDIUM DEPENDENT

RS-FEC = REED-SOLOMON FORWARD ERROR CORRECTION

**Figure 93–1—100GBASE-KR4 PMD relationship to the ISO/IEC Open Systems Interconnection (OSI) reference model and the IEEE 802.3 Ethernet model**

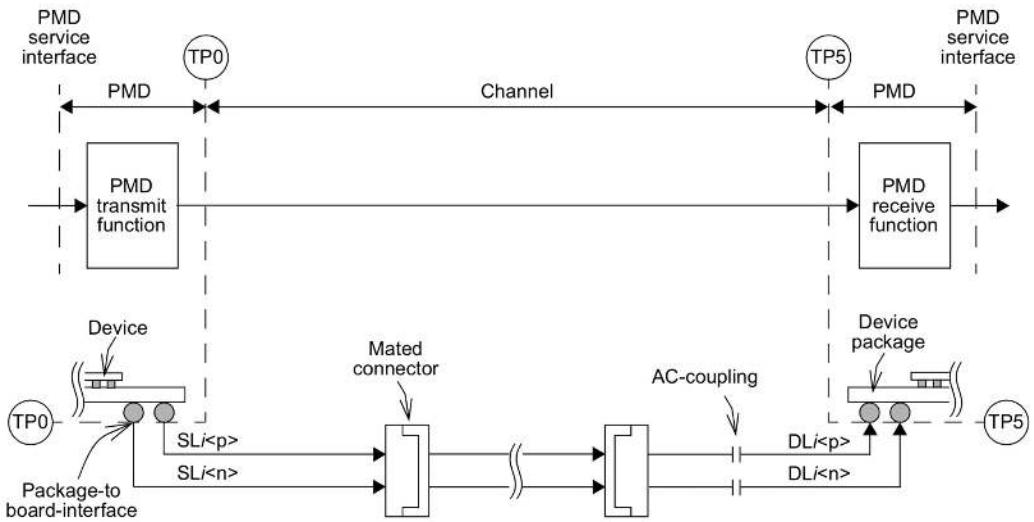


Figure 93–2—100GBASE-KR4 link (one direction for one lane is illustrated)

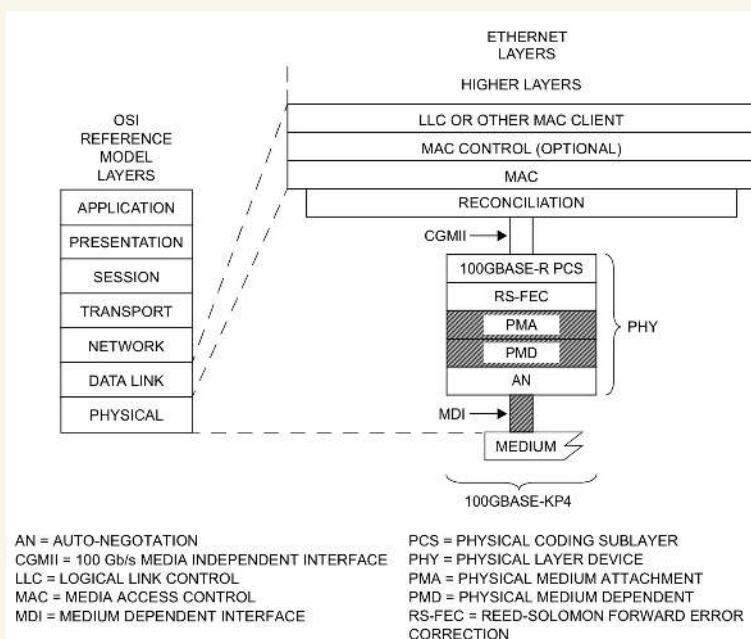
TX 发送先到 AC-coupling, 中间有电容对地 DC-common  
Voltage SPEC.

**Table 94–1—Physical Layer clauses associated with the 100GBASE-KP4 PMD**

Associated clause	100GBASE-KP4
81—RS	Required
81—CGMII <sup>a</sup>	Optional
82—PCS for 100GBASE-R	Required
83—PMA for 100GBASE-R	Optional
83A—CAUI-10	Optional
83D—CAUI-4	Optional
91—RS-FEC	Required
73—Auto-Negotiation	Required
78—Energy-Efficient Ethernet	Optional

<sup>a</sup>The CGMII is an optional interface. However, if the CGMII is not implemented, a conforming implementation must behave functionally as though the RS and CGMII were present.

$$BER < \epsilon - S$$



速度為  $26.5625 \text{ Gb/s}$  . 一隻四串

$$\frac{80 \times 64}{25} = \frac{5120}{X} \Rightarrow X = 26.5625.$$

lane

$\rightarrow$  2T FEC CW  
 $\rightarrow$  40 overhead

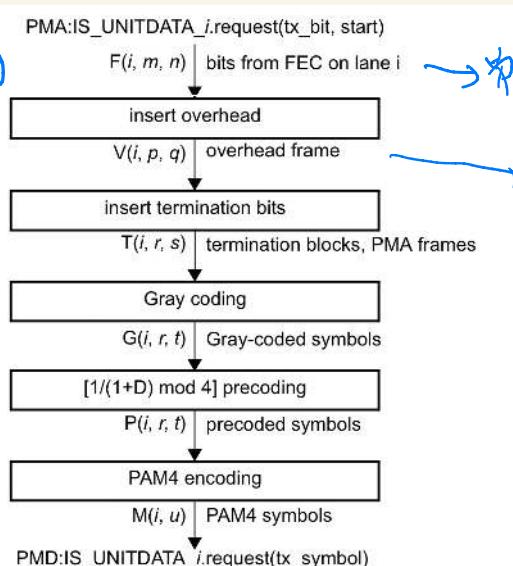


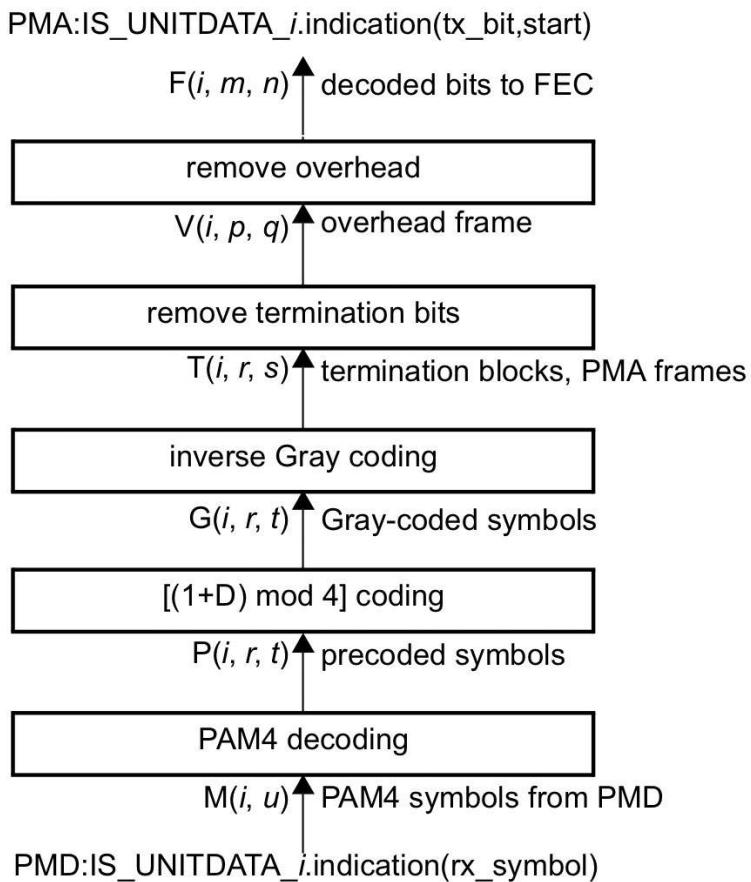
Figure 94-2—Transmit adaptation process diagram

PMA 亂語中再 start 標記位表示 codeword  
的開始

01100110  
01100110

Table 94-2—Default overhead configuration values

Parameter	Values (binary)
TX_OH_pattern(7:0)	01100110
TX_OH_sequence_0(4:0)	00110
TX_OH_sequence_1(4:0)	01010
TX_OH_sequence_2(4:0)	10101
TX_OH_sequence_3(4:0)	11001



**Figure 94–3—Receive adaptation process diagram**

1. PMD 从原语入参已经是PAM4信号。  
但实际上在图中显示为PMD到适配器的  
PMD 从何而来？

2. PMD 每条lane 速率是 12.5Gbps

≥ 10G 以上 由 BN 速率由 PLS + PMD 提供

供

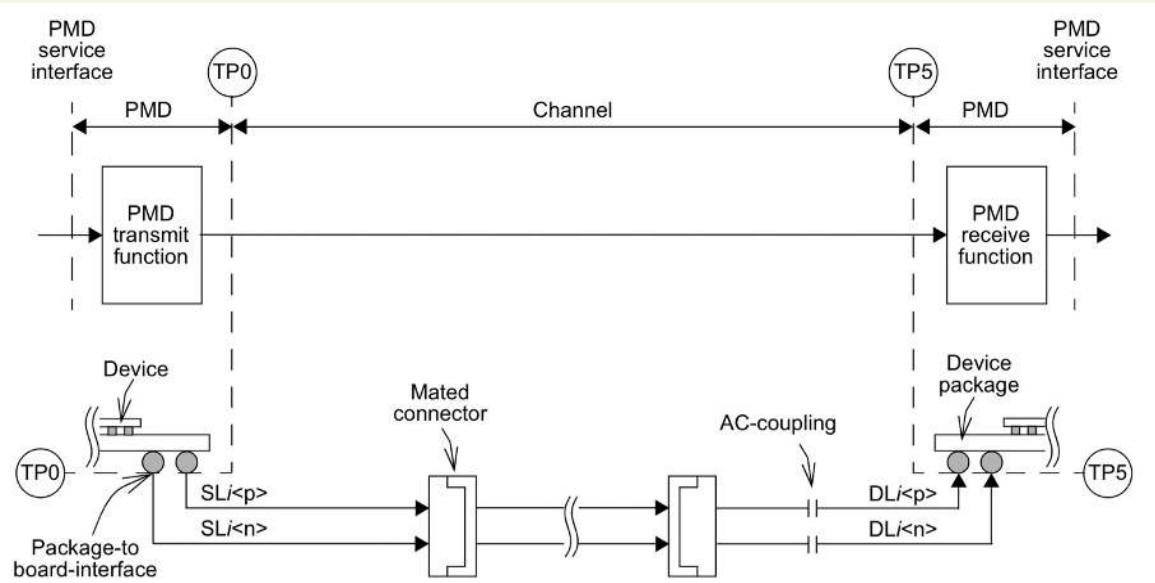


Figure 94-4—100GBASE-KP4 link (one direction for one lane is illustrated)

AN 因单向 manchester 编码，只用 PRM + 1 级  
- 两种 symbol.  
LINK TRAINING 时会有全局序号的重置。  
跟练是否所有 Lane 都完成了。  
正序用 PRBS 13 位 training pattern

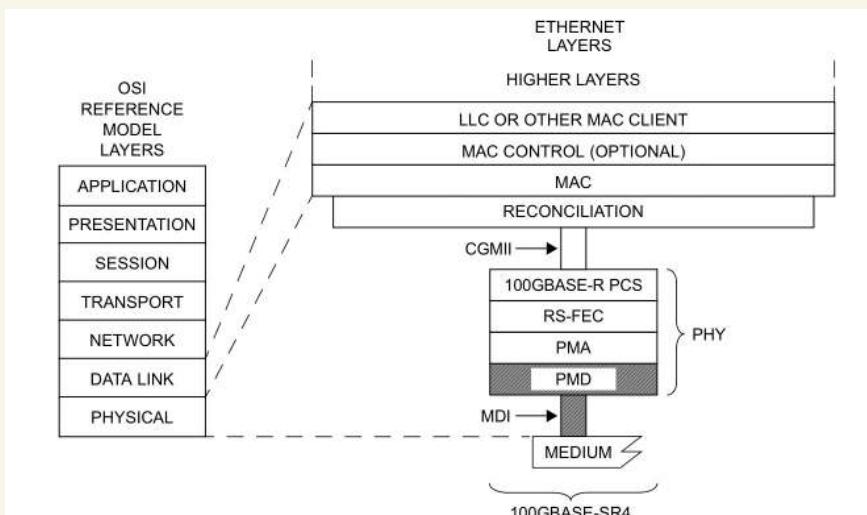
**Table 94–12—Training pattern initial sequences**

PMD Lane	Output of	Contents of first (top) and second (bottom) training frame words transmitted left to right
0	PRBS13	01001001101100111000101010110000100100111011100111010000011 101001011011010110110011010111101 000111110101101101111110100011011111010011110110010101110 0111001001110000111100001101011
	Gray code	1031320220111130103121231210112102121023131112 012221121322210113223312320320231023012301332
	Precoder	1301200200010130013201123322233220110021032320 01110101103333223211121021130331123112233001211
1	PRBS13	110111110101010000001001001101100111100010101011000010010011 0111001101101000011101001101110 1001100101001101100111111010110110111110100010110111110 10011110101001010110011100101111
	Gray code	2122111000310213123033320031023220233002331323 31202033230222332321122330321221022313113120312
	Precoder	23332322210023011221211312311202203002123021 320022120311112112011121302333220301012331233
2	PRBS13	11001011110000111101110110110011001100111000111000110000110 0001110111000001100110000001110 0010110000011001010100110010100110101010100001100 11110111010101011001100101010101
	Gray code	203220022323232020230230200232320020200023 02130130320131023333020310023123233202301111
	Precoder	2211131112030200220311220002220300022000021 0230012212001231121213312313301120303311301010
3	PRBS13	011011110100011101111101011001101111110001111011010111011110 01000010100010100010101111100 10010101010111001010011000010111111000101011010110010011111 100010101011001010001010111100
	Gray code	132210123223202122320221332232031130320332230 3133220311303122003211310222011132331011220
	Precoder	12023102111211313202133321203311232213202120213 323033312101221020003023210022232302123101113

**Table 95–1—Physical Layer clauses associated with the 100GBASE-SR4 PMD**

Associated clause	100GBASE-SR4
81—RS	Required
81—CGMII <sup>a</sup>	Optional
82—PCS for 100GBASE-R	Required
83—PMA for 100GBASE-R	Required
91—RS-FEC <sup>b</sup>	Required
83A—CAUI-10	Optional
83B—Chip-to-module CAUI-10 <sup>c</sup>	Optional
83D—CAUI-4	Optional
83E—Chip-to-module CAUI-4	Optional
78—Energy Efficient Ethernet	Optional

<sup>a</sup>The CGMII is an optional interface. However, if the CGMII is not implemented, a conforming implementation must behave functionally as though the RS and CGMII were present.



CGMII = 100 Gb/s MEDIA INDEPENDENT INTERFACE

LLC = LOGICAL LINK CONTROL

MAC = MEDIA ACCESS CONTROL

MDI = MEDIUM DEPENDENT INTERFACE

PCS = PHYSICAL CODING SUBLAYER

PHY = PHYSICAL LAYER DEVICE

PMA = PHYSICAL MEDIUM ATTACHMENT

PMD = PHYSICAL MEDIUM DEPENDENT

RS-FEC = REED-SOLOMON FORWARD ERROR

CORRECTION

SR = PMD FOR MULTIMODE FIBER

**Figure 95–1—100GBASE-SR4 PMD relationship to the ISO/IEC Open Systems Interconnection (OSI) reference model and the IEEE 802.3 Ethernet model**

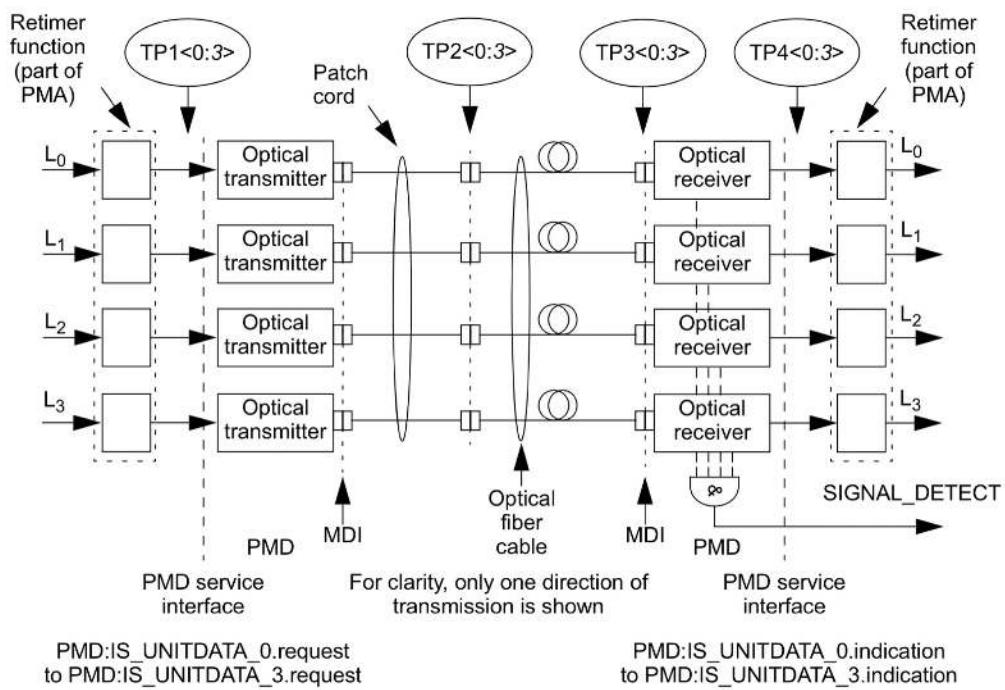


Figure 95–2—Block diagram for 100GBASE-SR4 transmit/receive paths

Table 95–6—100GBASE-SR4 transmit characteristics

Description	Value	Unit
Signaling rate, each lane (range)	$25.78125 \pm 100$ ppm	GBd
Center wavelength (range)	840 to 860	nm
RMS spectral width <sup>a</sup> (max)	0.6	nm
Average launch power, each lane (max)	2.4	dBm
Average launch power, each lane (min)	-8.4	dBm
Optical Modulation Amplitude (OMA), each lane (max)	3	dBm
Optical Modulation Amplitude (OMA), each lane (min) <sup>b</sup>	-6.4	dBm
Launch power in OMA minus TDEC (min)	-7.3	dBm
Transmitter and dispersion eye closure (TDEC), each lane (max)	4.3	dB
Average launch power of OFF transmitter, each lane (max)	-30	dBm
Extinction ratio (min)	2	dB
Optical return loss tolerance (max)	12	dB
Encircled flux <sup>c</sup>	$\geq 86\%$ at $19 \mu\text{m}$ $\leq 30\%$ at $4.5 \mu\text{m}$	
Transmitter eye mask definition {X1, X2, X3, Y1, Y2, Y3} Hit ratio $1.5 \times 10^{-3}$ hits per sample	{0.3, 0.38, 0.45, 0.35, 0.41, 0.5}	

<sup>a</sup>RMS spectral width is the standard deviation of the spectrum.

<sup>b</sup>Even if the TDEC < 0.9 dB, the OMA (min) must exceed this value.

<sup>c</sup>If measured into type A1a.2 or type A1a.3 50  $\mu\text{m}$  fiber in accordance with IEC 61280-1-4.

Table 95–13—Optical fiber and cable characteristics

Description	OM3 <sup>a</sup>	OM4 <sup>b</sup>	Unit
Nominal core diameter	50		μm
Nominal fiber specification wavelength	850		nm
Effective modal bandwidth (min) <sup>c</sup>	2000	4700	MHz.km
Cabled optical fiber attenuation (max)	3.5		dB/km
Zero dispersion wavelength ( $\lambda_0$ )	$1295 \leq \lambda_0 \leq 1340$		nm
Chromatic dispersion slope (max) ( $S_0$ )	0.105 for $1295 \leq \lambda_0 \leq 1310$ and 0.000375 × $(1590 - \lambda_0)$ for $1310 \leq \lambda_0 \leq 1340$		ps/nm <sup>2</sup> km

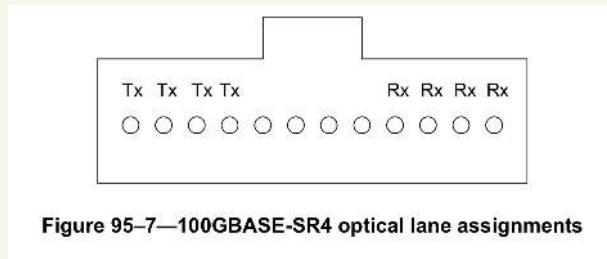
<sup>a</sup>IEC 60793-2-10 type A1a.2<sup>b</sup>IEC 60793-2-10 type A1a.3<sup>c</sup>When measured with the launch conditions specified in Table 95–6

Figure 95–7—100GBASE-SR4 optical lane assignments

PMA 和 PMD 的主要部分或  
相互通信 \* PUI 指令 (一般同子 chip to chip )  
PMA, PMD, module (无EDR) 之 [ ]  
可用 NPII ( 同 40GSR4, 40GLR4,  
100G SR40 )

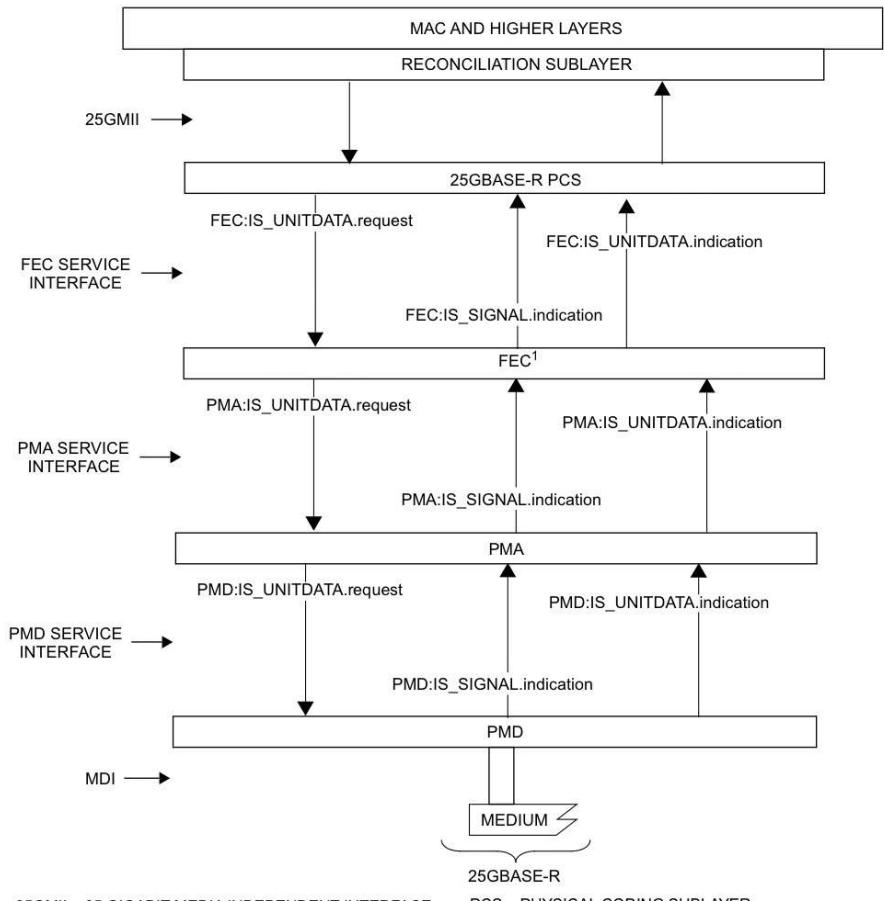
**Table 105–1—25 Gb/s PHYs**

Name	Description
25GBASE-CR	25 Gb/s PHY using 25GBASE-R encoding over one lane of twinaxial copper cable (see 1.4.480 and Clause 110).
25GBASE-CR-S	25 Gb/s PHY equivalent to 25GBASE-CR without support for the RS-FEC sublayer (see Clause 110).
25GBASE-KR	25 Gb/s PHY using 25GBASE-R encoding over one lane of an electrical backplane (see Clause 111).
25GBASE-KR-S	25 Gb/s PHY equivalent to 25GBASE-KR without support for the RS-FEC sublayer (see Clause 111).
25GBASE-SR	25 Gb/s PHY using 25GBASE-R encoding over a duplex multimode fiber (see Clause 112).
25GBASE-LR	25 Gb/s PHY using 25GBASE-R encoding over a duplex single-mode fiber, with reach up to at least 10 km (see Clause 114).
25GBASE-ER	25 Gb/s PHY using 25GBASE-R encoding over a duplex single-mode fiber, with reach up to at least 40 km (see Clause 114).
25GBASE-T	25 Gb/s PHY using RS-FEC and LDPC encoding over balanced twisted-pair structured cabling systems (see Clause 113).

**Table 105–2—Nomenclature and clause correlation, 25 Gb/s Ethernet PHYs**

Nomenclature	Clause/Annex															
	28	73	74	78	106	107	108	109	109A	109B	110	111	112	113	114	
25GBASE-CR	M <sup>a</sup>	M	O <sup>a</sup>	M	O	M	M	M	O	M	25GBASE-CR PMD	25GBASE-CR-S PMD	25GBASE-KR PMD	25GBASE-KR-S PMD	25GBASE-SR PMD	25GBASE-T PCS/PMA
25GBASE-CR-S	M	M	O	M	O	M	M	M	O	M	25GBASE-CR-S PMD	25GBASE-KR PMD	25GBASE-SR PMD	25GBASE-T PCS/PMA	25GBASE-LR PMD	25GBASE-FR PMD
25GBASE-KR	M	M	O	M	O	M	M	M	O	M	25GBASE-CR-S PMD	25GBASE-KR PMD	25GBASE-SR PMD	25GBASE-T PCS/PMA	25GBASE-LR PMD	25GBASE-FR PMD
25GBASE-KR-S	M	M	O	M	O	M	M	M	O	M	25GBASE-CR-S PMD	25GBASE-KR PMD	25GBASE-SR PMD	25GBASE-T PCS/PMA	25GBASE-LR PMD	25GBASE-FR PMD
25GBASE-SR			O	M	O	M	M	M	O	O	25GBASE-CR-S PMD	25GBASE-KR PMD	25GBASE-SR PMD	25GBASE-T PCS/PMA	25GBASE-LR PMD	25GBASE-FR PMD
25GBASE-T	M			O	M	O					25GBASE-CR-S PMD	25GBASE-KR PMD	25GBASE-SR PMD	25GBASE-T PCS/PMA	25GBASE-LR PMD	25GBASE-FR PMD
25GBASE-LR				O	M	O	M	M	M	O	25GBASE-CR-S PMD	25GBASE-KR PMD	25GBASE-SR PMD	25GBASE-T PCS/PMA	25GBASE-LR PMD	25GBASE-FR PMD
25GBASE-ER			O	M	O	M	M	M	O	O	25GBASE-CR-S PMD	25GBASE-KR PMD	25GBASE-SR PMD	25GBASE-T PCS/PMA	25GBASE-LR PMD	25GBASE-FR PMD

<sup>a</sup>O = Optional, M = Mandatory



25GMII = 25 GIGABIT MEDIA INDEPENDENT INTERFACE

FEC = FORWARD ERROR CORRECTION

MAC = MEDIA ACCESS CONTROL

MDI = MEDIUM DEPENDENT INTERFACE

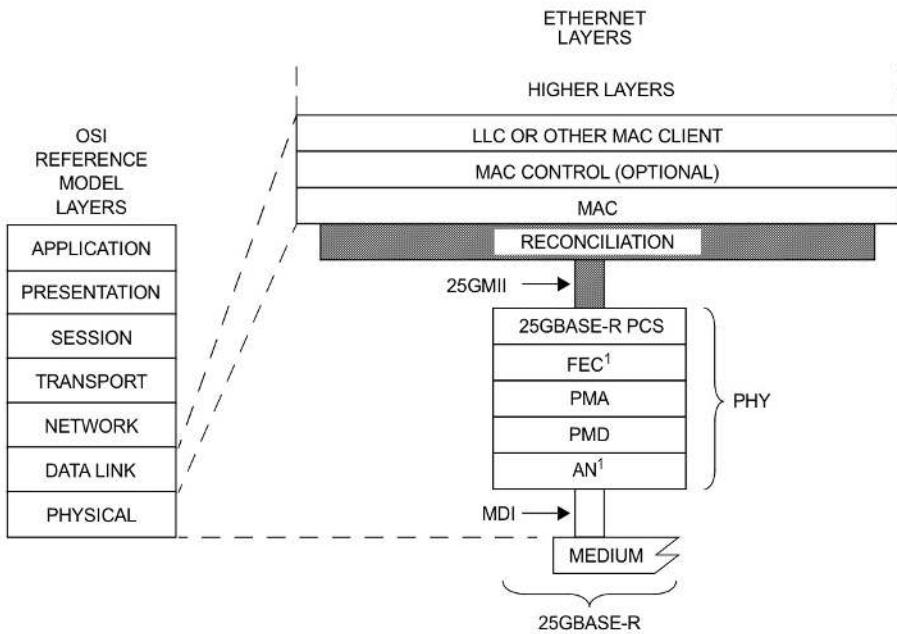
PCS = PHYSICAL CODING SUBLAYER

PMA = PHYSICAL MEDIUM ATTACHMENT

PMD = PHYSICAL MEDIUM DEPENDENT

NOTE 1—CONDITIONAL BASED ON PHY TYPE

**Figure 105–2—25GBASE-R inter-sublayer service interfaces**



25GMII = 25 GIGABIT MEDIA INDEPENDENT INTERFACE

AN = AUTO-NEGOTIATION

FEC = FORWARD ERROR CORRECTION

LLC = LOGICAL LINK CONTROL

MAC = MEDIA ACCESS CONTROL

MDI = MEDIUM DEPENDENT INTERFACE

PCS = PHYSICAL CODING SUBLAYER

PHY = PHYSICAL LAYER DEVICE

PMA = PHYSICAL MEDIUM ATTACHMENT

PMD = PHYSICAL MEDIUM DEPENDENT

NOTE 1—CONDITIONAL BASED ON PHY TYPE

**Figure 106–1—RS and 25GMII relationship to the ISO/IEC Open Systems Interconnection (OSI) reference model and the IEEE 802.3 Ethernet model**

The following are the major concepts of 25GMII:

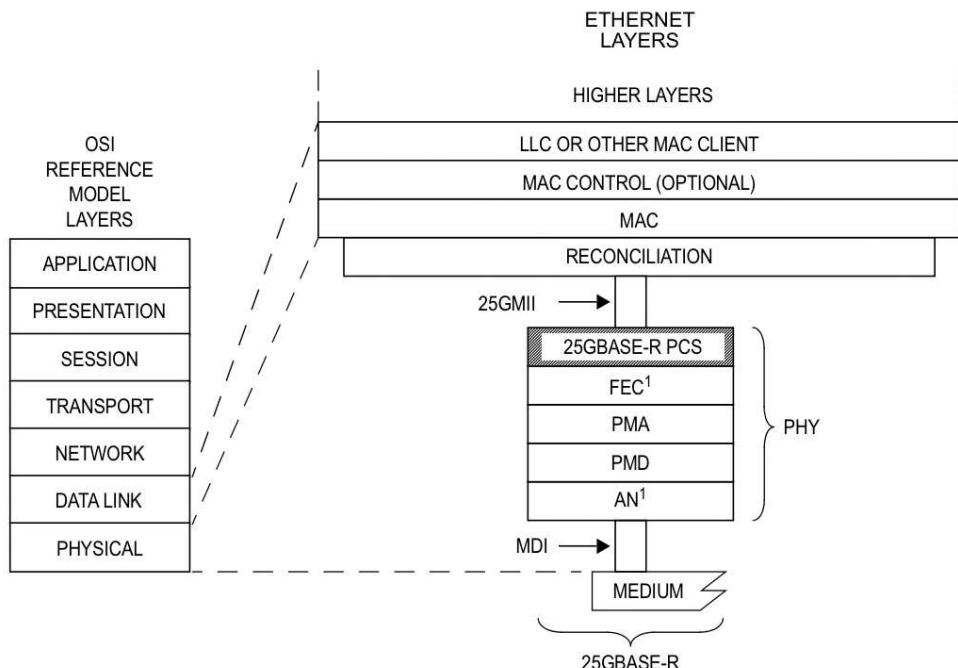
- a) The 25GMII is functionally similar to other media independent interfaces that have been defined for other speeds, as they all define an interface allowing independent development of MAC and PHY logic.
- b) The RS converts between the MAC serial data stream and the parallel data paths of the 25GMII.
- c) The RS maps the signal set provided at the 25GMII to the PLS service primitives provided at the MAC.
- d) Each direction of data transfer is independent and serviced by data, control, and clock signals.
- e) The RS generates continuous data or control characters on the transmit path and expects continuous data or control characters on the receive path.
- f) The RS participates in link fault detection and reporting by monitoring the receive path for status reports that indicate an unreliable link and generating status reports on the transmit path to report detected link faults to the DTE on the remote end of the connecting link.
- g) The 25GMII may also support Low Power Idle (LPI) signaling for PHY types supporting Energy-Efficient Ethernet (EEE) (see Clause 78).

25GMII 和 XGMII - 3A

The 25GBASE-R PCS is identical to the 10GBASE-R PCS specified in Clause 49 with three exceptions:

- 1) It has a single-bit interface to the Physical Medium Attachment (PMA) sublayer rather than the 16-bit interface described in Clause 49.
- 2) It has the ability to generate the scrambled idle test pattern.
- 3) hi\_ber is asserted if ber\_cnt reaches 97 in a 2 ms period. This differs from the definition in 49.2.13.3, which defines hi\_ber as occurring if ber\_cnt reaches 16 in a 125  $\mu$ s period.

手写说明：物理层接口 PMA 层只有 1 bit



25GMII = 25 GIGABIT MEDIA INDEPENDENT INTERFACE

AN = AUTO-NEGOTIATION

FEC = FORWARD ERROR CORRECTION

LLC = LOGICAL LINK CONTROL

MAC = MEDIA ACCESS CONTROL

MDI = MEDIUM DEPENDENT INTERFACE

PCS = PHYSICAL CODING SUBLAYER

PHY = PHYSICAL LAYER DEVICE

PMA = PHYSICAL MEDIUM ATTACHMENT

PMD = PHYSICAL MEDIUM DEPENDENT

NOTE 1—CONDITIONAL BASED ON PHY TYPE

**Figure 107-1—25GBASE-R PCS relationship to the ISO/IEC Open Systems Interconnection (OSI) reference model and IEEE 802.3 Ethernet model**

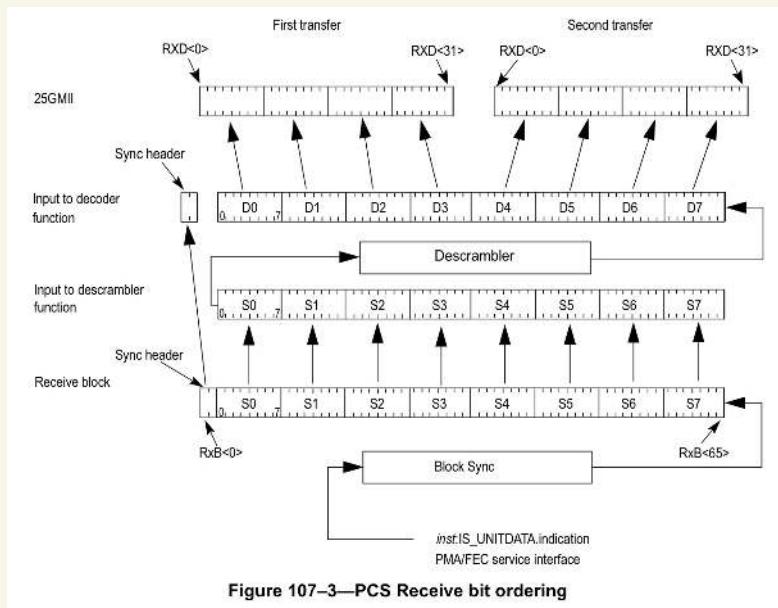
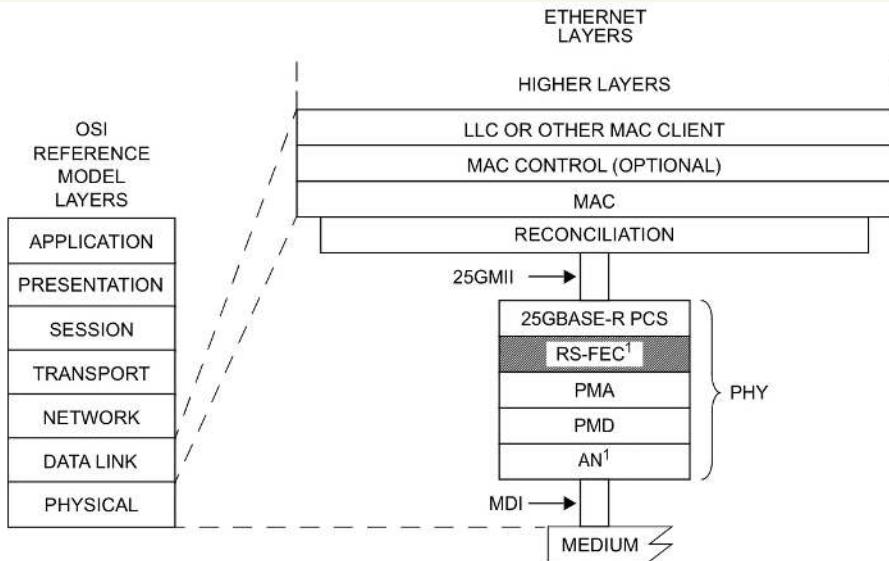


Figure 107-3—PCS Receive bit ordering

25G BASE-KR, KR-S, CR, CR-S  
P8段和PCS協同支撑AN.



25GMII = 25 GIGABIT MEDIA INDEPENDENT INTERFACE

AN = AUTO-NEGOTIATION

LLC = LOGICAL LINK CONTROL

MAC = MEDIA ACCESS CONTROL

MDI = MEDIUM DEPENDENT INTERFACE

PCS = PHYSICAL CODING SUBLAYER

PHY = PHYSICAL LAYER DEVICE

PMA = PHYSICAL MEDIUM ATTACHMENT

PMD = PHYSICAL MEDIUM DEPENDENT

RS-FEC = REED-SOLOMON FORWARD ERROR CORRECTION

NOTE 1—CONDITIONAL BASED ON PHY TYPE

**Figure 108–1—25GBASE-R RS-FEC relationship to the ISO/IEC Open Systems Interconnection (OSI) reference model and the IEEE 802.3 Ethernet model**

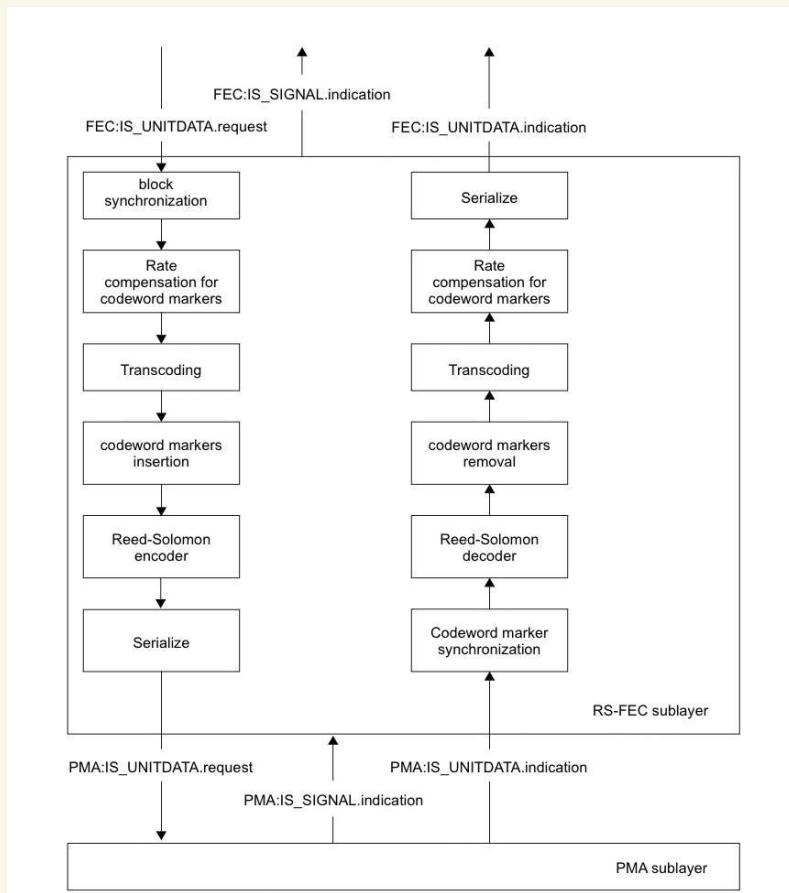
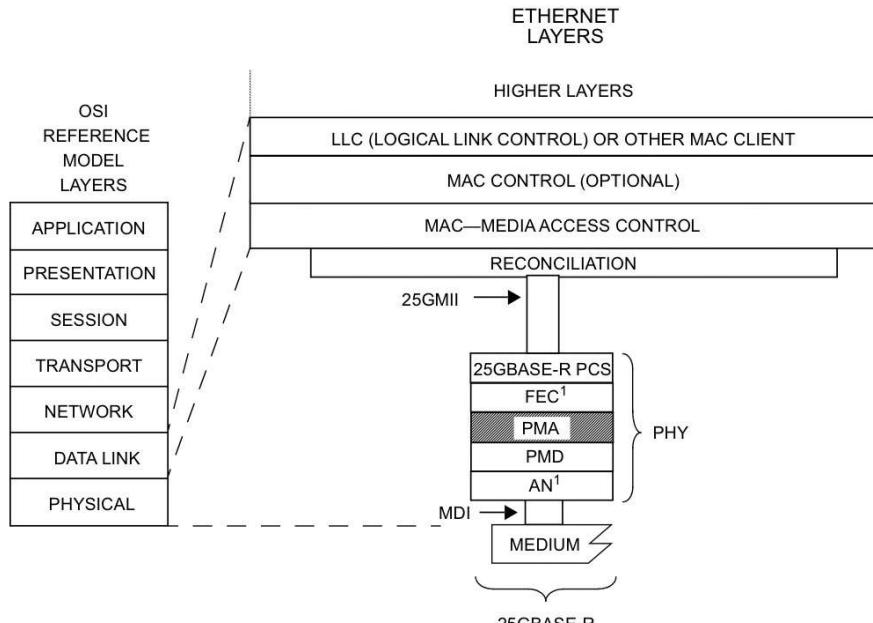


Figure 108-2—Functional block diagram

用於速率(528, 514)串行化728 symbol, 28  
高 BER 時的冗餘。  
FEC 有 BYPASS - correction 模式，只接收  
錯誤，不纠正错误。



25GMII = 25 GIGABIT MEDIA INDEPENDENT INTERFACE

AN = AUTO-NEGOTIATION

FEC = FORWARD ERROR CORRECTION

LLC = LOGICAL LINK CONTROL

MDI = MEDIUM DEPENDENT INTERFACE

PCS = PHYSICAL CODING SUBLAYER

PHY = PHYSICAL LAYER DEVICE

PMA = PHYSICAL MEDIUM ATTACHMENT

PMD = PHYSICAL MEDIUM DEPENDENT

NOTE 1—CONDITIONAL BASED ON PHY TYPE

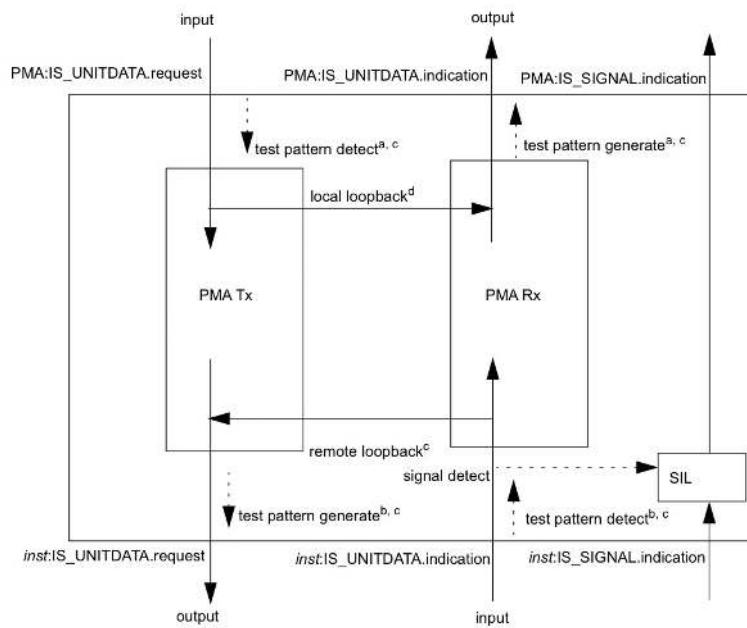
**Figure 109–1—25GBASE-R PMA relationship to the ISO/IEC Open Systems Interconnection (OSI) reference model and IEEE 802.3 Ethernet model**

1. CDR.

2. 傳輸延遲

3. Loopback 和 remote loopback.

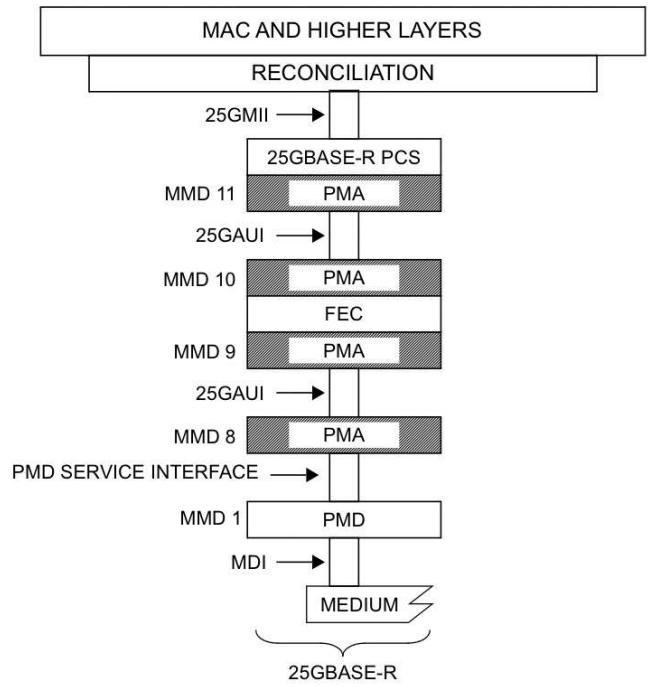
4. test-pattern



*inst* = PMD, PMA, or FEC, depending on which sublayer is below this PMA  
 SIL = Signal Indication Logic

- <sup>a</sup> If 25GAUI immediately above this PMA.
- <sup>b</sup> If 25GAUI or PMD service interface immediately below this PMA.
- <sup>c</sup> Optional.
- <sup>d</sup> Conditional (see 109.4.2)

**Figure 109–2—PMA Functional Block Diagram**

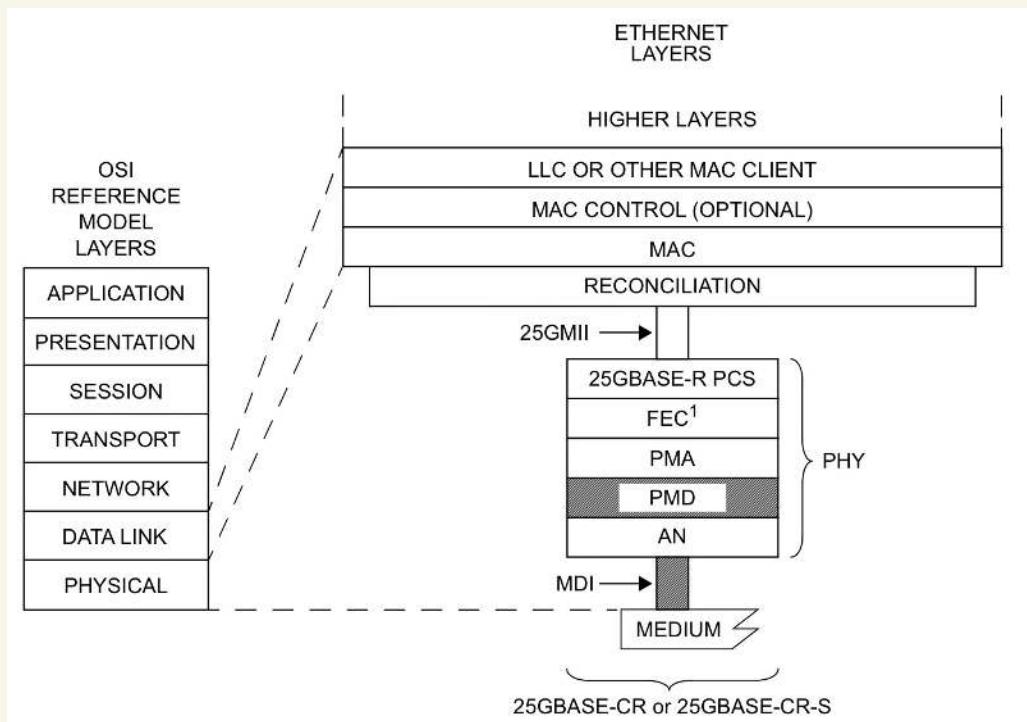


25GAUI = 25 GIGABIT ATTACHMENT UNIT INTERFACE  
 25GMII = 25 GIGABIT MEDIA INDEPENDENT INTERFACE  
 FEC = FORWARD ERROR CORRECTION  
 MAC = MEDIA ACCESS CONTROL  
 MDI = MEDIUM DEPENDENT INTERFACE

MMD = MDIO MANAGEABLE DEVICE  
 PCS = PHYSICAL CODING SUBLAYER  
 PMA = PHYSICAL MEDIUM ATTACHMENT  
 PMD = PHYSICAL MEDIUM DEPENDENT

**Figure 109–3—Example 25GBASE-R PMA layering**

PRBS 5 pattern 打死也 PRBS 31



25GBASE-CR: RS-PGL & RASG-R

FEC

25GBASE-CR-S: RASG-R FEC

One direction of a 25GBase-CR or 25GBase-CR-S link is shown in Figure 110-2.

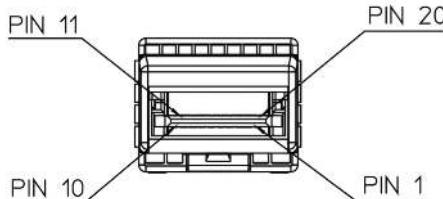
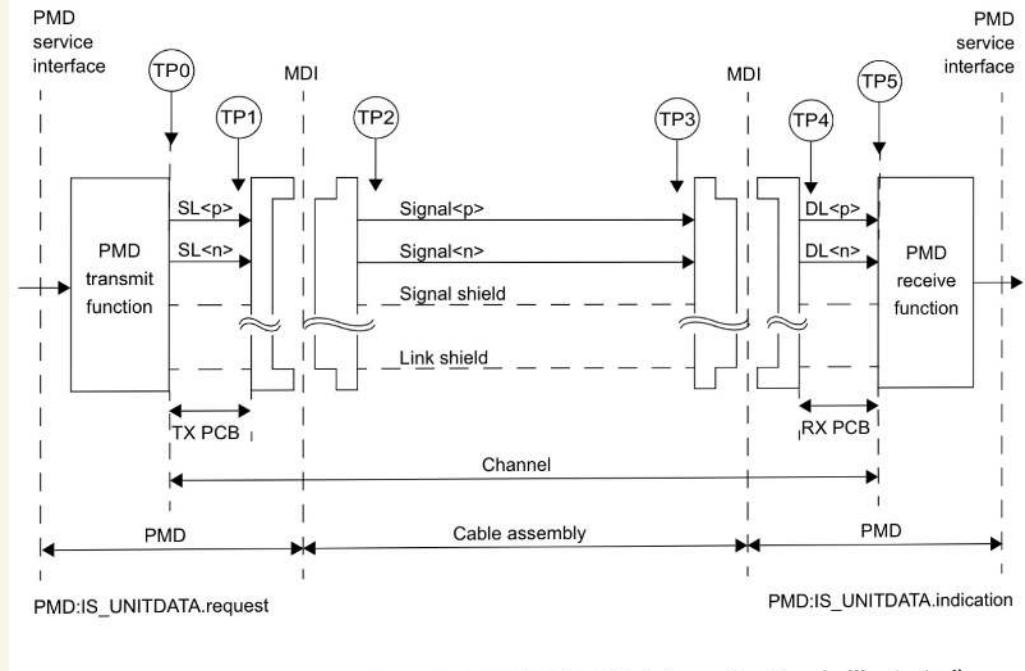


Figure 110-4—SFP28 cable assembly plug

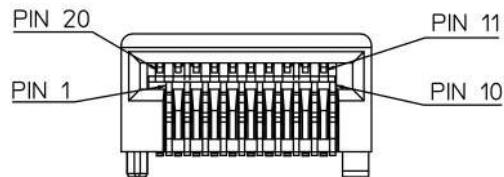


Figure 110-5—SFP28 example MDI board receptacle

Table 110-12—Lane to MDI connector contact mapping

Rx lane	MDI connector contact	Tx lane	MDI connector contact
signal gnd	S11	signal gnd	S17
DL<n>	S12	SL<p>	S18
DL<p>	S13	SL<n>	S19
signal gnd	S14	signal gnd	S20

Table 111-1—Physical Layer clauses associated with the 25GBASE-KR and 25GBASE-KR-S PMDs

Associated clause	25GBASE-KR	25GBASE-KR-S
106—RS	Required	Required
106—25GMII <sup>a</sup>	Optional	Optional
107—PCS	Required	Required
74—BASL-R FEC <sup>b</sup>	Required	Required
108—RS-FEC <sup>b</sup>	Required	N/A
109—PMA	Required	Required
109A—25GAUI C2C	Optional	Optional
73—Auto-Negotiation	Required	Required
78—Energy Efficient Ethernet	Optional	Optional

<sup>a</sup>The 25GMII is an optional interface. However, if the 25GMII is not implemented, a conforming implementation must behave functionally as though the RS and 25GMII were present.

<sup>b</sup>FEC sublayer can be enabled or disabled according to the FEC mode (see 111.6).

RS-FEC. 2-5 μs  
BBIG-R FEC. 2-8 μs  
无 FEC. 2-12 μs

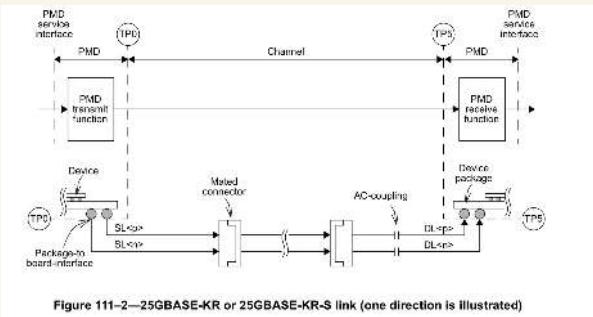
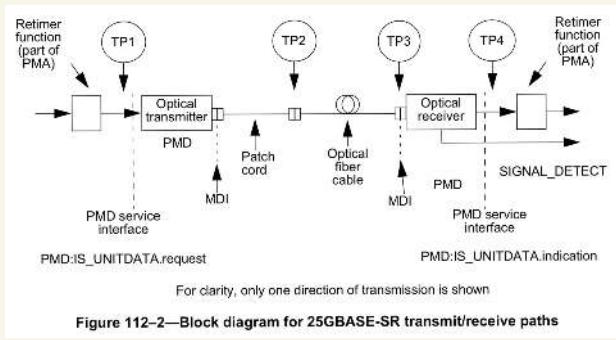


Figure 111-2—25GBASE-KR or 25GBASE-KR-S link (one direction is illustrated)

KR 62, PMD is implementation-dependent



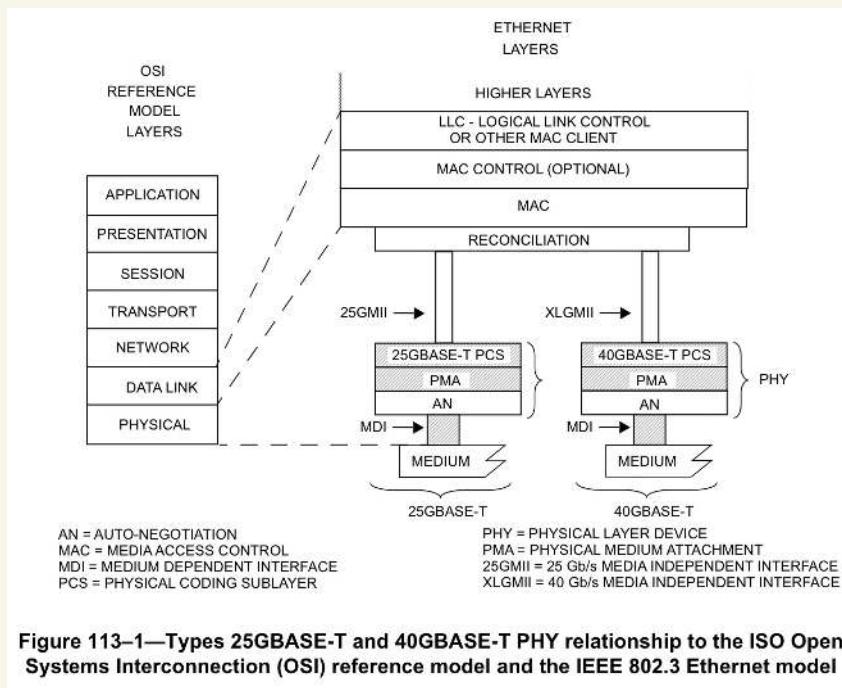


Figure 113-1—Types 25GBASE-T and 40GBASE-T PHY relationship to the ISO Open Systems Interconnection (OSI) reference model and the IEEE 802.3 Ethernet model

也是同 DS128

PC → ↔ PMA，和 SR, CR 不一样。  
PC 向上提供媒体无关接口 MII 接口。

自带 RS-FEC

**Table 114–1—Physical Layer clauses associated with the 25GBASE-LR and 25GBASE-ER PMDs**

Associated clause	25GBASE-LR	25GBASE-ER
106—RS	Required	Required
106—25GMII <sup>a</sup>	Optional	Optional
107—PCS for 25GBASE-R	Required	Required
108—RS-FEC <sup>b</sup>	Required	Required
109—PMA for 25GBASE-R	Required	Required
109A—25GAUI C2C	Optional	Optional
109B—25GAUI C2M	Optional	Optional
78—Energy Efficient Ethernet	Optional	Optional

<sup>a</sup>The 25GMII is an optional interface. However, if the 25GMII is not implemented, a conforming implementation must behave functionally as though the RS and 25GMII were present.

<sup>b</sup>The option to bypass the Clause 108 RS-FEC correction function is not supported.

圖15-3 POF 6-3P TIA-32

GMII → 65bit PDB → scrambled

→ MLCC → PAM1b → 225 MBd.

#### 115.1.6 Functional block diagram

Figure 115-3 provides a functional block diagram of the 1000BASE-RHx PHY.

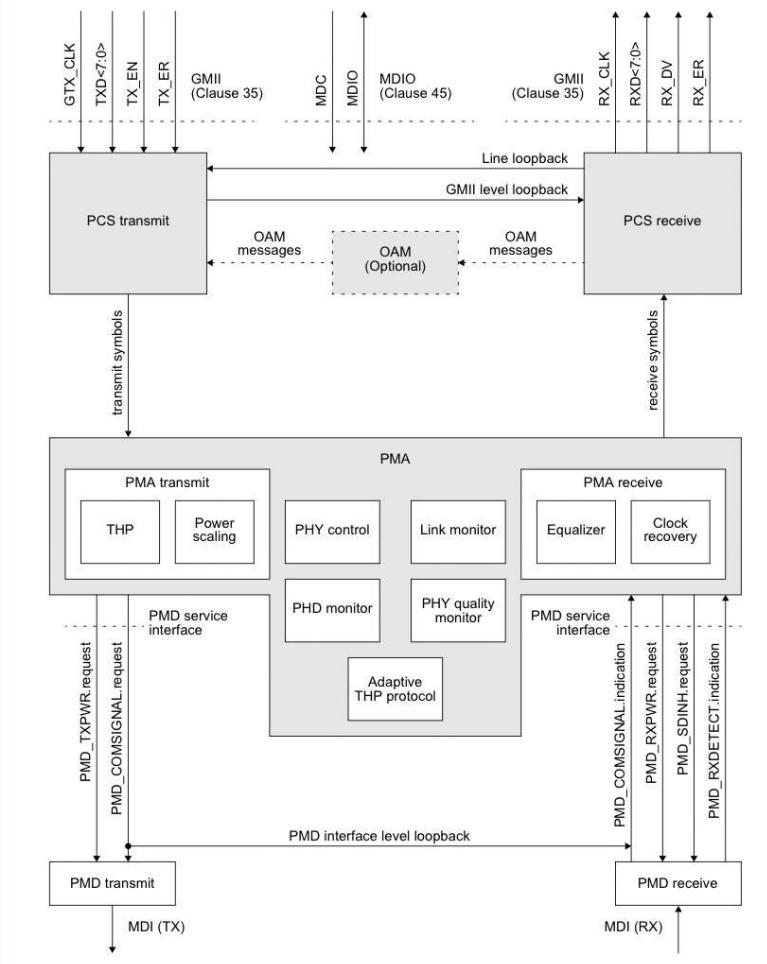
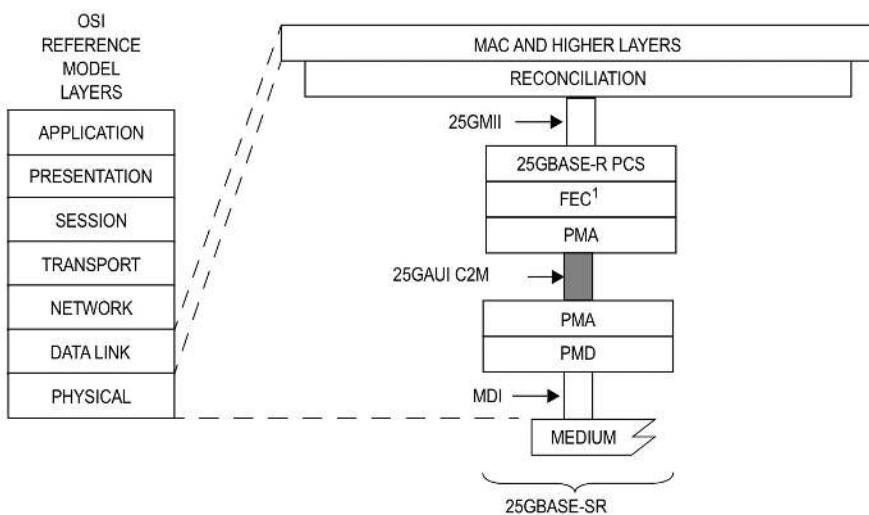


Figure 115-3—1000BASE-RHx functional block diagram

chmp  $\rightarrow$  chmp -般不具 pmp 层



25GAUI = 25 GIGABIT ATTACHMENT UNIT INTERFACE

25GMII = 25 GIGABIT MEDIA INDEPENDENT INTERFACE

FEC = FORWARD ERROR CORRECTION

MAC = MEDIA ACCESS CONTROL

MDI = MEDIUM DEPENDENT INTERFACE

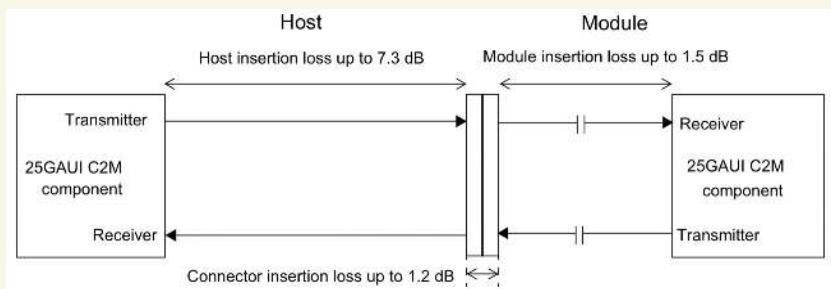
PCS = PHYSICAL CODING SUBLAYER

PMA = PHYSICAL MEDIUM ATTACHMENT

PMD = PHYSICAL MEDIUM DEPENDENT

NOTE 1—CONDITIONAL BASED ON PHY TYPE

**Figure 109B–1—Example 25GAUI C2M relationship to the ISO/IEC Open System Interconnection reference model and the IEEE 802.3 Ethernet model**



**Figure 109B–2—25GAUI C2M insertion loss budget at 12.89 GHz**

**Table 110C-1—Host and cable assembly combinations**

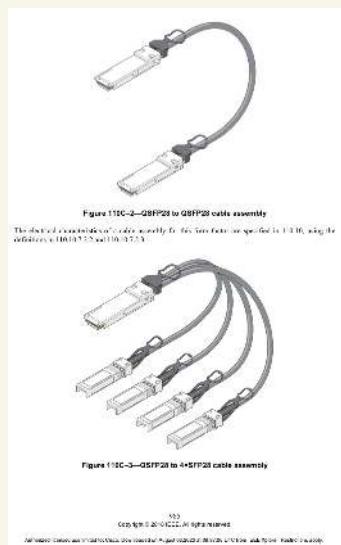
Cable assembly form factor	Cable assembly type	Host, first end	Hosts, second end	Length <sup>a</sup>	FEC modes supported <sup>b</sup>
SFP28 to SFP28 (see 110C.3.1)	CA-25G-L	One, SFP28 form factor (see 110C.2.1)	One, SFP28 form factor (see 110C.2.1)	5 m	RS-FEC
	CA-25G-S			3 m	RS-FEC BASE-R FEC
	CA-25G-N			3 m	RS-FEC BASE-R FEC no FEC
QSFP28 to QSFP28 (see 110C.3.2)	CA-25G-L	One, QSFP28 form factor (see 110C.2.2)	One, QSFP28 form factor (see 110C.2.2)	5 m	RS-FEC
	CA-25G-S			3 m	RS-FEC BASE-R FEC
	CA-25G-N			3 m	RS-FEC BASE-R FEC no FEC
QSFP28 to 4×SFP28 (see 110C.3.3)	CA-25G-L	One, QSFP28 form factor (see 110C.2.2)	Four, SFP28 form factor (see 110C.2.1)	5 m	RS-FEC
	CA-25G-S			3 m	RS-FEC BASE-R FEC
	CA-25G-N			3 m	RS-FEC BASE-R FEC no FEC

<sup>a</sup>Indicates the achievable length of compliant cable assemblies. It may be possible to construct compliant cable assemblies longer than indicated. Length of the cable assembly does not imply compliance to specifications.

<sup>b</sup>FEC mode is selected through Auto-Negotiation (Clause 73). See 110.6.



**Figure 110C-1—SFP28 to SFP28 cable assembly**



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Authorized licensed use limited to: University of Texas at Austin. Downloaded on: 10/20/2016 10:22:45 AM.

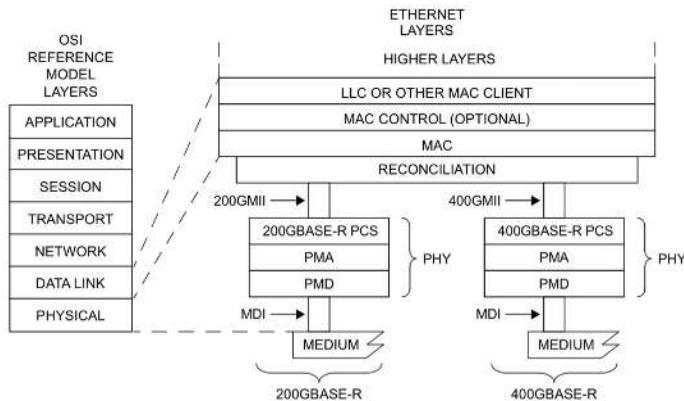


Figure 116-1—Architectural positioning of 200 Gigabit and 400 Gigabit Ethernet

Table 116-1—200 Gb/s PHYs

Name	Description
200GBASE-DR4	200 Gb/s PHY using 200GBASE-R encoding over four lanes of single-mode fiber, with reach up to at least 500 m (see Clause 121)
200GBASE-FR4	200 Gb/s PHY using 200GBASE-R encoding over four WDM lanes on single-mode fiber, with reach up to at least 2 km (see Clause 122)
200GBASE-LR4	200 Gb/s PHY using 200GBASE-R encoding over four WDM lanes on single-mode fiber, with reach up to at least 10 km (see Clause 122)

Table 116-3—PHY type and clause correlation (200GBASE optical)

PHY type	Clause <sup>a</sup>												
	78	117		118	119	120	120B	120C	120D	120E	121	122	122
	EEE	RS	200GMII	200GMII Extender	200GBASE-R PCS	200GBASE-R PMA	200GAUI-8 C2C	200GAUI-8 C2M	200GAUI-4 C2C	200GAUI-4 C2M	200GBASE-DR4 PMD	200GBASE-FR4 PMD	200GBASE-LR4 PMD
200GBASE-DR4	O	M	O	O	M	M	O	O	O	O	M		
200GBASE-FR4	O	M	O	O	M	M	O	O	O	O		M	
200GBASE-LR4	O	M	O	O	M	M	O	O	O	O			M

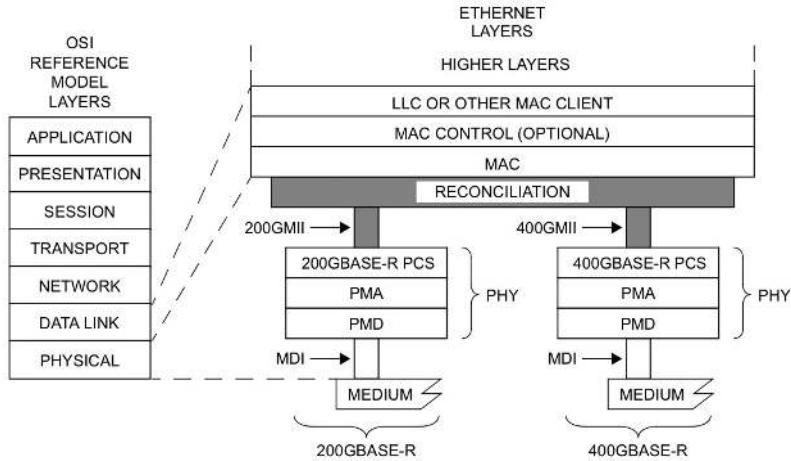
<sup>a</sup> O = Optional, M = Mandatory.

Table 116-4—PHY type and clause correlation (400GBASE optical)

PHY type	Clause <sup>a</sup>													
	78	117	118	119	120	120B	120C	120D	120E	123	124	122	122	
	EFE	RS	400GMII	400GMII Extender	400GBASE-R PCS	400GBASE-R PMA	400GAUI-16 C2C	400GAUI-16 C2M	400GAUI-8 C2C	400GAUI-8 C2M	400GBASE-SR16 PMID	400GBASE-DR4 PMID	400GBASE-FR8 PMID	400GBASE-LR8 PMID
400GBASE-SR16	O	M	O	O	M	M	O	O	O	O	M			
400GBASE-DR4	O	M	O	O	M	M	O	O	O	O		M		
400GBASE-FR8	O	M	O	O	M	M	O	O	O	O			M	
400GBASE-LR8	O	M	O	O	M	M	O	O	O	O				M

<sup>a</sup> O = Optional, M = Mandatory.

FEC degrade. — 超过一定量的 FEC corrected  
 计数从被通知到 MAC



200GMII = 200 Gb/s MEDIA INDEPENDENT INTERFACE

400GMII = 400 Gb/s MEDIA INDEPENDENT INTERFACE

LLC = LOGICAL LINK CONTROL

MAC = MEDIA ACCESS CONTROL

MDI = MEDIUM DEPENDENT INTERFACE

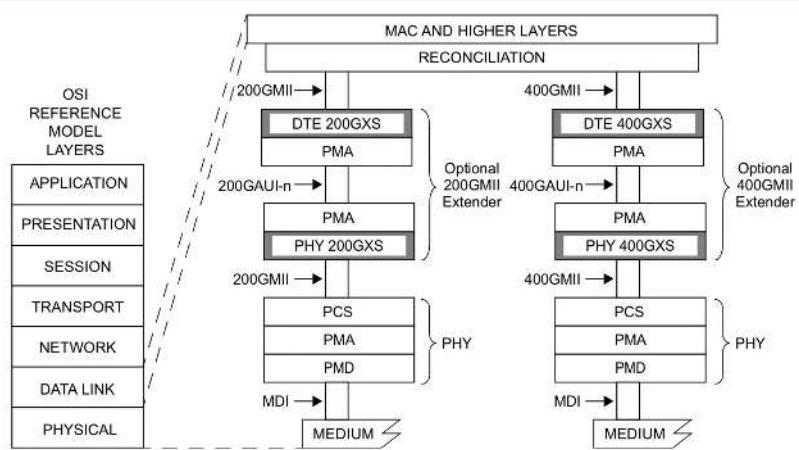
PCS = PHYSICAL CODING SUBLAYER

PHY = PHYSICAL LAYER DEVICE

PMA = PHYSICAL MEDIUM ATTACHMENT

PMD = PHYSICAL MEDIUM DEPENDENT

**Figure 117–1—RS and MII relationship to the ISO/IEC Open Systems Interconnection (OSI) reference model and IEEE 802.3 Ethernet model**



200GAUI-n = 200 Gb/s n-LANE ATTACHMENT UNIT  
INTERFACE

400GXS = 400GMII EXTENDER SUBLAYER  
DTE = DATA TERMINAL EQUIPMENT

200GMII = 200 Gb/s MEDIA INDEPENDENT INTERFACE

MAC = MEDIA ACCESS CONTROL

200GXS = 200GMII EXTENDER SUBLAYER

MDI = MEDIUM DEPENDENT INTERFACE

400GAUI-n = 400 Gb/s n-LANE ATTACHMENT UNIT

PCS = PHYSICAL CODING SUBLAYER

INTERFACE

PHY = PHYSICAL LAYER DEVICE

400GMII = 400 Gb/s MEDIA INDEPENDENT INTERFACE

PMA = PHYSICAL MEDIUM ATTACHMENT

400GXS = 400GMII EXTENDER SUBLAYER

PMD = PHYSICAL MEDIUM DEPENDENT

Figure 118–1—200GXS and 400GXS relationship to the ISO/IEC Open System Interconnection (OSI) reference model and the IEEE 802.3 Ethernet model

X3 200GXS 和 400GXS 的 MDI, AUI 一般指的是一段线

200 G:  $8 \times 26.5625$

400 G:  $16 \times 26.5625$

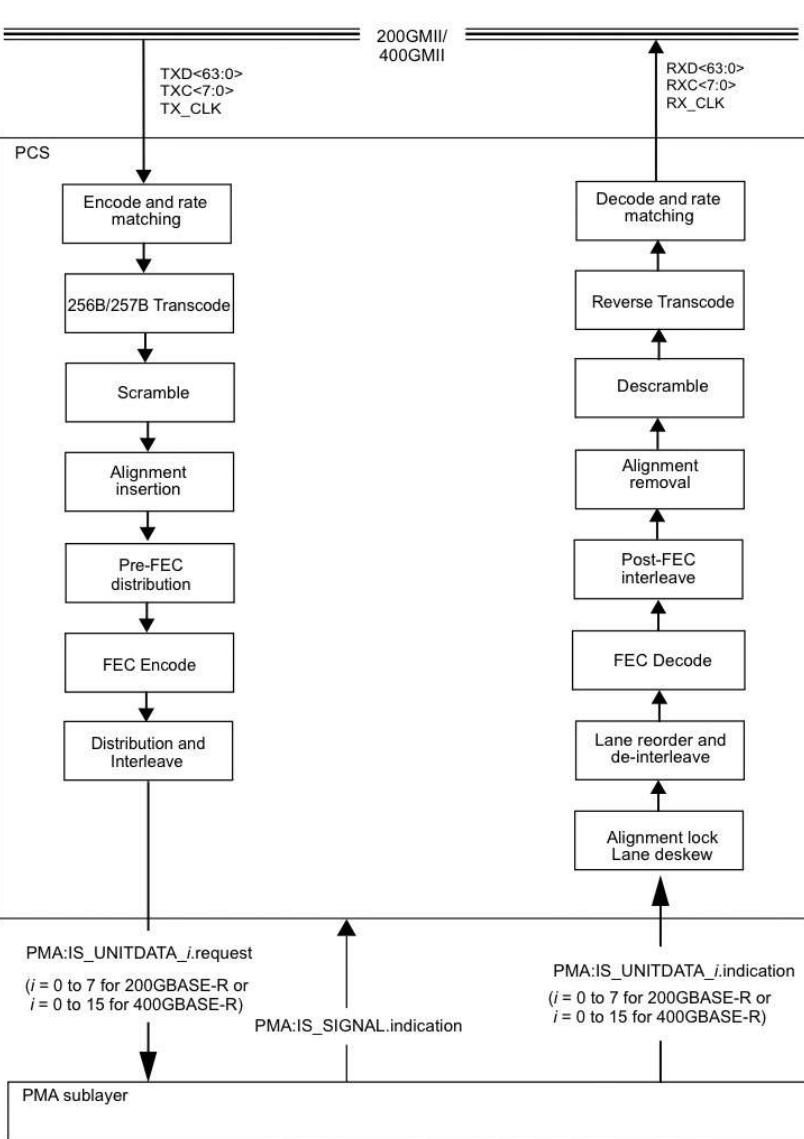


Figure 119–2—Functional block diagram

Bit Position:0	23:24	31:32	55:56	63:64	87:88	95:96	119
{CM <sub>0</sub> , CM <sub>1</sub> , CM <sub>2</sub> }	UP <sub>0</sub>	{CM <sub>3</sub> , CM <sub>4</sub> , CM <sub>5</sub> }	UP <sub>1</sub>	{UM <sub>0</sub> , UM <sub>1</sub> , UM <sub>2</sub> }	UP <sub>2</sub>	{UM <sub>3</sub> , UM <sub>4</sub> , UM <sub>5</sub> }	

Figure 119–4—Alignment marker format

Table 119–1—200GBASE-R alignment marker encodings

PCS lane number	Encoding <sup>a</sup>
0	0x9A,0x4A,0x26,0x05,0x65,0xB5,0xD9,0xD6,0xB3,0xC0,0x8C,0x29,0x4C,0x3F,0x73
1	0x9A,0x4A,0x26,0x04,0x65,0xB5,0xD9,0x67,0x5A,0xDE,0x7E,0x98,0xA5,0x21,0x81
2	0x9A,0x4A,0x26,0x46,0x65,0xB5,0xD9,0xFE,0x3E,0xF3,0x56,0x01,0xC1,0x0C,0xA9
3	0x9A,0x4A,0x26,0x5A,0x65,0xB5,0xD9,0x84,0x86,0x80,0xD0,0x7B,0x79,0x7F,0x2F
4	0x9A,0x4A,0x26,0xE1,0x65,0xB5,0xD9,0x19,0x2A,0x51,0xF2,0xE6,0xD5,0xAE,0x0D
5	0x9A,0x4A,0x26,0x29,0x2F,0x65,0xB5,0xD9,0x4E,0x12,0x4F,0xD1,0xB1,0xE1,0xB0,0x2F
6	0x9A,0x4A,0x26,0x3D,0x65,0xB5,0xD9,0xE1,0x42,0x9C,0xA1,0x11,0xBD,0x63,0x5E
7	0x9A,0x4A,0x26,0x22,0x65,0xB5,0xD9,0x32,0xD6,0x76,0x5B,0xCD,0x29,0x89,0xA4

<sup>a</sup> Each octet is transmitted LSB to MSB.

CM – common align marker

UM – unique portion

UP – unique pad

PCS lane, i	am_mapped 10-bit symbol index, k											
	0	1	2	3	4	5	6	7	8	9	10	11
0	A	B	A	B	A	R	A	R	A	R	A	R
	0	am_0										119
1	B	A	B	A	B	A	B	A	B	A	B	A
		am_1										
2	A	B	A	B	A	R	A	B	A	B	A	B
		am_2										
3	B	A	B	A	B	A	B	A	B	A	B	A
		am_3										
4	A	B	A	B	A	R	A	B	A	B	A	B
		am_4										
5	B	A	B	A	B	A	B	A	B	A	B	A
		am_5										
6	A	B	A	B	A	R	A	B	A	B	A	B
		am_6										
7	B	A	B	A	B	A	R	A	B	A	B	A
		am_7										

= 65-bit pad      = 3-bit status field      = Resumption of 257-bit blocks

A = from FEC codeword A

B = from FEC codeword B

Figure 119–5—200GBASE-R alignment marker mapping to PCS lanes

The PCS shall implement an RS(544,514) based FEC encoder. The PCS distributes a group of  $40 \times 257$ -bit blocks from tx\_scrambled\_am on a 10-bit round robin basis into two 5140-bit message blocks,  $m_A$  and  $m_B$ , as described in 119.2.4.5. These are then encoded using RS(544,514) encoder into codeword A and codeword B, respectively. The RS(544,514) code is based on the generating polynomial given by Equation (119–1).

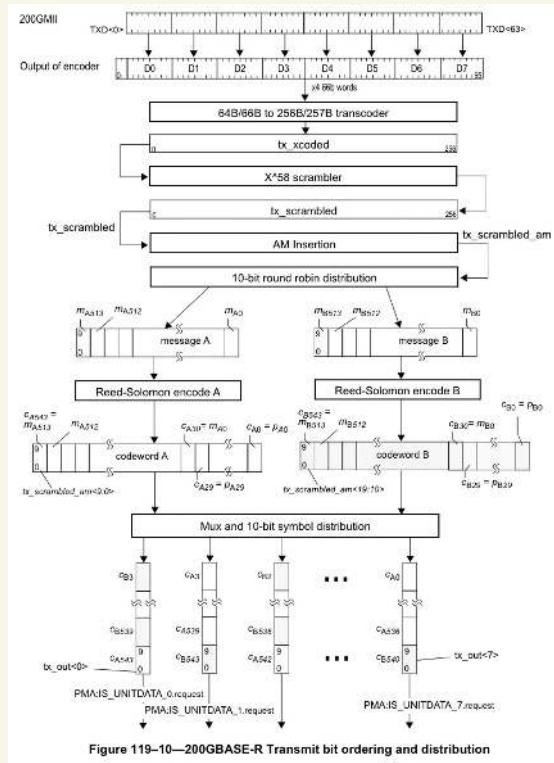


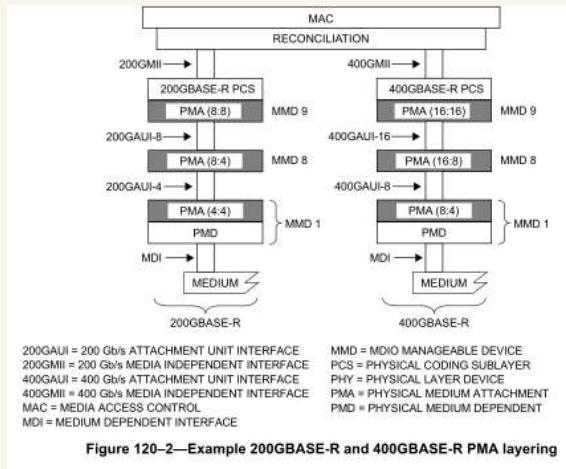
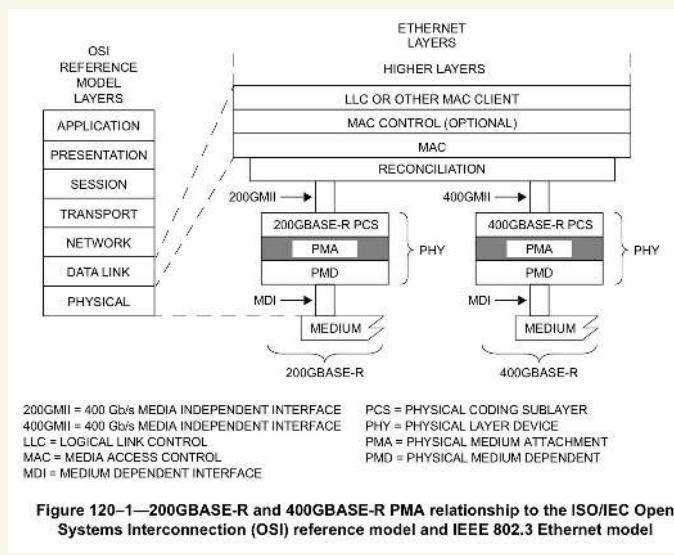
Figure 119-10—200GBASE-R Transmit bit ordering and distribution

### 120.1.3 Summary of functions

The following is a summary of the principal functions implemented (when required) by the PMA in both the transmit and receive directions:

- Adapt the PCSL formatted signal to the appropriate number of abstract or physical lanes.
- Provide per input-lane clock and data recovery.
- Provide bit-level multiplexing.
- Provide clock generation.
- Provide signal drivers.
- Optionally provide local loopback to/from the PMA service interface.
- Optionally provide remote loopback to/from the PMD service interface.
- Optionally provide test-pattern generation and detection.
- Tolerate Skew Variation.
- Perform PAM4 encoding and decoding for 200GBASE-R PMAs where the number of physical lanes is 4, and for 400GBASE-R PMAs where the number of physical lanes is 4 or 8.

In addition, the PMA provides receive link status information in the receive direction.



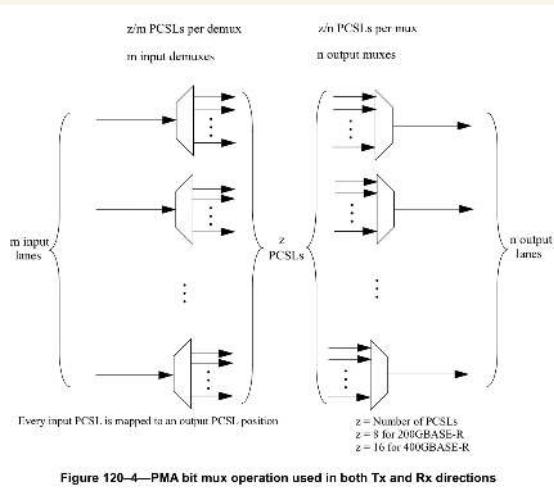
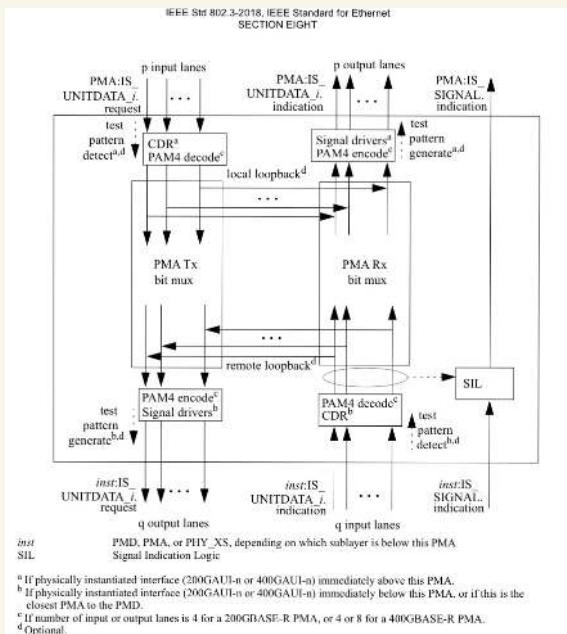


Figure 120-4—PMA bit mux operation used in both Tx and Rx directions



{0, 0} maps to 0,  
 {0, 1} maps to 1,  
 {1, 1} maps to 2, and  
 {1, 0} maps to 3.

gray map

PAM4 同后 PRBS13Q

PRBS13 又是重复<sup>~~~</sup>的 8191 symbol, 所以大.  
⇒ 两个 PRBS13 并入 PAM4 通过 gray map.

The PRBS13Q test pattern is a repeating 8191-symbol sequence formed by Gray coding pairs of bits from two repetitions of the PRBS13 pattern into PAM4 symbols as described in 120.5.7. The PRBS pattern generator produces the same result as the implementation shown in Figure 94-6, which implements the

Table 121–1—Physical Layer clauses associated with the 200GBASE-DR4 PMD

Associated clause	200GBASE-DR4
117—RS	Required
117—200GMII <sup>a</sup>	Optional
118—200GMII Extender	Optional
119—PCS	Required
120—PMA	Required
120B—Chip-to-chip 200GAUI-8	Optional
120C—Chip-to-module 200GAUI-8	Optional
120D—Chip-to-chip 200GAUI-4	Optional
120E—Chip-to-module 200GAUI-4	Optional
78—Energy Efficient Ethernet	Optional

<sup>a</sup> The 200GMII is an optional interface. However, if the 200GMII is not implemented, a conforming implementation must behave functionally as though the RS and 200GMII were present.

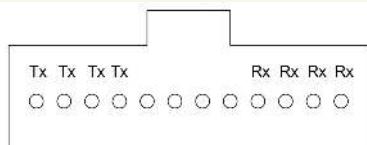
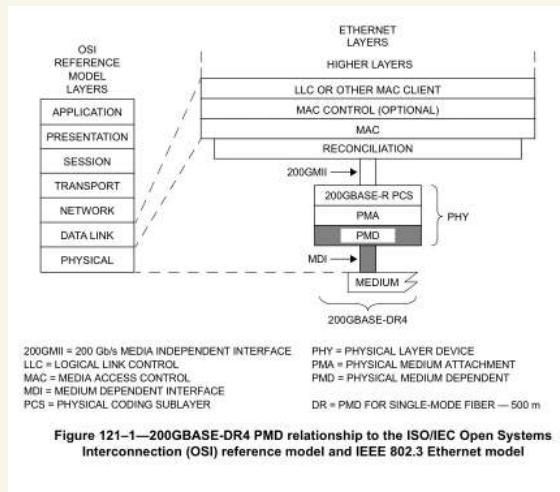


Figure 121–11—200GBASE-DR4 optical lane assignments

**Table 122–1—Physical Layer clauses associated with the 200GBASE-FR4, 200GBASE-LR4, 400GBASE-FR8, and 400GBASE-LR8 PMDs**

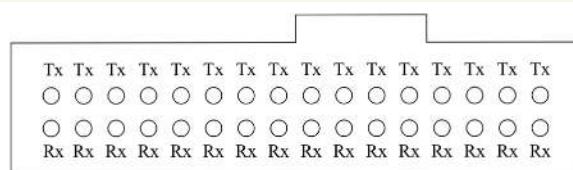
Associated clause	200GBASE-FR4, 200GBASE-LR4	400GBASE-FR8, 400GBASE-LR8
117—RS	Required	Required
117—200GMII <sup>a</sup>	Optional	Not applicable
117—400GMII <sup>a</sup>	Not applicable	Optional
118—200GMII Extender	Optional	Not applicable
118—400GMII Extender	Not applicable	Optional
119—PCS for 200GBASE-R	Required	Not applicable
119—PCS for 400GBASE-R	Not applicable	Required
120—PMA for 200GBASE-R	Required	Not applicable
120—PMA for 400GBASE-R	Not applicable	Required
120B—Chip-to-chip 200GAUI-8	Optional	Not applicable
120B—Chip-to-chip 400GAUI-16	Not applicable	Optional
120C—Chip-to-module 200GAUI-8	Optional	Not applicable
120C—Chip-to-module 400GAUI-16	Not applicable	Optional
120D—Chip-to-chip 200GAUI-4	Optional	Not applicable
120D—Chip-to-chip 400GAUI-8	Not applicable	Optional
120E—Chip-to-module 200GAUI-4	Optional	Not applicable
120E—Chip-to-module 400GAUI-8	Not applicable	Optional
78—Energy Efficient Ethernet	Optional	Optional

<sup>a</sup> 200GMII and 400GMII are optional interfaces. However, if the appropriate interface is not implemented, a conforming implementation must behave functionally as though the RS and 200GMII or 400GMII were present.

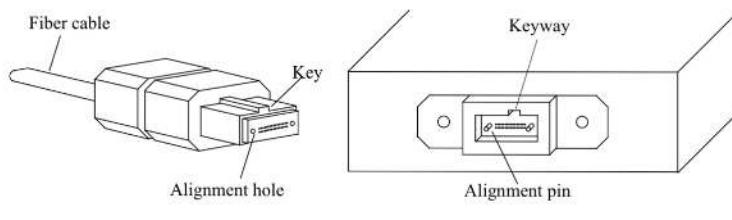
**Table 123–1—Physical Layer clauses associated with the 400GBASE-SR16 PMD**

Associated clause	400GBASE-SR16
117—RS	Required
117—400GMII <sup>a</sup>	Optional
118—400GMII Extender	Optional
119—PCS	Required
120—PMA	Required
120B—Chip-to-chip 400GAUI-16	Optional
120C—Chip-to-module 400GAUI-16	Optional
120D—Chip-to-chip 400GAUI-8	Optional
120E—Chip-to-module 400GAUI-8	Optional
78—Energy Efficient Ethernet	Optional

<sup>a</sup> The 400GMII is an optional interface. However, if the 400GMII is not implemented, a conforming implementation must behave functionally as though the RS and 400GMII were present.



**Figure 123–4—400GBASE-SR16 optical lane assignments**



MPO-16 female two-row plug with flat interface

MDI

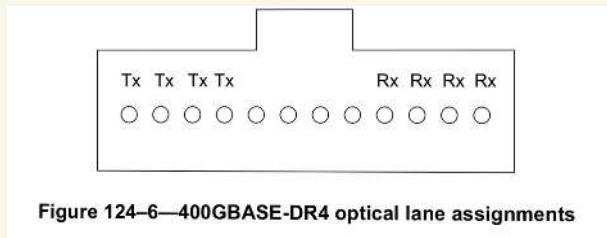
**Figure 123–5—MPO-16 female two-row plug with flat interface, and an MDI**

**Table 124–1—Physical Layer clauses associated with the 400GBASE-DR4 PMD**

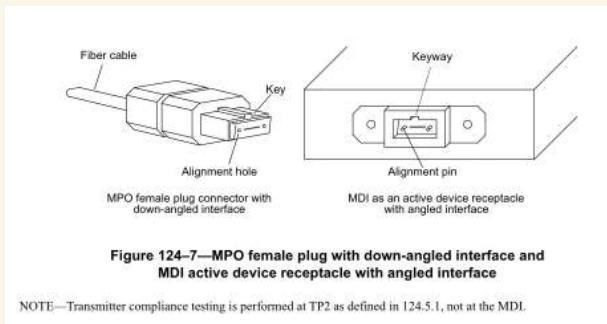
Associated clause	400GBASE-DR4
117—RS	Required
117—400GMII <sup>a</sup>	Optional
118—400GMII Extender	Optional
119—PCS	Required
120—PMA	Required
120B—Chip-to-chip 400GAUI-16	Optional
120C—Chip-to-module 400GAUI-16	Optional
120D—Chip-to-chip 400GAUI-8	Optional
120E—Chip-to-module 400GAUI-8	Optional
78—Energy Efficient Ethernet	Optional

<sup>a</sup> The 400GMII is an optional interface. However, if the 400GMII is not implemented, a conforming implementation must behave functionally as though the RS and 400GMII were present.

信号速率 per Lane: 53.125 G bps × 4  
 = 106.250 G bps per Lane



**Figure 124–6—400GBASE-DR4 optical lane assignments**



NOTE—Transmitter compliance testing is performed at TP2 as defined in 124.5.1, not at the MDI.

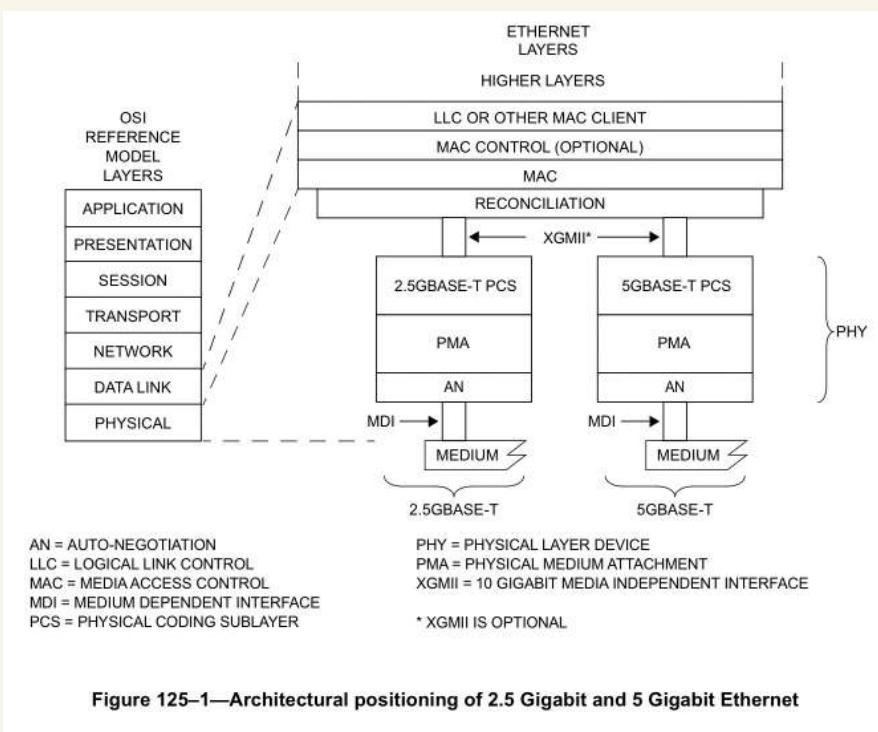


Figure 125–1—Architectural positioning of 2.5 Gigabit and 5 Gigabit Ethernet

手繪還是 2.5GBASE-T 和 5GBASE-T

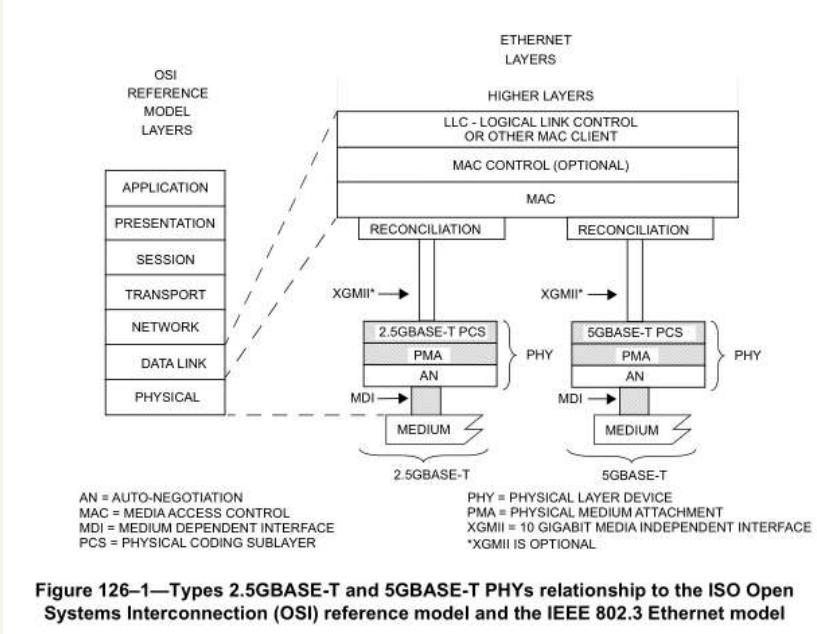
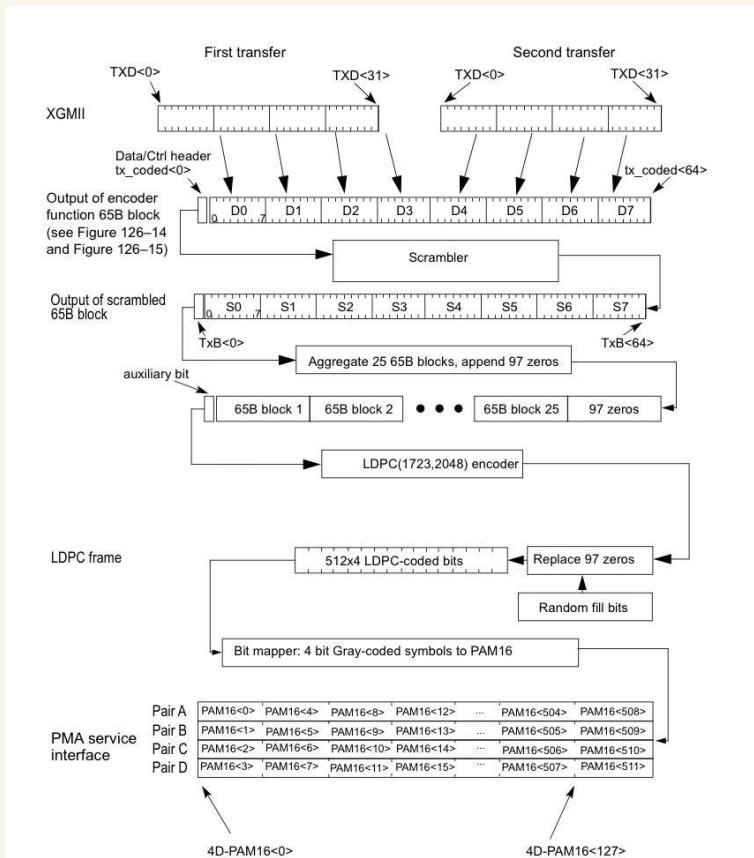


Figure 126-1—Types 2.5GBASE-T and 5GBASE-T PHYs relationship to the ISO Open Systems Interconnection (OSI) reference model and the IEEE 802.3 Ethernet model

BASE-T 這種模型有 MASTER-SLAVE 之分。  
 master: Local clock  
 slave: receive clock from RCU and  
 used for TX

- a) Forward error correction (FEC) coded symbol mapping for data.
- b) Algorithmic mapping from TXD<31:0> and TXC<3:0> to 4D symbols in the transmit path.
- c) Algorithmic mapping from the received 4D signals on the MDI port to RXD<31:0> and RXC<3:0> on the XGMII interface.
- d) Uncorrelated symbols in the transmitted symbol stream.
- e) No correlation between symbol streams traveling both directions on any pair combination.
- f) No correlation between symbol streams on pairs BI\_DA, BI\_DB, BI\_DC, and BI\_DD.
- g) Block framing and other control signals.
- h) Ability to signal the status of the local receiver to the remote PHY to indicate that the local receiver is not operating reliably and requires retraining.
- i) Ability to automatically detect and correct for pair swapping and crossover connections.
- j) Ability to automatically detect and correct for incorrect polarity in the connections.
- k) Ability to automatically correct for differential delay variations across the wire-pairs.
- l) Ability to support refresh, quiet and alert signaling during LPI operation.



NOTE—This figure shows the mapping from the XGMII to a 64B/65B block for a block containing eight data characters.

Figure 126–6—PCS Transmit bit ordering

一般來說，MAC-PLS-PMA 以太網傳輸  
PMD 以太網傳輸

Table 126-24—Assignment of PMA signal to MDI and MDI-X pin-outs

Contact	MDI	MDI-X
1	BI_DA+	BI_DB+
2	BI_DA-	BI_DB-
3	BI_DB+	BI_DA+
4	BI_DC+	BI_DD+
5	BI_DC-	BI_DD-
6	BI_DB-	BI_DA-
7	BI_DD+	BI_DC+
8	BI_DD-	BI_DC-