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IEEE Standard for Ethernet

Amendment 9: Media Access Control Parameters for 800 Gb/s and Physical Layers and Management Parameters for 400 Gb/s and 800 Gb/s Operation

IEEE Computer Society

Developed by the
LAN/MAN Standards Committee

IEEE Std 802.3df™-2024
(Amendment to IEEE Std 802.3™-2022
as amended by IEEE Std 802.3dd™-2022,
IEEE Std 802.3cs™-2022, IEEE Std 802.3db™-2022,
IEEE Std 802.3ck™-2022, IEEE Std 802.3de™-2022,
IEEE Std 802.3cx™-2023, IEEE Std 802.3cz™-2023,
and IEEE Std 802.3cy™-2023)

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IEEE Std 802.3df™-2024
(Amendment to IEEE Std 802.3™-2022
as amended by IEEE Std 802.3dd™-2022,
IEEE Std 802.3cs™-2022,
IEEE Std 802.3db™-2022,
IEEE Std 802.3ck™-2022,
IEEE Std 802.3de™-2022,
IEEE Std 802.3cx™-2023,
IEEE Std 802.3cz™-2023,
and IEEE Std 802.3cy™-2023)

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Approved 15 February 2024

IEEE SA Standards Board

Abstract: This amendment includes changes to IEEE Std 802.3-2022 and adds Clause 169 through Clause 173, Annex 172A, and Annex 173A. This amendment adds MAC parameters, Physical Layers, and management parameters for the transfer of IEEE 802.3 format frames at 400 Gb/s and 800 Gb/s.

Keywords: 800GAUI-8, 800GBASE-CR8, 400GBASE-DR4-2, 800GBASE-DR8, 800GBASE-DR8-2, 800GBASE-KR8, 800GBASE-R, 800GBASE-SR8, 800GBASE-VR8, 800 Gigabit Ethernet, 800GMII, 800GXS, amendment, FEC, IEEE 802.3™, IEEE 802.3df™, PCS, Physical Coding Sublayer, PMD, Physical Medium Attachment

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Introduction

This introduction is not part of IEEE Std 802.3df-2024, IEEE Standard for Ethernet—Amendment 9: Media Access Control Parameters for 800 Gb/s and Physical Layers and Management Parameters for 400 Gb/s and 800 Gb/s Operation.

IEEE Std 802.3™ was first published in 1985. Since the initial publication, many projects have added functionality or provided maintenance updates to the specifications and text included in the standard. Each IEEE 802.3 project/amendment is identified with a suffix (e.g., IEEE Std 802.3ba™-2010).

The half duplex Media Access Control (MAC) protocol specified in IEEE Std 802.3-1985 is Carrier Sense Multiple Access with Collision Detection (CSMA/CD). This MAC protocol was key to the experimental Ethernet developed at Xerox Palo Alto Research Center, which had a 2.94 Mb/s data rate. Ethernet at 10 Mb/s was jointly released as a public specification by Digital Equipment Corporation (DEC), Intel and Xerox in 1980. “Local Area Networks: Carrier sense multiple access with collision detection (CSMA/CD) access method and physical layer specifications” was approved as an IEEE standard by the IEEE Standards Board in 1983 and subsequently published in 1985 as IEEE Std 802.3-1985. Since 1985, new media options, new speeds of operation, and new capabilities have been added to IEEE Std 802.3. A full duplex MAC protocol and the ability to use an EtherType to specify the MAC client protocol were added in 1997. The title was changed to Standard for Ethernet with the 2012 Revision.

Some of the major additions to IEEE Std 802.3 are identified in the marketplace with their project number. This is most common for projects adding higher speeds of operation or new protocols. For example, IEEE Std 802.3u™ added 100 Mb/s operation (also called Fast Ethernet), IEEE Std 802.3z™ added 1000 Mb/s operation (also called Gigabit Ethernet), IEEE Std 802.3ae™ added 10 Gb/s operation (also called 10 Gigabit Ethernet), IEEE Std 802.3ah™ specified access network Ethernet (also called Ethernet in the First Mile) and IEEE Std 802.3ba added 40 Gb/s operation (also called 40 Gigabit Ethernet) and 100 Gb/s operation (also called 100 Gigabit Ethernet). These major additions are all now included in and are superseded by IEEE Std 802.3-2022 and are not maintained as separate documents.

At the date of IEEE Std 802.3df-2024 publication, IEEE Std 802.3 was composed of the following documents:

IEEE Std 802.3-2022

Section One—Includes Clause 1 through Clause 20 and Annex A through Annex K and Annex 4A. Section One includes the specifications for 10 Mb/s operation and the MAC, frame formats and service interfaces used for all speeds of operation.

Section Two—Includes Clause 21 through Clause 33 and Annex 22A through Annex 33A. Section Two includes management attributes for multiple protocols and speed of operation as well as specifications for providing power over twisted pair cabling for multiple operational speeds. It also includes general information on 100 Mb/s operation as well as most of the 100 Mb/s Physical Layer specifications.

Section Three—Includes Clause 34 through Clause 43 and Annex 36A through Annex 43C. Section Three includes general information on 1000 Mb/s operation as well as most of the 1000 Mb/s Physical Layer specifications.

Section Four—Includes Clause 44 through Clause 55 and Annex 44A through Annex 55B. Section Four includes general information on 10 Gb/s operation as well as most of the 10 Gb/s Physical Layer specifications.

Section Five—Includes Clause 56 through Clause 77 and Annex 57A through Annex 76A. Clause 56 through Clause 67 and Clause 75 through Clause 77, as well as associated annexes, specify subscriber access and other Physical Layers and sublayers for operation from 512 kb/s to 10 Gb/s, and defines services and protocol elements that enable the exchange of IEEE Std 802.3 format frames between stations in a subscriber access network. Clause 68 specifies a 10 Gb/s Physical Layer specification. Clause 69 through Clause 74 and associated annexes specify Ethernet operation over electrical backplanes at speeds of 1000 Mb/s and 10 Gb/s.

Section Six—Includes Clause 78 through Clause 95 and Annex 83A through Annex 93C. Clause 78 specifies Energy-Efficient Ethernet. Clause 79 specifies IEEE 802.3 Organizationally Specific Link Layer Discovery Protocol (LLDP) type, length, and value (TLV) information elements. Clause 80 through Clause 95 and associated annexes include general information on 40 Gb/s and 100 Gb/s operation as well as 40 Gb/s and 100 Gb/s Physical Layer specifications. Clause 90 specifies Ethernet support for time synchronization protocols.

Section Seven—Includes Clause 96 through Clause 115 and Annex 97A through Annex 115A. Clause 96 through Clause 98, Clause 104, and associated annexes, specify Physical Layers and optional features for 100 Mb/s and 1000 Mb/s operation over a single twisted pair. Clause 100 through Clause 103, as well as associated annexes, specify Physical Layers for the operation of the EPON protocol over coaxial distribution networks. Clause 105 through Clause 114 and associated annexes include general information on 25 Gb/s operation as well as 25 Gb/s Physical Layer specifications. Clause 99 specifies a MAC merge sublayer for the interspersing of express traffic. Clause 115 and its associated annex specify a Physical Layer for 1000 Mb/s operation over plastic optical fiber.

Section Eight—Includes Clause 116 through Clause 140 and Annex 119A through Annex 136D. Clause 116 through Clause 124 and associated annexes include general information on 200 Gb/s and 400 Gb/s operation as well as 200 Gb/s and 400 Gb/s Physical Layer specifications. Clause 125 includes general information on 2.5 Gb/s and 5 Gb/s operation. Clause 126 through Clause 130 and associated annexes include 2.5 Gb/s and 5 Gb/s Physical Layer specifications. Clause 131 provides general information on 50 Gb/s operation. Clause 132 through Clause 140 and associated annexes include 50 Gb/s Physical Layer specifications and additional 100 Gb/s, 200 Gb/s, and 400 Gb/s Physical Layer specifications.

Section Nine—Includes Clause 141 through Clause 160 and Annex 142A through Annex 154A. Clause 141 through Clause 144 and associated annexes specify symmetric and asymmetric operation of Ethernet passive optical networks over multiple 25 Gb/s channels. Clause 145 and associated annexes specify increased power delivery using all four pairs in the structured wiring plant. Clause 146 through Clause 149 and associated annexes specify Physical Layers for 10 Mb/s, 2.5 Gb/s, 5 Gb/s, and 10 Gb/s operation over a single balanced pair of conductors. Clause 150 and Clause 151 include additional 400 Gb/s Physical Layer specifications. Clause 153 and Clause 154 specify 100 Gb/s operation over DWDM channels. Clause 157 through Clause 160 include 10 Gb/s, 25 Gb/s, and 50 Gb/s bidirectional Physical Layer specifications.

IEEE Std 802.3dd™-2022

Amendment 1—This amendment includes editorial and technical corrections, refinements, and clarifications to Clause 104, Power over Data Lines of Single Pair Ethernet, and related portions of the standard.

IEEE Std 802.3cs™-2022

Amendment 2—This amendment to IEEE Std 802.3-2022 defines Super-PON optical subscriber access networks, in the family of Ethernet passive optical networks (EPONs). Super-PON has a reach of up to 50 km and up to 1024 ONUs over a point-to-multipoint passive optical distribution network (ODN)

through wavelength division multiplexing (WDM). A Super-PON ODN contains a passive wavelength router that determines the channels used by the ODN. This standard specifies the Super-PON Reconciliation Sublayer (RS), Physical Coding Sublayer (PCS), Physical Medium Attachment (PMA) sublayer, and Physical Medium Dependent (PMD) sublayer at a MAC data rate of 10 Gb/s in the downstream direction and of 10 Gb/s or 2.5 Gb/s in the upstream direction.

IEEE Std 802.3db™-2022

Amendment 3—This amendment includes changes to IEEE Std 802.3-2022 and adds Clause 167. This amendment adds Physical Layer specifications and management parameters for 100 Gb/s, 200 Gb/s, and 400 Gb/s over one, two, and four pairs of multimode fiber based on 100 Gb/s optical signaling.

IEEE Std 802.3ck™-2022

Amendment 4—This amendment includes changes to IEEE Std 802.3-2022 and adds Clause 161 through Clause 163, Annex 120F, Annex 120G, Annex 162A through Annex 162D, Annex 163A, and Annex 163B. This amendment includes Physical Layer specifications and management parameters for 100 Gb/s, 200 Gb/s, and 400 Gb/s electrical interfaces based on 100 Gb/s signaling.

IEEE Std 802.3de™-2022

Amendment 5—This amendment includes changes to IEEE Std 802.3-2022 to add 10 Mb/s Single-Pair Ethernet point-to-point PHYs to the PHYs supporting the MAC Merge function and the Time Synchronization Service Interface (TSSI).

IEEE Std 802.3cx™-2023

Amendment 6—This amendment to IEEE Std 802.3-2022 modifies Clause 30, Clause 45, and Clause 90, and adds Annex 90A to enhance support for time synchronization protocols by providing options for sub-nanosecond reporting of the transmit and receive path data delays, selection of the data delay measurement point, and dynamic reporting of path data delay variation.

IEEE Std 802.3cz™-2023

Amendment 7—This amendment includes changes to IEEE Std 802.3-2022 and adds Clause 166. This amendment adds 2.5 Gb/s, 5 Gb/s, 10 Gb/s, 25 Gb/s, and 50 Gb/s Physical Layer specifications and management parameters for optical automotive Ethernet using graded-index glass optical fiber.

IEEE Std 802.3cy™-2023

Amendment 8—This amendment includes changes to IEEE Std 802.3-2022 and adds Clause 165 and Annex 165A. This amendment adds Physical Layer specifications and management parameters for operation at 25 Gb/s over a single balanced pair of conductors.

IEEE Std 802.3df™-2024

Amendment 9—This amendment includes changes to IEEE Std 802.3-2022 and adds Clause 169 through Clause 173, Annex 172A, and Annex 173A. This amendment includes Physical Layer specifications and management parameters for 400 Gb/s and 800 Gb/s operation.

Two companion documents exist, IEEE Std 802.3.1 and IEEE Std 802.3.2. IEEE Std 802.3.1 describes Ethernet management information base (MIB) modules for use with the Simple Network Management Protocol (SNMP). IEEE Std 802.3.2 describes YANG data models for Ethernet. IEEE Std 802.3.1 and

IEEE Std 802.3.2 are updated to add management capability for enhancements to IEEE Std 802.3 after approval of those enhancements.

IEEE Std 802.3 will continue to evolve. New Ethernet capabilities are anticipated to be added within the next few years as amendments to this standard.

Contents

IEEE Standard for Ethernet

Amendment 9:
Media Access Control Parameters for 800 Gb/s and Physical Layers and Management Parameters for 400 Gb/s and 800 Gb/s Operation

(This amendment is based on IEEE Std 802.3™-2022 as amended by IEEE Std 802.3dd™-2022, IEEE Std 802.3cs™-2022, IEEE Std 802.3db™-2022, IEEE Std 802.3ck™-2022, IEEE Std 802.3de™-2022, IEEE Std 802.3cx™-2023, IEEE Std 802.3cz™-2023, and IEEE Std 802.3cy™-2023.)

NOTE—The editing instructions contained in this amendment define how to merge the material contained therein into the existing base standard and its amendments to form the comprehensive standard.

The editing instructions are shown in ***bold italic***. Four editing instructions are used: change, delete, insert, and replace. ***Change*** is used to make corrections in existing text or tables. The editing instruction specifies the location of the change and describes what is being changed by using ~~strikethrough~~ (to remove old material) and underscore (to add new material). ***Delete*** removes existing material. ***Insert*** adds new material without disturbing the existing material. Deletions and insertions may require renumbering. If so, renumbering instructions are given in the editing instruction. ***Replace*** is used to make changes in figures or equations by removing the existing figure or equation and replacing it with a new one. Editing instructions, change markings, and this NOTE will not be carried over into future editions because the changes will be incorporated into the base standard.

Cross references that refer to clauses, tables, equations, or figures not covered by this amendment are highlighted in green.[6]

[6] Notes in text, tables, and figures are given for information only and do not contain requirements needed to implement the standard.

1. Introduction

1.1 Overview

1.1.3 Architectural perspectives

1.1.3.2 Compatibility interfaces

Insert two new list items at the end of the lettered list in 1.1.3.2 as follows:

w) *800 Gb/s Media Independent Interface (800GMII).* The 800GMII is designed to connect an 800 Gb/s capable MAC to an 800 Gb/s PHY. The 800GMII is a logical interconnection intended for use as an intra-chip interface. No mechanical connector is specified for use with the 800GMII. The 800GMII is optional.

x) *800 Gb/s Attachment Unit Interface (800GAUI-n).* An 800GAUI-n is an optional physical instantiation of the PMA service interface to extend the connection between 800 Gb/s capable PMAs. 800GAUI-n C2C is intended for use as a chip-to-chip interface and 800GAUI-n C2M as a chip-to-module interface. One width of 800GAUI-n is defined: eight-lane 800GAUI-8 C2C in Annex 120F and 800GAUI-8 C2M in Annex 120G. No mechanical connector is specified for use with an 800GAUI-n.

1.4 Definitions

Change 1.4.103 as follows:

1.4.103 200GBASE-DR4: IEEE 802.3 Physical Layer specification for 200 Gb/s using 200GBASE-R encoding and 4-level pulse amplitude modulation over four ~~lanes of~~ single-mode fibers in each direction, with reach up to at least 500 m. (See IEEE Std 802.3, Clause 121.)

Change 1.4.108a (as inserted by IEEE Std 802.3db-2022) as follows:

1.4.108a 200GBASE-SR2: IEEE 802.3 Physical Layer specification for 200 Gb/s using 200GBASE-R encoding and 4-level pulse amplitude modulation over two ~~lanes of~~ multimode fibers in each direction, with reach up to at least 100 m. (See IEEE Std 802.3, Clause 167.)

Change 1.4.109 as follows:

1.4.109 200GBASE-SR4: IEEE 802.3 Physical Layer specification for 200 Gb/s using 200GBASE-R encoding over four ~~lanes of~~ multimode fibers in each direction, with reach up to at least 100 m. (See IEEE Std 802.3, Clause 138.)

Change 1.4.109a (as inserted by IEEE Std 802.3db-2022) as follows:

1.4.109a 200GBASE-VR2: IEEE 802.3 Physical Layer specification for 200 Gb/s using 200GBASE-R encoding and 4-level pulse amplitude modulation over two ~~lanes of~~ multimode fibers in each direction, with reach up to at least 50 m. (See IEEE Std 802.3, Clause 167.)

Change 1.4.135 as follows:

1.4.135 400GBASE-DR4: IEEE 802.3 Physical Layer specification for 400 Gb/s using 400GBASE-R encoding and 4-level pulse amplitude modulation over four ~~lanes of~~ single-mode fibers in each direction, with reach up to at least 500 m. (See IEEE Std 802.3, Clause 124.)

Insert the following new definition after 1.4.135 "400GBASE-DR4":

1.4.135a 400GBASE-DR4-2: IEEE 802.3 Physical Layer specification for 400 Gb/s using 400GBASE-R encoding and 4-level pulse amplitude modulation over four single-mode fibers in each direction, with reach up to at least 2 km. (See IEEE Std 802.3, Clause 124.)

Change 1.4.142 as follows:

1.4.142 400GBASE-SR16: IEEE 802.3 Physical Layer specification for 400 Gb/s using 400GBASE-R encoding over ~~sixteen~~16 ~~lanes of~~ multimode fibers in each direction, with reach up to at least 100 m. (See IEEE Std 802.3, Clause 123.)

Change 1.4.142a (as inserted by IEEE Std 802.3db-2022) as follows:

1.4.142a 400GBASE-SR4: IEEE 802.3 Physical Layer specification for 400 Gb/s using 400GBASE-R encoding and 4-level pulse amplitude modulation over four ~~lanes of~~ multimode fibers in each direction, with reach up to at least 100 m. (See IEEE Std 802.3, ~~Clause 1~~ Clause 167.)

Change 1.4.143 and 1.4.144 as follows:

1.4.143 400GBASE-SR4.2: IEEE 802.3 Physical Layer specification for 400 Gb/s using 400GBASE-R encoding over eight ~~lanes on~~ multimode ~~fiber~~ fibers in a bidirectional WDM format, with reach up to at least 150 m. (See IEEE Std 802.3, Clause 150.)

1.4.144 400GBASE-SR8: IEEE 802.3 Physical Layer specification for 400 Gb/s using 400GBASE-R encoding over eight ~~lanes of~~ multimode fibers in each direction, with reach up to at least 100 m. (See IEEE Std 802.3, Clause 138.)

Change 1.4.144a (as inserted by IEEE Std 802.3db-2022) as follows:

1.4.144a 400GBASE-VR4: IEEE 802.3 Physical Layer specification for 400 Gb/s using 400GBASE-R encoding and 4-level pulse amplitude modulation over four ~~lanes of~~ multimode fibers in each direction, with reach up to at least 50 m. (See IEEE Std 802.3, Clause 167.)

Insert the following 11 new definitions after 1.4.184 "64B/65B transmission code":

1.4.184a 800GBASE-CR8: IEEE 802.3 Physical Layer specification for 800 Gb/s using 800GBASE-R encoding over eight lanes of shielded balanced copper cabling. (See IEEE Std 802.3, Clause 162.)

1.4.184b 800GBASE-DR8: IEEE 802.3 Physical Layer specification for 800 Gb/s using 800GBASE-R encoding and 4-level pulse amplitude modulation over eight single-mode fibers in each direction, with reach up to at least 500 m. (See IEEE Std 802.3, Clause 124.)

1.4.184c 800GBASE-DR8-2: IEEE 802.3 Physical Layer specification for 800 Gb/s using 800GBASE-R encoding and 4-level pulse amplitude modulation over eight single-mode fibers in each direction, with reach up to at least 2 km. (See IEEE Std 802.3, Clause 124.)

1.4.184d 800GBASE-KR8: IEEE 802.3 Physical Layer specification for 800 Gb/s using 800GBASE-R encoding over eight lanes of an electrical backplane. (See IEEE Std 802.3, Clause 163.)

1.4.184e 800GBASE-R: An IEEE 802.3 family of Physical Layer devices using the physical coding sublayer defined in Clause 172 for 800 Gb/s operation. (See IEEE Std 802.3, Clause 172.)

1.4.184f 800GBASE-SR8: IEEE 802.3 Physical Layer specification for 800 Gb/s using 800GBASE-R encoding and 4-level pulse amplitude modulation over eight multimode fibers in each direction, with reach up to at least 100 m. (See IEEE Std 802.3, Clause 167.)

1.4.184g 800GBASE-VR8: IEEE 802.3 Physical Layer specification for 800 Gb/s using 800GBASE-R encoding and 4-level pulse amplitude modulation over eight multimode fibers in each direction, with reach up to at least 50 m. (See IEEE Std 802.3, Clause 167.)

1.4.184h 800 Gb/s Attachment Unit Interface (800GAUI-n): A physical instantiation of the PMA service interface to extend the connection between 800 Gb/s capable PMAs over n lanes, used for chip-to-chip or chip-to-module electrical interfaces. For chip-to-module interfaces and for chip-to-chip interfaces, one width of 800GAUI-n is defined: eight-lane 800GAUI-8 C2C and 800GAUI-8 C2M. (See IEEE Std 802.3, Annex 120F and Annex 120G.)

1.4.184i 800 Gb/s Media Independent Interface (800GMII): The interface between the Reconciliation Sublayer (RS) and the Physical Coding Sublayer (PCS) for 800 Gb/s operation. (See IEEE Std 802.3, Clause 170.)

1.4.184j 800GMII Extender: The 800 Gb/s Media Independent Interface Extender extends the reach of the 800GMII and consists of two 800GXS sublayers with one or two 800GAUI-n between them. (See IEEE Std 802.3, Clause 171.)

1.4.184k 800GXS: The 800GMII Extender Sublayer (800GXS) is part of the 800GMII Extender. In functionality, it is almost identical to the 800GBASE-R PCS defined in Clause 172. Two types of 800GXS are defined: the DTE 800GXS adjacent to the Reconciliation Sublayer (RS) and the PHY 800GXS adjacent to the PHY. (See IEEE Std 802.3, Clause 171.)

Change 1.4.205 as follows:

1.4.205 BASE-R: An IEEE 802.3 family of Physical Layer devices using the 64B/66B encoding defined in Clause 49, Clause 82, Clause 107, Clause 119, ~~or~~ Clause 129, or Clause 172 of IEEE Std 802.3.

Change 1.4.461 as follows:

1.4.461 PCS lane (PCSL): In 40GBASE-R, 50GBASE-R, 100GBASE-R, 200GBASE-R, ~~and~~ 400GBASE-R, and 800GBASE-R, the PCS distributes encoded data to multiple logical lanes~~, these logical lanes~~ that are called PCS lanes. One or more PCS lanes can be multiplexed and carried together on a physical lane~~ together~~ at the PMA service interface. (See IEEE Std 802.3, Clause 83, Clause 120, ~~and~~ Clause 135, and Clause 173.)

1.5 Abbreviations

Insert the following new abbreviations into the list in 1.5, in alphanumeric order:

800GAUI-n	800 Gb/s Attachment Unit Interface over n lanes
800GMII	800 Gb/s Media Independent Interface
800GXS	800GMII Extender Sublayer

4. Media Access Control

4.4 Specific implementations

4.4.2 MAC parameters

Change Table 4–2 as follows:

Table 4–2—MAC parameters

Parameters	MAC data rate			
	Up to and including 100 Mb/s	**1 Gb/s**	**2.5 Gb/s, 5 Gb/s, 25 Gb/s, 40 Gb/s, 50 Gb/s, 100 Gb/s, 200 Gb/s, ~~and~~ 400 Gb/s, and 800 Gb/s**	**10 Gb/s**
slotTime	512 bit times	4096 bit times	not applicable	not applicable
interPacketGap[a]	96 bits	96 bits	96 bits	96 bits
attemptLimit	16	16	not applicable	not applicable
backoffLimit	10	10	not applicable	not applicable
jamSize	32 bits	32 bits	not applicable	not applicable
maxBasicFrameSize	1518 octets	1518 octets	1518 octets	1518 octets
maxEnvelopeFrameSize	2000 octets	2000 octets	2000 octets	2000 octets
minFrameSize	512 bits (64 octets)	512 bits (64 octets)	512 bits (64 octets)	512 bits (64 octets)
burstLimit	not applicable	65 536 bits	not applicable	not applicable
ipgStretchRatio	not applicable	not applicable	not applicable	104 bits

[a] References to interFrameGap or interFrameSpacing in other clauses (e.g., Clause 13, Clause 35, and Clause 42) shall be interpreted as interPacketGap.

Change Note 7 in 4.4.2 as follows:

NOTE 7—For 40 Gb/s, 50 Gb/s, 100 Gb/s, 200 Gb/s, ~~and~~ 400 Gb/s, and 800 Gb/s operation, the received interpacket gap (the spacing between two packets, from the last bit of the FCS field of the first packet to the first bit of the Preamble of the second packet) can have a minimum value of 8 BT (bit times), as measured at the XLGMII, 50GMII, CGMII, 200GMII, ~~or~~ 400GMII, or 800GMII receive signals at the DTE due to clock tolerance and lane alignment requirements.

21. Introduction to 100 Mb/s baseband networks, type 100BASE-T

21.6 Protocol implementation conformance statement (PICS) proforma

21.6.2 Abbreviations and special symbols

Change 21.6.2 as follows:

The following symbols are used in the PICS proforma:

M	mandatory field/function
!	negation
O	optional field/function
O.<n>	optional field/function, but at least one of the group of options labeled by the same numeral <n> is required
O/<n>	optional field/function, but one and only one of the group of options labeled by the same numeral <n> is required
X	prohibited field/function
<item>:	simple-predicate condition, dependent on the support marked for <item>
<item1>*<item2>:	AND-predicate condition, the requirement has to be met if both optional items are implemented
<u><item1>+<item2>:</u>	<u>OR-predicate condition, the requirement has to be met if one or both of the items is implemented</u>

30. Management

30.3 Layer management for DTEs

30.3.2 PHY device managed object class

30.3.2.1 PHY device attributes

30.3.2.1.2 aPhyType

Insert the following new entry into the "APPROPRIATE SYNTAX" section of 30.3.2.1.2 after the entry for 400GBASE-R:

800GBASE-R	Clause 172 800 Gb/s multi-PCS lane 64B/66B

30.3.2.1.3 aPhyTypeList

Insert the following new entry into the "APPROPRIATE SYNTAX" section of 30.3.2.1.3 after the entry for 400GBASE-R:

800GBASE-R	Clause 172 800 Gb/s multi-PCS lane 64B/66B

30.5 Layer management for medium attachment units (MAUs)

30.5.1 MAU managed object class

30.5.1.1 MAU attributes

30.5.1.1.2 aMAUType

Insert the following new entry into the "APPROPRIATE SYNTAX" section of 30.5.1.1.2 after the entry for 400GBASE-DR4:

400GBASE-DR4-2	400GBASE-R PCS/PMA over 4 single-mode fibers in each direction PMD with reach up to at least 2 km as specified in Clause 124

Insert the following new entries into the "APPROPRIATE SYNTAX" section of 30.5.1.1.2 (as amended by IEEE Std 802.3db-2022) after the entry for 400GBASE-VR4:

800GBASE-CR8	800GBASE-R PCS/PMA over 8-lane shielded balanced copper cable PMD as specified in Clause 162
800GBASE-DR8	800GBASE-R PCS/PMA over 8 single-mode fibers in each direction PMD with reach up to at least 500 m as specified in Clause 124
800GBASE-DR8-2	800GBASE-R PCS/PMA over 8 single-mode fibers in each direction PMD with reach up to at least 2 km as specified in Clause 124
800GBASE-KR8	800GBASE-R PCS/PMA over an electrical backplane PMD as specified in Clause 163
800GBASE-R	Multi-lane PCS as specified in Clause 172 over undefined PMA/PMD
800GBASE-SR8	800GBASE-R PCS/PMA over 8 multimode fibers in each direction PMD with reach up to at least 100 m as specified in Clause 167
800GBASE-VR8	800GBASE-R PCS/PMA over 8 multimode fibers in each direction PMD with reach up to at least 50 m as specified in Clause 167

30.6 Management for link Auto-Negotiation

30.6.1 Auto-Negotiation managed object class

30.6.1.1 Auto-Negotiation attributes

30.6.1.1.5 aAutoNegLocalTechnologyAbility

Insert the following new entry into the "APPROPRIATE SYNTAX" section of 30.6.1.1.5 (as amended by IEEE Std 802.3ck-2022) after the entry for 400GR4:

800GR8	800GBASE-CR8 as specified in Clause 162 or 800GBASE-KR8 as specified in Clause 163

45. Management Data Input/Output (MDIO) Interface

45.2 MDIO Interface registers

45.2.1 PMA/PMD registers

Change the rows for registers 1.73 to 1.79, 1.1120 to 1.1199, 1.1220 to 1.1299, 1.1320 to 1.1399, and 1.1420 to 1.1499 in Table 45–3 (as amended by IEEE Std 802.3cz-2023) as follows (unchanged rows not shown):

Table 45–3—PMA/PMD registers

Register address	Register name	Subclause
…		
1.73	800G PMA/PMD ability	45.2.1.60b
1.74 through 1.79 ~~1.73 through 1.79~~	Reserved	
…		
1.1120 through 1.1127 ~~1.1120 through 1.1123~~	BASE-R PAM4 PMD training LP control, lane 0 through lane 7~~3~~	45.2.1.161
1.1128 through 1.1199 ~~1.1124 through 1.1199~~	Reserved	
…		
1.1220 through 1.1227 ~~1.1220 through 1.1223~~	BASE-R PAM4 PMD training LP status, lane 0 through lane 7~~3~~	45.2.1.163
1.1228 through 1.1299 ~~1.1224 through 1.1299~~	Reserved	
…		
1.1320 through 1.1327 ~~1.1320 through 1.1323~~	BASE-R PAM4 PMD training LD control, lane 0 through lane 7~~3~~	45.2.1.165
1.1328 through 1.1399 ~~1.1324 through 1.1399~~	Reserved	
…		
1.1420 through 1.1427 ~~1.1420 through 1.1423~~	BASE-R PAM4 PMD training LD status, lane 0 through lane 7~~3~~	45.2.1.167
1.1428 through 1.1449 ~~1.1424 through 1.1449~~	Reserved	
1.1450 through 1.1457 ~~1.1450 through 1.1453~~	PMD training pattern, lanes 0 to 7~~3~~	45.2.1.168
1.1458 through 1.1499 ~~1.1454 through 1.1499~~	Reserved	
…		

45.2.1.1 PMA/PMD control 1 register (Register 1.0)

Change Table 45–4 as follows (unchanged rows not shown):

Table 45–4—PMA/PMD control 1 register bit definitions

Bit(s)	Name	Description	R/W[a]
…			
1.0.5:2	Speed selection	5 4 3 2 1 1 x x = Reserved 1 0 1 1 = Reserved 1 0 1 0 = 800 Gb/s ~~1 0 1 x = Reserved~~ 1 0 0 1 = 400 Gb/s 1 0 0 0 = 200 Gb/s 0 1 1 1 = 5 Gb/s 0 1 1 0 = 2.5 Gb/s 0 1 0 1 = 50 Gb/s 0 1 0 0 = 25 Gb/s 0 0 1 1 = 100 Gb/s 0 0 1 0 = 40 Gb/s 0 0 0 1 = 10PASS-TS/2BASE-TL 0 0 0 0 = 10 Gb/s	R/W
…			

[a] R/W = Read/Write, SC = Self-clearing, RO = Read only.

45.2.1.1.3 Speed selection (1.0.13, 1.0.6, 1.0.5:2)

Change the last paragraph of 45.2.1.1.3 as follows:

When bits 5 through 2 are set to 0010 the use of a 40G PMA/PMD is selected; when set to 0011 the use of a 100G PMA/PMD is selected; when set to 0100 the use of a 25G PMA/PMD is selected; when set to 0101 the use of a 50G PMA/PMD is selected; when set to 0110 the use of a 2.5G PMA/PMD is selected; when set to 0111 the use of a 5G PMA/PMD is selected; when set to 1000 the use of a 200G PMA/PMD is selected; when set to 1001 the use of a 400G PMA/PMD is selected; when set to 1010 the use of an 800G PMA/PMD is selected. More specific selection is performed using the PMA/PMD control 2 register (register 1.7) (see 45.2.1.6.3).

45.2.1.6 PMA/PMD control 2 register (Register 1.7)

Change Table 45–7 (as amended by IEEE Std 802.3db-2022, IEEE Std 802.3ck-2022, and IEEE Std 802.3cz-2023) as follows:

Table 45–7—PMA/PMD control 2 register bit definitions

Bit(s)	Name	Description	R/W[a]
1.7.15:10	Reserved	Value always 0	RO
1.7.9	PIASE	PMA ingress AUI stop enable	R/W
1.7.8	PEASE	PMA egress AUI stop enable	R/W
~~1.7.7~~	~~Reserved~~	~~Value always 0~~	~~RO~~
1.7.7:0 ~~1.7.6:0~~	PMA/PMD type selection	7 6 5 4 3 2 1 0 1 1 x x x x x x = reserved 1 0 1 x x x x x = reserved 1 0 0 1 x x x x = reserved 1 0 0 0 1 x x x = reserved 1 0 0 0 0 1 1 x = reserved 1 0 0 0 0 1 0 1 = 800GBASE-DR8-2 PMA/PMD 1 0 0 0 0 1 0 0 = 800GBASE-DR8 PMA/PMD 1 0 0 0 0 0 1 1 = 800GBASE-SR8 PMA/PMD 1 0 0 0 0 0 1 0 = 800GBASE-VR8 PMA/PMD 1 0 0 0 0 0 0 1 = 800GBASE-CR8 PMA/PMD 1 0 0 0 0 0 0 0 = 800GBASE-KR8 PMA/PMD 0 1 1 1 1 1 1 1 = reserved 0 1 1 1 1 1 1 0 = 400GBASE-SR4 PMA/PMD 0 1 1 1 1 1 0 1 = 400GBASE-VR4 PMA/PMD 0 1 1 1 1 1 0 0 = 200GBASE-SR2 PMA/PMD 0 1 1 1 1 0 1 1 = 200GBASE-VR2 PMA/PMD 0 1 1 1 1 0 1 0 = 100GBASE-SR1 PMA/PMD 0 1 1 1 1 0 0 1 = 100GBASE-VR1 PMA/PMD 0 1 1 1 1 0 0 0 = 50GBASE-BR40-U PMA/PMD 0 1 1 1 0 1 1 1 = 50GBASE-BR20-U PMA/PMD 0 1 1 1 0 1 1 0 = 50GBASE-BR10-U PMA/PMD 0 1 1 1 0 1 0 1 = 50GBASE-BR40-D PMA/PMD 0 1 1 1 0 1 0 0 = 50GBASE-BR20-D PMA/PMD 0 1 1 1 0 0 1 1 = 50GBASE-BR10-D PMA/PMD 0 1 1 1 0 0 1 0 = 25GBASE-BR40-U PMA/PMD 0 1 1 1 0 0 0 1 = 25GBASE-BR20-U PMA/PMD 0 1 1 1 0 0 0 0 = 25GBASE-BR10-U PMA/PMD 0 1 1 0 1 1 1 1 = 25GBASE-BR40-D PMA/PMD 0 1 1 0 1 1 1 0 = 25GBASE-BR20-D PMA/PMD 0 1 1 0 1 1 0 1 = 25GBASE-BR10-D PMA/PMD 0 1 1 0 1 1 0 0 = 10GBASE-BR40-U PMA/PMD 0 1 1 0 1 0 1 1 = 10GBASE-BR20-U PMA/PMD 0 1 1 0 1 0 1 0 = 10GBASE-BR10-U PMA/PMD 0 1 1 0 1 0 0 1 = 10GBASE-BR40-D PMA/PMD 0 1 1 0 1 0 0 0 = 10GBASE-BR20-D PMA/PMD 0 1 1 0 0 1 1 1 = 10GBASE-BR10-D PMA/PMD 0 1 1 0 0 1 1 0 = reserved ~~1 1 0 0 1 0 x = reserved~~ 0 1 1 0 0 1 0 1 = reserved 0 1 1 0 0 1 0 0 = 400GBASE-DR4-2 PMA/PMD 0 1 1 0 0 0 1 1 = 400GBASE-ER8 PMA/PMD 0 1 1 0 0 0 1 0 = 400GBASE-LR4-6 PMA/PMD	R/W

Table 45–7—PMA/PMD control 2 register bit definitions *(continued)*

Bit(s)	Name	Description	R/W[a]
1.7.7:0 ~~1.7.6:0~~ (*continued*)	PMA/PMD type selection (*continued*)	0 1 1 0 0 0 0 1 = 400GBASE-FR4 PMA/PMD 0 1 1 0 0 0 0 0 = 400GBASE-SR4.2 PMA/PMD 0 1 0 1 1 1 1 1 = 400GBASE-SR8 PMA/PMD 0 1 0 1 1 1 1 0 = 400GBASE-CR4 PMA/PMD 0 1 0 1 1 1 0 1 = 400GBASE-KR4 PMA/PMD 0 1 0 1 1 1 0 0 = 400GBASE-LR8 PMA/PMD 0 1 0 1 1 0 1 1 = 400GBASE-FR8 PMA/PMD 0 1 0 1 1 0 1 0 = 400GBASE-DR4 PMA/PMD 0 1 0 1 1 0 0 1 = 400GBASE-SR16 PMA/PMD 0 1 0 1 1 0 0 0 = 200GBASE-ER4 PMA/PMD 0 1 0 1 0 1 1 1 = 200GBASE-CR2 PMA/PMD 0 1 0 1 0 1 1 0 = 200GBASE-KR2 PMA/PMD 0 1 0 1 0 1 0 1 = 200GBASE-LR4 PMA/PMD 0 1 0 1 0 1 0 0 = 200GBASE-FR4 PMA/PMD 0 1 0 1 0 0 1 1 = 200GBASE-DR4 PMA/PMD 0 1 0 1 0 0 1 0 = 200GBASE-SR4 PMA/PMD 0 1 0 1 0 0 0 1 = 200GBASE-CR4 PMA/PMD 0 1 0 1 0 0 0 0 = 200GBASE-KR4 PMA/PMD 0 1 0 0 1 1 1 1 = reserved 0 1 0 0 1 1 1 0 = 100GBASE-ZR PMA/PMD 0 1 0 0 1 1 0 1 = 100GBASE-LR1 PMA/PMD 0 1 0 0 1 1 0 0 = 100GBASE-FR1 PMA/PMD 0 1 0 0 1 0 1 1 = 100GBASE-DR PMA/PMD 0 1 0 0 1 0 1 0 = 100GBASE-SR2 PMA/PMD 0 1 0 0 1 0 0 1 = 100GBASE-CR2 PMA/PMD 0 1 0 0 1 0 0 0 = 100GBASE-KR2 PMA/PMD 0 1 0 0 0 1 1 1 = 100GBASE-CR1 PMA/PMD 0 1 0 0 0 1 1 0 = 100GBASE-KR1 PMA/PMD 0 1 0 0 0 1 0 1 = 50GBASE-ER PMA/PMD 0 1 0 0 0 1 0 0 = 50GBASE-LR PMA/PMD 0 1 0 0 0 0 1 1 = 50GBASE-FR PMA/PMD 0 1 0 0 0 0 1 0 = 50GBASE-SR PMA/PMD 0 1 0 0 0 0 0 1 = 50GBASE-CR PMA/PMD 0 1 0 0 0 0 0 0 = 50GBASE-KR PMA/PMD 0 0 1 1 1 1 1 1 = reserved 0 0 1 1 1 1 1 0 = BASE-AU PMA/PMD[b] 0 0 1 1 1 1 0 1 = BASE-T1 PMA/PMD[c] 0 0 1 1 1 1 0 0 = 5GBASE-KR PMA/PMD 0 0 1 1 1 0 1 1 = 2.5GBASE-KX PMA/PMD 0 0 1 1 1 0 1 0 = 25GBASE-SR PMA/PMD 0 0 1 1 1 0 0 1 = 25GBASE-KR or 25GBASE-KR-S PMA/PMD 0 0 1 1 1 0 0 0 = 25GBASE-CR or 25GBASE-CR-S PMA/PMD 0 0 1 1 0 1 1 1 = 25GBASE-T PMA 0 0 1 1 0 1 1 0 = 25GBASE-ER PMA/PMD 0 0 1 1 0 1 0 1 = 25GBASE-LR PMA/PMD 0 0 1 1 0 1 0 0 = BASE-H PMA/PMD[d] 0 0 1 1 0 0 1 1 = 10GPASS-XR-U PMA/PMD 0 0 1 1 0 0 1 0 = 10GPASS-XR-D PMA/PMD 0 0 1 1 0 0 0 1 = 5GBASE-T PMA 0 0 1 1 0 0 0 0 = 2.5GBASE-T PMA 0 0 1 0 1 1 1 1 = 100GBASE-SR4 PMA/PMD 0 0 1 0 1 1 1 0 = 100GBASE-CR4 PMA/PMD 0 0 1 0 1 1 0 1 = 100GBASE-KR4 PMA/PMD 0 0 1 0 1 1 0 0 = 100GBASE-KP4 PMA/PMD 0 0 1 0 1 0 1 1 = 100GBASE-ER4 PMA/PMD 0 0 1 0 1 0 1 0 = 100GBASE-LR4 PMA/PMD 0 0 1 0 1 0 0 1 = 100GBASE-SR10 PMA/PMD 0 0 1 0 1 0 0 0 = 100GBASE-CR10 PMA/PMD 0 0 1 0 0 1 1 1 = reserved	R/W

Table 45–7—PMA/PMD control 2 register bit definitions *(continued)*

Bit(s)	Name	Description	R/W[a]
1.7.7:0 ~~1.7.6:0~~ (*continued*)	PMA/PMD type selection (*continued*)	0 0 1 0 0 1 1 0 = 40GBASE-T PMA 0 0 1 0 0 1 0 1 = 40GBASE-ER4 PMA/PMD 0 0 1 0 0 1 0 0 = 40GBASE-FR PMA/PMD 0 0 1 0 0 0 1 1 = 40GBASE-LR4 PMA/PMD 0 0 1 0 0 0 1 0 = 40GBASE-SR4 PMA/PMD 0 0 1 0 0 0 0 1 = 40GBASE-CR4 PMA/PMD 0 0 1 0 0 0 0 0 = 40GBASE-KR4 PMA/PMD 0 0 0 1 1 1 1 1 = 10/1GBASE-PRX-U4 0 0 0 1 1 1 1 0 = 10GBASE-PR-U4 0 0 0 1 1 1 0 1 = 10/1GBASE-PRX-D4 0 0 0 1 1 1 0 0 = 10GBASE-PR-D4 0 0 0 1 1 0 1 1 = reserved 0 0 0 1 1 0 1 0 = 10GBASE-PR-U3 0 0 0 1 1 0 0 1 = 10GBASE-PR-U1 0 0 0 1 1 0 0 0 = 10/1GBASE-PRX-U3 0 0 0 1 0 1 1 1 = 10/1GBASE-PRX-U2 0 0 0 1 0 1 1 0 = 10/1GBASE-PRX-U1 0 0 0 1 0 1 0 1 = 10GBASE-PR-D3 0 0 0 1 0 1 0 0 = 10GBASE-PR-D2 0 0 0 1 0 0 1 1 = 10GBASE-PR-D1 0 0 0 1 0 0 1 0 = 10/1GBASE-PRX-D3 0 0 0 1 0 0 0 1 = 10/1GBASE-PRX-D2 0 0 0 1 0 0 0 0 = 10/1GBASE-PRX-D1 0 0 0 0 1 1 1 1 = 10BASE-T PMA/PMD 0 0 0 0 1 1 1 0 = 100BASE-TX PMA/PMD 0 0 0 0 1 1 0 1 = 1000BASE-KX PMA/PMD 0 0 0 0 1 1 0 0 = 1000BASE-T PMA/PMD 0 0 0 0 1 0 1 1 = 10GBASE-KR PMA/PMD 0 0 0 0 1 0 1 0 = 10GBASE-KX4 PMA/PMD 0 0 0 0 1 0 0 1 = 10GBASE-T PMA 0 0 0 0 1 0 0 0 = 10GBASE-LRM PMA/PMD 0 0 0 0 0 1 1 1 = 10GBASE-SR PMA/PMD 0 0 0 0 0 1 1 0 = 10GBASE-LR PMA/PMD 0 0 0 0 0 1 0 1 = 10GBASE-ER PMA/PMD 0 0 0 0 0 1 0 0 = 10GBASE-LX4 PMA/PMD 0 0 0 0 0 0 1 1 = 10GBASE-SW PMA/PMD 0 0 0 0 0 0 1 0 = 10GBASE-LW PMA/PMD 0 0 0 0 0 0 0 1 = 10GBASE-EW PMA/PMD 0 0 0 0 0 0 0 0 = 10GBASE-CX4 PMA/PMD	R/W

[a] R/W = Read/Write, RO = Read only.
[b] If BASE-AU PMA/PMD is selected, register 1.901 is used to differentiate which BASE-AU PMA/PMD is selected.
[c] If BASE-T1 is selected, bits 1.2100.3:0 are used to differentiate which BASE-T1 PMA/PMD is selected.
[d] If BASE-H PMA/PMD is selected, register 1.900 is used to differentiate which BASE-H PMA/PMD is selected.

45.2.1.7 PMA/PMD status 2 register (Register 1.8)

45.2.1.7.4 Transmit fault (1.8.11)

Change the rows that start with "100GBASE-KR1", "100GBASE-CR1", "100GBASE-VR1", and "400GBASE-DR4" in Table 45–9 (as amended by IEEE Std 802.3db-2022 and IEEE Std 802.3ck-2022) as follows (unchanged rows not shown):

Table 45–9—Transmit fault description location

PMA/PMD	Description location
…	
100GBASE-KR1, 200GBASE-KR2, 400GBASE-KR4, 800GBASE-KR8	163.8.9
…	
100GBASE-CR1, 200GBASE-CR2, 400GBASE-CR4, 800GBASE-CR8	162.8.9
…	
100GBASE-VR1, 100GBASE-SR1, 200GBASE-VR2, 200GBASE-SR2, 400GBASE-VR4, 400GBASE-SR4, 800GBASE-VR8, 800GBASE-SR8	167.5.10
…	
400GBASE-DR4, 400GBASE-DR4-2, 800GBASE-DR8, 800GBASE-DR8-2	124.5.10
…	

45.2.1.7.5 Receive fault (1.8.10)

Change the rows that start with "100GBASE-KR1", "100GBASE-CR1", "100GBASE-VR1", and "400GBASE-DR4" in Table 45–10 (as amended by IEEE Std 802.3db-2022 and IEEE Std 802.3ck-2022) as follows (unchanged rows not shown):

Table 45–10—Receive fault description location

PMA/PMD	Description location
…	
100GBASE-KR1, 200GBASE-KR2, 400GBASE-KR4, 800GBASE-KR8	163.8.10
…	
100GBASE-CR1, 200GBASE-CR2, 400GBASE-CR4, 800GBASE-CR8	162.8.10
…	

Table 45–10—Receive fault description location *(continued)*

PMA/PMD	Description location
100GBASE-VR1, 100GBASE-SR1, 200GBASE-VR2, 200GBASE-SR2, 400GBASE-VR4, 400GBASE-SR4, 800GBASE-VR8, 800GBASE-SR8	167.5.11
…	
400GBASE-DR4, 400GBASE-DR4-2, 800GBASE-DR8, 800GBASE-DR8-2	124.5.11
…	

45.2.1.8 PMD transmit disable register (Register 1.9)

Change the rows that start with "100GBASE-KR1", "100GBASE-CR1", "100GBASE-VR1", and "400GBASE-DR4" in Table 45–12 (as amended by IEEE Std 802.3db-2022 and IEEE Std 802.3ck-2022) as follows (unchanged rows not shown):

Table 45–12—Transmit disable description location

PMA/PMD	Description location
…	
100GBASE-KR1, 200GBASE-KR2, ~~and~~ 400GBASE-KR4, and 800GBASE-KR8	163.8.6
…	
100GBASE-CR1, 200GBASE-CR2, ~~and~~ 400GBASE-CR4, and 800GBASE-CR8	162.8.6
…	
100GBASE-VR1, 100GBASE-SR1, 200GBASE-VR2, 200GBASE-SR2, 400GBASE-VR4, ~~and~~ 400GBASE-SR4, 800GBASE-VR8, and 800GBASE-SR8	167.5.7
…	
400GBASE-DR4, 400GBASE-DR4-2, 800GBASE-DR8, and 800GBASE-DR8-2	124.5.7
…	

45.2.1.22 400G PMA/PMD extended ability register (Register 1.24)

Change the row for bit 1.24.14 in Table 45–25 (as amended by IEEE Std 802.3db-2022) as follows (unchanged rows not shown):

Table 45–25—400G PMA/PMD extended ability register bit definitions

Bit(s)	Name	Description	R/W[a]
…			
1.24.14	~~Reserved~~ 400GBASE-DR4-2 ability	~~Value always 0~~ 1 = PMA/PMD is able to perform 400GBASE-DR4-2 0 = PMA/PMD is not able to perform 400GBASE-DR4-2	RO
…			

[a] RO = Read only.

Insert 45.2.1.22.1aa after 45.2.1.22.1 as follows:

45.2.1.22.1aa 400GBASE-DR4-2 ability (1.24.14)

When read as a one, bit 1.24.14 indicates that the PMA/PMD is able to operate as a 400GBASE-DR4-2 PMA/PMD type. When read as a zero, bit 1.24.14 indicates that the PMA/PMD is not able to operate as a 400GBASE-DR4-2 PMA/PMD type.

45.2.1.23 PMA/PMD extended ability 2 (Register 1.25)

Change Table 45–26 as follows:

Table 45–26—PMA/PMD extended ability 2 register bit definitions

Bit(s)	Name	Description	R/W[a]
1.25.15:2 ~~1.25.15:1~~	Reserved	Value always 0	RO
1.25.1	800G capable	1 = PMA/PMD is capable of operating at 800 Gb/s and has the abilities listed in register 1.73 0 = PMA/PMD is not capable of operating at 800 Gb/s	RO
1.25.0	50G extended abilities	1 = PMA/PMD has 50G extended abilities listed in register 1.20 0 = PMA/PMD does not have 50G extended abilities	RO

[a] RO = Read only.

Insert 45.2.1.23.a before 45.2.1.23.1 as follows:

45.2.1.23.a 800G capable (1.25.1)

When read as a one, bit 1.25.1 indicates that the PMA/PMD is capable of operating at 800 Gb/s and has the abilities listed in register 1.73. When read as a zero, bit 1.25.1 indicates that the PMA/PMD is not capable of operating at 800 Gb/s.

Insert 45.2.1.60b after 45.2.1.60a (as inserted by IEEE Std 802.3cz-2023) as follows:

45.2.1.60b 800G PMA/PMD ability (Register 1.73)

The assignment of bits in the 800G PMA/PMD ability register is shown in Table 45–58b.

Table 45–58b—800G PMA/PMD ability register bit definitions

Bit(s)	Name	Description	R/W[a]
1.73.15	800G PMA remote loopback ability	1 = 800G PMA is able to perform a remote loopback function 0 = 800G PMA is not able to perform a remote loopback function	RO
1.73.14:6	Reserved	Value always 0	RO
1.73.5	800GBASE-DR8-2 ability	1 = PMA/PMD is able to perform 800GBASE-DR8-2 0 = PMA/PMD is not able to perform 800GBASE-DR8-2	RO
1.73.4	800GBASE-DR8 ability	1 = PMA/PMD is able to perform 800GBASE-DR8 0 = PMA/PMD is not able to perform 800GBASE-DR8	RO
1.73.3	800GBASE-SR8 ability	1 = PMA/PMD is able to perform 800GBASE-SR8 0 = PMA/PMD is not able to perform 800GBASE-SR8	RO
1.73.2	800GBASE-VR8 ability	1 = PMA/PMD is able to perform 800GBASE-VR8 0 = PMA/PMD is not able to perform 800GBASE-VR8	RO
1.73.1	800GBASE-CR8 ability	1 = PMA/PMD is able to perform 800GBASE-CR8 0 = PMA/PMD is not able to perform 800GBASE-CR8	RO
1.73.0	800GBASE-KR8 ability	1 = PMA/PMD is able to perform 800GBASE-KR8 0 = PMA/PMD is not able to perform 800GBASE-KR8	RO

[a] RO = Read only.

45.2.1.60b.1 800G PMA remote loopback ability (1.73.15)

When read as a one, bit 1.73.15 indicates that the 800G PMA is able to perform the remote loopback function. When read as a zero, bit 1.73.15 indicates that the 800G PMA is not able to perform the remote loopback function. If a PMA is able to perform the remote loopback function, then it is controlled using the PMA remote loopback bit 1.0.1 (see 45.2.1.1.4).

45.2.1.60b.2 800GBASE-DR8-2 ability (1.73.5)

When read as a one, bit 1.73.5 indicates that the PMA/PMD is able to operate as an 800GBASE-DR8-2 PMA/PMD type. When read as a zero, bit 1.73.5 indicates that the PMA/PMD is not able to operate as an 800GBASE-DR8-2 PMA/PMD type.

45.2.1.60b.3 800GBASE-DR8 ability (1.73.4)

When read as a one, bit 1.73.4 indicates that the PMA/PMD is able to operate as an 800GBASE-DR8 PMA/PMD type. When read as a zero, bit 1.73.4 indicates that the PMA/PMD is not able to operate as an 800GBASE-DR8 PMA/PMD type.

45.2.1.60b.4 800GBASE-SR8 ability (1.73.3)

When read as a one, bit 1.73.3 indicates that the PMA/PMD is able to operate as an 800GBASE-SR8 PMA/PMD type. When read as a zero, bit 1.73.3 indicates that the PMA/PMD is not able to operate as an 800GBASE-SR8 PMA/PMD type.

45.2.1.60b.5 800GBASE-VR8 ability (1.73.2)

When read as a one, bit 1.73.2 indicates that the PMA/PMD is able to operate as an 800GBASE-VR8 PMA/PMD type. When read as a zero, bit 1.73.2 indicates that the PMA/PMD is not able to operate as an 800GBASE-VR8 PMA/PMD type.

45.2.1.60b.6 800GBASE-CR8 ability (1.73.1)

When read as a one, bit 1.73.1 indicates that the PMA/PMD is able to operate as an 800GBASE-CR8 PMA/PMD type. When read as a zero, bit 1.73.1 indicates that the PMA/PMD is not able to operate as an 800GBASE-CR8 PMA/PMD type.

45.2.1.60b.7 800GBASE-KR8 ability (1.73.0)

When read as a one, bit 1.73.0 indicates that the PMA/PMD is able to operate as an 800GBASE-KR8 PMA/PMD type. When read as a zero, bit 1.73.0 indicates that the PMA/PMD is not able to operate as an 800GBASE-KR8 PMA/PMD type.

45.2.1.139 PMA precoder control Tx output (Register 1.600)

Change Table 45–109 as follows:

Table 45–109—PMA precoder control Tx output register bit definitions

Bit(s)	Name	Description	R/W[a]
1.600.15:8~~4~~	Reserved	Value always 0	RO
1.600.7	Lane 7 Tx output precoder enable	1 = Lane 7 Tx output precoder enabled 0 = Lane 7 Tx output precoder disabled	R/W
1.600.6	Lane 6 Tx output precoder enable	1 = Lane 6 Tx output precoder enabled 0 = Lane 6 Tx output precoder disabled	R/W
1.600.5	Lane 5 Tx output precoder enable	1 = Lane 5 Tx output precoder enabled 0 = Lane 5 Tx output precoder disabled	R/W
1.600.4	Lane 4 Tx output precoder enable	1 = Lane 4 Tx output precoder enabled 0 = Lane 4 Tx output precoder disabled	R/W
1.600.3	Lane 3 Tx output precoder enable	1 = Lane 3 Tx output precoder enabled 0 = Lane 3 Tx output precoder disabled	R/W
1.600.2	Lane 2 Tx output precoder enable	1 = Lane 2 Tx output precoder enabled 0 = Lane 2 Tx output precoder disabled	R/W
1.600.1	Lane 1 Tx output precoder enable	1 = Lane 1 Tx output precoder enabled 0 = Lane 1 Tx output precoder disabled	R/W
1.600.0	Lane 0 Tx output precoder enable	1 = Lane 0 Tx output precoder enabled 0 = Lane 0 Tx output precoder disabled	R/W

[a] R/W = Read/Write, RO = Read only.

Insert 45.2.1.139.a to 45.2.1.139.d before 45.2.1.139.1 as follows:

45.2.1.139.a Lane 7 Tx output precoder enable (1.600.7)

This bit enables the lane 7 Tx output precoder.

45.2.1.139.b Lane 6 Tx output precoder enable (1.600.6)

This bit enables the lane 6 Tx output precoder.

45.2.1.139.c Lane 5 Tx output precoder enable (1.600.5)

This bit enables the lane 5 Tx output precoder.

45.2.1.139.d Lane 4 Tx output precoder enable (1.600.4)

This bit enables the lane 4 Tx output precoder.

45.2.1.140 PMA precoder control Rx input (Register 1.601)

Change Table 45–110 as follows:

Table 45–110—PMA precoder control Rx input register bit definitions

Bit(s)	Name	Description	R/W[a]
1.601.15:8~~4~~	Reserved	Value always 0	RO
1.601.7	Lane 7 Rx input precoder enable	1 = Lane 7 Rx input precoder enabled 0 = Lane 7 Rx input precoder disabled	R/W
1.601.6	Lane 6 Rx input precoder enable	1 = Lane 6 Rx input precoder enabled 0 = Lane 6 Rx input precoder disabled	R/W
1.601.5	Lane 5 Rx input precoder enable	1 = Lane 5 Rx input precoder enabled 0 = Lane 5 Rx input precoder disabled	R/W
1.601.4	Lane 4 Rx input precoder enable	1 = Lane 4 Rx input precoder enabled 0 = Lane 4 Rx input precoder disabled	R/W
1.601.3	Lane 3 Rx input precoder enable	1 = Lane 3 Rx input precoder enabled 0 = Lane 3 Rx input precoder disabled	R/W
1.601.2	Lane 2 Rx input precoder enable	1 = Lane 2 Rx input precoder enabled 0 = Lane 2 Rx input precoder disabled	R/W
1.601.1	Lane 1 Rx input precoder enable	1 = Lane 1 Rx input precoder enabled 0 = Lane 1 Rx input precoder disabled	R/W
1.601.0	Lane 0 Rx input precoder enable	1 = Lane 0 Rx input precoder enabled 0 = Lane 0 Rx input precoder disabled	R/W

[a] R/W = Read/Write, RO = Read only.

Insert 45.2.1.140.a to 45.2.1.140.d before 45.2.1.140.1 as follows:

45.2.1.140.a Lane 7 Rx input precoder enable (1.601.7)

This bit enables the lane 7 Rx input precoder.

45.2.1.140.b Lane 6 Rx input precoder enable (1.601.6)

This bit enables the lane 6 Rx input precoder.

45.2.1.140.c Lane 5 Rx input precoder enable (1.601.5)

This bit enables the lane 5 Rx input precoder.

45.2.1.140.d Lane 4 Rx input precoder enable (1.601.4)

This bit enables the lane 4 Rx input precoder.

45.2.1.141 PMA precoder control Rx output (Register 1.602)

Change Table 45–111 as follows:

Table 45–111—PMA precoder control Rx output register bit definitions

Bit(s)	Name	Description	R/W[a]
1.602.15:8~~2~~	Reserved	Value always 0	RO
1.602.7	Lane 7 Rx output precoder enable	1 = Lane 7 Rx output precoder enabled 0 = Lane 7 Rx output precoder disabled	R/W
1.602.6	Lane 6 Rx output precoder enable	1 = Lane 6 Rx output precoder enabled 0 = Lane 6 Rx output precoder disabled	R/W
1.602.5	Lane 5 Rx output precoder enable	1 = Lane 5 Rx output precoder enabled 0 = Lane 5 Rx output precoder disabled	R/W
1.602.4	Lane 4 Rx output precoder enable	1 = Lane 4 Rx output precoder enabled 0 = Lane 4 Rx output precoder disabled	R/W
1.602.3	Lane 3 Rx output precoder enable	1 = Lane 3 Rx output precoder enabled 0 = Lane 3 Rx output precoder disabled	R/W
1.602.2	Lane 2 Rx output precoder enable	1 = Lane 2 Rx output precoder enabled 0 = Lane 2 Rx output precoder disabled	R/W
1.602.1	Lane 1 Rx output precoder enable	1 = Lane 1 Rx output precoder enabled 0 = Lane 1 Rx output precoder disabled	R/W
1.602.0	Lane 0 Rx output precoder enable	1 = Lane 0 Rx output precoder enabled 0 = Lane 0 Rx output precoder disabled	R/W

[a] R/W = Read/Write, RO = Read only.

Insert 45.2.1.141.a to 45.2.1.141.f before 45.2.1.141.1 as follows:

45.2.1.141.a Lane 7 Rx output precoder enable (1.602.7)

This bit enables the lane 7 Rx output precoder.

45.2.1.141.b Lane 6 Rx output precoder enable (1.602.6)

This bit enables the lane 6 Rx output precoder.

45.2.1.141.c Lane 5 Rx output precoder enable (1.602.5)

This bit enables the lane 5 Rx output precoder.

45.2.1.141.d Lane 4 Rx output precoder enable (1.602.4)

This bit enables the lane 4 Rx output precoder.

45.2.1.141.e Lane 3 Rx output precoder enable (1.602.3)

This bit enables the lane 3 Rx output precoder.

45.2.1.141.f Lane 2 Rx output precoder enable (1.602.2)

This bit enables the lane 2 Rx output precoder.

45.2.1.142 PMA precoder control Tx input (Register 1.603)

Change Table 45–112 as follows:

Table 45–112—PMA precoder control Tx input register bit definitions

Bit(s)	Name	Description	R/W[a]
1.603.15:8~~2~~	Reserved	Value always 0	RO
1.603.7	Lane 7 Tx input precoder enable	1 = Lane 7 Tx input precoder enabled 0 = Lane 7 Tx input precoder disabled	R/W
1.603.6	Lane 6 Tx input precoder enable	1 = Lane 6 Tx input precoder enabled 0 = Lane 6 Tx input precoder disabled	R/W
1.603.5	Lane 5 Tx input precoder enable	1 = Lane 5 Tx input precoder enabled 0 = Lane 5 Tx input precoder disabled	R/W
1.603.4	Lane 4 Tx input precoder enable	1 = Lane 4 Tx input precoder enabled 0 = Lane 4 Tx input precoder disabled	R/W
1.603.3	Lane 3 Tx input precoder enable	1 = Lane 3 Tx input precoder enabled 0 = Lane 3 Tx input precoder disabled	R/W
1.603.2	Lane 2 Tx input precoder enable	1 = Lane 2 Tx input precoder enabled 0 = Lane 2 Tx input precoder disabled	R/W

Table 45–112—PMA precoder control Tx input register bit definitions *(continued)*

Bit(s)	Name	Description	R/W[a]
1.603.1	Lane 1 Tx input precoder enable	1 = Lane 1 Tx input precoder enabled 0 = Lane 1 Tx input precoder disabled	R/W
1.603.0	Lane 0 Tx input precoder enable	1 = Lane 0 Tx input precoder enabled 0 = Lane 0 Tx input precoder disabled	R/W

[a] R/W = Read/Write, RO = Read only.

Insert 45.2.1.142.a to 45.2.1.142.f before 45.2.1.142.1 as follows:

45.2.1.142.a Lane 7 Tx input precoder enable (1.603.7)

This bit enables the lane 7 Tx input precoder.

45.2.1.142.b Lane 6 Tx input precoder enable (1.603.6)

This bit enables the lane 6 Tx input precoder.

45.2.1.142.c Lane 5 Tx input precoder enable (1.603.5)

This bit enables the lane 5 Tx input precoder.

45.2.1.142.d Lane 4 Tx input precoder enable (1.603.4)

This bit enables the lane 4 Tx input precoder.

45.2.1.142.e Lane 3 Tx input precoder enable (1.603.3)

This bit enables the lane 3 Tx input precoder.

45.2.1.142.f Lane 2 Tx input precoder enable (1.603.2)

This bit enables the lane 2 Tx input precoder.

45.2.1.144 PMA precoder request Rx input status (Register 1.605)

Change Table 45–114 as follows:

Table 45–114—PMA precoder request Rx input status register bit definitions

Bit(s)	Name	Description	R/W[a]
1.605.15:8~~2~~	Reserved	Value always 0	RO
1.605.7	Lane 7 Rx input precoder request status	1 = Lane 7 precoder Rx input requested 0 = Lane 7 precoder Rx input not requested	RO
1.605.6	Lane 6 Rx input precoder request status	1 = Lane 6 precoder Rx input requested 0 = Lane 6 precoder Rx input not requested	RO

Table 45–114—PMA precoder request Rx input status register bit definitions *(continued)*

Bit(s)	Name	Description	R/W[a]
1.605.5	Lane 5 Rx input precoder request status	1 = Lane 5 precoder Rx input requested 0 = Lane 5 precoder Rx input not requested	RO
1.605.4	Lane 4 Rx input precoder request status	1 = Lane 4 precoder Rx input requested 0 = Lane 4 precoder Rx input not requested	RO
1.605.3	Lane 3 Rx input precoder request status	1 = Lane 3 precoder Rx input requested 0 = Lane 3 precoder Rx input not requested	RO
1.605.2	Lane 2 Rx input precoder request status	1 = Lane 2 precoder Rx input requested 0 = Lane 2 precoder Rx input not requested	RO
1.605.1	Lane 1 Rx input precoder request status	1 = Lane 1 precoder Rx input requested 0 = Lane 1 precoder Rx input not requested	RO
1.605.0	Lane 0 Rx input precoder request status	1 = Lane 0 precoder Rx input requested 0 = Lane 0 precoder Rx input not requested	RO

[a] RO = Read only.

Insert 45.2.1.144.a to 45.2.1.144.f before 45.2.1.144.1 as follows:

45.2.1.144.a Lane 7 Rx input precoder request status (1.605.7)

This bit indicates the Rx input precoder request status for lane 7.

45.2.1.144.b Lane 6 Rx input precoder request status (1.605.6)

This bit indicates the Rx input precoder request status for lane 6.

45.2.1.144.c Lane 5 Rx input precoder request status (1.605.5)

This bit indicates the Rx input precoder request status for lane 5.

45.2.1.144.d Lane 4 Rx input precoder request status (1.605.4)

This bit indicates the Rx input precoder request status for lane 4.

45.2.1.144.e Lane 3 Rx input precoder request status (1.605.3)

This bit indicates the Rx input precoder request status for lane 3.

45.2.1.144.f Lane 2 Rx input precoder request status (1.605.2)

This bit indicates the Rx input precoder request status for lane 2.

45.2.1.145 PMA precoder request Tx input status (Register 1.606)

Change Table 45–115 as follows:

Table 45–115—PMA precoder request Tx input status register bit definitions

Bit(s)	Name	Description	R/W[a]
1.606.8~~2~~	Reserved	Value always 0	RO
1.606.7	Lane 7 Tx input precoder request status	1 = Lane 7 precoder Tx input requested 0 = Lane 7 precoder Tx input not requested	RO
1.606.6	Lane 6 Tx input precoder request status	1 = Lane 6 precoder Tx input requested 0 = Lane 6 precoder Tx input not requested	RO
1.606.5	Lane 5 Tx input precoder request status	1 = Lane 5 precoder Tx input requested 0 = Lane 5 precoder Tx input not requested	RO
1.606.4	Lane 4 Tx input precoder request status	1 = Lane 4 precoder Tx input requested 0 = Lane 4 precoder Tx input not requested	RO
1.606.3	Lane 3 Tx input precoder request status	1 = Lane 3 precoder Tx input requested 0 = Lane 3 precoder Tx input not requested	RO
1.606.2	Lane 2 Tx input precoder request status	1 = Lane 2 precoder Tx input requested 0 = Lane 2 precoder Tx input not requested	RO
1.606.1	Lane 1 Tx input precoder request status	1 = Lane 1 precoder Tx input requested 0 = Lane 1 precoder Tx input not requested	RO
1.606.0	Lane 0 Tx input precoder request status	1 = Lane 0 precoder Tx input requested 0 = Lane 0 precoder Tx input not requested	RO

[a] RO = Read only.

Insert 45.2.1.145.a to 45.2.1.145.f before 45.2.1.145.1 as follows:

45.2.1.145.a Lane 7 Tx input precoder request status(1.606.7)

This bit indicates the Tx input precoder request status for lane 7.

45.2.1.145.b Lane 6 Tx input precoder request status(1.606.6)

This bit indicates the Tx input precoder request status for lane 6.

45.2.1.145.c Lane 5 Tx input precoder request status(1.606.5)

This bit indicates the Tx input precoder request status for lane 5.

45.2.1.145.d Lane 4 Tx input precoder request status(1.606.4)

This bit indicates the Tx input precoder request status for lane 4.

45.2.1.145.e Lane 3 Tx input precoder request status(1.606.3)

This bit indicates the Tx input precoder request status for lane 3.

45.2.1.145.f Lane 2 Tx input precoder request status(1.606.2)

This bit indicates the Tx input precoder request status for lane 2.

Change the title and text of 45.2.1.161 as follows (Table 45–129 remains unchanged):

45.2.1.161 BASE-R PAM4 PMD training LP control, lane 0 through lane 7~~3~~ registers (Register 1.1120 through 1.112~~7~~7~~3~~)

The BASE-R PAM4 PMD training LP control, lane 0 through lane 7~~3~~ registers reflect the contents of the first 16-bit word of the training frame most recently received for each lane. Lanes 0 to 7 map to registers 1.1120 to 1.1127, respectively. ~~Lane 0 maps to register 1.1120, lane 1 maps to register 1.1121, lane 2 maps to register 1.1122, and lane 3 maps to register 1.1123.~~

The assignment of bits in the BASE-R PAM4 PMD training LP control, lane 0 register is shown in Table 45–129. The assignment of bits in the registers for lane 1 through lane 7~~3~~ is equivalent to the assignment for lane 0. When training is not disabled, the bits in registers 1.1120 through 1.112~~7~~7~~3~~ are read only; however, when training is disabled the R/W bits become writeable.

Change the title and text of 45.2.1.163 as follows (Table 45–130 remains unchanged):

45.2.1.163 BASE-R PAM4 PMD training LP status, lane 0 through lane 7~~3~~ registers (Register 1.1220 through 1.122~~7~~7~~3~~)

The BASE-R PAM4 PMD training LP status, lane 0 through lane 7~~3~~ registers reflect the contents of the second 16-bit word of the training frame most recently received for each lane. Lanes 0 to 7 map to registers 1.1220 to 1.1227, respectively. ~~Lane 0 maps to register 1.1220, lane 1 maps to register 1.1221, lane 2 maps to register 1.1222, and lane 3 maps to register 1.1223.~~

The assignment of bits in the BASE-R PAM4 PMD training LP status, lane 0 register is shown in Table 45–130. The assignment of bits in the registers for lane 1 through lane 7~~3~~ is equivalent to the assignment for lane 0.

Change the title and text of 45.2.1.165 as follows (Table 45–131 remains unchanged):

45.2.1.165 BASE-R PAM4 PMD training LD control, lane 0 through lane 7~~3~~ registers (Register 1.1320 through 1.132~~7~~7~~3~~)

The BASE-R PAM4 PMD training LD control, lane 0 through lane 7~~3~~ registers reflect the contents of the control field of the outgoing training frame for each lane. Lanes 0 to 7 map to registers 1.1320 to 1.1327, respectively. ~~Lane 0 maps to register 1.1320, lane 1 maps to register 1.1321, lane 2 maps to register 1.1322, and lane 3 maps to register 1.1323.~~

The assignment of bits in the BASE-R PAM4 PMD training LP control, lane 0 register is shown in Table 45–131. The assignment of bits in the registers for lane 1 through lane 7~~3~~ is equivalent to the assignment for lane 0.

Change the title and text of 45.2.1.167 as follows (Table 45–132 remains unchanged):

45.2.1.167 BASE-R PAM4 PMD training LD status, lane 0 through lane 7~~3~~ registers (Register 1.1420 through 1.142~~7~~7~~3~~)

The BASE-R PAM4 PMD training LD status, lane 0 through lane 7~~3~~ registers reflect the contents of the status field of the outgoing training frame for each lane. Lanes 0 to 7 map to registers 1.1420 to 1.1427,

respectively. ~~Lane 0 maps to register 1.1420, lane 1 maps to register 1.1421, lane 2 maps to register 1.1422, and lane 3 maps to register 1.1423.~~

The assignment of bits in the BASE-R PAM4 PMD training LD status, lane 0 register is shown in Table 45–132. The assignment of bits in the registers for lane 1 through lane 7~~3~~ is equivalent to the assignment for lane 0.

Change the title and first two paragraphs of 45.2.1.168 as follows:

45.2.1.168 PMD training pattern lanes 0 through 7~~3~~ (Register 1.1450 through 1.145~~73~~)

The assignment of bits in the PMD training pattern lane 0 register is shown in Table 45–133. The assignment of bits in the PMD training pattern lanes 1 through 7~~3~~ registers are defined similarly to lane 0. Registers 1.1450 to 1.1457 control the PMD training pattern for PMD lanes 0 to 7, respectively. ~~Register 1.1450 controls the PMD training pattern for PMD lane 0; register 1.1451 controls the PMD training pattern for PMD lane 1; etc.~~

Register bits 12:11 contain a 2-bit identifier that selects the polynomial used for training ~~in the~~ a particular PMD lane ~~according to the definition~~ as described in 92.7.12, 136.8.11.1.3, or 162.8.11.1. The polynomial identifier for adjacent lanes ~~each lane~~ should be unique to avoid a risk of impairment of the PMD control function. If the same polynomial identifier is used for multiple lanes, different initial seeds should be used for each of those lanes.~~; two lanes having the same identifier could impair operation of the PMD control function.~~ The default identifiers are (binary): for lane 0, 00; for lane 1, 01; for lane 2, 10; for lane 3, 11; for lane 4, 00; for lane 5, 01; for lane 6, 10; for lane 7, 11.

Change the last sentence of the last paragraph of 45.2.1.168 as follows:

The default PRBS13 seed values are given in Table 136–8 for PMDs with one, two, or four lanes, and in Table 162–10a for PMDs with eight lanes.

45.2.3 PCS registers

Change the rows for registers 3.50 to 3.59, 3.220 to 3.499, and 3.600 to 3.799 in Table 45–233 as follows (unchanged rows not shown):

Table 45–233—PCS registers

Register address	Register name	Subclause
…		
~~3.50 through 3.53~~ 3.50 through 3.54	Multi-lane BASE-R PCS alignment status 1 through 5 ~~4~~	45.2.3.23, 45.2.3.24, 45.2.3.25
~~3.54 through 3.59~~ 3.55 through 3.59	Reserved	
~~3.220 through 3.399~~ 3.220 through 3.299	Reserved	
3.300 through 3.302	RS-FEC codeword counter	45.2.3.48a
3.303 through 3.339	Reserved	
3.340 through 3.369	RS-FEC codeword error bin 1 through 15	45.2.3.48b
3.370 through 3.399	Reserved	
~~3.400 through 3.419~~ 3.400 through 3.431	PCS lane mapping registers, lanes 0 through 31 ~~19~~	45.2.3.49, 45.2.3.50
~~3.420 through 3.499~~ 3.432 through 3.499	Reserved	
…		
~~3.600 through 3.631~~ 3.600 through 3.663	PCS FEC symbol error counter, lane 0 to 31 ~~15~~	45.2.3.58, 45.2.3.59
~~3.632 through 3.799~~ 3.664 through 3.799	Reserved	
…		

45.2.3.4 PCS speed ability (Register 3.4)

Change the row for bits 3.4.15:10 in Table 45–236 as follows (unchanged rows not shown):

Table 45–236—PCS speed ability register bit definitions

Bit(s)	Name	Description	R/W[a]
3.4.15:11 ~~10~~	Reserved for future speeds	Value always 0	RO
3.4.10	800G capable	1 = PCS is capable of operating at 800 Gb/s 0 = PCS is not capable of operating at 800 Gb/s	RO
…			

[a] RO = Read only.

Insert 45.2.3.4.11 after 45.2.3.4.10 as follows:

45.2.3.4.11 800G capable (3.4.10)

When read as a one, bit 3.4.10 indicates that the PCS is able to operate at a data rate of 800 Gb/s. When read as a zero, bit 3.4.10 indicates that the PCS is not able to operate at a data rate of 800 Gb/s.

45.2.3.19 BASE-R PCS test-pattern control register (Register 3.42)

Change the fourth and fifth sentences of 45.2.3.19 as follows:

Scrambled idle test patterns are defined for 25/40/50/100/200/400/800GBASE-R PCS only. The test-pattern methodology is described in 49.2.8, ~~and~~ 82.2.11, 119.2.4.9, and 172.2.4.11.

Change the title and text of 45.2.3.25 as follows (Table 45–254 remains unchanged):

45.2.3.25 Multi-lane BASE-R PCS alignment status ~~3~~ registers 3 through 5 (Register 3.52, 3.53, 3.54)

The assignment of bits in the multi-lane BASE-R PCS alignment status ~~3~~ registers 3 through 5 is shown in Table 45–254, Table 45–255, and Table 45–255a. All the bits in the multi-lane BASE-R PCS alignment status ~~3~~ registers 3 through 5 are read only; a write to the multi-lane BASE-R PCS alignment status ~~3~~ registers 3 through 5 shall have no effect. A PCS device that does not implement multi-lane BASE-R PCS shall return a zero for all bits in the multi-lane BASE-R PCS alignment status ~~3~~ registers 3 through 5. A device that implements multi-lane BASE-R PCS shall return a zero for all bits in the multi-lane BASE-R PCS alignment status ~~3~~ registers 3 through 5 that are not required for the PCS configuration. It is the responsibility of the STA management entity to ensure that a port type is supported by all MMDs before interrogating any of its status bits.

Insert Table 45–255 and Table 45–255a after Table 45–254 as follows (the existing Table 45–255 is deleted from the existing 45.2.3.26 below):

Table 45–255—Multi-lane BASE-R PCS alignment status 4 register bit definitions

Bit(s)	Name	Description	R/W[a]
3.53.15	Lane 23 aligned	1 = Lane 23 alignment marker is locked 0 = Lane 23 alignment marker is not locked	RO
3.53.14	Lane 22 aligned	1 = Lane 22 alignment marker is locked 0 = Lane 22 alignment marker is not locked	RO
3.53.13	Lane 21 aligned	1 = Lane 21 alignment marker is locked 0 = Lane 21 alignment marker is not locked	RO
3.53.12	Lane 20 aligned	1 = Lane 20 alignment marker is locked 0 = Lane 20 alignment marker is not locked	RO
3.53.11	Lane 19 aligned	1 = Lane 19 alignment marker is locked 0 = Lane 19 alignment marker is not locked	RO
3.53.10	Lane 18 aligned	1 = Lane 18 alignment marker is locked 0 = Lane 18 alignment marker is not locked	RO

Table 45–255—Multi-lane BASE-R PCS alignment status 4 register bit definitions *(continued)*

Bit(s)	Name	Description	R/W[a]
3.53.9	Lane 17 aligned	1 = Lane 17 alignment marker is locked 0 = Lane 17 alignment marker is not locked	RO
3.53.8	Lane 16 aligned	1 = Lane 16 alignment marker is locked 0 = Lane 16 alignment marker is not locked	RO
3.53.7	Lane 15 aligned	1 = Lane 15 alignment marker is locked 0 = Lane 15 alignment marker is not locked	RO
3.53.6	Lane 14 aligned	1 = Lane 14 alignment marker is locked 0 = Lane 14 alignment marker is not locked	RO
3.53.5	Lane 13 aligned	1 = Lane 13 alignment marker is locked 0 = Lane 13 alignment marker is not locked	RO
3.53.4	Lane 12 aligned	1 = Lane 12 alignment marker is locked 0 = Lane 12 alignment marker is not locked	RO
3.53.3	Lane 11 aligned	1 = Lane 11 alignment marker is locked 0 = Lane 11 alignment marker is not locked	RO
3.53.2	Lane 10 aligned	1 = Lane 10 alignment marker is locked 0 = Lane 10 alignment marker is not locked	RO
3.53.1	Lane 9 aligned	1 = Lane 9 alignment marker is locked 0 = Lane 9 alignment marker is not locked	RO
3.53.0	Lane 8 aligned	1 = Lane 8 alignment marker is locked 0 = Lane 8 alignment marker is not locked	RO

[a] RO = Read only.

Table 45–255a—Multi-lane BASE-R PCS alignment status 5 register bit definitions

Bit(s)	Name	Description	R/W[a]
3.54.15:8	Reserved	Value always 0	RO
3.54.7	Lane 31 aligned	1 = Lane 31 alignment marker is locked 0 = Lane 31 alignment marker is not locked	RO
3.54.6	Lane 30 aligned	1 = Lane 30 alignment marker is locked 0 = Lane 30 alignment marker is not locked	RO
3.54.5	Lane 29 aligned	1 = Lane 29 alignment marker is locked 0 = Lane 29 alignment marker is not locked	RO
3.54.4	Lane 28 aligned	1 = Lane 28 alignment marker is locked 0 = Lane 28 alignment marker is not locked	RO

Table 45–255a—Multi-lane BASE-R PCS alignment status 5 register bit definitions *(continued)*

Bit(s)	Name	Description	R/W[a]
3.54.3	Lane 27 aligned	1 = Lane 27 alignment marker is locked 0 = Lane 27 alignment marker is not locked	RO
3.54.2	Lane 26 aligned	1 = Lane 26 alignment marker is locked 0 = Lane 26 alignment marker is not locked	RO
3.54.1	Lane 25 aligned	1 = Lane 25 alignment marker is locked 0 = Lane 25 alignment marker is not locked	RO
3.54.0	Lane 24 aligned	1 = Lane 24 alignment marker is locked 0 = Lane 24 alignment marker is not locked	RO

[a] RO = Read only.

Delete 45.2.3.25.1 to 45.2.3.25.8.

Insert new subclauses 45.2.3.25.1 and 45.2.3.25.2 as follows:

45.2.3.25.1 Lane 0 aligned (3.52.0)

When read as a one, bit 3.52.0 indicates that the PCS receiver has achieved alignment marker lock for service interface lane 0. When read as a zero, bit 3.52.0 indicates that the PCS receiver lane 0 has not achieved alignment marker lock. This bit reflects the state of am_lock[0] (see 82.2.19.2.2) or amps_lock[0] (see 119.2.6.2.2 and 172.2.6.2.2).

45.2.3.25.2 Lanes 1 through 31 aligned (bits 3.52.1 through 3.54.7)

The definition of lanes 1 through 31 aligned is identical to that described for lane 0 in 45.2.3.25.1.

The lane aligned status for lanes 1 through 7 is indicated in bits 3.52.1 through 3.52.7, respectively. The lane aligned status for lanes 8 through 23 is indicated in bits 3.53.0 through 3.53.15, respectively. The lane aligned status for lanes 24 through 31 is in bits 3.54.0 through 3.54.7, respectively.

Delete 45.2.3.26 (including its subclauses and the existing Table 45–255).

Insert 45.2.3.48a and 45.2.3.48b after 45.2.3.48 as follows:

45.2.3.48a RS-FEC codeword counter register (Register 3.300, 3.301, 3.302)

The assignment of bits in the RS-FEC codeword counter register is shown in Table 45–276a. The RS-FEC codeword counter register applies to the RS-FEC defined in Clause 172. See 172.3.5 for a definition of this counter. It is a 48-bit counter that counts once for each FEC codeword received when align status (3.50.12) is set to one. Its bits are reset to all zeros when the register is read by the management function or upon reset, and held at all ones in the case of overflow.

Registers 3.300, 3.301, and 3.302 are used to read the value of the 48-bit counter. When using these registers to read the 48-bit counter value, the register 3.300 is read first, the values of the registers 3.301 and 3.302 are

latched when (and only when) register 3.300 is read, and reads of registers 3.301 and 3.302 return their latched values rather than the current value of the counter.

Table 45–276a—RS-FEC codeword counter bit definitions

Bit(s)	Name	Description	R/W[a]
3.300.15:0	RS-FEC codewords lower	FEC_cw_counter[15:0]	RO, NR
3.301.15:0	RS-FEC codewords middle	FEC_cw_counter[31:16]	RO, NR
3.302.15:0	RS-FEC codewords upper	FEC_cw_counter[47:32]	RO, NR

[a] RO = Read only, NR = Non Roll-over.

45.2.3.48b RS-FEC codeword error bin registers 1 through 15 (Registers 3.340 through 3.369)

The assignment of bits in the RS-FEC codeword error bin 1 register is shown in Table 45–276b. The assignment of bits in the other RS-FEC codeword error bin registers is identical to that of bin 1. The RS-FEC codeword error bin registers increment depending upon the error signature of a corrected codeword (see 172.3.6). Their bits are reset to all zeros when the register is read by the management function or upon reset, and held at all ones in the case of overflow.

Two registers are used to read the value of each 32-bit counter, the value of the second register is latched when the first register is read. For example when registers 3.340 and 3.341 are used to read the 32-bit counter value of FEC_codeword_error_bin_1, the register 3.340 is read first, the value of the register 3.341 is latched when (and only when) register 3.340 is read, and reads of register 3.341 return the latched value rather than the current value of the counter.

Table 45–276b—RS-FEC codeword error bin 1 bit definitions

Bit(s)	Name	Description	R/W[a]
3.340.15:0	RS-FEC codeword error bin 1 lower	FEC_codeword_error_bin_1[15:0]	RO, NR
3.341.15:0	RS-FEC codeword error bin 1 upper	FEC_codeword_error_bin_1[31:16]	RO, NR

[a] RO = Read only, NR = Non Roll-over.

45.2.3.49 Lane 0 mapping register (Register 3.400)

Change the text of 45.2.3.49 as follows (Table 45–277 remains unchanged):

The assignment of bits in the Lane 0 mapping register is shown in Table 45–277. When the multi-lane PCS described in Clause 82, ~~or~~ Clause 119, or Clause 172 detects and locks the alignment marker for service interface lane 0, the detected PCS lane number is recorded in this register. The contents of the Lane 0 mapping register ~~is~~ are valid when Lane 0 aligned bit (3.52.0) is set to one and ~~is~~ are invalid otherwise.

45.2.3.50 Lanes 1 through 31~~19~~ mapping registers (Registers 3.401 through 3.431~~419~~)

Change 45.2.3.50 as follows:

The definition of lanes 1 through 31~~19~~ mapping registers is identical to that described for lane 0 in 45.2.3.49. The lane mapping for lane 1 is in register 3.401; lane 2 is in register 3.402; etc.

45.2.3.58 PCS FEC symbol error counter lane 0 (Register 3.600, 3.601)

Change the text of 45.2.3.58 as follows (Table 45–285 remains unchanged):

The assignment of bits in the PCS FEC symbol error counter lane 0 register is shown in Table 45–285. See 119.3.4 and 172.3.4 for a definition of this counter. Symbol errors detected in PCS lane 0 are counted and shown in register 3.600.15:0 and 3.601.15:0. These bits shall be reset to all zeros when the register is read by the management function or upon PHY reset. These bits shall be held at all ones in the case of overflow. Registers 3.600~~,~~ and 3.601 are used to read the value of a 32-bit counter. When registers 3.600 and 3.601 are used to read the 32-bit counter value, the register 3.600 is read first, the value of the register 3.601 is latched when (and only when) register 3.600 is read, and reads of register 3.601 return the latched value rather than the current value of the counter.

Change the title and text of 45.2.3.59 as follows:

45.2.3.59 PCS FEC symbol error counter lane 1 through 31~~15~~ (Registers 3.602 through 3.663~~631~~)

The behavior of the PCS FEC symbol error counters, lane 1 through 31~~15~~ is identical to that described for PCS lane 0 in 45.2.3.58. Errors detected in each PCS lane are counted and shown in the corresponding register. PCS lane 1, lower 16 bits are shown in register 3.602; PCS lane 1, upper 16 bits are shown in register 3.603; PCS lane 2, lower 16 bits are shown in register 3.604; through register 3.663~~631~~ for PCS lane 31~~15~~, upper 16 bits.

45.2.3.60 PCS FEC control register (Register 3.800)

45.2.3.60.1 PCS FEC degraded SER enable (3.800.2)

Change 45.2.3.60.1 as follows:

This bit enables the PCS FEC decoder to signal the presence of a degraded SER. When set to a one, this bit enables degraded SER signaling. When set to a zero, degraded SER signaling is disabled. Writes to this bit are ignored and reads return a zero if the PCS FEC does not have the ability to signal the presence of a degraded SER (see 119.2.5.3 and 172.2.5.3).

45.2.3.60.2 PCS FEC bypass indication enable (3.800.1)

Change 45.2.3.60.2 as follows:

This bit enables the PCS FEC decoder to bypass error indication to the upper layers through the sync bits. When set to a one, this bit enables bypass of the error indication. When set to a zero, errors are indicated to the upper layers through the sync bits. Writes to this bit are ignored and reads return a zero if the PCS FEC does not have the ability to bypass indicating decoding errors (see 119.2.5.3 and 172.2.5.3).

45.2.3.61 PCS FEC status register (Register 3.801)

Change 45.2.3.61.1 to 45.2.3.61.6 as follows:

45.2.3.61.1 Local degraded SER received (3.801.6)

When read as a one, bit 3.801.6 indicates that the local degraded SER signal has been received. This bit reflects the state of rx_local_degraded (see 119.2.6.2.2 and 172.2.6.2.2).

45.2.3.61.2 Remote degraded SER received (3.801.5)

When read as a one, bit 3.801.5 indicates that the remote degraded SER signal has been received. This bit reflects the state of rx_rm_degraded (see 119.2.6.2.2 and 172.2.6.2.2).

45.2.3.61.3 PCS FEC degraded SER (3.801.4)

When read as a one, bit 3.801.4 indicates that the local PCS has detected a degradation of the received signal. This bit reflects the state of the variable FEC_degraded_SER (see 119.2.6.2.2 and 172.2.6.2.2). The value of bit 3.801.4 is unspecified if the value of the PCS FEC degraded SER activate threshold (registers 3.806 and 3.807) is less than the value of the PCS FEC degraded SER deactivate threshold (registers 3.808 and 3.809).

45.2.3.61.4 PCS FEC degraded SER ability (3.801.3)

The PCS FEC decoder may have the option to signal the presence of a degraded SER (see 119.2.5.3 and 172.2.5.3). This bit is set to one to indicate that the decoder has the ability to signal the presence of a degraded SER. The bit is set to zero if this ability is not supported.

45.2.3.61.5 PCS FEC high SER (3.801.2)

When PCS FEC bypass indication enable (bit 3.800.1) is set to one, this bit is set to one if the number of FEC symbol errors in a window of 8192 codewords exceeds the threshold (see 119.2.5.3 and 172.3.1) and is set to zero otherwise. The bit is set to zero if PCS FEC bypass indication enable (bit 3.800.1) is set to zero. This bit shall be implemented with latching high behavior.

45.2.3.61.6 PCS FEC bypass indication ability (3.801.1)

The PCS FEC decoder may have the option to perform error detection without error indication (see 119.2.5.3 and 172.2.5.3) to reduce the delay contributed by the FEC decoder. This bit is set to one to indicate that the decoder has this ability to bypass error indication. The bit is set to zero if this ability is not supported.

Change the text of 45.2.3.62 to 45.2.3.66 as follows (Table 45–288 to Table 45–292 remain unchanged):

45.2.3.62 PCS FEC corrected codewords counter (Register 3.802, 3.803)

The assignment of bits in the PCS FEC corrected codewords counter register is shown in Table 45–288. See 119.3.2 and 172.3.2 for a definition of this counter. These bits shall be reset to all zeros when the register is read by the management function or upon PHY reset. These bits shall be held at all ones in the case of overflow. Registers 3.802~~,~~ and 3.803 are used to read the value of a 32-bit counter. When registers 3.802 and 3.803 are used to read the 32-bit counter value, the register 3.802 is read first, the value of the register 3.803 is latched when (and only when) register 3.802 is read, and reads of register 3.803 return the latched value rather than the current value of the counter.

45.2.3.63 PCS FEC uncorrected codewords counter (Register 3.804, 3.805)

The assignment of bits in the PCS FEC uncorrected codewords counter register is shown in Table 45–289. See 119.3.3 and 172.3.3 for a definition of this counter. These bits shall be reset to all zeros when the register is read by the management function or upon PHY reset. These bits shall be held at all ones in the case of overflow. Registers 3.804~~,~~ and 3.805 are used to read the value of a 32-bit counter. When registers 3.804 and 3.805 are used to read the 32-bit counter value, the register 3.804 is read first, the value of the register 3.805 is latched when (and only when) register 3.804 is read, and reads of register 3.805 return the latched value rather than the current value of the counter.

45.2.3.64 PCS FEC degraded SER activate threshold register (Register 3.806, 3.807)

The assignment of bits in the PCS FEC degraded SER activate threshold register is shown in Table 45–290. The value controls the threshold used to set the PCS FEC degraded SER bit (3.801.4) as defined in 119.2.5.3 and 172.2.5.3.

45.2.3.65 PCS FEC degraded SER deactivate threshold register (Register 3.808, 3.809)

The assignment of bits in the PCS FEC degraded SER deactivate threshold register is shown in Table 45–291. The value controls the threshold used to clear the PCS FEC degraded SER bit (3.801.4) as defined in 119.2.5.3 and 172.2.5.3.

45.2.3.66 PCS FEC degraded SER interval register (Register 3.810, 3.811)

The assignment of bits in the PCS FEC degraded SER interval register is shown in Table 45–292. The value controls the interval used to set and clear the PCS FEC degraded SER bit (3.801.4) as defined in 119.2.5.3 and 172.2.5.3.

45.2.4 PHY XS registers

Change the rows for registers 4.52 to 4.799 in Table 45–314 as follows (unchanged rows not shown):

Table 45–314—PHY XS registers

Register address	Register name	Subclause
…		
4.52 through 4.54	Multi-lane BASE-R PHY XS alignment status 3 through 5	45.2.4.15
~~4.53~~	~~Multi-lane BASE-R PHY XS alignment status 4~~	~~45.2.4.16~~
~~4.54~~ 4.55 through 4.299	Reserved	
4.300 through 4.302	PHY XS RS-FEC codeword counter	45.2.4.16
4.303 through 4.339	Reserved	
4.340 through 4.369	PHY XS RS-FEC codeword error bin 1 through 15	45.2.4.16a
4.370 through 4.399	Reserved	
~~4.400 through 4.415~~ 4.400 through 4.431	PHY XS lane mapping, lane 0 through 31~~15~~	45.2.4.17, 45.2.4.18
~~4.415 through 4.599~~ 4.432 through 4.599	Reserved	

Table 45–314—PHY XS registers *(continued)*

Register address	Register name	Subclause
~~4.600 through 4.631~~ 4.600 through 4.663	PHY XS FEC symbol error counter, lane 0 to 31~~15~~	45.2.4.19, 45.2.4.20
~~4.632 through 4.799~~ 4.664 through 4.799	Reserved	
…		

45.2.4.4 PHY XS speed ability (Register 4.4)

Change the row for bits 4.4.15:10 in Table 45–317 as follows (unchanged rows not shown):

Table 45–317—PHY XS speed ability register bit definitions

Bit(s)	Name	Description	R/W[a]
4.4.15:11 ~~10~~	Reserved	Value always 0	RO
4.4.10	800G capable	1 = PHY XS is capable of operating at 800 Gb/s 0 = PHY XS is not capable of operating at 800 Gb/s	RO
…			

[a] RO = Read only.

Insert 45.2.4.4.a before 45.2.4.4.1 as follows:

45.2.4.4.a 800G capable (4.4.10)

When read as a one, bit 4.4.10 indicates that the PHY XS is able to operate at a data rate of 800 Gb/s. When read as a zero, bit 4.4.10 indicates that the PHY-XS is not able to operate at a data rate of 800 Gb/s.

Change the title and text of 45.2.4.15 as follows (Table 45–325 remains unchanged):

45.2.4.15 Multi-lane BASE-R PHY XS alignment status ~~3~~ registers 3 through 5 (Register 4.52, 4.53, 4.54)

The assignment of bits in the multi-lane BASE-R PHY XS alignment status ~~3~~ registers 3 through 5 is shown in Table 45–325, Table 45–326, and Table 45–326a. A PHY XS device that does not implement multi-lane BASE-R PHY XS shall return a zero for all bits in the multi-lane BASE-R PHY XS alignment status ~~3~~ registers 3 through 5. A device that implements multi-lane BASE-R PHY XS shall return a zero for all bits in the multi-lane BASE-R PHY XS alignment status ~~3~~ registers 3 through 5 that are not required for the PHY XS configuration. It is the responsibility of the STA management entity to ensure that a port type is supported by all MMDs before interrogating any of its status bits.

Insert Table 45–326 and Table 45–326a after Table 45–325 as follows (the existing Table 45–326 is deleted from the existing 45.2.4.16 below):

Table 45–326—Multi-lane BASE-R PHY XS alignment status 4 register bit definitions

Bit(s)	Name	Description	R/W[a]
4.53.15	Lane 23 aligned	1 = Lane 23 alignment marker is locked 0 = Lane 23 alignment marker is not locked	RO
4.53.14	Lane 22 aligned	1 = Lane 22 alignment marker is locked 0 = Lane 22 alignment marker is not locked	RO
4.53.13	Lane 21 aligned	1 = Lane 21 alignment marker is locked 0 = Lane 21 alignment marker is not locked	RO
4.53.12	Lane 20 aligned	1 = Lane 20 alignment marker is locked 0 = Lane 20 alignment marker is not locked	RO
4.53.11	Lane 19 aligned	1 = Lane 19 alignment marker is locked 0 = Lane 19 alignment marker is not locked	RO
4.53.10	Lane 18 aligned	1 = Lane 18 alignment marker is locked 0 = Lane 18 alignment marker is not locked	RO
4.53.9	Lane 17 aligned	1 = Lane 17 alignment marker is locked 0 = Lane 17 alignment marker is not locked	RO
4.53.8	Lane 16 aligned	1 = Lane 16 alignment marker is locked 0 = Lane 16 alignment marker is not locked	RO
4.53.7	Lane 15 aligned	1 = Lane 15 alignment marker is locked 0 = Lane 15 alignment marker is not locked	RO
4.53.6	Lane 14 aligned	1 = Lane 14 alignment marker is locked 0 = Lane 14 alignment marker is not locked	RO
4.53.5	Lane 13 aligned	1 = Lane 13 alignment marker is locked 0 = Lane 13 alignment marker is not locked	RO
4.53.4	Lane 12 aligned	1 = Lane 12 alignment marker is locked 0 = Lane 12 alignment marker is not locked	RO
4.53.3	Lane 11 aligned	1 = Lane 11 alignment marker is locked 0 = Lane 11 alignment marker is not locked	RO
4.53.2	Lane 10 aligned	1 = Lane 10 alignment marker is locked 0 = Lane 10 alignment marker is not locked	RO
4.53.1	Lane 9 aligned	1 = Lane 9 alignment marker is locked 0 = Lane 9 alignment marker is not locked	RO
4.53.0	Lane 8 aligned	1 = Lane 8 alignment marker is locked 0 = Lane 8 alignment marker is not locked	RO

[a] RO = Read only.

Table 45–326a—Multi-lane BASE-R PHY XS alignment status 5 register bit definitions

Bit(s)	Name	Description	R/W[a]
4.54.15:8	Reserved	Value always 0	RO
4.54.7	Lane 31 aligned	1 = Lane 31 alignment marker is locked 0 = Lane 31 alignment marker is not locked	RO
4.54.6	Lane 30 aligned	1 = Lane 30 alignment marker is locked 0 = Lane 30 alignment marker is not locked	RO
4.54.5	Lane 29 aligned	1 = Lane 29 alignment marker is locked 0 = Lane 29 alignment marker is not locked	RO
4.54.4	Lane 28 aligned	1 = Lane 28 alignment marker is locked 0 = Lane 28 alignment marker is not locked	RO
4.54.3	Lane 27 aligned	1 = Lane 27 alignment marker is locked 0 = Lane 27 alignment marker is not locked	RO
4.54.2	Lane 26 aligned	1 = Lane 26 alignment marker is locked 0 = Lane 26 alignment marker is not locked	RO
4.54.1	Lane 25 aligned	1 = Lane 25 alignment marker is locked 0 = Lane 25 alignment marker is not locked	RO
4.54.0	Lane 24 aligned	1 = Lane 24 alignment marker is locked 0 = Lane 24 alignment marker is not locked	RO

[a] RO = Read only.

Delete 45.2.4.15.1 to 45.2.4.15.8.

Insert new subclauses 45.2.4.15.1 and 45.2.4.15.2 at the end of 45.2.4.15 as follows:

45.2.4.15.1 Lane 0 aligned (4.52.0)

When read as a one, bit 4.52.0 indicates that the PHY XS receiver has achieved alignment marker lock for service interface lane 0. When read as a zero, bit 4.52.0 indicates that the PHY XS receiver lane 0 has not achieved alignment marker lock. This bit reflects the state of amps_lock[0] (see 119.2.6.2.2 and 172.2.6.2.2).

45.2.4.15.2 Lanes 1 through 31 aligned (bits 4.52.1 through 4.54.7)

The definition of lanes 1 through 31 aligned is identical to that described for lane 0 in 45.2.4.15.1.

The lane aligned status for lanes 1 through 7 is indicated in bits 4.52.1 through 4.52.7, respectively. The lane aligned status for lanes 8 through 23 is indicated in bits 4.53.0 through 4.53.15, respectively. The lane aligned status for lanes 24 through 31 is in bits 4.54.0 through 4.54.7, respectively.

Delete 45.2.4.16 (including its subclauses and the existing Table 45–326).

Insert new subclauses 45.2.4.16 and 45.2.4.16a after 45.2.4.15 as follows:

45.2.4.16 PHY XS RS-FEC codeword counter register (Register 4.300, 4.301, 4.302)

The assignment of bits in the PHY XS RS-FEC codeword counter register is shown in Table 45–326b. The PHY XS RS-FEC codeword counter register applies to the RS-FEC defined in Clause 172. See 172.3.5 for a definition of this counter. It is a 48-bit counter that counts once for each FEC codeword received when align status (4.50.12) is set to one. Its bits are reset to all zeros when the register is read by the management function or upon reset, and held at all ones in the case of overflow.

Registers 4.300, 4.301, and 4.302 are used to read the value of the 48-bit counter. When using these registers to read the 48-bit counter value, the register 4.300 is read first, the values of the registers 4.301 and 4.302 are latched when (and only when) register 4.300 is read, and reads of registers 4.301 and 4.302 return their latched values rather than the current value of the counter.

Table 45–326b—PHY XS RS-FEC codeword counter bit definitions

Bit(s)	Name	Description	R/W[a]
4.300.15:0	RS-FEC codewords lower	FEC_cw_counter[15:0]	RO, NR
4.301.15:0	RS-FEC codewords middle	FEC_cw_counter[31:16]	RO, NR
4.302.15:0	RS-FEC codewords upper	FEC_cw_counter[47:32]	RO, NR

[a] RO = Read only, NR = Non Roll-over.

45.2.4.16a PHY XS RS-FEC codeword error bin registers 1 through 15 (Registers 4.340 through 4.369)

The assignment of bits in the PHY XS RS-FEC codeword error bin 1 register is shown in Table 45–326c. The assignment of bits in the other PHY XS RS-FEC codeword error bin registers is identical to that of bin 1. The RS-FEC codeword error bin registers increment depending upon the error signature of a corrected codeword (see 172.3.6). Their bits are reset to all zeros when the register is read by the management function or upon reset, and held at all ones in the case of overflow.

Two registers are used to read the value of each 32-bit counter, the value of the second register is latched when the first register is read. For example when registers 4.340 and 4.341 are used to read the 32-bit counter value of FEC_codeword_error_bin_1, the register 4.340 is read first, the value of the register 4.341 is latched when (and only when) register 4.340 is read, and reads of register 4.341 return the latched value rather than the current value of the counter.

Table 45–326c—PHY XS RS-FEC codeword error bin 1 bit definitions

Bit(s)	Name	Description	R/W[a]
4.340.15:0	RS-FEC codeword error bin 1 lower	FEC_codeword_error_bin_1[15:0]	RO, NR
4.341.15:0	RS-FEC codeword error bin 1 upper	FEC_codeword_error_bin_1[31:16]	RO, NR

[a] RO = Read only, NR = Non Roll-over.

45.2.4.17 PHY XS lane mapping, lane 0 register (Register 4.400)

Change the text of 45.2.4.17 as follows (Table 45–327 remains unchanged):

The assignment of bits in the PHY XS lane mapping, lane 0 register is shown in Table 45–327. When the multi-lane PHY XS described in Clause 118 and Clause 171 detects and locks the alignment marker for service interface lane 0, the detected PCS lane number is recorded in this register. The contents of the PHY XS lane mapping, lane 0 register is valid when Lane 0 aligned bit (4.52.0) is set to one and is invalid otherwise.

Change the title and text of 45.2.4.18 as follows:

45.2.4.18 PHY XS lane mapping, lane 1 through lane 31 ~~15~~ registers (Registers 4.401 through 4.431~~415~~)

The definition of the PHY XS lane mapping, lane 1 through 31 ~~15~~ registers is identical to that described for lane 0 in 45.2.4.17. The lane mapping for lane 1 is in register 4.401; lane 2 is in register 4.402; etc.

45.2.4.19 PHY XS FEC symbol error counter lane 0 (Register 4.600, 4.601)

Change the text of 45.2.4.19 as follows (Table 45–328 remains unchanged):

The assignment of bits in the PHY XS FEC symbol error counter lane 0 register is shown in Table 45–328. See 119.3.4 and 172.3.4 for a definition of this counter. Symbol errors detected in PHY XS FEC lane 0 are counted and shown in register 4.600.15:0 and 4.601.15:0. These bits shall be reset to all zeros when the register is read by the management function or upon PHY reset. These bits shall be held at all ones in the case of overflow. Registers 4.600~~,~~ and 4.601 are used to read the value of a 32-bit counter. When registers 4.600 and 4.601 are used to read the 32-bit counter value, the register 4.600 is read first, the value of the register 4.601 is latched when (and only when) register 4.600 is read, and reads of register 4.601 return the latched value rather than the current value of the counter.

Change the title and text of 45.2.4.20 as follows:

45.2.4.20 PHY XS FEC symbol error counter lane 1 through 31 ~~15~~ (Registers 4.602 through 4.663~~631~~)

The behavior of the PHY XS FEC symbol error counters, lane 1 through 31 ~~15~~ is identical to that described for PHY XS FEC lane 0 in 45.2.4.19. Errors detected in each PHY XS FEC lane are counted and shown in the corresponding register. PHY XS FEC lane 1, lower 16 bits are shown in register 4.602; PHY XS FEC lane 1, upper 16 bits are shown in register 4.603; PHY XS FEC lane 2, lower 16 bits are shown in register 4.604; through register 4.663~~631~~ for PHY XS FEC lane 31 ~~15~~, upper 16 bits.

45.2.4.21 PHY XS FEC control register (Register 4.800)

45.2.4.21.1 PHY XS FEC degraded SER enable (4.800.2)

Change 45.2.4.21.1 as follows:

This bit enables the PHY XS FEC decoder to signal the presence of a degraded SER. When set to a one, this bit enables degraded SER signaling. When set to a zero, degraded SER signaling is disabled. Writes to this bit are ignored and reads return a zero if the PHY XS FEC does not have the ability to signal the presence of a degraded SER (see 119.2.5.3 and 172.2.5.3 for equivalent PCS behavior).

45.2.4.21.2 PHY XS FEC bypass indication enable (4.800.1)

Change 45.2.4.21.2 as follows:

This bit enables the PHY XS FEC decoder to bypass error indication to the upper layers through the sync bits. When set to a one, this bit enables bypass of the error indication. When set to a zero, errors are indicated to the upper layers through the sync bits. Writes to this bit are ignored and reads return a zero if the PHY XS FEC does not have the ability to bypass indicating decoding errors (see 119.2.5.3 and 172.2.5.3 for equivalent PCS behavior).

45.2.4.22 PHY XS FEC status register (Register 4.801)

Change the rows for bits 4.801.15:6 in Table 45–330 as follows (unchanged rows not shown):

Table 45–330—PHY XS FEC status register bit definitions

Bit(s)	Name	Description	R/W[a]
4.801.15:7 ~~6~~	Reserved	Value always 0	RO
4.801.6	Local degraded SER received	1 = local degraded SER received 0 = no local degraded SER received	RO
…			

[a] RO = Read only, LH = Latching high.

Insert 45.2.4.22.a before 45.2.4.22.1 as follows:

45.2.4.22.a Local degraded SER received (4.801.6)

When read as a one, bit 4.801.6 indicates that the local degraded SER signal has been received. This bit reflects the state of rx_local_degraded for the PHY XS (see 119.2.6.2.2 and 172.2.6.2.2 for equivalent PCS behavior).

Change 45.2.4.22.1 to 45.2.4.22.5 as follows:

45.2.4.22.1 Remote degraded SER received (4.801.5)

When read as a one, bit 4.801.5 indicates that the remote degraded SER signal has been received. This bit reflects the state of rx_rm_degraded for the PHY XS (see 119.2.6.2.2 and 172.2.6.2.2 for equivalent PCS behavior).

45.2.4.22.2 PHY XS FEC degraded SER (4.801.4)

When PHY XS FEC degraded SER enable (bit 4.800.2) is set to one, bit 4.801.4 is set to one if the number of FEC symbol errors in a window of PHY XS FEC degraded SER interval (registers 4.810 and 4.811) codewords exceeds the PHY XS FEC degraded SER activate threshold (registers 4.806 and 4.807) and is cleared if the number of FEC symbol errors in the same window is below the PHY XS FEC degraded SER deactivate threshold (registers 4.808 and 4.809). If the number of FEC symbol errors in the window is between the two thresholds, then bit 4.801.4 remains in its previous state. The bit is set to zero if PHY XS FEC degraded SER enable (bit 4.800.2) is set to zero (see 119.2.5.3 and 172.2.5.3 for equivalent PCS

behavior). The value of bit 4.801.4 is undefined if the value of the PHY XS FEC degraded SER activate threshold is less than the value of the PHY XS FEC degraded SER deactivate threshold.

45.2.4.22.3 PHY XS FEC degraded SER ability (4.801.3)

The PHY XS FEC decoder may have the option to signal the presence of a degraded SER (see 119.2.5.3 and 172.2.5.3 for equivalent PCS behavior). This bit is set to one to indicate that the decoder has the ability to signal the presence of a degraded SER. The bit is set to zero if this ability is not supported.

45.2.4.22.4 PHY XS FEC high SER (4.801.2)

When PHY XS FEC bypass indication enable (bit 4.800.1) is set to one, this bit is set to one if the number of FEC symbol errors in a window of 8192 codewords exceeds the threshold (see 119.2.5.3 and 172.2.5.3 for equivalent PCS behavior) and is set to zero otherwise. The bit is set to zero if PHY XS FEC bypass indication enable (bit 4.800.1) is set to zero. This bit shall be implemented with latching high behavior.

45.2.4.22.5 PHY XS FEC bypass indication ability (4.801.1)

The PHY XS FEC decoder may have the option to perform error detection without error indication (see 119.2.5.3 and 172.2.5.3 for equivalent PCS behavior) to reduce the delay contributed by the FEC decoder. This bit is set to one to indicate that the decoder has this ability to bypass error indication. The bit is set to zero if this ability is not supported.

Change the text of 45.2.4.23 to 45.2.4.27 as follows (Table 45–331 to Table 45–335 remain unchanged):

45.2.4.23 PHY XS FEC corrected codewords counter (Register 4.802, 4.803)

The assignment of bits in the PHY XS FEC corrected codewords counter register is shown in Table 45–331. See 119.3.2 and 172.3.2 for a definition of this counter. These bits shall be reset to all zeros when the register is read by the management function or upon PHY reset. These bits shall be held at all ones in the case of overflow. Registers 4.802~~,~~ and 4.803 are used to read the value of a 32-bit counter. When registers 4.802 and 4.803 are used to read the 32-bit counter value, the register 4.802 is read first, the value of the register 4.803 is latched when (and only when) register 4.802 is read, and reads of register 4.803 return the latched value rather than the current value of the counter.

45.2.4.24 PHY XS FEC uncorrected codewords counter (Register 4.804, 4.805)

The assignment of bits in the PHY XS FEC uncorrected codewords counter register is shown in Table 45–332. See 119.3.3 and 172.3.3 for a definition of this counter. These bits shall be reset to all zeros when the register is read by the management function or upon PHY reset. These bits shall be held at all ones in the case of overflow. Registers 4.804~~,~~ and 4.805 are used to read the value of a 32-bit counter. When registers 4.804 and 4.805 are used to read the 32-bit counter value, the register 4.804 is read first, the value of the register 4.805 is latched when (and only when) register 4.804 is read, and reads of register 4.805 return the latched value rather than the current value of the counter.

45.2.4.25 PHY XS FEC degraded SER activate threshold register (Register 4.806, 4.807)

The assignment of bits in the PHY XS FEC degraded SER activate threshold register is shown in Table 45–333. The value controls the threshold used to set the PHY XS FEC degraded SER bit (4.801.4) in an equivalent manner to that defined for the FEC_degraded_SER bit in 119.2.5.3 and 172.2.5.3.

45.2.4.26 PHY XS FEC degraded SER deactivate threshold register (Register 4.808, 4.809)

The assignment of bits in the PHY XS FEC degraded SER deactivate threshold register is shown in Table 45–334. The value controls the threshold used to clear the PHY XS FEC degraded SER bit (4.801.4) in an equivalent manner to that defined for the FEC_degraded_SER bit in 119.2.5.3 and 172.2.5.3.

45.2.4.27 PHY XS FEC degraded SER interval register (Register 4.810, 4.811)

The assignment of bits in the PHY XS FEC degraded SER interval register is shown in Table 45–335. The value controls the interval used to set and clear the PHY XS FEC degraded SER bit (4.801.4) in an equivalent manner to that defined for the FEC_degraded_SER bit in 119.2.5.3 and 172.2.5.3.

45.2.5 DTE XS registers

Change the rows for registers 5.52 to 5.799 in Table 45–339 as follows (unchanged rows not shown):

Table 45–339—DTE XS registers

Register address	Register name	Subclause
…		
5.52 through 5.54	Multi-lane BASE-R DTE XS alignment status 3 through 5	45.2.5.15
~~5.53~~	~~Multi-lane BASE-R DTE XS alignment status 4~~	~~45.2.5.16~~
~~5.54~~ 5.55 through 5.299	Reserved	
5.300 through 5.302	DTE XS RS-FEC codeword counter	45.2.5.16
5.303 through 5.339	Reserved	
5.340 through 5.369	DTE XS RS-FEC codeword error bin 1 through 15	45.2.5.16a
5.370 through 5.399	Reserved	
~~5.400 through 5.415~~ 5.400 through 5.431	DTE XS lane mapping, lane 0 through 31~~15~~	45.2.5.17, 45.2.5.18
~~5.415 through 5.599~~ 5.432 through 5.599	Reserved	
~~5.600 through 5.631~~ 5.600 through 5.663	DTE XS FEC symbol error counter, lane 0 to 31~~15~~	45.2.5.19, 45.2.5.20
~~5.632 through 5.799~~ 5.664 through 5.799	Reserved	
…		

45.2.5.4 DTE XS speed ability (Register 5.4)

Change the row for bits 5.4.15:10 in Table 45–342 as follows (unchanged rows not shown):

Table 45–342— DTE XS speed ability register bit definitions

Bit(s)	Name	Description	R/W[a]
5.4.15:11 ~~10~~	Reserved	Value always 0	RO
5.4.10	800G capable	1 = DTE XS is capable of operating at 800 Gb/s 0 = DTE XS is not capable of operating at 800 Gb/s	RO
…			

[a] RO = Read only,

Insert 45.2.5.4.a before 45.2.5.4.1 as follows:

45.2.5.4.a 800G capable (5.4.10)

When read as a one, bit 5.4.10 indicates that the DTE XS is able to operate at a data rate of 800 Gb/s. When read as a zero, bit 5.4.10 indicates that the DTE XS is not able to operate at a data rate of 800 Gb/s.

Change the title and text of 45.2.5.15 as follows (Table 45–350 remains unchanged):

45.2.5.15 Multi-lane BASE-R PHY DTE alignment status ~~3~~ registers 3 through 5 (Register 5.52, 5.53, 5.54)

The assignment of bits in the multi-lane BASE-R DTE XS alignment status ~~3~~ registers 3 through 5 is shown in Table 45-350, Table 45–351, and Table 45–351a. A DTE XS device that does not implement multi-lane BASE-R DTE XS shall return a zero for all bits in the multi-lane BASE-R DTE XS alignment status ~~3~~ registers 3 through 5. A device that implements multi-lane BASE-R DTE XS shall return a zero for all bits in the multi-lane BASE-R DTE XS alignment status ~~3~~ registers 3 through 5 that are not required for the DTE XS configuration. It is the responsibility of the STA management entity to ensure that a port type is supported by all MMDs before interrogating any of its status bits.

Insert Table 45–351 and Table 45–351a after Table 45–350 as follows (the existing Table 45–351 is deleted from the existing 45.2.4.16 below):

Table 45–351—Multi-lane BASE-R DTE XS alignment status 4 register bit definitions

Bit(s)	Name	Description	R/W[a]
5.53.15	Lane 23 aligned	1 = Lane 23 alignment marker is locked 0 = Lane 23 alignment marker is not locked	RO
5.53.14	Lane 22 aligned	1 = Lane 22 alignment marker is locked 0 = Lane 22 alignment marker is not locked	RO
5.53.13	Lane 21 aligned	1 = Lane 21 alignment marker is locked 0 = Lane 21 alignment marker is not locked	RO
5.53.12	Lane 20 aligned	1 = Lane 20 alignment marker is locked 0 = Lane 20 alignment marker is not locked	RO
5.53.11	Lane 19 aligned	1 = Lane 19 alignment marker is locked 0 = Lane 19 alignment marker is not locked	RO
5.53.10	Lane 18 aligned	1 = Lane 18 alignment marker is locked 0 = Lane 18 alignment marker is not locked	RO
5.53.9	Lane 17 aligned	1 = Lane 17 alignment marker is locked 0 = Lane 17 alignment marker is not locked	RO
5.53.8	Lane 16 aligned	1 = Lane 16 alignment marker is locked 0 = Lane 16 alignment marker is not locked	RO
5.53.7	Lane 15 aligned	1 = Lane 15 alignment marker is locked 0 = Lane 15 alignment marker is not locked	RO
5.53.6	Lane 14 aligned	1 = Lane 14 alignment marker is locked 0 = Lane 14 alignment marker is not locked	RO
5.53.5	Lane 13 aligned	1 = Lane 13 alignment marker is locked 0 = Lane 13 alignment marker is not locked	RO
5.53.4	Lane 12 aligned	1 = Lane 12 alignment marker is locked 0 = Lane 12 alignment marker is not locked	RO
5.53.3	Lane 11 aligned	1 = Lane 11 alignment marker is locked 0 = Lane 11 alignment marker is not locked	RO
5.53.2	Lane 10 aligned	1 = Lane 10 alignment marker is locked 0 = Lane 10 alignment marker is not locked	RO
5.53.1	Lane 9 aligned	1 = Lane 9 alignment marker is locked 0 = Lane 9 alignment marker is not locked	RO
5.53.0	Lane 8 aligned	1 = Lane 8 alignment marker is locked 0 = Lane 8 alignment marker is not locked	RO

[a] RO = Read only.

Table 45–351a—Multi-lane BASE-R DTE XS alignment status 5 register bit definitions

Bit(s)	Name	Description	R/W[a]
4.54.15:8	Reserved	Value always 0	RO
5.54.7	Lane 31 aligned	1 = Lane 31 alignment marker is locked 0 = Lane 31 alignment marker is not locked	RO
5.54.6	Lane 30 aligned	1 = Lane 30 alignment marker is locked 0 = Lane 30 alignment marker is not locked	RO
5.54.5	Lane 29 aligned	1 = Lane 29 alignment marker is locked 0 = Lane 29 alignment marker is not locked	RO
5.54.4	Lane 28 aligned	1 = Lane 28 alignment marker is locked 0 = Lane 28 alignment marker is not locked	RO
5.54.3	Lane 27 aligned	1 = Lane 27 alignment marker is locked 0 = Lane 27 alignment marker is not locked	RO
5.54.2	Lane 26 aligned	1 = Lane 26 alignment marker is locked 0 = Lane 26 alignment marker is not locked	RO
5.54.1	Lane 25 aligned	1 = Lane 25 alignment marker is locked 0 = Lane 25 alignment marker is not locked	RO
5.54.0	Lane 24 aligned	1 = Lane 24 alignment marker is locked 0 = Lane 24 alignment marker is not locked	RO

[a] RO = Read only.

Delete 45.2.5.15.1 to 45.2.5.15.8.

Insert new subclauses 45.2.5.15.1 and 45.2.5.15.2 at the end of 45.2.5.15 as follows:

45.2.5.15.1 Lane 0 aligned (5.52.0)

When read as a one, bit 5.52.0 indicates that the DTE XS receiver has achieved alignment marker lock for service interface lane 0. When read as a zero, bit 5.52.0 indicates that the DTE XS receiver lane 0 has not achieved alignment marker lock. This bit reflects the state of amps_lock[0] (see 119.2.6.2.2 and 172.2.6.2.2).

45.2.5.15.2 Lanes 1 through 31 aligned (bits 4.52.1 through 4.54.7)

The definition of lanes 1 through 31 aligned is identical to that described for lane 0 in 45.2.5.15.1.

The lane aligned status for lanes 1 through 7 is indicated in bits 5.52.1 through 5.52.7, respectively. The lane aligned status for lanes 8 through 23 is indicated in bits 5.53.0 through 5.53.15, respectively. The lane aligned status for lanes 24 through 31 is in bits 5.54.0 through 5.54.7, respectively.

Insert 45.2.5.16 and 45.2.5.16a after 45.2.5.15 as follows:

45.2.5.16 DTE XS RS-FEC codeword counter register (Register 5.300, 5.301, 5.302)

The assignment of bits in the DTE XS RS-FEC codeword counter register is shown in Table 45–351b. The DTE XS RS-FEC codeword counter register applies to the RS-FEC defined in Clause 172. See 172.3.5 for a definition of this counter. It is a 48-bit counter that counts once for each FEC codeword received when align status (5.50.12) is set to one. Its bits are reset to all zeros when the register is read by the management function or upon reset, and held at all ones in the case of overflow.

Registers 5.300, 5.301, and 5.302 are used to read the value of the 48-bit counter. When using these registers to read the 48-bit counter value, the register 5.300 is read first, the values of the registers 5.301 and 5.302 are latched when (and only when) register 5.300 is read, and reads of registers 5.301 and 5.302 return their latched values rather than the current value of the counter.

Table 45–351b—DTE XS RS-FEC codeword counter bit definitions

Bit(s)	Name	Description	R/W[a]
5.300.15:0	RS-FEC codewords lower	FEC_cw_counter[15:0]	RO, NR
5.301.15:0	RS-FEC codewords middle	FEC_cw_counter[31:16]	RO, NR
5.302.15:0	RS-FEC codewords upper	FEC_cw_counter[47:32]	RO, NR

[a] RO = Read only, NR = Non Roll-over.

45.2.5.16a DTE XS RS-FEC codeword error bin registers 1 through 15 (Registers 5.340 through 5.369)

The assignment of bits in the DTE XS RS-FEC codeword error bin 1 register is shown in Table 45–351c. The assignment of bits in the other DTE XS RS-FEC codeword error bin registers is identical to that of bin 1. The RS-FEC codeword error bin registers increment depending upon the error signature of a corrected codeword (see 172.3.6). Their bits are reset to all zeros when the register is read by the management function or upon reset, and held at all ones in the case of overflow.

Two registers are used to read the value of each 32-bit counter, the value of the second register is latched when the first register is read. For example when registers 5.340 and 5.341 are used to read the 32-bit counter value of FEC_codeword_error_bin_1, the register 5.340 is read first, the value of the register 5.341 is latched when (and only when) register 5.340 is read, and reads of register 5.341 return the latched value rather than the current value of the counter.

Table 45–351c—DTE XS RS-FEC codeword error bin 1 bit definitions

Bit(s)	Name	Description	R/W[a]
5.340.15:0	RS-FEC codeword error bin 1 lower	FEC_codeword_error_bin_1[15:0]	RO, NR
5.341.15:0	RS-FEC codeword error bin 1 upper	FEC_codeword_error_bin_1[31:16]	RO, NR

[a] RO = Read only, NR = Non Roll-over.

45.2.5.17 DTE XS lane mapping, lane 0 register (Register 5.400)

Change the text of 45.2.5.17 as follows (Table 45–352 remains unchanged):

The assignment of bits in the DTE XS lane mapping, lane 0 register is shown in Table 45–352. When the multi-lane DTE XS described in Clause 118 and Clause 171 detects and locks the alignment marker for service interface lane 0, the detected PCS lane number is recorded in this register. The contents of the DTE XS lane mapping, lane 0 register is valid when Lane 0 aligned bit (5.52.0) is set to one and is invalid otherwise.

Change the title and text of 45.2.5.18 as follows:

45.2.5.18 DTE XS lane mapping, lane 1 through lane 31 ~~15~~ registers (Registers 5.401 through 5.431~~415~~)

The definition of the DTE XS lane mapping, lane 1 through 31 ~~15~~ registers is identical to that described for lane 0 in 45.2.5.17. The lane mapping for lane 1 is in register 5.401; lane 2 is in register 5.402; etc.

45.2.5.19 DTE XS FEC symbol error counter lane 0 (Register 5.600, 5.601)

Change the text of 45.2.5.19 as follows (Table 45–353 remains unchanged):

The assignment of bits in the DTE XS FEC symbol error counter lane 0 register is shown in Table 45–353. See 119.3.4 and 172.3.4 for a definition of this counter. Symbol errors detected in DTE XS FEC lane 0 are counted and shown in register 5.600.15:0 and 5.601.15:0. These bits shall be reset to all zeros when the register is read by the management function or upon PHY reset. These bits shall be held at all ones in the case of overflow. Registers 5.600~~,~~ and 5.601 are used to read the value of a 32-bit counter. When registers 5.600 and 5.601 are used to read the 32-bit counter value, the register 5.600 is read first, the value of the register 5.601 is latched when (and only when) register 5.600 is read, and reads of register 5.601 return the latched value rather than the current value of the counter.

Change the title and text of 45.2.5.20 as follows:

45.2.5.20 DTE XS FEC symbol error counter lane 1 through 31 ~~15~~ (Registers 5.602 through 5.663~~631~~)

The behavior of the DTE XS FEC symbol error counters, lane 1 through 31 ~~15~~ is identical to that described for DTE XS FEC lane 0 in 45.2.5.19. Errors detected in each DTE XS FEC lane are counted and shown in the corresponding register. DTE XS FEC lane 1, lower 16 bits are shown in register 5.602; DTE XS FEC lane 1, upper 16 bits are shown in register 5.603; DTE XS FEC lane 2, lower 16 bits are shown in register 5.604; through register 5.663~~631~~ for DTE XS FEC lane 31 ~~15~~, upper 16 bits.

45.2.5.21 DTE XS FEC control register (Register 5.800)

45.2.5.21.1 DTE XS FEC degraded SER enable (5.800.2)

Change 45.2.5.21.1 as follows:

This bit enables the DTE XS FEC decoder to signal the presence of a degraded SER. When set to a one, this bit enables degraded SER signaling. When set to a zero, degraded SER signaling is disabled. Writes to this bit are ignored and reads return a zero if the DTE XS FEC does not have the ability to signal the presence of a degraded SER (see 119.2.5.3 and 172.2.5.3 for equivalent PCS behavior).

45.2.5.21.2 DTE XS FEC bypass indication enable (5.800.1)

Change 45.2.5.21.2 as follows:

This bit enables the DTE XS FEC decoder to bypass error indication to the upper layers through the sync bits. When set to a one, this bit enables bypass of the error indication. When set to a zero, errors are indicated to the upper layers through the sync bits. Writes to this bit are ignored and reads return a zero if the DTE XS FEC does not have the ability to bypass indicating decoding errors (see 119.2.5.3 and 172.2.5.3 for equivalent PCS behavior).

45.2.5.22 DTE XS FEC status register (Register 5.801)

Change 45.2.5.22.1 to 45.2.5.22.5 as follows:

45.2.5.22.1 Local degraded SER received (5.801.6)

When read as a one, bit 5.801.6 indicates that the local degraded SER signal has been received. This bit reflects the state of rx_local_degraded (see 118.2.1 and 172.2.6.2.2) for the DTE XS.

45.2.5.22.2 Remote degraded SER received (5.801.5)

When read as a one, bit 5.801.5 indicates that the remote degraded SER signal has been received. This bit reflects the state of rx_rm_degraded for the DTE XS (see 119.2.5.3 and 172.2.5.3 for equivalent PCS behavior).

45.2.5.22.3 DTE XS FEC degraded SER (5.801.4)

When DTE XS FEC degraded SER enable (bit 5.800.2) is set to one, bit 5.801.4 is set to one if the number of FEC symbol errors in a window of DTE XS FEC degraded SER interval (registers 5.810 and 5.811) codewords exceeds the DTE XS FEC degraded SER activate threshold (registers 5.806 and 5.807) and is cleared if the number of FEC symbol errors in the same window is below the DTE XS FEC degraded SER deactivate threshold (registers 5.808 and 5.809). If the number of FEC symbol errors in the window is between the two thresholds, then bit 5.801.4 remains in its previous state. The bit is set to zero if DTE XS FEC degraded SER enable (bit 5.800.2) is set to zero (see 119.2.5.3 and 172.2.5.3 for equivalent PCS behavior). The value of bit 5.801.4 is undefined if the value of the DTE XS FEC degraded SER activate threshold is less than the value of the DTE XS FEC degraded SER deactivate threshold.

45.2.5.22.4 DTE XS FEC degraded SER ability (5.801.3)

The DTE XS FEC decoder may have the option to signal the presence of a degraded SER (see 119.2.5.3 and 172.2.5.3 for equivalent PCS behavior). This bit is set to one to indicate that the decoder has the ability to signal the presence of a degraded SER. The bit is set to zero if this ability is not supported.

45.2.5.22.5 DTE XS FEC high SER (5.801.2)

When DTE XS FEC bypass indication enable (bit 5.800.1) is set to one, this bit is set to one if the number of FEC symbol errors in a window of 8192 codewords exceeds the threshold (see 119.2.5.3 and 172.2.5.3) and is set to zero otherwise. The bit is set to zero if DTE XS FEC bypass indication enable (bit 5.800.1) is set to zero. This bit shall be implemented with latching high behavior.

Change the text of 45.2.5.23 to 45.2.5.27 as follows (Table 45–356 to Table 45–360 remain unchanged):

45.2.5.23 DTE XS FEC corrected codewords counter (Register 5.802, 5.803)

The assignment of bits in the DTE XS FEC corrected codewords counter register is shown in Table 45–356. See 119.3.2 and 172.3.2 for a definition of this counter. These bits shall be reset to all zeros when the register is read by the management function or upon PHY reset. These bits shall be held at all ones in the case of overflow. Registers 5.802~~,~~ and 5.803 are used to read the value of a 32-bit counter. When registers 5.802 and 5.803 are used to read the 32-bit counter value, the register 5.802 is read first, the value of the register 5.803 is latched when (and only when) register 5.802 is read, and reads of register 5.803 return the latched value rather than the current value of the counter.

45.2.5.24 DTE XS FEC uncorrected codewords counter (Register 5.804, 5.805)

The assignment of bits in the DTE XS FEC uncorrected codewords counter register is shown in Table 45–357. See 119.3.3 and 172.3.3 for a definition of this counter. These bits shall be reset to all zeros when the register is read by the management function or upon PHY reset. These bits shall be held at all ones in the case of overflow. Registers 5.804~~,~~ and 5.805 are used to read the value of a 32-bit counter. When registers 5.804 and 5.805 are used to read the 32-bit counter value, the register 5.804 is read first, the value of the register 5.805 is latched when (and only when) register 5.804 is read, and reads of register 5.805 return the latched value rather than the current value of the counter.

45.2.5.25 DTE XS FEC degraded SER activate threshold register (Register 5.806, 5.807)

The assignment of bits in the DTE XS FEC degraded SER activate threshold register is shown in Table 45–358. The value controls the threshold used to set the DTE XS FEC degraded SER bit (5.801.4) in an equivalent manner to that defined for the FEC_degraded_SER bit in 119.2.5.3 and 172.2.5.3.

45.2.5.26 DTE XS FEC degraded SER deactivate threshold register (Register 5.808, 5.809)

The assignment of bits in the DTE XS FEC degraded SER deactivate threshold register is shown in Table 45–359. The value controls the threshold used to clear the DTE XS FEC degraded SER bit (5.801.4) in an equivalent manner to that defined for the FEC_degraded_SER bit in 119.2.5.3 and 172.2.5.3.

45.2.5.27 DTE XS FEC degraded SER interval register (Register 5.810, 5.811)

The assignment of bits in the DTE XS FEC degraded SER interval register is shown in Table 45–360. The value controls the interval used to set and clear the DTE XS FEC degraded SER bit (5.801.4) in an equivalent manner to that defined for the FEC_degraded_SER bit in 119.2.5.3 and 172.2.5.3.

45.2.7 Auto-Negotiation registers

45.2.7.12 Backplane Ethernet, BASE-R copper status (Register 7.48)

Change the title of 45.2.7.12.3 (as amended by IEEE Std 802.3ck-2022) as follows:

45.2.7.12.3 Negotiated Port Type (7.48.1, 7.48.2, 7.48.3, 7.48.5, 7.48.6, 7.48.8, 7.48.9, 7.48.10, 7.48.11, 7.48.12, 7.48.13, 7.48.14, 7.48.15, 7.49.0, 7.49.1, 7.49.2, 7.49.3, 7.49.4, 7.49.5, 7.49.7)

45.2.7.13 Backplane Ethernet, BASE-R copper status 2 (Register 7.49)

Change the rows for bits 7.49.15:7 in Table 45–388 (as amended by IEEE Std 802.3ck-2022) as follows (unchanged rows not shown):

Table 45–388—Backplane Ethernet, BASE-R copper status 2 register (Register 7.49) bit definitions

Bit(s)	Name	Description	RO[a]
7.49.15:8 ~~7.49.15:7~~	Reserved	Value always 0	RO
7.49.7	800GBASE-KR8 or 800GBASE-CR8	1 = PMA/PMD is negotiated to perform 800GBASE-KR8 or 800GBASE-CR8 0 = PMA/PMD is not negotiated to perform 800GBASE-KR8 or 800GBASE-CR8	RO
…			

[a] RO = Read only.

69. Introduction to Ethernet operation over electrical backplanes

69.1 Overview

69.1.1 Scope

Change the second paragraph of 69.1.1 (as amended by IEEE Std 802.3ck-2022) as follows:

Backplane Ethernet supports the IEEE 802.3 full duplex MAC operating at 1000 Mb/s, 2.5 Gb/s, 5 Gb/s, 10 Gb/s, 25 Gb/s, 40 Gb/s, 50 Gb/s, 100 Gb/s, 200 Gb/s, ~~or~~ 400 Gb/s, or 800 Gb/s. The following Physical Layers are supported:

Change the dashed list after the second paragraph of 69.1.1 (as amended by IEEE Std 802.3ck-2022) as follows:

- 1000BASE-KX for 1 Gb/s operation over a single lane
- 2.5GBASE-KX for 2.5 Gb/s operation over a single lane
- 5GBASE-KR for 5 Gb/s operation over a single lane
- 10GBASE-KX4 for 10 Gb/s operation over four lanes
- 10GBASE-KR for 10 Gb/s operation over a single lane
- 25GBASE-KR and 25GBASE-KR-S for 25 Gb/s operation over a single lane
- 40GBASE-KR4 for 40 Gb/s operation over four lanes
- 50GBASE-KR for 50 Gb/s operation over a single lane
- 100GBASE-KR4 and 100GBASE-KP4 for 100 Gb/s operation over four lanes
- 100GBASE-KR2 for 100 Gb/s operation over two lanes
- 100GBASE-KR1 for 100 Gb/s operation over one lane
- 200GBASE-KR4 for 200 Gb/s operation over four lanes
- 200GBASE-KR2 for 200 Gb/s operation over two lanes
- 400GBASE-KR4 for 400 Gb/s operation over four lanes
- 800GBASE-KR8 for 800 Gb/s operation over eight lanes

69.1.2 Relationship of Backplane Ethernet to the ISO OSI reference model

Replace Figure 69–5 (as amended by IEEE Std 802.3ck-2022) with the following figure:

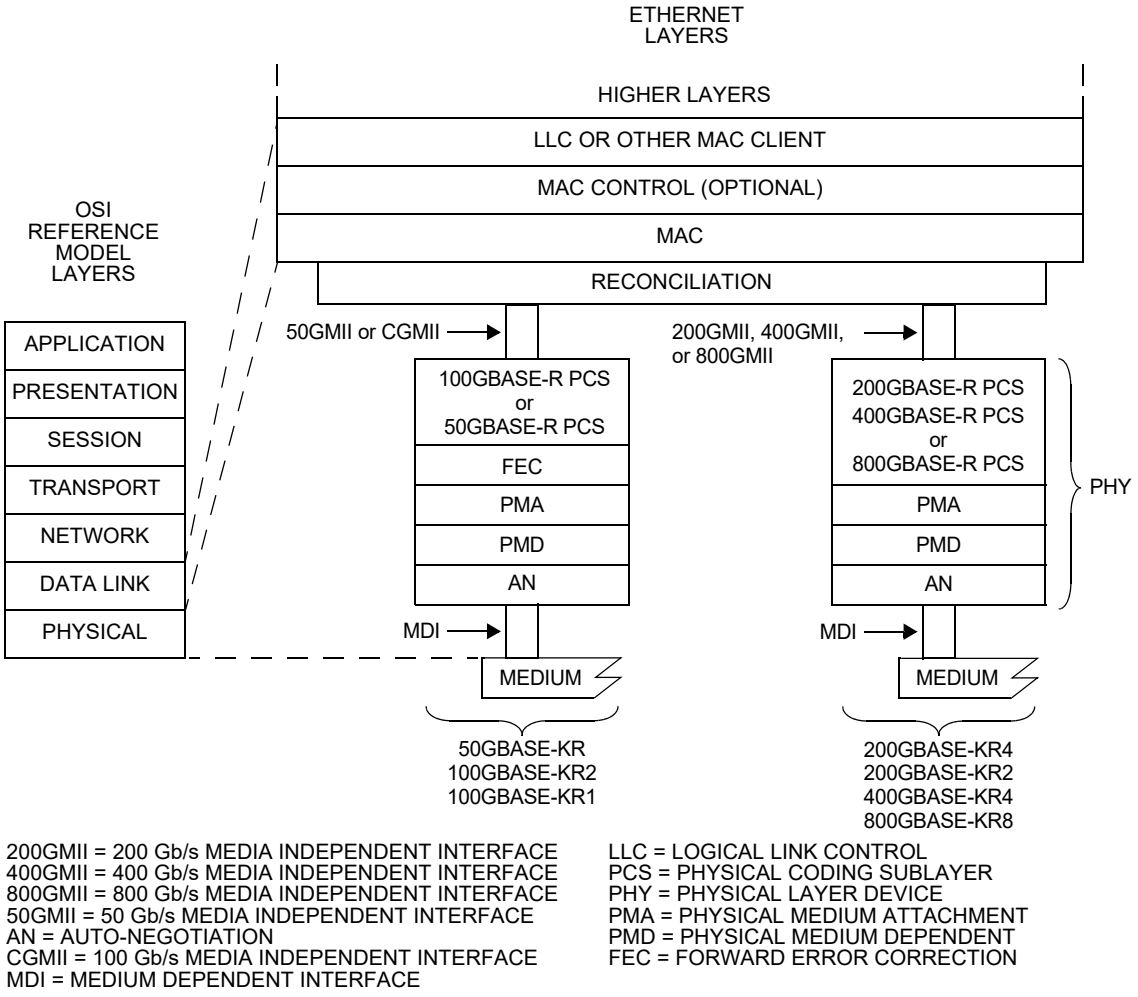


Figure 69–5—Architectural positioning of 50 Gb/s, 100 Gb/s, 200 Gb/s, 400 Gb/s, and 800 Gb/s PAM4 Backplane Ethernet

69.2 Summary of Backplane Ethernet Sublayers

69.2.1 Reconciliation sublayer and media independent interfaces

Change 69.2.1 (as amended by IEEE Std 802.3ck-2022) as follows:

The Clause 35 RS and GMII, the Clause 46 RS and XGMII, the Clause 106 RS and 25GMII, the Clause 81 RS, XLGMII, and CGMII, the Clause 132 RS and 50GMII, ~~and~~ the Clause 117 RS, 200GMII, and 400GMII, and the Clause 170 RS and 800GMII are employed for the same purpose in Backplane Ethernet, that being the interconnection between the MAC sublayer and the PHY.

69.2.3 Physical Layer signaling systems

Change the 11th paragraph in 69.2.3 (as inserted by IEEE Std 802.3ck-2022) as follows:

Backplane Ethernet also specifies 100GBASE-KR1, 200GBASE-KR2, ~~and~~ 400GBASE-KR4, and 800GBASE-KR8. The 100GBASE-KR1 embodiment employs the PCS defined in Clause 82, the RS-FEC defined in Clause 91, the RS-FEC-Int defined in Clause 161, the PMA defined in Clause 135, and the PMD defined in Clause 163, and specifies 100 Gb/s operation using 4-level PAM over one differential path in each direction. The 200GBASE-KR2 embodiment employs the PCS defined in Clause 119, the PMA defined in Clause 120, and the PMD defined in Clause 163, and specifies 200 Gb/s operation using 4-level PAM over two differential paths in each direction. The 400GBASE-KR4 embodiment employs the PCS defined in Clause 119, the PMA defined in Clause 120, and the PMD defined in Clause 163, and specifies 400 Gb/s operation using 4-level PAM over four differential paths in each direction. The 800GBASE-KR8 embodiment employs the PCS defined in Clause 172, the PMA defined in Clause 173, and the PMD defined in Clause 163, and specifies 800 Gb/s operation using 4-level PAM over eight differential paths in each direction.

Change the last paragraph in 69.2.3 (as amended by IEEE Std 802.3ck-2022) as follows:

Table 69–1 specifies the correlation between nomenclature and clauses for 1 Gb/s and 10 Gb/s backplane Ethernet. For other backplane PHY types, refer to Table 125–2 (2.5 Gb/s and 5 Gb/s), Table 105–1 (25 Gb/s), Table 80–2 (40 Gb/s), Table 131–2 (50 Gb/s), Table 80–3 (100 Gb/s), Table 116–3 (200 Gb/s), ~~and~~ Table 116–3a (400 Gb/s), and Table 169–2 (800 Gb/s).

69.3 Delay constraints

Insert the following new paragraph into 69.3 after the now 13th paragraph "For 200GBASE-KR2…" (as inserted by IEEE Std 802.3ck-2022):

For 800GBASE-KR8, normative delay specifications may be found in 170.1.4, 172.5, 173.5.4, and 163.5, and also referenced in 169.4.

69.5 Protocol implementation conformance statement (PICS) proforma

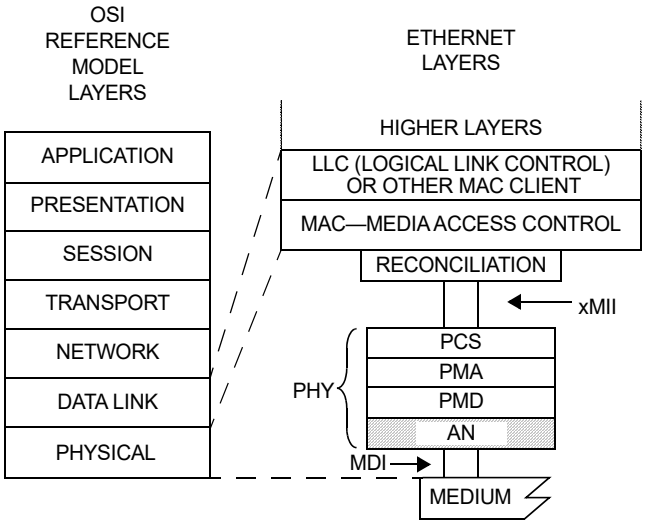
Change the first paragraph of 69.5 (as amended by IEEE Std 802.3ck-2022) as follows:

The supplier of a protocol implementation that is claimed to conform to any part of IEEE Std 802.3, Clause 70 through Clause 74, Clause 84, Clause 91, Clause 93, Clause 94, Clause 108, Clause 111, Clause 119, Clause 128, Clause 130, Clause 134, Clause 137, Clause 161, Clause 163, Clause 172, and related annexes demonstrates compliance by completing a protocol implementation conformance statement (PICS) proforma.

73. Auto-Negotiation for backplane and copper cable assembly

73.2 Relationship to the ISO/IEC Open Systems Interconnection (OSI) reference model

Replace Figure 73–1 (as amended by IEEE Std 802.3ck-2022) with the following figure:



xMII = GENERIC MEDIA INDEPENDENT INTERFACE
AN = AUTO-NEGOTIATION
MDI = MEDIUM DEPENDENT INTERFACE
PCS = PHYSICAL CODING SUBLAYER
PHY = PHYSICAL LAYER DEVICE
PMA = PHYSICAL MEDIUM ATTACHMENT
PMD = PHYSICAL MEDIUM DEPENDENT

Figure 73–1—Location of Auto-Negotiation function within the ISO/IEC OSI reference model

73.6 Link codeword encoding

73.6.4 Technology Ability Field

Change Table 73–4 (as amended by IEEE Std 802.3ck-2022) as follows (some unchanged rows not shown):

Table 73–4—Technology Ability Field encoding

Bit	Technology
…	
A18	400GBASE-KR4 or 400GBASE-CR4
A19	800GBASE-KR8 or 800GBASE-CR8
~~A19~~A20 through A21	Reserved

Change the last paragraph of 73.6.4 (as amended by IEEE Std 802.3ck-2022) as follows:

The fields A[21:20~~19~~] are reserved for future use. Reserved fields shall be sent as zero and ignored on receive.

73.7 Receive function requirements

73.7.6 Priority Resolution function

Replace Table 73–5 (as amended by IEEE Std 802.3ck-2022) with the following table:

Table 73–5—Priority Resolution

Technology	Capability
800GBASE-KR8 or 800GBASE-CR8	800 Gb/s 8 lane, highest priority
400GBASE-KR4 or 400GBASE-CR4	400 Gb/s 4 lane
200GBASE-KR2 or 200GBASE-CR2	200 Gb/s 2 lane
200GBASE-KR4 or 200GBASE-CR4	200 Gb/s 4 lane
100GBASE-KR1 or 100GBASE-CR1	100 Gb/s 1 lane
100GBASE-KR2 or 100GBASE-CR2	100 Gb/s 2 lane
100GBASE-CR4	100 Gb/s 4 lane
100GBASE-KR4	100 Gb/s 4 lane
100GBASE-KP4	100 Gb/s 4 lane
100GBASE-CR10	100 Gb/s 10 lane
50GBASE-KR or 50GBASE-CR	50 Gb/s 1 lane
40GBASE-CR4	40 Gb/s 4 lane
40GBASE-KR4	40 Gb/s 4 lane
25GBASE-KR or 25GBASE-CR	25 Gb/s 1 lane
25GBASE-KR-S or 25GBASE-CR-S	25 Gb/s 1 lane, short reach
10GBASE-KR	10 Gb/s 1 lane
10GBASE-KX4	10 Gb/s 4 lane
5GBASE-KR	5 Gb/s 1 lane
2.5GBASE-KX	2.5 Gb/s 1 lane
1000BASE-KX	1 Gb/s 1 lane, lowest priority

73.10 State diagrams and variable definitions

73.10.1 State diagram variables

Insert the following new entry into the list below the first paragraph of 73.10.1 (as amended by IEEE Std 802.3ck-2022) after the "400GR4" entry:

800GR8; represents the 800GBASE-KR8 or 800GBASE-CR8 PMD.

Change the entry for single_link_ready in 73.10.1 (as amended by IEEE Std 802.3ck-2022) as follows:

single_link_ready

Status indicating that an_receive_idle = true and only one of the following indications is being received:

1) link_status_[1GKX] = OK
2) link_status_[2.5GKX] = OK
3) link_status_[5GKR] = OK
4) link_status_[10GKX4] = OK
5) link_status_[10GKR] = OK
6) link_status_[25GR] = OK
7) link_status_[40GKR4] = OK
8) link_status_[40GCR4] = OK
9) link_status_[50GR] = OK
10) link_status_[100GCR10] = OK
11) link_status_[100GKP4] = OK
12) link_status_[100GKR4] = OK
13) link_status_[100GCR4] = OK
14) link_status_[100GR2] = OK
15) link_status_[100GR1] = OK
16) link_status_[200GR4] = OK
17) link_status_[200GR2] = OK
18) link_status_[400GR4] = OK
19) link_status_[800GR8] = OK

73.10.2 State diagram timers

Change Table 73–7 (as amended by IEEE Std 802.3ck-2022) as follows (some unchanged rows not shown):

Table 73–7—Timer min/max value summary

Parameter	Min	Value and tolerance	Max	Units
…				
interval_timer		3.2 ± 0.01%		ns
link_fail_inhibit_timer (when the link is 100GBASE-KR1, 100GBASE-CR1, 200GBASE-KR2, 200GBASE-CR2, 400GBASE-KR4, ~~or~~ 400GBASE-CR4, 800GBASE-KR8, or 800GBASE-CR8)	12.3		12.4	s
link_fail_inhibit_timer (when the link is 50GBASE-KR, 50GBASE-CR, 100GBASE-KR2, 100GBASE-CR2, 200GBASE-KR4, or 200GBASE-CR4)	3.1		3.2	s
…				

90. Ethernet support for time synchronization protocols

90.1 Introduction

Change the second paragraph of 90.1 (as amended by IEEE Std 802.3de-2022) as follows:

The TSSI is defined for 10BASE-T1S (see Clause 147) in full-duplex and point-to-point half-duplex modes of operation, and for other PHY types in full-duplex mode. It supports MAC operation at various data rates. The MII (Clause 22), GMII (Clause 35), XGMII (Clause 46), 25GMII (Clause 106), XLGMII (Clause 81), CGMII (Clause 81), 50GMII (Clause 132), 200GMII (Clause 117), ~~and~~ 400GMII (Clause 117), and 800GMII (Clause 170) specifications are all compatible with the generic Reconciliation Sublayer (gRS) defined in 90.5.

116. Introduction to 200 Gb/s and 400 Gb/s networks

116.1 Overview

116.1.2 Relationship of 200 Gigabit and 400 Gigabit Ethernet to the ISO OSI reference model

Change lettered list item i) in 116.1.2 (as amended by IEEE Std 802.3db-2022 and IEEE Std 802.3ck-2022) as follows:

i) The MDIs as specified in:

— Clause 121 for 200GBASE-DR4
— Clause 122 for 200GBASE-FR4, 200GBASE-LR4, and 200GBASE-ER4
— Clause 124 for 400GBASE-DR4 and 400GBASE-DR4-2
— Clause 136 for 200GBASE-CR4
— Clause 137 for 200GBASE-KR4
— Clause 138 for 200GBASE-SR4
— Clause 151 for 400GBASE-FR4 and 400GBASE-LR4-6
— Clause 162 for 400GBASE-CR4
— Clause 163 for 400GBASE-KR4
— Clause 167 for 400GBASE-VR4 and 400GBASE-SR4

all use a 4-lane data path.

116.1.3 Nomenclature

Change Table 116–1 and Table 116–2 (as amended by IEEE Std 802.3db-2022 and IEEE Std 802.3ck-2022) as follows (unchanged rows not shown):

Table 116–1—200 Gb/s PHYs

Name	Description
…	
200GBASE-VR2	200 Gb/s PHY using 200GBASE-R encoding over two ~~lanes of~~ multimode fibers in each direction, with reach up to at least 50 m (see Clause 167)
200GBASE-SR4	200 Gb/s PHY using 200GBASE-R encoding over four ~~lanes of~~ multimode fibers in each direction (see Clause 138)
200GBASE-SR2	200 Gb/s PHY using 200GBASE-R encoding over two ~~lanes of~~ multimode fibers in each direction, with reach up to at least 100 m (see Clause 167)
200GBASE-DR4	200 Gb/s PHY using 200GBASE-R encoding over four ~~lanes of~~ single-mode fibers in each direction, with reach up to at least 500 m (see Clause 121)
…	

Table 116–2—400 Gb/s PHYs

Name	Description
…	
400GBASE-VR4	400 Gb/s PHY using 400GBASE-R encoding over four ~~lanes of~~ multimode fibers in each direction, with reach up to at least 50 m (see Clause 167)
400GBASE-SR16	400 Gb/s PHY using 400GBASE-R encoding over ~~sixteen~~ 16 ~~lanes of~~ multimode fibers in each direction, with reach up to at least 100 m (see Clause 123)
400GBASE-SR8	400 Gb/s PHY using 400GBASE-R encoding over eight ~~lanes of~~ multimode fibers in each direction, with reach up to at least 100 m (see Clause 138)
400GBASE-SR4	400 Gb/s PHY using 400GBASE-R encoding over four ~~lanes of~~ multimode fibers in each direction, with reach up to at least 100 m (see Clause 167)
400GBASE-SR4.2	400 Gb/s PHY using 400GBASE-R encoding over eight ~~lanes on~~ multimode fibers in a bidirectional WDM format, with reach up to at least 150 m (see Clause 150)
400GBASE-DR4	400 Gb/s PHY using 400GBASE-R encoding over four ~~lanes of~~ single-mode fibers in each direction, with reach up to at least 500 m (see Clause 124)
400GBASE-DR4-2	400 Gb/s PHY using 400GBASE-R encoding over four single-mode fibers in each direction, with reach up to at least 2 km (see Clause 124)
…	

116.1.4 Physical Layer signaling systems

Change Table 116–5 (as amended by IEEE Std 802.3db-2022 and IEEE Std 802.3ck-2022) as follows:

Table 116–5—PHY type and clause correlation (400GBASE optical)

PHY type	Clause[a]																								
	78	117		118	119	120	120B	120C	120D	120E	120F	120G	167		123	138	150	124		122	151		122	
	EEE	RS	400GMII	400GMII Extender	400GBASE-R PCS	400GBASE-R PMA	400GAUI-16 C2C	400GAUI-16 C2M	400GAUI-8 C2C	400GAUI-8 C2M	400GAUI-4 C2C	400GAUI-4 C2M	400GBASE-VR4 PMD	400GBASE-SR4 PMD	400GBASE-SR16 PMD	400GBASE-SR8 PMD	400GBASE-SR4.2 PMD	400GBASE-DR4 PMD	400GBASE-DR4-2 PMD	400GBASE-FR8 PMD	400GBASE-FR4 PMD	400GBASE-LR4 PMD	400GBASE-LR8 PMD	400GBASE-ER8 PMD
400GBASE-VR4	O	M	O	O	M	M	O	O	O	O	O	O	M											
400GBASE-SR16	O	M	O	O	M	M	O	O	O	O	O	O			M									
400GBASE-SR8	O	M	O	O	M	M	O	O	O	O	O	O				M								
400GBASE-SR4	O	M	O	O	M	M	O	O	O	O	O	O		M										
400GBASE-SR4.2	O	M	O	O	M	M	O	O	O	O	O	O					M							
400GBASE-DR4	O	M	O	O	M	M	O	O	O	O	O	O						M						
400GBASE-DR4-2	O	M	O	O	M	M	O	O	O	O	O	O							M					
400GBASE-FR8	O	M	O	O	M	M	O	O	O	O	O	O								M				
400GBASE-FR4	O	M	O	O	M	M	O	O	O	O	O	O									M			
400GBASE-LR4-6	O	M	O	O	M	M	O	O	O	O	O	O										M		
400GBASE-LR8	O	M	O	O	M	M	O	O	O	O	O	O											M	
400GBASE-ER8	O	M	O	O	M	M	O	O	O	O	O	O												M

[a] O = Optional, M = Mandatory.

116.4 Delay constraints

Change Table 116–7 (as amended by IEEE Std 802.3db-2022 and IEEE Std 802.3ck-2022) as follows (some unchanged rows and footnotes not shown):

Table 116–7—Sublayer delay constraints (400GBASE)

Sublayer	Maximum (bit time)[a]	Maximum (pause_quanta)[b]	Maximum (ns)	Notes[c]
…				
400GBASE-DR4 PMD	8 192	16	20.48	Includes 2 m of fiber. See 124.3.1.
400GBASE-DR4-2 PMD	8 192	16	20.48	Includes 2 m of fiber. See 124.3.1.
400GBASE-FR8 PMD	8 192	16	20.48	Includes 2 m of fiber. See 122.3.1.
…				

[a] For 400GBASE-R, 1 bit time (BT) is equal to 2.5 ps. (See 1.4.215 for the definition of bit time.)
[b] For 400GBASE-R, 1 pause_quantum is equal to 1.28 ns. (See 31B.2 for the definition of pause_quanta.)
[c] Should there be a discrepancy between this table and the delay requirements of the relevant sublayer clause, the sublayer clause prevails.

120. Physical Medium Attachment (PMA) sublayer, type 200GBASE-R and 400GBASE-R

120.5 Functions within the PMA

120.5.11 PMA test patterns (optional)

120.5.11.2 Test patterns for PAM4 encoded signals

Insert the following paragraph at the end of 120.5.11.2 (as amended by IEEE Std 802.3ck-2022):

All test patterns specified in 120.5.11.2.a, 120.5.11.2.1, 120.5.11.2.2, 120.5.11.2.3, and 120.5.11.2.4 are defined without precoding.

120.5.11.2.2 PRBS31Q test pattern

Insert the following paragraph at the end of 120.5.11.2.2:

Precoding may be applied to the PRBS31Q pattern by enabling precoding in the PMA output or input as required.

Change the title of Clause 124 as follows:

124. Physical Medium Dependent (PMD) sublayer and medium, type 400GBASE-DR4, 400GBASE-DR4-2, 800GBASE-DR8, and 800GBASE-DR8-2

124.1 Overview

Change the first paragraph in 124.1 as follows:

This clause specifies the 400GBASE-DR4, 400GBASE-DR4-2, 800GBASE-DR8, and 800GBASE-DR8-2 PMDs together with the single-mode fiber medium. The optical signal generated by this PMD type is modulated using a 4-level pulse amplitude modulation (PAM4) format. When forming a complete Physical Layer, a PMD shall be connected to the appropriate PMA as shown in Table 124–1 for 400GBASE-DR4 and 400GBASE-DR4-2 and in Table 124–1a for 800GBASE-DR8 and 800GBASE-DR8-2, to the medium through the MDI and optionally with the management functions that may be accessible through the management interface defined in Clause 45, or equivalent.

Change Table 124–1 (as amended by IEEE Std 802.3ck-2022) as follows:

Table 124–1—Physical Layer clauses associated with the 400GBASE-DR4 and 400GBASE-DR4-2 PMDs

Associated clause	400GBASE-DR4, 400GBASE-DR4-2
117—RS	Required
117—400GMII[a]	Optional
118—400GMII Extender	Optional
119—PCS	Required
120—PMA	Required
120B—Chip-to-chip 400GAUI-16	Optional
120C—Chip-to-module 400GAUI-16	Optional
120D—Chip-to-chip 400GAUI-8	Optional
120E—Chip-to-module 400GAUI-8	Optional
120F—Chip-to-chip 400GAUI-4 (400GAUI-4 C2C)	Optional
120G—Chip-to-module 400GAUI-4 (400GAUI-4 C2M)	Optional
78—Energy Efficient Ethernet	Optional

[a] The 400GMII is an optional interface. However, if the 400GMII is not implemented, a conforming implementation behaves functionally as though the RS and 400GMII were present.

Insert new Table 124–1a after Table 124–1 as follows:

Table 124–1a—Physical Layer clauses associated with the 800GBASE-DR8 and 800GBASE-DR8-2 PMDs

Associated clause	800GBASE-DR8, 800GBASE-DR8-2
170—RS	Required
170—800GMII[a]	Optional
171—800GMII Extender	Optional
172—PCS	Required
173—PMA	Required
120F—Chip-to-chip 800GAUI-8	Optional
120G—Chip-to-module 800GAUI-8	Optional

[a] The 800GMII is an optional interface. However, if the 800GMII is not implemented, a conforming implementation behaves functionally as though the RS and 800GMII were present.

Change the second paragraph in 124.1 as follows:

Figure 124–1 shows the relationship of the PMD and MDI (shown shaded) with other sublayers to the ISO/IEC Open System Interconnection (OSI) reference model. 400 Gb/s Ethernet is introduced in Clause 116 and the purpose of each PHY sublayer is summarized in 116.2. 800 Gb/s Ethernet is introduced in Clause 169 and the purpose of each PHY sublayer is summarized in 169.2.

Insert the following new paragraph before the last paragraph in 124.1:

400GBASE-DR4 and 400GBASE-DR4-2 use four lanes, while 800GBASE-DR8 and 800GBASE-DR8-2 use eight lanes. In this clause, where there are four or eight items (depending on PMD type) such as lanes, the items are numbered from 0 to $n - 1$, where n is 4 or 8, and an example item is numbered i.

Replace Figure 124–1 with the following figure:

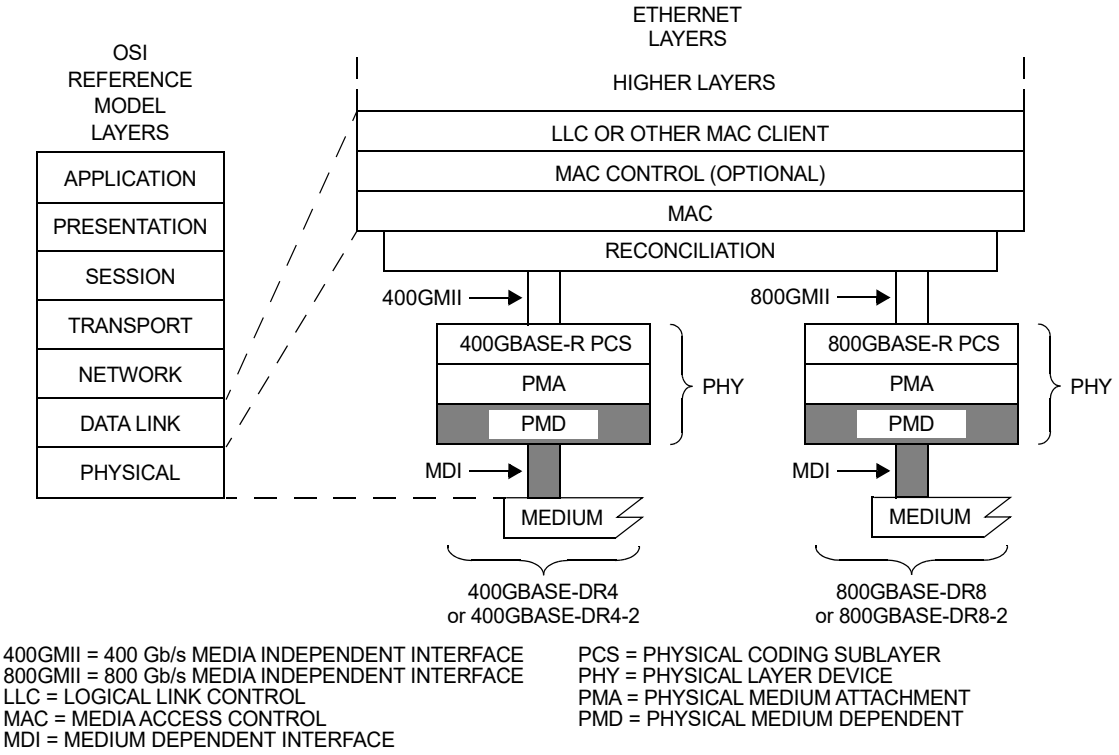


Figure 124–1—400GBASE-DR4, 400GBASE-DR4-2, 800GBASE-DR8, and 800GBASE-DR8-2 PMD relationship to the ISO/IEC Open Systems Interconnection (OSI) reference model and IEEE 802.3 Ethernet model

Change the last paragraph in 124.1 as follows:

400GBASE-DR4 and 400GBASE-DR4-2 PHYs with the optional Energy Efficient Ethernet (EEE) fast wake capability may enter the Low Power Idle (LPI) mode to conserve energy during periods of low link utilization (see Clause 78). The deep sleep mode of EEE is not supported.

124.1.1 Bit error ratio

Change 124.1.1 as follows:

The bit error ratio (BER) for 400GBASE-DR4 and 400GBASE-DR4-2 PMDs, when processed according to Clause 120, shall be less than 2.4×10^{-4} provided that the error statistics are sufficiently random that this results in a frame loss ratio (see 1.4.344) of less than 1.7×10^{-12} for 64-octet frames with minimum interpacket gap when processed according to Clause 120 and then Clause 119. ~~For a complete Physical Layer, the frame loss ratio may be degraded to 6.2×10^{-11} for 64-octet frames with minimum interpacket gap due to additional errors from the electrical interfaces.~~ If the error statistics are not sufficiently random to meet this requirement, then the BER shall be less than that required to give a frame loss ratio of less than 1.7×10^{-12} for 64-octet frames with minimum interpacket gap.

The bit error ratio (BER) for 800GBASE-DR8 and 800GBASE-DR8-2 PMDs, when processed according to Clause 173, shall be less than 2.4×10^{-4} provided that the error statistics are sufficiently random that this results in a frame loss ratio (see 1.4.344) of less than 3.4×10^{-12} for 64-octet frames with minimum

interpacket gap when processed according to Clause 173 and then Clause 172. If the error statistics are not sufficiently random to meet this requirement, then the BER shall be less than that required to give a frame loss ratio of less than 3.4×10^{-12} for 64-octet frames with minimum interpacket gap.

For a complete Physical Layer, the frame loss ratio may be degraded to 6.2×10^{-11} for 64-octet frames with minimum interpacket gap due to additional errors from the electrical interfaces.

~~If the error statistics are not sufficiently random to meet this requirement, then the BER shall be less than that required to give a frame loss ratio of less than 1.7×10^{-12} for 64-octet frames with minimum interpacket gap.~~

124.2 Physical Medium Dependent (PMD) service interface

Change the first six paragraphs in 124.2 as follows:

This subclause specifies the services provided by the 400GBASE-DR4, 400GBASE-DR4-2, 800GBASE-DR8, and 800GBASE-DR8-2 PMDs. The service interface for ~~this~~ these PMDs is described in an abstract manner and does not imply any particular implementation. The PMD service interface supports the exchange of encoded data between the PMA entity that resides just above the PMD, and the PMD entity. The PMD translates the encoded data to and from signals suitable for the specified medium.

The PMD service interface is an instance of the inter-sublayer service interface defined in 116.3 for the 400GBASE-DR4 and 400GBASE-DR4-2 PMDs and in 169.3 for the 800GBASE-DR8 and 800GBASE-DR8-2 PMDs. The PMD service interface primitives are summarized as follows:

PMD:IS_UNITDATA_*i*.request
PMD:IS_UNITDATA_*i*.indication
PMD:IS_SIGNAL.indication

The 400GBASE-DR4 and 400GBASE-DR4-2 PMDs ~~has~~ have four parallel symbol streams, hence $i = 0$ to 3. The 800GBASE-DR8 and 800GBASE-DR8-2 PMDs have eight parallel symbol streams, hence $i = 0$ to 7.

In the transmit direction, the PMA continuously sends ~~four~~ *n* parallel symbol streams to the PMD, one per lane, each at a nominal signaling rate of 53.125 GBd. The PMD then converts these streams of data units into the appropriate signals on the MDI.

In the receive direction, the PMD continuously sends ~~four~~ *n* parallel symbol streams to the PMA corresponding to the signals received from the MDI, one per lane, each at a nominal signaling rate of 53.125 GBd. ~~See~~ For 400GBASE-DR4 and 400GBASE-DR4-2, see NOTE at the end of 120.5.2 concerning the transition density of lanes operating at this nominal signaling rate.

The SIGNAL_DETECT parameter defined in this clause maps to the SIGNAL_OK parameter in the PMD:IS_SIGNAL.indication(SIGNAL_OK) inter-sublayer service interface primitive defined in 116.3 for 400GBASE-DR4 and 400GBASE-DR4-2 and defined in 169.3 for 800GBASE-DR8 and 800GBASE-DR8-2.

124.3 Delay and Skew

124.3.1 Delay constraints

Change 124.3.1 as follows:

The sum of the transmit and receive delays at one end of the link contributed by the 400GBASE-DR4 or 400GBASE-DR4-2 PMD including 2 m of fiber in one direction shall be no more than 8192 bit times (16 pause_quanta or 20.48 ns). ~~A description of overall system delay constraints and the definitions for bit times and pause_quanta can be found in 116.4 and its references.~~

The sum of the transmit and receive delays at one end of the link contributed by the 800GBASE-DR8 or 800GBASE-DR8-2 PMD including 2 m of fiber in one direction shall be no more than 16 384 bit times (32 pause_quanta or 20.48 ns).

Descriptions of overall system delay constraints and the definitions for bit times and pause_quanta can be found in 116.4 for 400GBASE-DR4 and 400GBASE-DR4-2, and in 169.4 for 800GBASE-DR8 and 800GBASE-DR8-2.

124.3.2 Skew constraints

Change 124.3.2 as follows:

The Skew (relative delay between the lanes) and Skew Variation are kept within limits so that the information on the lanes can be reassembled by the PCS.

124.3.2.1 Skew constraints for 400GBASE-DR4 and 400GBASE-DR4-2

Skew and Skew Variation are defined in 116.5 and specified at the points SP1 to SP6 shown in Figure 116–4 and Figure 116–5.

If the PMD service interface is physically instantiated so that the Skew at SP2 can be measured, then the Skew at SP2 is limited to 43 ns and the Skew Variation at SP2 is limited to 400 ps.

The Skew at SP3 (the transmitter MDI) shall be less than 54 ns and the Skew Variation at SP3 shall be less than 600 ps.

The Skew at SP4 (the receiver MDI) shall be less than 134 ns and the Skew Variation at SP4 shall be less than 3.4 ns.

If the PMD service interface is physically instantiated so that the Skew at SP5 can be measured, then the Skew at SP5 shall be less than 145 ns and the Skew Variation at SP5 shall be less than 3.6 ns.

For more information on Skew and Skew Variation see 116.5. The measurements of Skew and Skew Variation are defined in 86.8.3.1.

124.3.2.2 Skew constraints for 800GBASE-DR8 and 800GBASE-DR8-2

Skew and Skew Variation are defined in 169.5 and specified at the points SP1 to SP6 shown in Figure 169–4 and Figure 169–5.

If the PMD service interface is physically instantiated so that the Skew at SP2 can be measured, then the Skew at SP2 is limited to 25 ns and the Skew Variation at SP2 is limited to 400 ps.

The Skew at SP3 (the transmitter MDI) shall be less than 36 ns and the Skew Variation at SP3 shall be less than 600 ps.

The Skew at SP4 (the receiver MDI) shall be less than 116 ns and the Skew Variation at SP4 shall be less than 3.4 ns.

If the PMD service interface is physically instantiated so that the Skew at SP5 can be measured, then the Skew at SP5 shall be less than 127 ns and the Skew Variation at SP5 shall be less than 3.6 ns.

For more information on Skew and Skew Variation see 169.5. The measurements of Skew and Skew Variation are defined in 86.8.3.1.

124.4 PMD MDIO function mapping

Change Table 124–2 and Table 124–3 as follows:

Table 124–2—MDIO/PMD control variable mapping

MDIO control variable	PMA/PMD register name	Register/bit number	PMD control variable
Reset	PMA/PMD control 1 register	1.0.15	PMD_reset
Global PMD transmit disable	PMD transmit disable register	1.9.0	PMD_global_transmit_disable
PMD transmit disable ~~3~~ *n*–1 to PMD transmit disable 0	PMD transmit disable register	~~1.9.4 to 1.9.1~~ 1.9.*n* to 1.9.1	PMD_transmit_disable_~~3~~*n*–1 to PMD_transmit_disable_0

Table 124–3—MDIO/PMD status variable mapping

MDIO status variable	PMA/PMD register name	Register/ bit number	PMD status variable
Fault	PMA/PMD status 1 register	1.1.7	PMD_fault
Transmit fault	PMA/PMD status 2 register	1.8.11	PMD_transmit_fault
Receive fault	PMA/PMD status 2 register	1.8.10	PMD_receive_fault
Global PMD receive signal detect	PMD receive signal detect register	1.10.0	PMD_global_signal_detect
PMD receive signal detect ~~3~~ *n*–1 to PMD receive signal detect 0	PMD receive signal detect register	~~1.10.4 to~~ 1.10.*n* to 1.10.1	PMD_signal_detect_~~3~~*n*–1 to PMD_signal_detect_0

124.5 PMD functional specifications

Change 124.5 as follows:

The 400GBASE-DR4, 400GBASE-DR4-2, 800GBASE-DR8, and 800GBASE-DR8-2 PMDs perform ~~performs~~ the Transmit and Receive functions, which convey data between the PMD service interface and the MDI.

124.5.1 PMD block diagram

Change the first paragraph in 124.5.1 as follows:

The PMD block diagram for 400GBASE-DR4 or 400GBASE-DR4-2 is shown in Figure 124–2. The block diagrams for 800GBASE-DR8 and 800GBASE-DR8-2 are equivalent to Figure 124–2, but for eight lanes per direction, instead of four. For purposes of system conformance, the PMD sublayer is standardized at the points described in this subclause. The optical transmit signal is defined at the output end of a single-mode fiber patch cord (TP2), between 2 m and 5 m in length. Unless specified otherwise, all transmitter measurements and tests defined in 124.8 are made at TP2. The optical receive signal is defined at the output of the fiber optic cabling (TP3) at the MDI (see 124.11.3). Unless specified otherwise, all receiver measurements and tests defined in 124.8 are made at TP3.

Change the title of Figure 124–2 as follows:

Figure 124–2—Block diagram for 400GBASE-DR4 or 400GBASE-DR4-2 transmit/receive paths

124.5.2 PMD transmit function

Change 124.5.2 as follows:

The PMD Transmit function shall convert the ~~four~~ *n* symbol streams requested by the PMD service interface messages PMD:IS_UNITDATA_0.request to PMD:IS_UNITDATA_~~3~~*n*–1.request into ~~four~~ *n* separate optical signals. The ~~four~~ *n* optical signals shall then be delivered to the MDI, which contains ~~four~~ *n* parallel light paths for transmit, according to the transmit optical specifications in this clause. The highest optical power level in each signal shall correspond to tx_symbol = three and the lowest shall correspond to tx_symbol = zero.

124.5.3 PMD receive function

Change 124.5.3 as follows:

The PMD Receive function shall convert the ~~four~~ *n* parallel optical signals received from the MDI into separate symbol streams for delivery to the PMD service interface using the messages PMD:IS_UNITDATA_0.indication to PMD:IS_UNITDATA_~~3~~*n*–1.indication, all according to the receive optical specifications in this clause. The higher optical power level in each signal shall correspond to rx_symbol = three and the lowest shall correspond to rx_symbol = zero.

124.5.4 PMD global signal detect function

Change the first two paragraphs in 124.5.4 as follows:

The PMD global signal detect function shall report the state of SIGNAL_DETECT via the PMD service interface. The SIGNAL_DETECT parameter is signaled continuously, while the PMD:IS_SIGNAL.indication message is generated when a change in the value of SIGNAL_DETECT occurs. The SIGNAL_DETECT parameter defined in this clause maps to the SIGNAL_OK parameter in the inter-sublayer service interface primitives defined in 116.3 for 400GBASE-DR4 and 400GBASE-DR4-2, and in 169.3 for 800GBASE-DR8 and 800GBASE-DR8-2.

SIGNAL_DETECT shall be a global indicator of the presence of optical signals on all ~~four~~ *n* lanes. The value of the SIGNAL_DETECT parameter shall be generated according to the conditions defined in Table 124–4. The PMD receiver is not required to verify whether a compliant

~~400GBASE-DR4~~400GBASE-R or 800GBASE-R signal is being received. This standard imposes no response time requirements on the generation of the SIGNAL_DETECT parameter.

Change Table 124–4 as follows:

Table 124–4—SIGNAL_DETECT value definition

Receive conditions	SIGNAL_DETECT value
For any lane; Average optical power at TP3 ≤ –15 dBm	FAIL
For all lanes; [(Optical power at TP3 ≥ average receive power, each lane (min) in Table 124–7) AND (compliant 400GBASE–R or 800GBASE–R signal input)]	OK
All other conditions	Unspecified

124.5.5 PMD lane-by-lane signal detect function

Change 124.5.5 as follows:

Various implementations of the Signal Detect function are permitted by this standard. When the MDIO is implemented, each PMD_signal_detect_*i*, where *i* represents the lane number in the range 0:~~3~~*n*–1, shall be continuously set in response to the magnitude of the optical signal on its associated lane, according to the requirements of Table 124–4.

124.5.8 PMD lane-by-lane transmit disable function (optional)

Change item a) in the lettered list in 124.5.8 as follows:

a) When a PMD_transmit_disable_*i* variable (where *i* represents the lane number in the range 0:~~3~~*n*–1) is set to one, this function shall turn off the optical transmitter associated with that variable so that the transmitter meets the requirements of the average launch power of the OFF transmitter in Table 124–6.

124.6 Lane assignments

Change 124.6 as follows:

There are no lane assignments (within a group of transmit or receive lanes) for 400GBASE-DR4, 400GBASE-DR4-2, 800GBASE-DR8, or 800GBASE-DR8-2. While it is expected that a PMD will map electrical lane *i* to optical lane *i* and vice versa, there is no need to define the physical ordering of the lanes, as the PCS sublayer is capable of receiving the lanes in any arrangement. The positioning of transmit and receive lanes at the MDI is specified in 124.11.3.1.

Change the title and text of 124.7 as follows:

124.7 PMD to MDI optical specifications for 400GBASE-DR4, 400GBASE-DR4-2, 800GBASE-DR8, and 800GBASE-DR8-2

The operating ranges for the 400GBASE-DR4, 400GBASE-DR4-2, 800GBASE-DR8, and 800GBASE-DR8-2 PMDs are ~~is~~ defined in Table 124–5. A 400GBASE-DR4, 400GBASE-DR4-2, 800GBASE-DR8, or 800GBASE-DR8-2 compliant PMD operates on type B1.1, B1.3, or B6_a single-mode fibers according to the specifications defined in Table 124–11. A PMD that exceeds the operating range requirement while meeting all other optical specifications is considered compliant (e.g., a 400GBASE-DR4 PMD operating at 600 m meets the operating range requirement of 2 m to 500 m).

Change Table 124–5 as follows:

Table 124–5—400GBASE-DR4, 400GBASE-DR4-2, 800GBASE-DR8, and 800GBASE-DR8-2 operating ranges

PMD type	Required operating range
400GBASE-DR4 and 800GBASE-DR8	2 m to 500 m
400GBASE-DR4-2 and 800GBASE-DR8-2	2 m to 2 km

Change the title and text of 124.7.1 as follows:

124.7.1 ~~400GBASE-DR4 transmitter~~ Transmitter optical specifications

~~The 400GBASE-DR4~~ A transmitter shall meet the specifications defined in Table 124–6 per the definitions in 124.8.

Replace Table 124–6 with the following table:

Table 124–6—400GBASE-DR4, 800GBASE-DR8, 400GBASE-DR4-2, and 800GBASE-DR8-2 transmit characteristics

Description	400GBASE-DR4	800GBASE-DR8	400GBASE-DR4-2 800GBASE-DR8-2	Unit
Signaling rate, each lane (range) 400GBASE-DR4, 400GBASE-DR4-2 800GBASE-DR8, 800GBASE-DR8-2	53.125 ± 100 ppm 53.125 ± 50 ppm			GBd GBd
Modulation format	PAM4			—
Lane wavelength (range)	1304.5 to 1317.5			nm
Side-mode suppression ratio (SMSR), (min)	30			dB
Average launch power, each lane (max)	4			dBm
Average launch power, each lane[a] (min)	–2.9[b]			dBm
Outer Optical Modulation Amplitude (OMA_{outer}), each lane (max)	4.2			dBm
Outer Optical Modulation Amplitude (OMA_{outer}), each lane (min)[c] for TDECQ ≤ 3.4 dB for TDECQ < 1.4 dB for 1.4 dB ≤ TDECQ ≤ 3.4 dB	 –0.8 — —	 — –0.8 –2.2 + TDECQ	 — –0.1 –1.5 + TDECQ	 dBm dBm dBm
Launch power in OMA_{outer} minus TDECQ, each lane (min)	–2.2	—		dBm
Transmitter and dispersion eye closure for PAM4 (TDECQ), each lane (max)	3.4			dB
TDECQ – $10\log_{10}(C_{eq})$[d] (max)	3.4	—		dB
Transmitter eye closure for PAM4 (TECQ) (max)	—	3.4		dB
| TDECQ – TECQ | (max)	—	2.5		dB
Transmitter overshoot and undershoot (max)	—	22		%
Transmitter power excursion (max)	—	5		dBm
Extinction ratio, each lane (min)	3.5			dB
Transmitter transition time (max)	17			ps
Average launch power of OFF transmitter, each lane (max)	–15			dBm

Table 124–6—400GBASE-DR4, 800GBASE-DR8, 400GBASE-DR4-2, and 800GBASE-DR8-2 transmit characteristics *(continued)*

Description	400GBASE-DR4	800GBASE-DR8	400GBASE-DR4-2 800GBASE-DR8-2	Unit
$RIN_{21.4}OMA$ (max)	–136			dB/Hz
Optical return loss tolerance (max)	21.4			dB
Transmitter reflectance[e] (max)	–26			dB

[a] Average launch power, each lane (min) is not the principal indicator of signal strength. A transmitter with launch power below this value cannot be compliant; however, a value above this does not ensure compliance.
[b] Average launch power of –2.9 dBm corresponds to an OMA of –0.8 dBm with an extinction ratio of approximately 10 dB or an OMA of –0.1 dBm with an extinction ratio of approximately 16 dB.
[c] For 400GBASE-DR4, the requirement on the OMA_{outer} (min) applies even in the cases where TDECQ < 1.4 dB.
[d] C_{eq} is a coefficient defined in 121.8.5.3, which accounts for the reference equalizer noise enhancement.
[e] Transmitter reflectance is defined looking into the transmitter.

Insert a new paragraph and Figure 124–2a at the end of 124.7.1 as follows:

For 400GBASE-DR4-2, 800GBASE-DR8, and 800GBASE-DR8-2, the values for OMA_{outer} (min) in Table 124–6 vary with TDECQ, as illustrated in Figure 124–2a along with the values for OMA_{outer} (max).

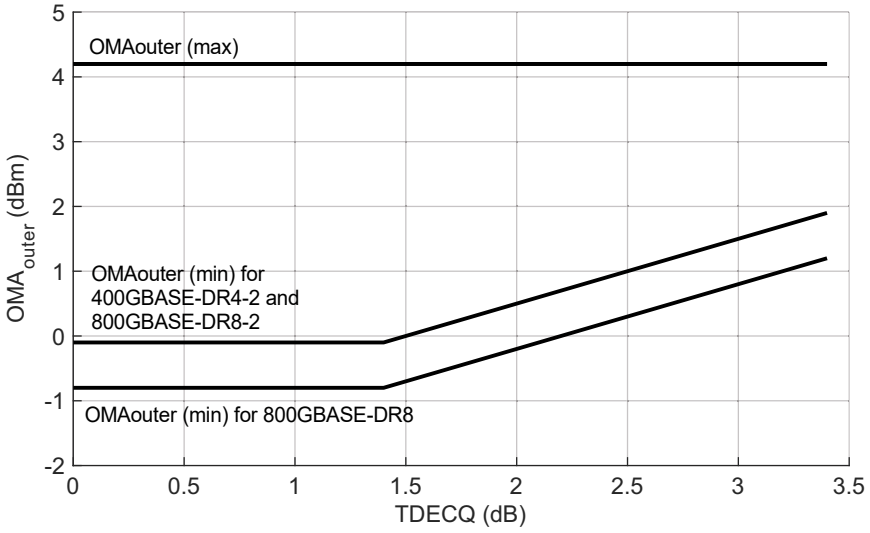


Figure 124–2a—OMAouter (max) and OMAouter (min) versus TDECQ for 400GBASE-DR4-2, 800GBASE-DR8, and 800GBASE-DR8-2

Change the title and text of 124.7.2 as follows:

124.7.2 ~~400GBASE-DR4 receive~~ Receive optical specifications

~~The 400GBASE-DR4~~ A receiver shall meet the specifications defined in Table 124–7 per the definitions in 124.8. ~~See~~ For 400GBASE-DR4 and 400GBASE-DR4-2, see NOTE at the end of 120.5.2 concerning the transition density of lanes operating at this nominal signaling rate.

Replace Table 124–7 with the following table:

Table 124–7—400GBASE-DR4, 800GBASE-DR8, 400GBASE-DR4-2, and 800GBASE-DR8-2 receive characteristics

Description	400GBASE-DR4	800GBASE-DR8	400GBASE-DR4-2 800GBASE-DR8-2	Unit
Signaling rate, each lane (range) 400GBASE-DR4, 400GBASE-DR4-2 800GBASE-DR8, 800GBASE-DR8-2	53.125 ± 100 ppm 53.125 ± 50 ppm			GBd GBd
Modulation format	PAM4			—
Lane wavelengths (range)	1304.5 to 1317.5			nm
Damage threshold[a], each lane	5			dBm
Average receive power, each lane (max)	4			dBm
Average receive power, each lane[b] (min)	–5.9		–6.9	dBm
Receive power (OMA_{outer}), each lane (max)	4.2			dBm
Receiver reflectance (max)	–26			dB
Receiver sensitivity (OMA_{outer}), each lane (max) for SECQ ≤ 3.4 dB for TECQ < 1.4 dB for 1.4 dB ≤ TECQ ≤ 3.4 dB	Equation (124–1)[c] — —	— –3.9 –5.3 + TECQ	— –4.3 –5.7 + TECQ	dBm dBm dBm
Stressed receiver sensitivity (OMA_{outer}), each lane[d] (max)	–1.9		–2.3	dBm

Table 124–7—400GBASE-DR4, 800GBASE-DR8, 400GBASE-DR4-2, and 800GBASE-DR8-2 receive characteristics *(continued)*

Description	400GBASE-DR4	800GBASE-DR8	400GBASE-DR4-2 800GBASE-DR8-2	Unit
Conditions of stressed receiver sensitivity test:[e]				
Stressed eye closure for PAM4 (SECQ), lane under test	3.4			dB
SECQ – $10\log_{10}(C_{eq})$[f] (max), lane under test	3.4	—		dB
OMA_{outer} of each aggressor lane	4.2			dBm

[a] The receiver shall be able to tolerate, without damage, continuous exposure to an optical input signal having this average power level. The receiver does not have to operate correctly at this input power.
[b] Average receive power, each lane (min) is not the principal indicator of signal strength. A received power below this value cannot be compliant; however, a value above this does not ensure compliance.
[c] For 400GBASE-DR4, receiver sensitivity (OMA_{outer}), each lane (max) is optional and is defined for a transmitter with a value of SECQ up to 3.4 dB.
[d] Measured with conformance test signal at TP3 (see 124.8.10) for the BER specified in 124.1.1.
[e] These test conditions are for measuring stressed receiver sensitivity. They are not characteristics of the receiver.
[f] C_{eq} is a coefficient defined in 121.8.5.3, which accounts for the reference equalizer noise enhancement.

Insert a new paragraph and Figure 124–2b at the end of 124.7.2 as follows:

For 400GBASE-DR4-2, 800GBASE-DR8, and 800GBASE-DR8-2, the values for receiver sensitivity (OMA_{outer}) (max) in Table 124–7 vary with TECQ as illustrated in Figure 124–2b.

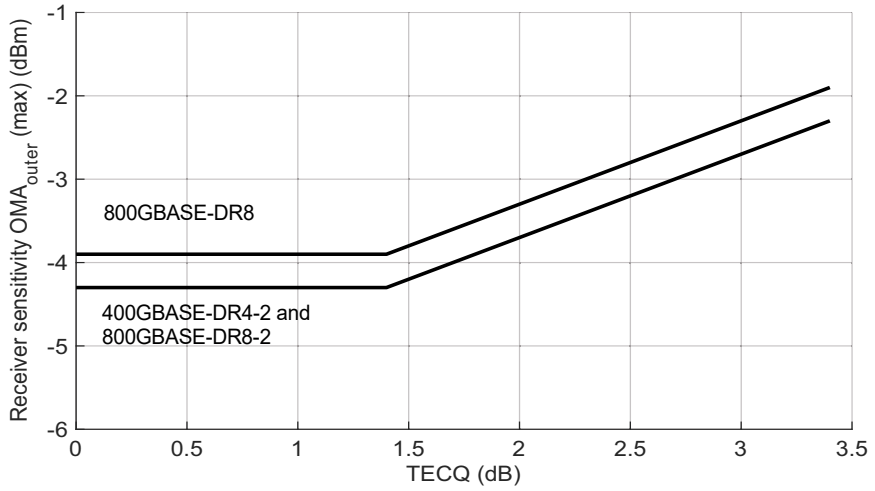


Figure 124–2b—Receiver sensitivity (OMAouter) (max) for 400GBASE-DR4-2, 800GBASE-DR8, and 800GBASE-DR8-2

Change the title and text of 124.7.3 as follows:

124.7.3 ~~400GBASE-DR4 illustrative~~ Illustrative link power ~~budget~~ budgets

~~An illustrative~~ Illustrative power budgets and penalties for 400GBASE-DR4, 400GBASE-DR4-2, 800GBASE-DR8, and 800GBASE-DR8-2 channels are shown in Table 124–8.

Change Table 124–8 as follows:

Table 124–8—400GBASE-DR4, 800GBASE-DR8, 400GBASE-DR4-2, and 800GBASE-DR8-2 illustrative link power budgets

Parameter	400GBASE-DR4 800GBASE-DR8	400GBASE-DR4-2 800GBASE-DR8-2	Unit
Power budget (for max TDECQ)	6.5	7.6	dB
Operating distance	500	2000	m
Channel insertion loss[a]	3	4	dB
Maximum discrete reflectance	See 124.11.2.2	See 124.11.2.2	dB
Allocation for penalties[b] (for max TDECQ)	3.5	3.6	dB
Additional insertion loss allowed	0	0	dB

[a] The channel insertion loss is calculated using the maximum distance specified in Table 124–5 and cabled optical fiber attenuation of 0.5 dB/km at 1304.5 nm plus an allocation for connection and splice loss given in 124.11.2.1.
[b] Link penalties are used for link budget calculations. They are not requirements and are not meant to be tested.

Insert a new paragraph, Figure 124–2c, and Figure 124–2d at the end of 124.7.3 as follows:

The values of transmitter OMA_{outer} (max), transmitter OMA_{outer} (min) versus TDECQ, and receiver sensitivity (OMA_{outer}) (max) versus TECQ are illustrated in Figure 124–2c for 800GBASE-DR8, and in Figure 124–2d for 400GBASE-DR4-2 and 800GBASE-DR8-2.

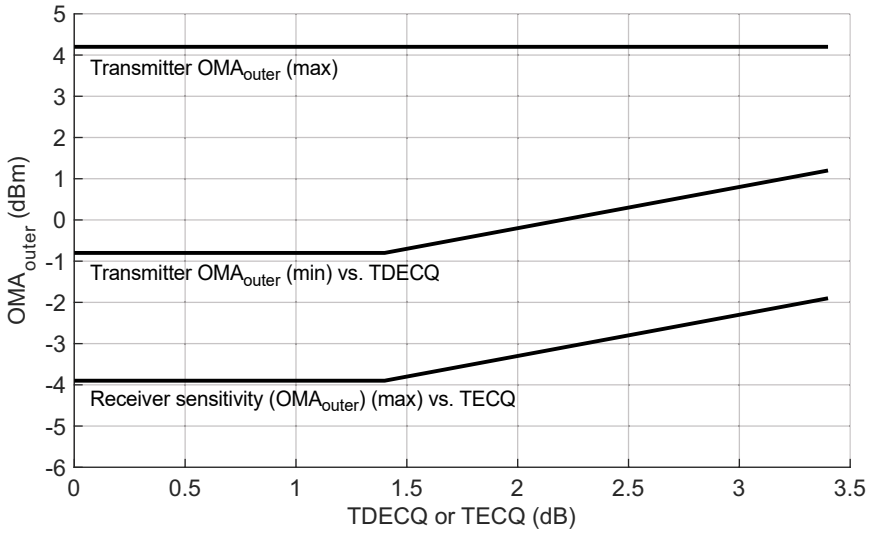


Figure 124–2c—Transmitter OMAouter versus TDECQ and receiver sensitivity (OMAouter) versus TECQ for 800GBASE-DR8

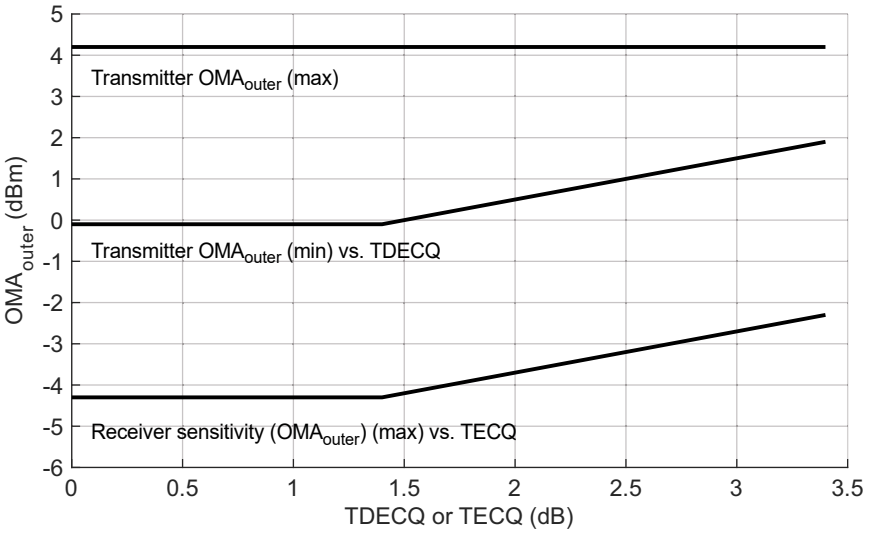


Figure 124–2d—Transmitter OMAouter versus TDECQ and receiver sensitivity (OMAouter) versus TECQ for 400GBASE-DR4-2 and 800GBASE-DR8-2

124.8 Definition of optical parameters and measurement methods

124.8.1 Test patterns for optical parameters

Change Table 124–9 as follows:

Table 124–9—Test patterns

Pattern	Pattern description	Defined in
Square wave	Square wave (8 threes, 8 zeros)	120.5.11.2.4
3	PRBS31Q	120.5.11.2.2
4	PRBS13Q	120.5.11.2.1
5	Scrambled idle	119.2.4.9 or 172.2.4.11
6	SSPRQ	120.5.11.2.3

Change Table 124–10 as follows:

Table 124–10—Test-pattern definitions and related subclauses

Parameter	Pattern	Related subclause
Wavelength	Square wave, 3, 4, 5, 6, or valid 400GBASE-R or 800GBASE-R signal	124.8.2
Side mode suppression ratio	3, 5, 6, or valid 400GBASE-R or 800GBASE-R signal	124.8.2
Average optical power	3, 5, 6, or valid 400GBASE-R or 800GBASE-R signal	124.8.3
Outer Optical Modulation Amplitude (OMA_{outer})	4 or 6	124.8.4
Transmitter and dispersion eye closure for PAM4 (TDECQ)	6	124.8.5
Transmitter eye closure for PAM4 (TECQ)	6	124.8.5a
Transmitter overshoot and undershoot	6	124.8.5b
Transmitter power excursion	6	124.8.5c
Extinction ratio	4 or 6	124.8.6
Transmitter transition time	Square wave or 6	124.8.7
$RIN_{21.4}OMA$	Square wave	124.8.8
Receiver sensitivity	3 or 5	124.8.9
Stressed receiver conformance test signal calibration	6	124.8.10
Stressed receiver sensitivity	3 or 5	124.8.10

124.8.5 Transmitter and dispersion eye closure for PAM4 (TDECQ)

Change 124.8.5 as follows:

The TDECQ and, for 400GBASE-DR4 only, TDECQ – $10\log_{10}(C_{eq})$ of each lane shall be within the limits given in Table 124–6 if measured using the methods specified in 121.8.5.1, 121.8.5.2, and 121.8.5.3 using a reference equalizer as described in 121.8.5.4 where T is the symbol period for 400GBASE-DR4, 400GBASE-DR4-2, 800GBASE-DR8, and 800GBASE-DR8-2, with the following exceptions:

- The signaling rate of the test pattern generator is as given in Table 124–6 and uses the test pattern specified for TDECQ in Table 124–10.
- The combination of the O/E converter and the oscilloscope has a 3 dB bandwidth of approximately 26.5625 GHz with a fourth-order Bessel-Thomson response to at least 1.3 × 53.125 GHz, and at frequencies above 1.3 × 53.125 GHz, the response should not exceed –20 dB. Compensation may be made for any deviation from an ideal fourth-order Bessel-Thomson response.
- The normalized noise power density spectrum $N(f)$ is equivalent to white noise filtered by a fourth-order Bessel-Thomson response filter with a 3 dB bandwidth of 26.5625 GHz.
- The 400GBASE-DR4-2 or 800GBASE-DR8-2 transmitter is tested using an optical channel as specified in 124.8.5.1.

Insert new subclause 124.8.5.1 at the end of 124.8.5 as follows:

124.8.5.1 Channel requirements

The 400GBASE-DR4-2 or 800GBASE-DR8-2 transmitter is tested using an optical channel that meets the requirements listed in Table 124–10a.

Table 124–10a—Transmitter compliance channel specifications

PMD type	Dispersion[a] (ps/nm)		Insertion loss[b]	Optical return loss[c]	Max mean DGD
	Minimum	Maximum			
400GBASE-DR4-2 or 800GBASE-DR4-2	$0.046\times\lambda\times[1-(1324/\lambda)^4]$	$0.046\times\lambda\times[1-(1300/\lambda)^4]$	Minimum	21.4 dB	0.8 ps

[a] The dispersion is measured for the wavelength of the transmitter lane under test (λ in nm). The coefficient assumes 2 km for 400GBASE-DR4-2 or 800GBASE-DR8-2.
[b] There is no intent to stress the sensitivity of the O/E converter associated with the oscilloscope.
[c] The optical return loss is applied at TP2.

A 400GBASE-DR4-2 or 800GBASE-DR8-2 transmitter is to be compliant with a total dispersion at least as negative as the "minimum dispersion" and at least as positive as the "maximum dispersion" columns specified in Table 124–10a for the wavelength of the transmitter lane under test. This may be achieved with channels consisting of fibers with lengths chosen to meet the dispersion requirements.

To verify that the fiber has the correct amount of dispersion, the measurement method defined in IEC 60793-1-42 may be used. The measurement is made in the linear power regime of the fiber.

The channel provides an optical return loss specified in Table 124–10a. The state of polarization of the back reflection is adjusted to create the greatest RIN.

The mean DGD of the channel is to be less than the value specified in Table 124–10a.

Insert new subclauses 124.8.5a, 124.8.5b, and 124.8.5c after 124.8.5 as follows:

124.8.5a Transmitter eye closure for PAM4 (TECQ)

The transmitter eye closure for PAM4 (TECQ) is a measure of the optical transmitter's eye closure at TP2. For 400GBASE-DR4-2, 800GBASE-DR8, and 800GBASE-DR8-2, TECQ shall be within the limits given in Table 124–6 if measured using a test pattern specified for TECQ in Table 124–10. TECQ is measured using the methods specified for TDECQ in 124.8.5, except that the test fiber is not used.

124.8.5b Transmitter overshoot and undershoot

For 400GBASE-DR4-2, 800GBASE-DR8, and 800GBASE-DR8-2, the overshoot and undershoot shall be within the limits given in Table 124–6 if measured using a test pattern specified for overshoot and undershoot in Table 124–10.

Overshoot and undershoot are measured using the waveforms captured for the TDECQ test (see 124.8.5) and the waveform captured for the TECQ test (see 124.8.5a), but without the reference equalizer being applied in either case.

Overshoot and undershoot are defined in 140.7.7.

124.8.5c Transmitter power excursion

For 400GBASE-DR4-2, 800GBASE-DR8, and 800GBASE-DR8-2, the transmitter power excursion shall be within the limits given in Table 124–6 if measured using a test pattern specified for transmitter power excursion in Table 124–10.

Transmitter power excursion is measured using the waveforms captured for the TECQ test (see 124.8.5a), but without the reference equalizer being applied.

Transmitter power excursion is defined in 140.7.8.

124.8.9 Receiver sensitivity

Insert a new subclause heading 124.8.9.1 after the heading for 124.8.9 as follows:

124.8.9.1 Receiver sensitivity for 400GBASE-DR4

Change the text in 124.8.9.1 (formerly in 124.8.9) as follows (Figure 124–4 remains unchanged):

~~Receiver~~ The receiver sensitivity for 400GBASE-DR4 is optional and is defined for a transmitter with a value of SECQ up to 3.4 dB. Receiver sensitivity should meet Equation (124–1), which is illustrated in Figure 124–4.

$$RS = \max(-3.9, SECQ - 5.3) \quad \text{(dBm)} \tag{124–1}$$

where

RS	is the receiver sensitivity
$SECQ$	is the SECQ of the transmitter used to measure the receiver sensitivity

The normative requirement for 400GBASE-DR4 receivers is stressed receiver sensitivity.

Insert new subclause 124.8.9.2 after 124.8.9.1 as follows:

124.8.9.2 Receiver sensitivity for 400GBASE-DR4-2, 800GBASE-DR8, and 800GBASE-DR8-2

The receiver sensitivity (OMA_{outer}) for 400GBASE-DR4-2, 800GBASE-DR8, and 800GBASE-DR8-2 shall be within the limits given in Table 124–7 if measured using a test pattern for receiver sensitivity in Table 124–10. The conformance test signal at TP3 meets the requirements for a 400GBASE-DR4-2, 800GBASE-DR8, and 800GBASE-DR8-2 transmitter followed by an attenuator.

The TECQ of the conformance test signal is measured according to 124.8.5, except that the test fiber is not used. The measured value of TECQ is then used to calculate the limit for receiver sensitivity (OMA_{outer}) as specified in Table 124–7 for 400GBASE-DR4-2, 800GBASE-DR8, and 800GBASE-DR8-2.

124.9 Safety, installation, environment, and labeling

124.9.2 Laser safety

Change the first paragraph in 124.9.2 as follows:

400GBASE-DR4, 400GBASE-DR4-2, 800GBASE-DR8, and 800GBASE-DR8-2 optical transceivers shall conform to Hazard Level 1 laser requirements as defined in IEC 60825-1 and IEC 60825-2, under any condition of operation. This includes single fault conditions whether coupled into a fiber or out of an open bore.

124.9.4 Environment

Change the first paragraph in 124.9.4 as follows:

Normative specifications in this clause shall be met by a system integrating a 400GBASE-DR4, 400GBASE-DR4-2, 800GBASE-DR8, or 800GBASE-DR8-2 PMD over the life of the product while the product operates within the manufacturer's range of environmental, power, and other specifications.

124.9.5 Electromagnetic emission

Change 124.9.5 as follows:

A system integrating a 400GBASE-DR4, 400GBASE-DR4-2, 800GBASE-DR8, or 800GBASE-DR8-2 PMD shall comply with applicable local and national codes for the limitation of electromagnetic interference.

124.10 Fiber optic cabling model

Change Table 124–11 as follows:

Table 124–11—Fiber optic cabling (channel) characteristics

Description	400GBASE-DR4 800GBASE-DR8	400GBASE-DR4-2 800GBASE-DR8-2	Unit
Operating distance (max)	500	2000	m
Channel insertion loss[a,b] (max)	3	4	dB
Channel insertion loss (min)	0	0	dB
Positive dispersion[b] (max)	0.8	3.2	ps/nm
Negative dispersion[b] (min)	–0.93	–3.7	ps/nm
DGD_max[c]	2.24	2.3	ps
Optical return loss (min)	37	37	dB

[a] These channel insertion loss values include cable, connectors, and splices.
[b] Over the wavelength range 1304.5 nm to 1317.5 nm.
[c] Differential Group Delay (DGD) is the time difference at reception between the fractions of a pulse that were transmitted in the two principal states of polarization of an optical signal. DGD_max is the maximum differential group delay that the system is required to tolerate.

124.11 Characteristics of the fiber optic cabling (channel)

Change 124.11 as follows:

The ~~400GBASE-DR4~~ fiber optic cabling shall meet the specifications defined in Table 124–12. The fiber optic cabling consists of one or more sections of fiber optic cable and any intermediate connections required to connect sections together.

124.11.2 Optical fiber connection

124.11.2.1 Connection insertion loss

Change 124.11.2.1 as follows:

~~The~~ For 400GBASE-DR4 and 800GBASE-DR8 the maximum link distance is based on an allocation of 2.75 dB total connection and splice loss. For example, this allocation supports five connections with an average insertion loss per connection of 0.5 dB. Connections with different loss characteristics may be used provided the requirements of Table 124–11 are met.

For 400GBASE-DR4-2 and 800GBASE-DR8-2 the maximum link distance is based on an allocation of 3 dB total connection and splice loss. For example, this allocation supports six connections with an average insertion loss per connection of 0.5 dB. Connections with different loss characteristics may be used provided the requirements of Table 124–11 are met.

124.11.3 Medium Dependent Interface (MDI)

Change 124.11.3 as follows:

The ~~400GBASE-DR4~~ PMD is coupled to the fiber optic cabling at the MDI. The MDI is the interface between the PMD and the "fiber optic cabling" (as shown in Figure 124–5). The ~~400GBASE-DR4~~ PMD is coupled to the fiber optic cabling through one connector plug into the MDI optical receptacle as shown in Figure 124–7. Example constructions of the MDI include the following:

a) PMD with a connectorized fiber pigtail plugged into an adapter
b) PMD receptacle

124.11.3.1 Optical lane assignments

Insert new subclause heading 124.11.3.1.1 after the heading 124.11.3.1 as follows:

124.11.3.1.1 Optical lane assignments for 400GBASE-DR4 and 400GBASE-DR4-2

Change 124.11.3.1.1 (formerly 124.11.3.1) and the title of Figure 124–6 as follows:

The four transmit and four receive optical lanes of 400GBASE-DR4 and 400GBASE-DR4-2 shall occupy the positions depicted in Figure 124–6 when looking into the MDI receptacle with the connector keyway feature on top. The interface contains eight active lanes within ~~twelve~~ 12 total positions. The transmit optical lanes occupy the left-most four positions. The receive optical lanes occupy the right-most four positions. The four center positions are unused.

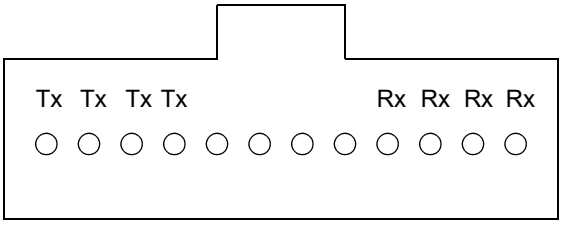


Figure 124–6—400GBASE-DR4 and 400GBASE-DR4-2 optical lane assignments

Insert new subclause 124.11.3.1.2, including Figure 124–6a, after Figure 124–6 as follows:

124.11.3.1.2 Optical lane assignments for 800GBASE-DR8 and 800GBASE-DR8-2

800GBASE-DR8 and 800GBASE-DR8-2 shall use a single-row 16-fiber interface. The eight transmit and eight receive optical lanes of 800GBASE-DR8 and 800GBASE-DR8-2 shall occupy the positions depicted in Figure 124–6a when looking into the MDI receptacle with the connector keyway feature on top. The interface contains 16 active lanes within 16 total positions. The transmit optical lanes occupy the leftmost eight positions. The receive optical lanes occupy the rightmost eight positions.

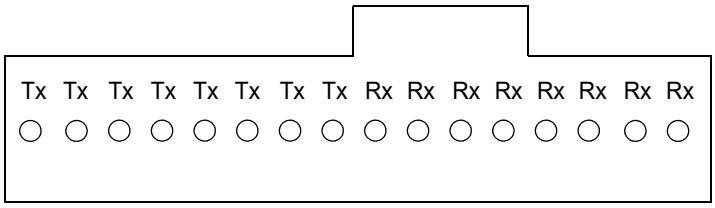


Figure 124–6a—Optical lane assignments for 800GBASE-DR8 and 800GBASE-DR8-2

Change the title of 124.11.3.2 as follows:

124.11.3.2 ~~Medium Dependent Interface (MDI)~~ MDI requirements for 400GBASE-DR4 and 400GBASE-DR4-2

Insert new subclause 124.11.3.3 after 124.11.3.2 as follows:

124.11.3.3 MDI requirements for 800GBASE-DR8 and 800GBASE-DR8-2

The MDI shall optically mate with the compatible plug on the optical fiber cabling. The MDI shall meet the interface performance specifications of IEC 61753-021-2 for performance level D/2. 800GBASE-DR8 and 800GBASE-DR8-2 have a single-row 16-fiber interface optical lane assignment.

If the MDI is constructed with a connectorized fiber pigtail into an adapter, the connectorized pigtail shall meet the dimensional specifications of designation FOCIS 18 P-1x16-1-8-1-1-1 and the adapter shall meet the dimensional specifications of designation FOCIS 18 A-1-0 as defined in ANSI/TIA-604-18-A. If the MDI is constructed with a receptacle, it shall meet the dimensional specifications of designation FOCIS 18 R-1x16-1-8-1-1-2, as defined in ANSI/TIA-604-18-A. The plug terminating the optical fiber cabling that interconnects to either MDI configuration shall meet the dimensional specifications of designation FOCIS 18 P-1x16-1-8-2-1-1, as defined in ANSI/TIA-604-18-A. The MPO-16 female plug connector and MDI are structurally similar to those depicted in Figure 124–7, but with an angled end facet, 16 fibers, an offset keyway, and different pin diameters and locations.

Insert new subclause 124.11a after 124.11 as follows:

124.11a Interoperation between 400GBASE-DR4 and 400GBASE-DR4-2, and between 800GBASE-DR8 and 800GBASE-DR8-2

124.11a.1 Interoperation between 400GBASE-DR4 and 400GBASE-DR4-2

The 400GBASE-DR4 and 400GBASE-DR4-2 PMDs can interoperate with each other provided that the fiber optic cabling (channel) characteristics for 400GBASE-DR4 (see 124.10 and Table 124–11) are met.

124.11a.2 Interoperation between 800GBASE-DR8 and 800GBASE-DR8-2

The 800GBASE-DR8 and 800GBASE-DR8-2 PMDs can interoperate with each other provided that the fiber optic cabling (channel) characteristics for 800GBASE-DR8 (see 124.10 and Table 124–11) are met.

Change the title of 124.12 as follows:

124.12 Protocol implementation conformance statement (PICS) proforma for Clause 124, Physical Medium Dependent (PMD) sublayer and medium, type 400GBASE-DR4, 400GBASE-DR4-2, 800GBASE-DR8, and 800GBASE-DR8-2[7]

124.12.1 Introduction

Change the first paragraph in 124.12.1 as follows:

The supplier of a protocol implementation that is claimed to conform to Clause 124, Physical Medium Dependent (PMD) sublayer and medium, type 400GBASE-DR4, 400GBASE-DR4-2, 800GBASE-DR8, and 800GBASE-DR8-2, shall complete the following protocol implementation conformance statement (PICS) proforma.

124.12.2 Identification

124.12.2.2 Protocol summary

Change the table in 124.12.2.2 as follows:

Identification of protocol standard	IEEE Std 802.3df-2024, Clause 124, Physical Medium Dependent (PMD) sublayer and medium, type 400GBASE-DR4, 400GBASE-DR4-2, 800GBASE-DR8, and 800GBASE-DR8-2
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3df-2024.)	

Date of Statement	

[7] *Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

124.12.3 Major capabilities/options

Insert four new rows at the start of the table in 124.12.3 as follows (unchanged rows not shown):

Item	Feature	Subclause	Value/Comment	Status	Support
*DR4	400GBASE-DR4 PMD	124.7	Device supports requirements for 400GBASE-DR4 PHY	O.1	Yes [ ] No [ ]
*DR42	400GBASE-DR4-2 PMD	124.7	Device supports requirements for 400GBASE-DR4-2 PHY	O.1	Yes [ ] No [ ]
*DR8	800GBASE-DR8 PMD	124.7	Device supports requirements for 800GBASE-DR8 PHY	O.1	Yes [ ] No [ ]
*DR82	800GBASE-DR8-2 PMD	124.7	Device supports requirements for 800GBASE-DR8-2 PHY	O.1	Yes [ ] No [ ]
…					

Change the title of 124.12.4 as follows:

124.12.4 PICS proforma tables for Physical Medium Dependent (PMD) sublayer and medium, type 400GBASE-DR4, 400GBASE-DR4-2, 800GBASE-DR8, and 800GBASE-DR8-2

124.12.4.1 PMD functional specifications

Change the row for item "F1" in the table in 124.12.4.1 as follows (unchanged rows not shown):

Item	Feature	Subclause	Value/Comment	Status	Support
F1	Compatible with 400GBASE-R, or 800GBASE-R PCS and PMA	124.1		M	Yes [ ]
…					

124.12.4.3 PMD to MDI optical specifications for 400GBASE-DR4

Change the table in 124.12.4.3 as follows:

Item	Feature	Subclause	Value/Comment	Status	Support
DDR1	Transmitter meets specifications in Table 124–6	124.7.1	Per definitions in 124.8	DR4:M	Yes [ ] N/A [ ]
DDR2	Receiver meets specifications in Table 124–7	124.7.2	Per definitions in 124.8	DR4:M	Yes [ ] N/A [ ]

Insert new subclauses 124.12.4.3a, 124.12.4.3b, and 124.12.4.3c after 124.12.4.3 as follows:

124.12.4.3a PMD to MDI optical specifications for 400GBASE-DR4-2

Item	Feature	Subclause	Value/Comment	Status	Support
EDR1	Transmitter meets specifications in Table 124–6	124.7.1	Per definitions in 124.8	DR42:M	Yes [ ] N/A [ ]
EDR2	Receiver meets specifications in Table 124–7	124.7.2	Per definitions in 124.8	DR42:M	Yes [ ] N/A [ ]

124.12.4.3b PMD to MDI optical specifications for 800GBASE-DR8

Item	Feature	Subclause	Value/Comment	Status	Support
FDR1	Transmitter meets specifications in Table 124–6	124.7.1	Per definitions in 124.8	DR8:M	Yes [ ] N/A [ ]
FDR2	Receiver meets specifications in Table 124–7	124.7.2	Per definitions in 124.8	DR8:M	Yes [ ] N/A [ ]

124.12.4.3c PMD to MDI optical specifications for 800GBASE-DR8-2

Item	Feature	Subclause	Value/Comment	Status	Support
GDR1	Transmitter meets specifications in Table 124–6	124.7.1	Per definitions in 124.8	DR82:M	Yes [ ] N/A [ ]
GDR2	Receiver meets specifications in Table 124–7	124.7.2	Per definitions in 124.8	DR82:M	Yes [ ] N/A [ ]

124.12.4.4 Optical measurement methods

Change the table in 124.12.4.4 as follows:

Item	Feature	Subclause	Value/Comment	Status	Support
OM1	Measurement cable	124.8	2 m to 5 m in length	M	Yes [ ]
OM2	Center wavelength and SMSR	124.8.2	Per IEC 61280-1-3 under modulated conditions	M	Yes [ ]
OM3	Average optical power	124.8.3	Per IEC 61280-1-1	M	Yes [ ]
OM4	OMA measurements	124.8.4	Each lane	M	Yes [ ]
OM5	Transmitter and dispersion eye closure for PAM4 (TDECQ)	124.8.5	Each lane	M	Yes [ ]
OM6	Extinction ratio	124.8.6	Each lane	M	Yes [ ]
OM7	Transmitter transition time	124.8.7	Each lane	M	Yes [ ]
OM8	Stressed receiver sensitivity	124.8.10	Each lane	M	Yes [ ]
OM9	Transmitter eye closure for PAM4 (TECQ)	124.8.5a	Each lane	DR42+ DR8+ DR82:M	Yes [ ] N/A [ ]
OM10	Transmitter overshoot and undershoot	124.8.5b	Each lane	DR42+ DR8+ DR82:M	Yes [ ] N/A [ ]
OM11	Transmitter power excursion	124.8.5c	Each lane	DR42+ DR8+ DR82:M	Yes [ ] N/A [ ]
OM12	Receiver sensitivity	124.8.9.2	Each lane	DR42+ DR8+ DR82:M	Yes [ ] N/A [ ]

124.12.4.6 Characteristics of the fiber optic cabling and MDI

Change the table in 124.12.4.6 as follows (some unchanged rows not shown):

Item	Feature	Subclause	Value/Comment	Status	Support
OC1	Fiber optic cabling	124.11	Meets requirements specified in Table 124–11	INS:M	Yes [ ] N/A [ ]
OC2	Maximum discrete reflectance	124.11.2.2	Meets requirements specified in Table 124–13	INS:M	Yes [ ] N/A [ ]
OC3	MDI layout	~~124.11.3.1~~ 124.11.3.1.1	Optical lane assignments per Figure 124–6	DR4+DR42:M	Yes [ ] N/A [ ]
OC4	MDI dimensions	124.11.3.2	Per IEC 61754-7-1 interface 7-1-9	DR4+DR42:M	Yes [ ] N/A [ ]
OC5	Cabling connector dimensions	124.11.3.2	Per IEC 61754-7-1 interface 7-1-1	(DR4+DR42)* INS:M	Yes [ ] N/A [ ]
OC6	MDI mating	124.11.3.2	MDI optically mates with plug on the cabling	DR4+DR42:M	Yes [ ] N/A [ ]
OC7	MDI layout	124.11.3.1.2	Optical lane assignments per Figure 124–6a	DR8+DR82:M	Yes [ ] N/A [ ]
OC8	MDI mating	124.11.3.3	MDI optically mates with plug on the cabling, performance grade Bm/1m	DR8+DR82:M	Yes [ ] N/A [ ]
OC9	MDI dimensions	124.11.3.3	Per ANSI/TIA-604-18-A designation FOCIS 18 P-1x16-1-8-1-1-1 and designation FOCIS 18 A-1-0 or designation FOCIS 18 R-1x16-1-8-1-1-2	DR8+DR82:M	Yes [ ] N/A [ ]
OC10	Cabling connector dimensions	124.11.3.3	Per ANSI/TIA-604-18-A designation FOCIS 18 P-1x16-1-8-2-1-1	(DR8+DR82)* INS:M	Yes [ ] N/A [ ]

Change the title of Clause 162 (added by IEEE Std 802.3ck-2022) as follows:

162. Physical Medium Dependent (PMD) sublayer and baseband medium, type 100GBASE-CR1, 200GBASE-CR2, ~~and~~ 400GBASE-CR4, and 800GBASE-CR8

162.1 Overview

Change the first three paragraphs of 162.1 as follows:

This clause specifies the 100GBASE-CR1 ~~PMD~~, ~~the~~ 200GBASE-CR2 ~~PMD~~, ~~the~~ 400GBASE-CR4, and 800GBASE-CR8 PMDs, and the baseband medium. The specifications for the ~~three~~ four PMDs are similar, except for the number of lanes and associated parameters and the MDI.

There are four associated annexes. Annex 162A provides information on parameters ~~with test points that may~~ that might not be testable in an implemented system, since the test points they are associated with are typically inaccessible. Annex 162B specifies test fixtures. Annex 162C specifies MDIs. Annex 162D describes host and cable assembly types.

When forming a complete Physical Layer, a PMD shall be connected as illustrated in Figure 162–1, to the appropriate sublayers (as specified in Table 162–1, Table 162–2, ~~and~~ Table 162–3, and Table 162–3a), to the medium through the appropriate MDI, and to the management functions that are optionally accessible through the management interface defined in Clause 45, or equivalent.

Insert new Table 162–3a after Table 162–3 as follows:

Table 162–3a—Physical Layer clauses associated with the 800GBASE-CR8 PMD

Associated clause	800GBASE-CR8
170—RS	Required
170—800GMII[a]	Optional
171—800GMII Extender	Optional
172—PCS for 800GBASE-R	Required
173—PMA for 800GBASE-R	Required
120F—800GAUI-8 C2C	Optional
73—Auto-Negotiation	Required

[a] The 800GMII is an optional interface. However, if the 800GMII is not implemented, a conforming implementation behaves functionally as though the RS and 800GMII were present.

Insert the following paragraph after the fifth paragraph of 162.1:

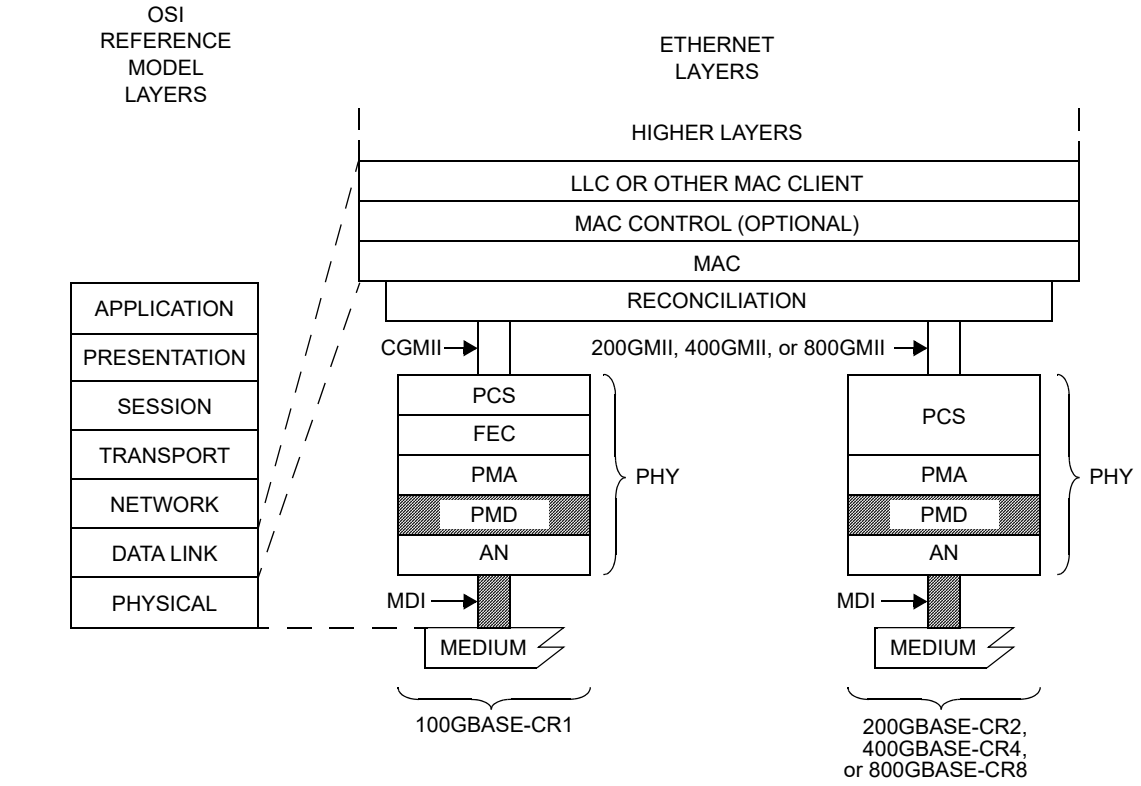
For the 800GBASE-CR8 PHY, in order to support the required frame loss ratio (see 1.4.344) of less than 6.2×10^{-11} for 64-octet frames with minimum interpacket gap, the PMD and the adjacent PMA are expected to detect bits from a compliant input signal at a BER lower than 2.4×10^{-4} assuming errors are sufficiently uncorrelated. This BER allocation enables a frame loss ratio lower than 3.4×10^{-12} after processing by the

PCS (Clause 172) if there are negligible errors due to other electrical interfaces (800GAUI-n). If the PMD and PMA create errors that are not sufficiently uncorrelated, the BER is required to be lower as appropriate to maintain a frame loss ratio lower than 3.4×10^{-12}.

Change last paragraph of 162.1 as follows:

Figure 162–1 shows the relationship of the ~~100GBASE-CR1, 200GBASE-CR2, and 400GBASE-CR4~~ PMD ~~sublayers~~ and MDI~~s~~ to the ISO/IEC Open System Interconnection (OSI) reference model.

Replace Figure 162–1 with the following figure:



200GMII = 200 Gb/s MEDIA INDEPENDENT INTERFACE
400GMII = 400 Gb/s MEDIA INDEPENDENT INTERFACE
800GMII = 800 Gb/s MEDIA INDEPENDENT INTERFACE
AN = AUTO-NEGOTIATION
CGMII = 100 Gb/s MEDIA INDEPENDENT INTERFACE
FEC = FORWARD ERROR CORRECTION
LLC = LOGICAL LINK CONTROL
MAC = MEDIA ACCESS CONTROL
MDI = MEDIUM DEPENDENT INTERFACE
PCS = PHYSICAL CODING SUBLAYER
PHY = PHYSICAL LAYER DEVICE
PMA = PHYSICAL MEDIUM ATTACHMENT
PMD = PHYSICAL MEDIUM DEPENDENT

Figure 162–1—100GBASE-CR1, 200GBASE-CR2, 400GBASE-CR4, and 800GBASE-CR8 relationship to the ISO/IEC Open Systems Interconnection (OSI) reference model and the IEEE 802.3 Ethernet model

162.2 Conventions

Change 162.2 as follows:

Clause 162 describes ~~three~~ four PMDs~~:~~, 100GBASE-CR1, 200GBASE-CR2, ~~and~~ 400GBASE-CR4, and 800GBASE-CR8, which have one, two, ~~and~~ four, and eight lanes, respectively. For efficient description, the parameter *n* is used to describe the number of lanes in a specific PMD. Accordingly, *n* = 1 for 100GBASE-CR1, *n* = 2 for 200GBASE-CR2, ~~and~~ *n* = 4 for 400GBASE-CR4, and *n* = 8 for 800GBASE-CR8.

The parameter *i* is used as an index or a suffix to identify a specific lane, and takes the values 0 to *n* – 1.

Within this clause, the unqualified term "PMD" refers to any of 100GBASE-CR1 PMD, 200GBASE-CR2 PMD, ~~or~~ 400GBASE-CR4 PMD, or 800GBASE-CR8 PMD.

Within this clause, the term FEC refers to either Clause 91 RS-FEC or ~~the~~ Clause 161 RS-FEC-Int for 100GBASE-CR1, ~~or~~ the RS-FEC within the Clause 119 PCS for 200GBASE-CR2 and 400GBASE-CR4, or the RS-FEC within the Clause 172 PCS for 800GBASE-CR8.

162.3 PMD service interfaces

Change the first paragraph of 162.3 as follows:

This subclause specifies the services provided by the 100GBASE-CR1, 200GBASE-CR2, ~~and~~ 400GBASE-CR4, and 800GBASE-CR8 PMDs. The service interfaces for these PMDs are described in an abstract manner and do not imply any particular implementation. The PMD service interface supports the exchange of encoded data between the PMA entity that resides just above the PMD, and the PMD entity. The PMD translates the encoded data to and from signals suitable for the specified medium.

Insert the following paragraph after the fourth paragraph of 162.3:

The 800GBASE-CR8 PMD service interface is an instance of the inter-sublayer service interface defined in 169.3, with eight parallel symbol streams (*n* = 8).

Insert the following paragraph after the eighth (now ninth) paragraph of 162.3:

The 800GBASE-CR8 PMD has eight parallel symbol streams, hence *i* = 0 to 7.

162.4 PCS requirements for Auto-Negotiation (AN) service interface

Change the text in 162.4 as follows:

The PCSs associated with the ~~100GBASE-CR1, 200GBASE-CR2, and 400GBASE-CR4~~ PMDs are required to support the AN service interface primitive AN_LINK.indication defined in 73.9. (See 82.6, ~~and~~ 119.6, and 172.6.)

100GBASE-CR1, 200GBASE-CR2, ~~and~~ 400GBASE-CR4, and 800GBASE-CR8 PHYs may be extended using CAUI-n/100GAUI-n C2C, 200GAUI-n C2C, ~~and~~ 400GAUI-n C2C, and 800GAUI-n C2C, respectively, as physical instantiations of the inter-sublayer service interface between devices. If such extension is used, then the AN_LINK(link_status).indication is relayed from the device with the PCS sublayer to the device with the AN sublayer by means at the discretion of the implementer. As examples, the

implementer may employ use of pervasive management or employ a dedicated electrical signal to relay the state of link_status as indicated by the PCS sublayer on one device to the AN sublayer on the other device.

162.5 Delay constraints

Change Table 162–4 as follows:

Table 162–4—Delay constraints

PMD	Maximum (bit times)[a]	Maximum (pause_quanta)[b]	Maximum (ns)
100GBASE-CR1	4 096	8	40.96
200GBASE-CR2	8 192	16	40.96
400GBASE-CR4	16 384	32	40.96
800GBASE-CR8	32 768	64	40.96

[a] One bit time is equal to 10 ps for 100GBASE-CR1, 5 ps for 200GBASE-CR2, ~~and~~ 2.5 ps for 400GBASE-CR4, and 1.25 ps for 800GBASE-CR8. (See 1.4.215 for the definition of bit time.)

[b] One pause_quantum is equal to 5.12 ns for 100GBASE-CR1, 2.56 ns for 200GBASE-CR2, ~~and~~ 1.28 ns for 400GBASE-CR4, and 0.64 ns for 800GBASE-CR8. (See 31B.2 for the definition of pause_quanta.)

162.6 Skew constraints

Insert new subclause 162.6.3 after 162.6.2 as follows:

162.6.3 Skew Constraints for 800GBASE-CR8

Skew and Skew Variation are defined in 169.5 and specified at the points SP1 to SP6 shown in Figure 169–5.

If the PMD service interface is physically instantiated so that the Skew at SP2 can be measured, then the Skew at SP2 is limited to 25 ns and the Skew Variation at SP2 is limited to 400 ps.

The Skew at SP3 (the transmitter MDI) shall be less than 36 ns and the Skew Variation at SP3 shall be less than 600 ps.

The Skew at SP4 (the receiver MDI) shall be less than 116 ns and the Skew Variation at SP4 shall be less than 3.4 ns.

If the PMD service interface is physically instantiated so that the Skew at SP5 can be measured, then the Skew at SP5 shall be less than 127 ns and the Skew Variation at SP5 shall be less than 3.6 ns.

For more information on Skew and Skew Variation see 169.5.

162.7 PMD MDIO function mapping

Change Table 162–5, Table 162–6, and Table 162–7, including footnotes, as follows:

Table 162–5—MDIO/PMD control variable mapping

MDIO control variable	PMA/PMD register name	Register/bit number	PMD control variable
Reset	PMA/PMD control 1	1.0.15	PMD_reset
Global PMD transmit disable	PMD transmit disable	1.9.0	Global_PMD_transmit_disable
PMD transmit disable 7 to PMD transmit disable 4[a]	PMD transmit disable	1.9.8:5	PMD_transmit_disable_7, PMD_transmit_disable_6, PMD_transmit_disable_5, PMD_transmit_disable_4
PMD transmit disable 3 to PMD transmit disable 2[b]	PMD transmit disable	1.9.4:3	PMD_transmit_disable_3, PMD_transmit_disable_2
PMD transmit disable 1[c]	PMD transmit disable	1.9.2	PMD_transmit_disable_1
PMD transmit disable 0	PMD transmit disable	1.9.1	PMD_transmit_disable_0

[a] Available only in 800GBASE-CR8.
[b] Available only in 400GBASE-CR4 and 800GBASE-CR8.
[c] Available only in 200GBASE-CR2, ~~and~~ 400GBASE-CR4, and 800GBASE-CR8.

Table 162–6—MDIO/PMD status variable mapping

MDIO status variable	PMA/PMD register name	Register/bit number	PMD status variable
Fault	PMA/PMD status 1	1.1.7	PMD_fault
Transmit fault	PMA/PMD status 2	1.8.11	PMD_transmit_fault
Receive fault	PMA/PMD status 2	1.8.10	PMD_receive_fault
Global PMD receive signal detect	PMD receive signal detect	1.10.0	Global_PMD_signal_detect
PMD receive signal detect 7 to PMD receive signal detect 4[a]	PMD receive signal detect	1.10.8:5	PMD_signal_detect_7, PMD_signal_detect_6, PMD_signal_detect_5, PMD_signal_detect_4
PMD receive signal detect 3 to PMD receive signal detect 2[b]	PMD receive signal detect	1.10.4:3	PMD_signal_detect_3, PMD_signal_detect_2
PMD receive signal detect 1[c]	PMD receive signal detect	1.10.2	PMD_signal_detect_1
PMD receive signal detect 0	PMD receive signal detect	1.10.1	PMD_signal_detect_0

[a] Available only in 800GBASE-CR8.
[b] Available only in 400GBASE-CR4 and 800GBASE-CR8.
[c] Available only in 200GBASE-CR2, ~~and~~ 400GBASE-CR4, and 800GBASE-CR8.

Table 162–7—MDIO/PMD control function mapping

MDIO variable	PMA/PMD register name	Register/bit number	PMD variable
Restart training	BASE-R PMD control	1.150.0	mr_restart_training
Training enable	BASE-R PMD control	1.150.1	mr_training_enable
Receiver status	BASE-R PMD status	1.151.0[a]	local_trained
Frame lock	BASE-R PMD status	1.151.1[a]	local_tf_lock
Start-up protocol status	BASE-R PMD status	1.151.2[a]	training
Training failure	BASE-R PMD status	1.151.3[a]	training_failure
Polynomial identifier	PMD training pattern, lanes 0 to ~~3~~ 7	1.1450.12:11[b]	identifier_i
Seed	PMD training pattern, lanes 0 to ~~3~~ 7	1.1450.15:14 1.1450.10:0[b]	seed_i
Initial condition request	BASE-R PAM4 PMD training LP control, lanes 0 to ~~3~~ 7	1.1120.13:12[b]	ic_req
Coefficient select	BASE-R PAM4 PMD training LP control, lanes 0 to ~~3~~ 7	1.1120.4:2[b]	coef_sel
Coefficient request	BASE-R PAM4 PMD training LP control, lanes 0 to ~~3~~ 7	1.1120.1:0[b]	coef_req
Receiver ready	BASE-R PAM4 PMD training LP status, lanes 0 to ~~3~~ 7	1.1220.15[b]	remote_rx_ready
Modulation and precoding status	BASE-R PAM4 PMD training LP status, lanes 0 to ~~3~~ 7	1.1220.11:10[b]	remote_tp_mode
Receiver frame lock	BASE-R PAM4 PMD training LP status, lanes 0 to ~~3~~ 7	1.1220.9[b]	remote_tf_lock
Modulation and precoding request	BASE-R PAM4 PMD training LD control, lanes 0 to ~~3~~ 7	1.1320.11:10[b]	local_tp_mode
Local receiver ready	BASE-R PAM4 PMD training LD status, lanes 0 to ~~3~~ 7	1.1420.15[b]	local_rx_ready
Initial condition status	BASE-R PAM4 PMD training LD status, lanes 0 to ~~3~~ 7	1.1420.8[b]	ic_sts
Coefficient select echo	BASE-R PAM4 PMD training LD status, lanes 0 to ~~3~~ 7	1.1420.5:3[b]	k
Coefficient status	BASE-R PAM4 PMD training LD status, lanes 0 to ~~3~~ 7	1.1420.2:0[b]	coef_sts

[a] Bit reference is provided for lane 0. Status bits for lanes 1 to 3 are located in the same register. Status bits for lanes 4 to 7 are located in BASE-R PMD status 2 register (Register 1.156).
[b] Address reference is provided for lane 0. Registers for lanes 1 to ~~3~~ 7 are located at ~~an~~ offsets from the lane 0 register.

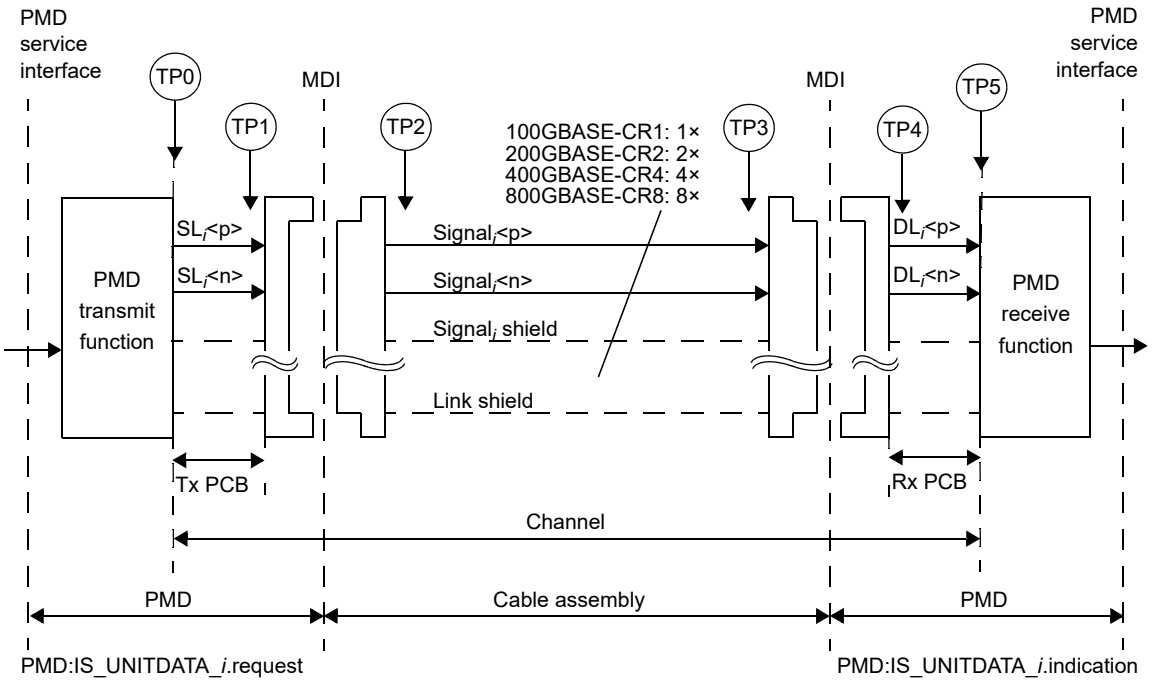
162.8 PMD functional specifications

162.8.1 Link block diagram

Change the first paragraph of 162.8.1 as follows:

One direction of a 100GBASE-CR1, 200GBASE-CR2, ~~or~~ 400GBASE-CR4, or 800GBASE-CR8 link is shown in Figure 162–2. The PMDs on both ends of the link have connected ground references. Each differential pair in the cable is separately shielded as illustrated in Figure 162–2. The signal shields are connected to ground contacts in the MDI plug connectors on both ends of the cable assembly.

Replace Figure 162–2 with the following figure:



NOTE—One direction is illustrated.

Figure 162–2—100GBASE-CR1, 200GBASE-CR2, 400GBASE-CR4, or 800GBASE-CR8 link

162.8.11 PMD control function

Insert a new item h) at the end of the lettered list in 162.8.11, as follows:

h) The default polynomials and seeds for the training pattern (see 136.8.11.1.3) on each lane are defined in 162.8.11.1.

Insert new subclause 162.8.11.1 at the end of 162.8.11 as follows:

162.8.11.1 Training pattern polynomials and seeds

The PRBS generator for each lane shall implement four generator polynomials. The polynomial used in each lane *i* is selected by the variable identifier_*i*.

At the start of the training pattern in each lane *i*, the state of the PRBS generator shall be set to the value of the variable seed_*i*. A value of all zeros is not valid.

Table 162–10a specifies the default identifier, the corresponding polynomial, and the recommended default value of seed_*i* for each lane *i*, as well as the first 13 symbols of the training pattern for each modulation and precoding mode created using the default polynomial and seed.

The training pattern is generated from the PRBS generator output as specified in 136.8.11.1.3.

Table 162–10a—Training pattern default polynomials and seeds

i	Default identifier	Polynomial, *G*(*x*)	Default seed_*i*[a]	Initial output, PAM2	Initial output, PAM4	Initial output, PAM4 with precoding
0	0[b]	$1+x+x^2+x^{12}+x^{13}$	0000010101011	0030330330000	1031320220111	1301200200101
1	1	$1+x^2+x^3+x^7+x^{13}$	0011101000001	3030303030333	3030213021333	3122012201212
2	2	$1+x^2+x^4+x^8+x^{13}$	1001000101100	0303333033030	1212332133031	1102120121301
3	3	$1+x^2+x^5+x^9+x^{13}$	0100010000010	3330300030330	2231210121221	2032013201110
4	0[b]	$1+x+x^2+x^{12}+x^{13}$	1111110100110	3030000303303	3030001313212	3122223012011
5	1	$1+x^2+x^3+x^7+x^{13}$	1100011101110	0003030003033	0113130013133	0103213103212
6	2	$1+x^2+x^4+x^8+x^{13}$	0000001101000	3300303000300	2300212111300	2131102323000
7	3	$1+x^2+x^5+x^9+x^{13}$	0011000100111	3333000333030	2232000322031	2033131202210

[a] The leftmost bit in the sequence corresponds to the initial value of S0 and the rightmost bit corresponds to the initial value of S12 in Figure 136–5.
[b] This training pattern is equivalent to the PRBS13Q test pattern defined in 120.5.11.2.1.

NOTE—The set of polynomials, and the default seed bits for identifiers 0 through 3, are identical to those specified in Table 136–8.

162.9 PMD electrical characteristics

162.9.2 Signal paths

Change the second paragraph of 162.9.2 as follows:

For 100GBASE-CR1, there is one differential lane in each direction for a total of two pairs, or four connections. For 200GBASE-CR2, there are two differential lanes in each direction for a total of four pairs, or eight connections. For 400GBASE-CR4, there are four differential lanes in each direction for a total of eight pairs, or ~~sixteen~~ 16 connections. For 800GBASE-CR8, there are eight differential lanes in each direction for a total of 16 pairs, or 32 connections.

162.9.4 Transmitter characteristics

Change footnote a in Table 162–11 as follows (unchanged rows and footnotes not shown):

Table 162–11—Summary of transmitter specifications at TP2

Parameter	Subclause reference	Value	Units
Signaling rate, each lane (range)	—	53.125 ± 50 ppm[a]	GBd
…			

[a] For a 100GBASE-CR1, 200GBASE-CR2, or 400GBASE-CR4 PMD in the same package as the PCS sublayer or for any 800GBASE-CR8 PMD. In other cases, the signaling rate is derived from the input to the PMD transmit function provided by the adjacent PMA sublayer.

162.9.5 Receiver characteristics

Change Table 162–15 as follows (most unchanged rows not shown):

Table 162–15—Summary of receiver specifications at TP3

Parameter	Subclause reference	Value	Units
Signaling rate, each lane (range) 100GBASE-CR1, 200GBASE-CR2, or 400GBASE-CR4 800GBASE-CR8	162.9.5.1	53.125 ± 100 ppm 53.125 ± 50 ppm	GBd GBd
…			
Differential-mode to common-mode return loss, *RLcd* (min)	162.9.5.6	Equation (162–18)	dB
NOTE—For 100GBASE-CR1, 200GBASE-CR2, or 400GBASE-CR4, although the PMD transmitter is specified with a signaling rate range of ±50 ppm when in the same package as the PCS, the signaling rate range may be ±100 ppm when derived from an intermediate interface (e.g., 100GAUI-4).			

162.9.5.1 Receiver signaling rate

Change 162.9.5.1 as follows:

A PHY shall comply with the receiver requirements of 162.9.5.2, 162.9.5.3, and 162.9.5.4 for any signaling rate in the range specified in Table 162–15 ~~53.125 GBd ± 100 ppm~~.

~~NOTE—Although the PMD transmitter is specified with a signaling rate range of ±50 ppm when in the same package as the PCS sublayer, the signaling rate range may be ±100 ppm, when derived from an intermediate interface (e.g., 100GAUI-4).~~

162.10 Channel characteristics

Change the second paragraph of 162.10 as follows:

Channel definitions apply for links between two PHYs of the same type: 100GBASE-CR1, 200GBASE-CR2, ~~or~~ 400GBASE-CR4, or 800GBASE-CR8.

162.11 Cable assembly characteristics

Change the text in 162.11 as follows:

Cable assemblies defined in this subclause contain insulated conductors terminated in a connector at each end for use as link segments between MDIs. Cable assemblies are primarily intended as point-to-point links between 100GBASE-CR1, 200GBASE-CR2, ~~or~~ 400GBASE-CR4, or 800GBASE-CR8 PHYs using controlled impedance cables.

~~Three~~ Four cable assembly types are specified:

a) 100GBASE-CR1: Cable assembly that supports single-lane links between two 100GBASE-CR1 PHYs with achievable cable length of at least 2 m.
b) 200GBASE-CR2: Cable assembly that supports two-lane links between two 200GBASE-CR2 PHYs with achievable cable length of at least 2 m.
c) 400GBASE-CR4: Cable assembly that supports four-lane links between two 400GBASE-CR4 PHYs with achievable cable length of at least 2 m.
d) 800GBASE-CR8: Cable assembly that supports eight-lane links between two 800GBASE-CR8 PHYs with achievable cable length of at least 2 m.

NOTE—It may be possible to construct compliant cable assemblies longer than indicated. Length of a cable assembly does not imply compliance to specifications.

100GBASE-CR1, 200GBASE-CR2, ~~and~~ 400GBASE-CR4, and 800GBASE-CR8 cable assembly types are described in Annex 162D. The MDIs are defined in Annex 162C.

For 100GBASE-CR1, 200GBASE-CR2, ~~and~~ 400GBASE-CR4, and 800GBASE-CR8, the lanes are AC-coupled. The AC-coupling shall be within the cable assembly. It is recommended that it is within the plug connectors. It should be noted that there may be various methods for AC-coupling in actual implementations. The low-frequency 3 dB cutoff of the AC-coupling shall be less than 50 kHz. It is recommended that the value of the coupling capacitors be 100 nF. The capacitor limits the inrush charge and baseline wander.

All cable assembly measurements are to be made between TP1 and TP4 with cable assembly test fixtures as specified in Annex 162B. These cable assembly specifications are based upon twinaxial cable characteristics, but other cable types are acceptable if the specifications of this subclause are met.

Table 162–18 provides a summary of the cable assembly characteristics for 100GBASE-CR1, 200GBASE-CR2, ~~and~~ 400GBASE-CR4, and 800GBASE-CR8, and references to the subclauses addressing each parameter.

The specifications for the ~~three~~ four cable assembly types are identical except the number of lanes.

162.12 MDI specifications

Change the text in 162.12 as follows:

The MDI couples the PMD (specified in 162.8 and 162.9) to the cable assembly (specified in 162.11).

100GBASE-CR1 has six specified MDI connectors: SFP112, SFP-DD112, DSFP, QSFP112, QSFP-DD800, and OSFP.

200GBASE-CR2 has five specified MDI connectors: SFP-DD112, DSFP, QSFP112, QSFP-DD800, and OSFP.

400GBASE-CR4 has three specified MDI connectors: QSFP112, QSFP-DD800, and OSFP.

800GBASE-CR8 has two specified MDI connectors: QSFP-DD800 and OSFP.

Annex 162C specifies the MDIs for 100GBASE-CR1, 200GBASE-CR2, 400GBASE-CR4, and 800GBASE-CR8.

Change the heading of 162.14 as follows:

162.14 Protocol implementation conformance statement (PICS) proforma for Clause 162, Physical Medium Dependent (PMD) sublayer and baseband medium, type 100GBASE-CR1, 200GBASE-CR2, ~~and~~ 400GBASE-CR4, and 800GBASE-CR8[8]

162.14.1 Introduction

Change the first paragraph of 162.14.1 as follows:

The supplier of a protocol implementation that is claimed to conform to Clause 162, Physical Medium Dependent (PMD) sublayer and baseband medium, type 100GBASE-CR1, 200GBASE-CR2, ~~and~~ 400GBASE-CR4, and 800GBASE-CR8, shall complete the following protocol implementation conformance statement (PICS) proforma.

162.14.2 Identification

162.14.2.2 Protocol summary

Change the table in 162.14.2.2 as follows:

Identification of protocol standard	IEEE Std 802.3df-2024, Clause 162, Physical Medium Dependent (PMD) sublayer and baseband medium, type 100GBASE-CR1, 200GBASE-CR2, ~~and~~ 400GBASE-CR4, and 800GBASE-CR8
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3df-2024.)	

Date of Statement	

[8] *Copyright release for PICS proformas*: Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

162.14.3 Major capabilities/options

Change the table in 162.14.3 as follows (some unchanged rows not shown):

Item[a]	Feature	Subclause	Value/Comment	Status	Support
…					
*CR4	400GBASE-CR4 PMD	162.1	Can operate as a 400GBASE-CR4 PMD	O.1	Yes [ ] No [ ]
*CR8	800GBASE-CR8 PMD	162.1	Can operate as an 800GBASE-CR8 PMD	O.1	Yes [ ] No [ ]
PMA100	100GBASE-P PMA	162.1	Device implements Clause 135 PMA for 100GBASE-P	CR1:M	Yes [ ] N/A [ ]
…					
PMA400	400GBASE-R PMA	162.1	Device implements Clause 120 PMA for 400GBASE-R	CR4:M	Yes [ ] N/A [ ]
PMA800	800GBASE-R PMA	162.1	Device implements Clause 173 PMA for 800GBASE-R	CR8:M	Yes [ ] N/A [ ]
*AUIPMD	100GAUI-n C2C, 200GAUI-n C2C, ~~or~~ 400GAUI-n C2C, or 800GAUI-n C2C	162.1	Service interface of PMA adjacent to PMD is physically instantiated	O.2	Yes [ ] No [ ]
~~AUIFEC~~	~~CAUI-n C2C or 100GAUI-n C2C~~	~~162.1~~	~~Service interface of PMA between PCS and RS-FEC is physically instantiated~~	~~!CR4:O.2~~	~~Yes [ ] No [ ] N/A [ ]~~
*nGMII	CGMII, 200GMII, ~~or~~ 400GMII, or 800GMII and RS	162.1	Interface is implemented or functionally equivalent	O.2	Yes [ ] No [ ]
…					
PCS400	400GBASE-R PCS	162.1	Device implements Clause 119 400GBASE-R PCS	CR4* nGMII:M	Yes [ ] N/A [ ]
PCS800	800GBASE-R PCS	162.1	Device implements Clause 172 800GBASE-R PCS	CR8* nGMII:M	Yes [ ] N/A [ ]
PCSAN	PCS requirements for AN service interface	162.4	PCS supports service interface primitive AN_LINK.indication	nGMII:M	Yes [ ] N/A [ ]
…					

[a] A "*" preceding an "Item" identifier indicates there are other PICS that depend on whether or not this item is supported.

Change the title of 162.14.4 as follows:

162.14.4 PICS proforma tables for Physical Medium Dependent (PMD) sublayer and baseband medium, type 100GBASE-CR1, 200GBASE-CR2, ~~and~~ 400GBASE-CR4, and 800GBASE-CR8

162.14.4.2 PMD control function

Change the rows for items PC2 and PC3 in the table in 162.14.4.2 as follows (unchanged rows not shown):

Item	Feature	Subclause	Value/Comment	Status	Support
…					
PC2	Training pattern	~~136.8.11.1.3~~ 162.8.11.1	Each lane implements four generator polynomials defined in ~~Table 136–8~~ Table 162–10a	M	Yes [ ]
PC3	Training pattern	~~136.8.11.1.3~~ 162.8.11.1	State set to the value of seed_*i* at the start of the training pattern	M	Yes [ ]
…					

Change the title of Clause 163 (added by IEEE Std 802.3ck-2022) as follows:

163. Physical Medium Dependent (PMD) sublayer and baseband medium, type 100GBASE-KR1, 200GBASE-KR2, ~~and~~ 400GBASE-KR4, and 800GBASE-KR8

163.1 Overview

Change the first three paragraphs in 163.1 as follows:

This clause specifies the 100GBASE-KR1 ~~PMD~~, ~~the~~ 200GBASE-KR2 ~~PMD~~, ~~the~~ 400GBASE-KR4 ~~PMD~~, and 800GBASE-KR8 PMDs and the baseband medium. The specifications for the ~~three~~ four PMDs are similar, except for the number of lanes and associated parameters and the MDI.

There are two associated annexes. Annex 163A provides measurement methods and test points for backplane and chip-to-chip interfaces. Annex 163B provides information on an example test fixture.

When forming a complete Physical Layer, a PMD shall be connected as illustrated in Figure 163–1, to the appropriate sublayers (as specified in Table 163–1, Table 163–2, ~~and~~ Table 163–3, and Table 163–3a), to the medium through the appropriate MDI, and to the management functions that are optionally accessible through the management interface defined in Clause 45, or equivalent.

Insert Table 163–3a after Table 163–3 as follows:

Table 163–3a—Physical Layer clauses associated with the 800GBASE-KR8 PMD

Associated clause	800GBASE-KR8
170—RS	Required
170—800GMII[a]	Optional
171—800GMII Extender	Optional
172—PCS for 800GBASE-R	Required
173—PMA for 800GBASE-R	Required
120F—800GAUI-8 C2C	Optional
73—Auto-Negotiation	Required

[a] The 800GMII is an optional interface. However, if the 800GMII is not implemented, a conforming implementation behaves functionally as though the RS and 800GMII were present.

Insert the following paragraph after the fifth paragraph of 163.1:

For the 800GBASE-KR8 PHY, in order to support the required frame loss ratio (see 1.4.344) of less than 6.2×10^{-11} for 64-octet frames with minimum interpacket gap, the PMD and the adjacent PMA are expected to detect bits from a compliant input signal at a BER lower than 2.4×10^{-4} assuming errors are sufficiently uncorrelated. This BER allocation enables a frame loss ratio lower than 3.4×10^{-12} after processing by the PCS (Clause 172) if there are negligible errors due to other electrical interfaces (800GAUI-n). If the PMD

and PMA create errors that are not sufficiently uncorrelated, the BER is required to be lower as appropriate to maintain a frame loss ratio lower than 3.4×10^{-12}.

Replace Figure 163–1 with the following figure:

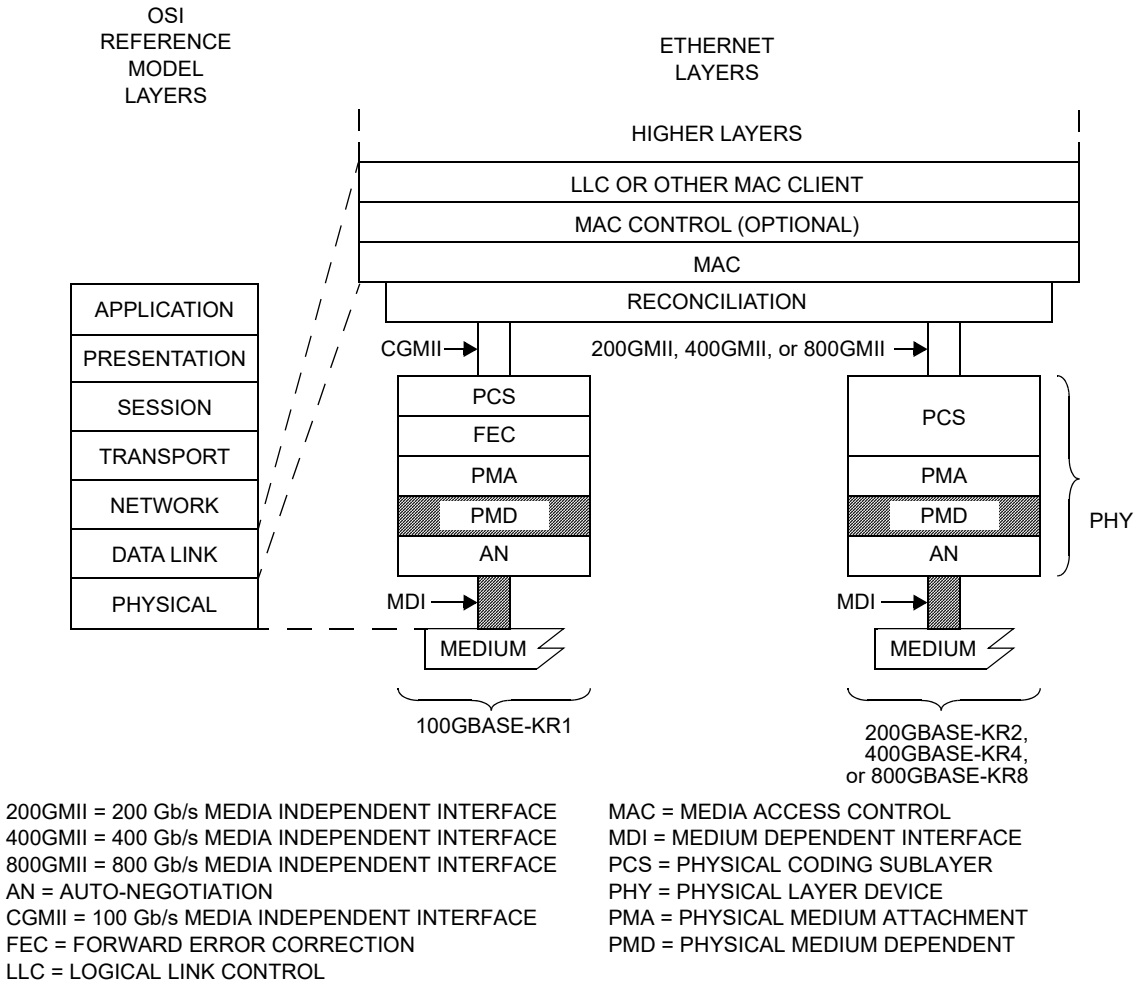


Figure 163–1—100GBASE-KR1, 200GBASE-KR2, 400GBASE-KR4, and 800GBASE-KR8 relationship to the ISO/IEC Open Systems Interconnection (OSI) reference model and the IEEE 802.3 Ethernet model

163.2 Conventions

Change 163.2 as follows:

Clause 163 describes ~~three~~ four PMDs, 100GBASE-KR1, 200GBASE-KR2, ~~and~~ 400GBASE-KR4, and 800GBASE-KR8, which have one, two, ~~and~~ four, and eight lanes, respectively. For efficient description, the parameter n is used to describe the number of lanes in a specific PMD. Accordingly, $n = 1$ for 100GBASE-KR1, $n = 2$ for 200GBASE-KR2, ~~and~~ $n = 4$ for 400GBASE-KR4, and $n = 8$ for 800GBASE-KR8.

The parameter i is used as an index or a suffix to identify a specific lane, and takes the values 0 to $n - 1$.

Within this clause, the unqualified term "PMD" refers to any of 100GBASE-KR1 PMD, 200GBASE-KR2 PMD, ~~or~~ 400GBASE-KR4 PMD, or 800GBASE-KR8 PMD.

Within this clause, the term FEC refers to either Clause 91 RS-FEC or ~~the~~ Clause 161 RS-FEC-Int for 100GBASE-KR1, ~~or~~ the RS-FEC within the Clause 119 PCS for 200GBASE-KR2 and 400GBASE-KR4, or the RS-FEC within the Clause 172 PCS for 800GBASE-KR8.

163.3 PMD service interfaces

Change 163.3 as follows:

The service interfaces of the 100GBASE-KR1, 200GBASE-KR2, ~~and~~ 400GBASE-KR4, and 800GBASE-KR8 PMDs are identical to those of the 100GBASE-CR1, 200GBASE-CR2, ~~and~~ 400GBASE-CR4, and 800GBASE-CR8 PMDs, respectively (see 162.3).

163.5 Delay constraints

Change Table 163–4 as follows:

Table 163–4—Delay constraints

PMD	Maximum (bit times)[a]	Maximum (pause_quanta)[b]	Maximum (ns)
100GBASE-KR1	4 096	8	40.96
200GBASE-KR2	8 192	16	40.96
400GBASE-KR4	16 384	32	40.96
800GBASE-KR8	32 768	64	40.96

[a] One bit time is equal to 10 ps for 100GBASE-KR1, 5 ps for 200GBASE-KR2, ~~and~~ 2.5 ps for 400GBASE-KR4, and 1.25 ps for 800GBASE-KR8. (See 1.4.215 for the definition of bit time.)

[b] One pause_quantum is equal to 5.12 ns for 100GBASE-KR1, 2.56 ns for 200GBASE-KR2, ~~and~~ 1.28 ns for 400GBASE-KR4, and 0.64 ns for 800GBASE-KR8. (See 31B.2 for the definition of pause_quanta.)

Change the second paragraph of 163.5 as follows:

Descriptions of overall system delay constraints can be found in 80.4 for 100GBASE-KR1 ~~and~~, in 116.4 for 200GBASE-KR2 and 400GBASE-KR4, and in 169.4 for 800GBASE-KR8.

163.6 Skew constraints

Insert new subclause 163.6.3 after 163.6.2 as follows:

163.6.3 Skew Constraints for 800GBASE-KR8

Skew and Skew Variation are defined in 169.5 and specified at the points SP1 to SP6 shown in Figure 169–5.

If the PMD service interface is physically instantiated so that the Skew at SP2 can be measured, then the Skew at SP2 is limited to 25 ns and the Skew Variation at SP2 is limited to 400 ps.

The Skew at SP3 (the transmitter MDI) shall be less than 36 ns and the Skew Variation at SP3 shall be less than 600 ps.

The Skew at SP4 (the receiver MDI) shall be less than 116 ns and the Skew Variation at SP4 shall be less than 3.4 ns.

If the PMD service interface is physically instantiated so that the Skew at SP5 can be measured, then the Skew at SP5 shall be less than 127 ns and the Skew Variation at SP5 shall be less than 3.6 ns.

For more information on Skew and Skew Variation see 169.5.

163.8 PMD functional specifications

163.8.1 Link block diagram

Change the text in 163.8.1 as follows:

One direction of a 100GBASE-KR1, 200GBASE-KR2, ~~or~~ 400GBASE-KR4, or 800GBASE-KR8 link is shown in Figure 163–2. The PMDs on both ends of the link have connected ground references.

Change the title of Figure 163–2 as follows:

Figure 163–2—100GBASE-KR1, 200GBASE-KR2, ~~or~~ 400GBASE-KR4, or 800GBASE-KR8 link

163.9 Electrical characteristics

163.9.2 Transmitter characteristics

Change footnote a in Table 163–5 as follows (unchanged rows and footnotes not shown):

Table 163–5—Summary of transmitter specifications at TP0v

Parameter	Reference	Value	Units
Signaling rate, each lane (range)		53.125 ± 50 ppm[a]	GBd
…			

[a] For a 100GBASE-KR1, 200GBASE-KR2, or 400GBASE-KR4 PMD in the same package as the PCS sublayer or for any 800GBASE-KR8 PMD. In other cases, the signaling rate is derived from the input to the PMD transmit function provided by the adjacent PMA sublayer.

163.9.3 Receiver characteristics

Change Table 163-8 as follows (most unchanged rows not shown):

Table 163–8—Summary of receiver specifications at TP5v

Parameter	Reference	Value	Units
Signaling rate, each lane (range) 100GBASE-KR1, 200GBASE-KR2, or 400GBASE-KR4 800GBASE-KR8	163.9.3.1	53.125 ± 100 ppm 53.125 ± 50 ppm	GBd GBd
…			
Jitter tolerance	163.9.3.6	Table 162–17	—
NOTE—For 100GBASE-KR1, 200GBASE-KR2, or 400GBASE-KR4, although the PMD transmitter is specified with a signaling rate range of ±50 ppm when in the same package as the PCS, the signaling rate range may be ±100 ppm when derived from an intermediate interface (e.g., 100GAUI-4).			

163.9.3.1 Receiver signaling rate

Change 163.9.3.1 as follows:

A PHY shall comply with the receiver requirements of 163.9.3.5 and 163.9.3.6 for any signaling rate in the range specified in Table 163–8.

~~NOTE—Although the PMD transmitter is specified with a signaling rate range of ±50 ppm when in the same package as the PCS sublayer, the signaling rate range may be ±100 ppm when derived from an intermediate interface (e.g., 100GAUI-4).~~

163.9.3.5 Receiver interference tolerance

Change item i) in the lettered list in 163.9.3.5 as follows:

i) The test pattern is the scrambled idle test pattern defined in 119.2.4.9 or 172.2.4.11.

163.10 Channel characteristics

Change 163.10 as follows:

Table 163–10 provides a summary of the channel characteristics ~~for 100GBASE-KR1, 200GBASE-KR2, and 400GBASE-KR4,~~ and references to the subclauses addressing each parameter.

163.11 MDI specifications

The MDI for the 100GBASE-KR1, 200GBASE-KR2, ~~and~~ 400GBASE-KR4, and 800GBASE-KR8 PHYs is an implementation-dependent direct electrical connection between the PMD and the medium. The MDI is composed of 2 × *n* differential pairs, one pair for the transmit function and one pair for the receive function on each lane, marked by TP0 and TP5 in Figure 163–2.

Change the title of 163.13 as follows:

163.13 Protocol implementation conformance statement (PICS) proforma for Clause 163, Physical Medium Dependent (PMD) sublayer and baseband medium, type 100GBASE-KR1, 200GBASE-KR2, ~~and~~ 400GBASE-KR4, and 800GBASE-KR8[9]

163.13.1 Introduction

Change the first paragraph of 163.13.1 as follows:

The supplier of a protocol implementation that is claimed to conform to Clause 163, Physical Medium Dependent (PMD) sublayer and baseband medium, type 100GBASE-KR1, 200GBASE-KR2, ~~and~~ 400GBASE-KR4, and 800GBASE-KR8, shall complete the following protocol implementation conformance statement (PICS) proforma.

163.13.2 Identification

163.13.2.2 Protocol summary

Change the table in 162.13.2.2 as follows:

Identification of protocol standard	IEEE Std 802.3df-2024, Clause 163, Physical Medium Dependent (PMD) sublayer and baseband medium, type 100GBASE-KR1, 200GBASE-KR2, ~~and~~ 400GBASE-KR4, and 800GBASE-KR8
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3df-2024.)	

Date of Statement	

[9] *Copyright release for PICS proformas*: Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

163.13.3 Major capabilities/options

Change the table in 163.13.3 as follows (some unchanged rows not shown):

Item[a]	Feature	Subclause	Value/Comment	Status	Support
…					
*KR4	400GBASE-KR4 PMD	163.1	Can operate as a 400GBASE-KR4 PMD	O.1	Yes [ ] No [ ]
*KR8	800GBASE-KR8 PMD	163.1	Can operate as an 800GBASE-KR8 PMD	O.1	Yes [ ] No [ ]
PMA100	100GBASE-R PMA	163.1	Device implements Clause 135 PMA for 100GBASE-P	KR1:M	Yes [ ] N/A [ ]
…					
PMA400	400GBASE-R PMA	163.1	Device implements Clause 120 PMA for 400GBASE-R	KR4:M	Yes [ ] N/A [ ]
PMA800	800GBASE-R PMA	163.1	Device implements Clause 173 PMA for 800GBASE-R	KR8:M	Yes [ ] N/A [ ]
*AUIPMD	100GAUI-n C2C, 200GAUI-n C2C, ~~or~~ 400GAUI-n C2C, or 800GAUI-n C2C	163.1	Service interface of PMA adjacent to PMD is physically instantiated	O.2	Yes [ ] No [ ]
~~AUIFEC~~	~~CAUI-n C2C or 100GAUI-n C2C~~	~~163.1~~	~~Service interface of PMA between PCS and RS-FEC is physically instantiated~~	~~!KR4:O.2~~	~~Yes [ ] No [ ] N/A []~~
*nGMII	CGMII, 200GMII, ~~or~~ 400GMII, or 800GMII, and RS	163.1	Interface is implemented or functionally equivalent	O.2	Yes [ ] No [ ]
…					
PCS400	400GBASE-R PCS	163.1	Device implements Clause 119 400GBASE-R PCS	KR4* nGMII:M	Yes [ ] N/A [ ]
PCS800	800GBASE-R PCS	163.1	Device implements Clause 172 800GBASE-R PCS	KR8* nGMII:M	Yes [ ] N/A [ ]
PCSAN	PCS requirements for AN service interface	163.4	PCS supports service interface primitive AN_LINK.indication	nGMII:M	Yes [ ] N/A [ ]
…					

[a] A "*" preceding an "Item" identifier indicates there are other PICS that depend on whether or not this item is supported.

Change the title of 163.13.4 as follows:

163.13.4 PICS proforma tables for Physical Medium Dependent (PMD) sublayer and baseband medium, type 100GBASE-KR1, 200GBASE-KR2, ~~and~~ 400GBASE-KR4, and 800GBASE-KR8

163.13.4.2 PMD control function

Change the rows for items PC2 and PC3 in the table in 163.13.4.2 as follows (unchanged rows not shown):

Item	Feature	Subclause	Value/Comment	Status	Support
…					
PC2	Training pattern	~~136.8.11.1.3~~ 162.8.11.1	Each lane implements four generator polynomials defined in ~~Table 136–8~~ Table 162–10a	M	Yes [ ]
PC3	Training pattern	~~136.8.11.1.3~~ 162.8.11.1	State set to the value of seed_*i* at the start of the training pattern	M	Yes [ ]
…					

Change the title of Clause 167 (added by IEEE Std 802.3db-2022) as follows:

167. Physical Medium Dependent (PMD) sublayer and medium, type 100GBASE-VR1, 200GBASE-VR2, 400GBASE-VR4, 800GBASE-VR8, 100GBASE-SR1, 200GBASE-SR2, ~~and~~ 400GBASE-SR4, and 800GBASE-SR8

167.1 Overview

Change the text of 167.1 as follows:

This clause specifies the 100GBASE-VR1, 200GBASE-VR2, 400GBASE-VR4, 800GBASE-VR8, 100GBASE-SR1, 200GBASE-SR2, ~~and~~ 400GBASE-SR4, and 800GBASE-SR8 PMDs together with the multimode fiber medium. The optical signals generated by these PMD types are modulated using a 4-level pulse amplitude modulation (PAM4) format. The PMD sublayers provide point-to-point 100, 200, ~~and~~ 400, and 800 Gigabit Ethernet links over one, two, ~~or~~ four, or eight pairs of multimode fiber, respectively.

When forming a complete Physical Layer, a PMD shall be connected to the appropriate PMA, as shown in Table 167–1, ~~or~~ Table 167–2, or Table 167–2a, to the medium through the MDI and optionally with the management functions that may be accessible through the management interface defined in Clause 45, or equivalent. Figure 167–1 shows the relationship of the PMDs and MDIs (shown shaded) with other sublayers to the ISO/IEC Open System Interconnection (OSI) reference model. 100 Gigabit Ethernet is introduced in Clause 80 and the purpose of each PHY sublayer is summarized in 80.2. 200 Gigabit Ethernet and 400 Gigabit Ethernet are introduced in Clause 116 and the purpose of each PHY sublayer is summarized in 116.2. 800 Gigabit Ethernet is introduced in Clause 169 and the purpose of each PHY sublayer is summarized in 169.2.

100GBASE-VR1, 200GBASE-VR2, 400GBASE-VR4, 100GBASE-SR1, 200GBASE-SR2, and 400GBASE-SR4 PHYs with the optional Energy-Efficient Ethernet (EEE) fast wake capability may enter the Low Power Idle (LPI) mode to conserve energy during periods of low link utilization (see Clause 78). The deep sleep mode of EEE is not supported. 800GBASE-VR8 and 800GBASE-SR8 PHYs do not support EEE capability.

The 100GBASE-VR1, 200GBASE-VR2, ~~and~~ 400GBASE-VR4, and 800GBASE-VR8 sublayers provide point-to-point 100, 200, ~~and~~ 400, and 800 Gigabit Ethernet links over one, two, ~~or~~ four, or eight pairs of multimode fiber, respectively, up to at least 30 m on OM3, 50 m on OM4, and 50 m on OM5 (see 167.7). The 100GBASE-SR1, 200GBASE-SR2, ~~and~~ 400GBASE-SR4, and 800GBASE-SR8 sublayers provide point-to-point 100, 200, ~~and~~ 400, and 800 Gigabit Ethernet links over one, two, ~~or~~ four, or eight pairs of multimode fiber, respectively, up to at least 60 m on OM3, 100 m on OM4, and 100 m on OM5 (see 167.7).

Further relevant information may be found in Clause 1 (terminology and conventions, references, definitions, and abbreviations) and Annex A (bibliography, referenced as [B1], [B2], etc.).

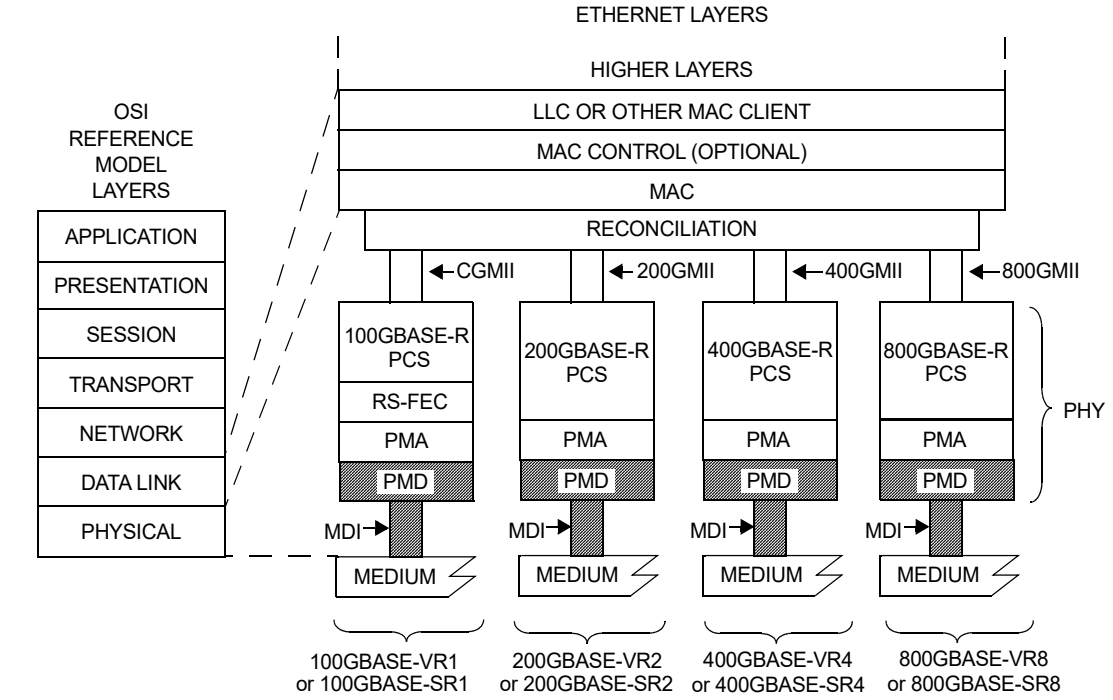
Insert new Table 167–2a after Table 167–2 as follows:

Table 167–2a—Physical Layer clauses associated with the 800GBASE-VR8 and 800GBASE-SR8 PMDs

Associated clause	800GBASE-VR8, 800GBASE-SR8	Status
170	RS	Required
170	800GMII[a]	Optional
171	800GMII Extender	Optional
172	800GBASE-R PCS	Required
173	800GBASE-R PMA	Required
120F	800GAUI-8 C2C	Optional
120G	800GAUI-8 C2M	Optional

[a] The 800GMII is an optional interface. However, if the appropriate interface is not implemented, a conforming implementation behaves functionally as though the RS and 800GMII was present.

Replace Figure 167–1 with the following figure:



800GMII = 800 Gb/s MEDIA INDEPENDENT INTERFACE
400GMII = 400 Gb/s MEDIA INDEPENDENT INTERFACE
200GMII = 200 Gb/s MEDIA INDEPENDENT INTERFACE
CGMII = 100 Gb/s MEDIA INDEPENDENT INTERFACE
LLC = LOGICAL LINK CONTROL
MAC = MEDIA ACCESS CONTROL
MDI = MEDIUM DEPENDENT INTERFACE
PCS = PHYSICAL CODING SUBLAYER
PHY = PHYSICAL LAYER DEVICE
PMA = PHYSICAL MEDIUM ATTACHMENT
PMD = PHYSICAL MEDIUM DEPENDENT
RS-FEC = REED-SOLOMON FORWARD ERROR CORRECTION
VR = PMD FOR MULTIMODE FIBER — 50 m
SR = PMD FOR MULTIMODE FIBER — 100 m

Figure 167–1—100GBASE-VR1, 200GBASE-VR2, 400GBASE-VR4, 800GBASE-VR8, 100GBASE-SR1, 200GBASE-SR2, 400GBASE-SR4, and 800GBASE-SR8 PMD relationship to the ISO/IEC Open Systems Interconnection (OSI) reference model and the IEEE 802.3 Ethernet model

167.1.1 Bit error ratio

Insert a new paragraph at the end of 167.1.1 as follows:

For the 800GBASE-VR8 and 800GBASE-SR8 PMDs, the bit error ratio (BER) when processed by the PMA (Clause 173) shall be less than 2.4×10^{-4} provided that the error statistics are sufficiently random that this results in a frame loss ratio (see 1.4.344) of less than 3.4×10^{-12} for 64-octet frames with minimum interpacket gap when processed according to Clause 173 and then Clause 172. For a complete Physical Layer, the frame loss ratio may be degraded to 6.2×10^{-11} for 64-octet frames with minimum interpacket gap due to additional errors from the electrical interfaces. If the error statistics are not sufficiently random to meet this requirement, then the BER shall be less than that required to give a frame loss ratio of less than 3.4×10^{-12} for 64-octet frames with minimum interpacket gap.

167.2 Physical Medium Dependent (PMD) service interface

Change the first paragraph in 167.2 as follows:

This subclause specifies the services provided by the 100GBASE-VR1, 200GBASE-VR2, 400GBASE-VR4, 800GBASE-VR8, 100GBASE-SR1, 200GBASE-SR2, ~~and~~ 400GBASE-SR4, and 800GBASE-SR8 PMDs. The service interfaces for these PMDs are described in an abstract manner and do not imply any particular implementation. The PMD service interface supports the exchange of encoded data between the PMA entity that resides just above the PMD, and the PMD entity. The PMD translates the encoded data to and from signals suitable for the specified medium.

Insert a new paragraph after the fourth paragraph in 167.2 as follows:

The 800GBASE-VR8 or 800GBASE-SR8 PMD service interface is an instance of the inter-sublayer service interface defined in 169.3, with eight parallel symbol streams (n = 8).

Insert a new paragraph after the eighth (now ninth) paragraph in 167.2 as follows:

The 800GBASE-VR8 or 800GBASE-SR8 PMD has eight parallel symbol streams, hence i = 0 to 7.

167.3 Delay and Skew

167.3.1 Delay constraints

Insert a new paragraph after the fourth paragraph in 167.3.1 as follows:

The sum of the transmit and receive delays at one end of the link contributed by the 800GBASE-VR8 or 800GBASE-SR8 PMD including 2 m of fiber in one direction shall be no more than 16 384 bit times (32 pause_quanta or 20.48 ns).

Change the last paragraph in 167.3.1 as follows:

Descriptions of overall system delay constraints and the definitions for bit times and pause_quanta can be found in 80.4 for 100GBASE-VR1 and 100GBASE-SR1, ~~and~~ in 116.4~~ and its references~~ for 200GBASE-VR2, 200GBASE-SR2, 400GBASE-VR4, and 400GBASE-SR4, and in 169.4 for 800GBASE-VR8 and 800GBASE-SR8.

167.3.2 Skew constraints

Change 167.3.2 as follows:

The Skew (relative delay) between the PCS or FEC lanes is kept within limits so that the information on the PCS or FEC lanes can be reassembled by the PCS or FEC. The Skew Variation also needs to be limited to ensure that a given PCS or FEC lane always traverses the same physical lane.

167.3.2.1 Skew constraints for 100GBASE-VR1, 100GBASE-SR1, 200GBASE-VR2, 200GBASE-SR2, 400GBASE-VR4, and 400GBASE-SR4

Skew and Skew Variation are defined in 80.5 and 116.5 and specified at the points SP1 to SP6 shown in Figure 80–8 and Figure 116–5.

If the PMD service interface is physically instantiated so that the Skew at SP2 can be measured, then the Skew at SP2 is limited to 43 ns and the Skew Variation at SP2 is limited to 400 ps. For 100GBASE-VR1

and 100GBASE-SR1, since the signal at the PMD service interface represents a serial bit stream, there is no Skew Variation at this point.

The Skew at SP3 (the transmitter MDI) shall be less than 54 ns and the Skew Variation at SP3 shall be less than 600 ps.

The Skew at SP4 (the receiver MDI) shall be less than 134 ns and the Skew Variation at SP4 shall be less than 3.4 ns.

If the PMD service interface is physically instantiated so that the Skew at SP5 can be measured, then the Skew at SP5 shall be less than 145 ns and the Skew Variation at SP5 shall be less than 3.6 ns. For 100GBASE-VR1 and 100GBASE-SR1, since the signal at the PMD service interface represents a serial bit stream, there is no Skew Variation at this point.

For more information on Skew and Skew Variation see 80.5 and 116.5.

167.3.2.2 Skew constraints for 800GBASE-VR8 and 800GBASE-SR8

Skew and Skew Variation are defined in 169.5 and specified at the points SP1 to SP6 shown in Figure 169–4.

If the PMD service interface is physically instantiated so that the Skew at SP2 can be measured, then the Skew at SP2 is limited to 25 ns and the Skew Variation at SP2 is limited to 400 ps.

The Skew at SP3 (the transmitter MDI) shall be less than 36 ns and the Skew Variation at SP3 shall be less than 600 ps.

The Skew at SP4 (the receiver MDI) shall be less than 116 ns and the Skew Variation at SP4 shall be less than 3.4 ns.

If the PMD service interface is physically instantiated so that the Skew at SP5 can be measured, then the Skew at SP5 shall be less than 127 ns and the Skew Variation at SP5 shall be less than 3.6 ns.

For more information on Skew and Skew Variation see 169.5.

167.5 PMD functional specifications

167.5.1 PMD block diagram

Change the first paragraph in 167.5.1 as follows:

The PMD block diagram for 400GBASE-VR4 or 400GBASE-SR4 is shown in Figure 167–2. The block diagrams for ~~200GBASE-VR2~~ 100GBASE-VR1 and ~~200GBASE-SR2~~ 100GBASE-SR1 are equivalent to Figure 167–2, but for ~~two lanes~~ one lane per direction. The block diagrams for ~~100GBASE-VR1~~ 200GBASE-VR2 and ~~100GBASE-VR1~~ 200GBASE-SR2 are equivalent to Figure 167–2, but for ~~one lane~~ two lanes per direction. The block diagrams for 800GBASE-VR8 and 800GBASE-SR8 are equivalent to Figure 167–2, but for eight lanes per direction.

167.5.2 PMD transmit function

Change 167.5.2 as follows:

The PMD Transmit function shall convert the one, two, ~~or~~ four, or eight symbol streams requested by the PMD service interface messages PMD:IS_UNITDATA_*i*.request into one, two, ~~or~~ four, or eight separate optical signals. The 100GBASE-VR1 and 100GBASE-SR1 PMDs have a single symbol stream, hence $i = 0$. The 200GBASE-VR2 and 200GBASE-SR2 PMDs have two parallel symbol streams, hence $i = 0$ to 1. The 400GBASE-VR4 and 400GBASE-SR4 PMDs have four parallel symbol streams, hence $i = 0$ to 3. The 800GBASE-VR8 and 800GBASE-SR8 PMDs have eight parallel symbol streams, hence $i = 0$ to 7. Each optical signal shall then be delivered to the MDI, which contains one, two, ~~or~~ four, or eight parallel light paths for transmit, according to the transmit optical specifications in this clause. The four optical power levels in each signal in order from lowest to highest shall correspond to tx_symbol values zero, one, two, and three, respectively.

167.5.3 PMD receive function

Change 167.5.3 as follows:

The PMD Receive function shall convert the one, two, ~~or~~ four, or eight parallel optical signals received from the MDI into one, two, ~~or~~ four, or eight separate symbol streams for delivery to the PMD service interface using the messages PMD:IS_UNITDATA_0.indication to PMD:IS_UNITDATA_*i*.indication, all according to the receive optical specifications in this clause. The four optical power levels in each signal in order from lowest to highest shall correspond to rx_symbol values zero, one, two, and three, respectively.

167.5.4 PMD global signal detect function

Change the second paragraph in 167.5.4 as follows:

SIGNAL_DETECT shall be a global indicator of the presence of optical signals on all lanes. The value of the SIGNAL_DETECT parameter shall be generated according to the conditions defined in Table 167–5. The PMD receiver is not required to verify whether a compliant 100GBASE-VR1, 200GBASE-VR2, 400GBASE-VR4, 800GBASE-VR8, 100GBASE-SR1, 200GBASE-SR2, ~~or~~ 400GBASE-SR4, or 800GBASE-SR8 signal is being received. This standard imposes no response time requirements on the generation of the SIGNAL_DETECT parameter.

Change Table 167–5 as follows:

Table 167–5—SIGNAL_DETECT value definition

Receive conditions	SIGNAL_DETECT value
For any lane; Average optical power at TP3 ≤ –30 dBm	FAIL
For all lanes; [(Optical power at TP3 ≥ average receive power, each lane (min) in Table 167–8) AND (compliant 100GBASE-VR1, 200GBASE-VR2, 400GBASE-VR4, 800GBASE-VR8, 100GBASE-SR1, 200GBASE-SR2, ~~or~~ 400GBASE-SR4, or 800GBASE-SR8 signal input)]	OK
All other conditions	Unspecified

167.6 Lane assignments

Change 167.6 as follows:

There are no lane assignments (within a group of transmit or receive lanes) for 200GBASE-VR2, 400GBASE-VR4, 800GBASE-VR8, 200GBASE-SR2, ~~or~~ 400GBASE-SR4, or 800GBASE-SR8. While it is expected that a PMD will map electrical lane *i* to optical lane *i* and vice versa, there is no need to define the physical ordering of the lanes, as the PCS sublayer is capable of receiving the lanes in any arrangement. The positioning of transmit and receive lanes at the MDI is specified in 167.10.3.1 and 167.10.3.1a.

Change the title and text of 167.7 as follows:

167.7 PMD to MDI optical specifications for 100GBASE-VR1, 200GBASE-VR2, 400GBASE-VR4, 800GBASE-VR8, 100GBASE-SR1, 200GBASE-SR2, ~~and~~ 400GBASE-SR4, and 800GBASE-SR8

The operating ranges for the 100GBASE-VR1, 200GBASE-VR2, 400GBASE-VR4, 800GBASE-VR8, 100GBASE-SR1, 200GBASE-SR2, ~~and~~ 400GBASE-SR4, and 800GBASE-SR8 PMDs are defined in Table 167–6. A compliant PMD operates on 50/125 µm multimode fibers, type A1a.2 (OM3), type A1a.3 (OM4), or type A1a.4 (OM5), according to the specifications defined in Table 167–14. A PMD that exceeds the operating range requirement while meeting all other optical specifications is considered compliant (e.g., a 100GBASE-SR1 PMD operating at 120 m meets the operating range requirement of 0.5 m to 100 m).

Change Table 167–6 as follows:

Table 167–6—Operating range

PMD type	Required operating range[a]
100GBASE-VR1 200GBASE-VR2 400GBASE-VR4 800GBASE-VR8	0.5 m to 30 m for OM3
	0.5 m to 50 m for OM4
	0.5 m to 50 m for OM5
100GBASE-SR1 200GBASE-SR2 400GBASE-SR4 800GBASE-SR8	0.5 m to 60 m for OM3
	0.5 m to 100 m for OM4
	0.5 m to 100 m for OM5

[a] The RS-FEC correction function may not be bypassed for any operating distance.

167.7.1 Transmitter optical specifications

Change the first paragraph in 167.7.1 as follows:

Each lane of a 100GBASE-VR1, 200GBASE-VR2, 400GBASE-VR4, 800GBASE-VR8, 100GBASE-SR1, 200GBASE-SR2, ~~and~~ 400GBASE-SR4, and 800GBASE-SR8 transmitter shall meet the specifications in Table 167–7 per the definitions in 167.8.

Change Table 167–7 as follows:

Table 167–7—Transmit characteristics

Description	100GBASE-VR1 200GBASE-VR2 400GBASE-VR4 800GBASE-VR8	100GBASE-SR1 200GBASE-SR2 400GBASE-SR4 800GBASE-SR8	Unit
Signaling rate, each lane (range) Other PMDs 800GBASE-VR8, 800GBASE-SR8 PMDs	53.125 ± 100 ppm 53.125 ± 50 ppm		GBd GBd
Modulation format	PAM4		—
Center wavelength (range)	842 to 948	844 to 863	nm
RMS spectral width[a] (max)	0.65	0.6	nm
Average launch power, each lane (max)	4		dBm
Average launch power, each lane (min)	–4.6		dBm
Outer Optical Modulation Amplitude (OMA_{outer}), each lane (max)	3.5		dBm
Outer Optical Modulation Amplitude (OMA_{outer}), each lane (min) For max (TECQ, TDECQ) ≤ 1.8 dB For 1.8 < max (TECQ, TDECQ) ≤ 4.4 dB	 –2.6 –4.4 + max (TECQ, TDECQ)		 dBm dBm
Transmitter and dispersion eye closure for PAM4 (TDECQ), each lane (max)	4.4	4.4	dB
Transmitter eye closure for PAM4 (TECQ), each lane (max)	4.4		dB
Overshoot/undershoot (max)	29		%
Transmitter power excursion, each lane (max)	2.3		dBm
Extinction ratio, each lane (min)	2.5		dB
Transmitter transition time, each lane (max)	17		ps
Average launch power of OFF transmitter, each lane (max)	–30		dBm
$RIN_{14}OMA$ (max)	–132		dB/Hz
Optical return loss tolerance (max)	14		dB
Encircled flux[b]	≥ 86% at 19 μm ≤ 30% at 4.5 μm		—

[a] RMS spectral width is the standard deviation of the spectrum.
[b] If measured into type A1a.2 or type A1a.3, or A1a.4, 50 μm fiber, in accordance with IEC 61280-1-4.

167.7.2 Receiver optical specifications

Change the first paragraph of 167.7.2 as follows:

Each lane of a 100GBASE-VR1, 200GBASE-VR2, 400GBASE-VR4, 800GBASE-VR8, 100GBASE-SR1, 200GBASE-SR2, ~~and~~ 400GBASE-SR4, and 800GBASE-SR8 receiver shall meet the specifications in Table 167–8 per the definitions in 167.8.

Change Table 167–8 as follows:

Table 167–8—Receive characteristics

Description	**100GBASE-VR1 200GBASE-VR2 400GBASE-VR4 800GBASE-VR8**	**100GBASE-SR1 200GBASE-SR2 400GBASE-SR4 800GBASE-SR8**	**Unit**
Signaling rate, each lane (range) Other PMDs 800GBASE-VR8, 800GBASE-SR8 PMDs	53.125 ± 100 ppm 53.125 ± 50 ppm		GBd GBd
Modulation format	PAM4		—
Center wavelength (range)	842 to 948		nm
Damage threshold[a] (min)	5		dBm
Average receive power, each lane (max)	4		dBm
Average receive power, each lane[b] (min)	–6.3	–6.4	dBm
Receive power, each lane (OMA_{outer}) (max)	3.5		dBm
Receiver reflectance (max)	–15		dB
Receiver sensitivity (OMA_{outer}) (max) For TECQ ≤ 1.8 dB For 1.8 < TECQ ≤ 4.4 dB	 –4.4 –6.2 + TECQ	 –4.6 –6.4 + TECQ	 dBm dBm
Stressed receiver sensitivity (OMA_{outer})[c] (max)	–1.8	–2	dBm
Conditions of stressed receiver sensitivity test:[d]			
Stressed eye closure for PAM4 (SECQ), lane under test	4.4		dB
OMA_{outer} of each aggressor lane	3.5		dBm

[a] The receiver shall be able to tolerate, without damage, continuous exposure to an optical input signal having this average power level on one lane. The receiver does not have to operate correctly at this input power.
[b] Average receive power, each lane (min) is not the principal indicator of signal strength. A received power below this value cannot be compliant; however, a value above this does not ensure compliance.
[c] Measured with conformance test signal at TP3 (see 167.8.14) for the BER specified in 167.1.1.
[d] These test conditions are for measuring stressed receiver sensitivity. They are not characteristics of the receiver.

167.7.3 Illustrative link power budget

Change the first paragraph in 167.7.3 as follows:

An illustrative power budget and penalties for 100GBASE-VR1, 200GBASE-VR2, 400GBASE-VR4, 800GBASE-VR8, 100GBASE-SR1, 200GBASE-SR2, ~~and~~ 400GBASE-SR4, and 800GBASE-SR8 channels are shown in Table 167–9.

Change Table 167–9 as follows:

Table 167–9—Illustrative link power ~~budget~~ budgets

Parameter	100GBASE-VR1 200GBASE-VR2 400GBASE-VR4 800GBASE-VR8			100GBASE-SR1 200GBASE-SR2 400GBASE-SR4 800GBASE-SR8			Unit
	OM3	OM4	OM5	OM3	OM4	OM5	
Effective modal bandwidth at 850 nm[a]	2000	4700		2000	4700		MHz · km
Power budget (for max TDECQ)	6.2			6.4			dB
Operating distance	0.5 to 30	0.5 to 50		0.5 to 60	0.5 to 100		m
Channel insertion loss[b]	1.6	1.7		1.7	1.8		dB
Allocation for penalties[c] (for max TDECQ)	4.5			4.6			dB
Additional insertion loss allowed	0.1	0		0.1	0		dB

[a] Per IEC 60793-2-10, see Table 167–15 for information on effective modal bandwidth at other wavelengths.
[b] The channel insertion loss is calculated using the maximum distance specified in Table 167–6 and cabled optical fiber attenuation of 3 dB/km at 850 nm plus an allocation for connection and splice loss given in 167.10.2.2.1.
[c] Link penalties are used for link budget calculations. They are not requirements and are not meant to be tested.

167.8 Definition of optical parameters and measurement methods

167.8.1 Test patterns for optical parameters

Change Table 167–10 as follows:

Table 167–10—Test patterns

Pattern	Pattern description	Defined in
Square wave	Square wave (8 threes, 8 zeros)	120.5.11.2.4
3	PRBS31Q	120.5.11.2.2
4	PRBS13Q	120.5.11.2.1
5	Scrambled idle encoded by RS-FEC	82.2.11 and 91, ~~or~~ 119.2.4.9, or 172.2.4.11
6	SSPRQ	120.5.11.2.3

Change Table 167–11 as follows:

Table 167–11—Test-pattern definitions and related subclauses

Parameter	Pattern	Related subclause
Wavelength, spectral width	3, 4, 5, 6, or valid ~~100GBASE-VR1, 200GBASE-VR2, 400GBASE-VR4, 100GBASE-SR1, 200GBASE-SR2, or 400GBASE-SR4~~ 100GBASE-R, 200GBASE-R, 400GBASE-R, or 800GBASE-R signal	167.8.3
Average optical power	3, 4, 5, 6, or valid ~~100GBASE-VR1, 200GBASE-VR2, 400GBASE-VR4, 100GBASE-SR1, 200GBASE-SR2, or 400GBASE-SR4~~ 100GBASE-R, 200GBASE-R, 400GBASE-R, or 800GBASE-R signal	167.8.4
Outer Optical Modulation Amplitude (OMA_{outer})	4 or 6	167.8.5
Transmitter and dispersion eye closure for PAM4 (TDECQ)	6	167.8.6
Transmitter eye closure for PAM4 (TECQ)	6	167.8.7
Overshoot/undershoot	6	167.8.8
Transmitter power excursion	6	167.8.9
Extinction ratio	4 or 6	167.8.10
Transmitter transition time	Square wave or 6	167.8.11
$RIN_{14}OMA$	Square wave	167.8.12
Receiver sensitivity	3 or 5	167.8.13
Stressed receiver sensitivity	3, 5, or valid ~~100GBASE-VR1, 200GBASE-VR2, 400GBASE-VR4, 100GBASE-SR1, 200GBASE-SR2, or 400GBASE-SR4~~ 100GBASE-R, 200GBASE-R, 400GBASE-R, or 800GBASE-R signal	167.8.14
Stressed eye closure (SEC), calibration	6	167.8.14

167.8.6 Transmitter and dispersion eye closure for PAM4 (TDECQ).

Change Table 167–12 as follows:

Table 167–12—The 3 dB bandwidth f_A of the fiber emulation filter for TDECQ measurement

PMD type	Center wavelength (range) (nm)	3 dB bandwidth f_A (GHz)
100GBASE-VR1 200GBASE-VR2 400GBASE-VR4 800GBASE-VR8	842 to 868	33.6
	842 to 888	29.6
	842 to 918	24.5
	842 to 948	20.7
100GBASE-SR1 200GBASE-SR2 400GBASE-SR4 800GBASE-SR8	844 to 863	18.0

167.8.13 Receiver sensitivity

Change the second paragraph in 167.8.13 as follows:

The conformance test signal at TP3 meets the requirements for a 100GBASE-VR1, 200GBASE-VR2, 400GBASE-VR4, 800GBASE-VR8, 100GBASE-SR1, 200GBASE-SR2, ~~or~~ 400GBASE-SR4, or 800GBASE-SR8 transmitter followed by an attenuator. For multi-lane testing considerations, see 167.8.2. The BER requirements are given in 167.1.1.

167.9 Safety, installation, environment, and labeling

167.9.2 Laser safety

Change the first paragraph in 167.9.2 as follows:

100GBASE-VR1, 200GBASE-VR2, 400GBASE-VR4, 800GBASE-VR8, 100GBASE-SR1, 200GBASE-SR2, ~~and~~ 400GBASE-SR4, and 800GBASE-SR8 optical transceivers shall conform to Hazard Level 1M laser requirements as defined in IEC 60825-1 and IEC 60825-2, under any condition of operation. This includes single fault conditions whether coupled into a fiber or out of an open bore.

167.9.4 Environment

Change the first paragraph in 167.9.4 as follows:

Normative specifications in this clause shall be met by a system integrating a 100GBASE-VR1, 200GBASE-VR2, 400GBASE-VR4, 800GBASE-VR8, 100GBASE-SR1, 200GBASE-SR2, ~~or~~ 400GBASE-SR4, or 800GBASE-SR8 PMD over the life of the product while the product operates within the manufacturer's range of environmental, power, and other specifications.

167.9.5 Electromagnetic emission

Change 167.9.5 as follows:

A system integrating a 100GBASE-VR1, 200GBASE-VR2, 400GBASE-VR4, 800GBASE-VR8, 100GBASE-SR1, 200GBASE-SR2, ~~or~~ 400GBASE-SR4, or 800GBASE-SR8 PMD shall comply with applicable local and national codes for the limitation of electromagnetic interference.

167.9.7 PMD labeling requirements

Change the first paragraph in 167.9.7 as follows:

It is recommended that each PHY (and supporting documentation) be labeled in a manner visible to the user, with at least the applicable safety warnings and the applicable port type designation (e.g., 100GBASE-VR1, 200GBASE-VR2, 400GBASE-VR4, 800GBASE-VR8, 100GBASE-SR1, 200GBASE-SR2, ~~or~~ 400GBASE-SR4, or 800GBASE-SR8). It is recommended that each PHY with an angled fiber interface indicate that it uses an angled MDI.

167.10 Fiber optic cabling model

Change 167.10 as follows:

The fiber optic cabling (channel) contains one optical fiber for each direction to support 100GBASE-VR1 or 100GBASE-SR1, two optical fibers for each direction to support 200GBASE-VR2 or 200GBASE-SR2, ~~or~~ four optical fibers for each direction to support 400GBASE-VR4 or 400GBASE-SR4, or eight optical fibers for each direction to support 800GBASE-VR8 or 800GBASE-SR8. The fiber optic cabling interconnects the transmitters at the MDI on one end of the channel to the receivers at the MDI on the other end of the channel. As defined in 167.10.3, the optical lanes appear in defined locations at the MDI but the locations are not assigned specific lane numbers within this standard because any transmitter lane may be connected to any receiver lane.

167.10.1 Fiber optic cabling model

Change Table 167–14 as follows:

Table 167–14—Fiber optic cabling (channel) characteristics

Description	100GBASE-VR1 200GBASE-VR2 400GBASE-VR4 800GBASE-VR8			100GBASE-SR1 200GBASE-SR2 400GBASE-SR4 800GBASE-SR8			Unit
	OM3	OM4	OM5	OM3	OM4	OM5	
Operating distance (max)	30	50		60	100		m
Cabling Skew (max)[a]	79						ns
Cabling Skew Variation[a, b] (max)	2.4						ns
Channel insertion loss[c] (max)	1.6	1.7		1.7	1.8		dB
Channel insertion loss (min)	0			0			dB

[a] Applies only to 200GBASE-VR2, 400GBASE-VR4, 800GBASE-VR8, 200GBASE-SR2, ~~and~~ 400GBASE-SR4, and 800GBASE-SR8.

[b] An additional 400 ps of Skew Variation could be caused by wavelength changes, which are attributable to the transmitter not the channel.

[c] These channel insertion loss values include cable loss plus 1.5 dB allocated for connection and splice loss, over the wavelength range 842 nm to 948 nm for VR and over the wavelength range 844 nm to 863 nm for SR.

167.10.2.1 Optical fiber cable

Change Table 167–15 as follows:

Table 167–15—Optical fiber and cable characteristics

Description	OM3[a]	OM4[b]	OM5[c]	Unit
Nominal core diameter	50			μm
Nominal fiber specification wavelength	850		850 and 953	nm
Effective modal bandwidth at 850 nm (min)[d]	2000	4700		MHz · km
Effective modal bandwidth at 953 nm (min)	Not Specified[e]		2470[e]	MHz · km
Cabled optical fiber attenuation (max)	3.0			dB/km
Zero dispersion wavelength (λ_0)[f]	$1297 \le \lambda_0 \le 1328$			nm
Chromatic dispersion slope (max) (S_0)[f]	$-412/(840(1-(\lambda_0/840)^4))$			ps/nm^2 km

[a] IEC 60793-2-10 type A1a.2.
[b] IEC 60793-2-10 type A1a.3.
[c] IEC 60793-2-10 type A1a.4.

[d] When measured with the launch conditions specified in Table 167–7.
[e] Guidance is provided for effective modal bandwidth at all wavelengths in the 840 nm to 953 nm range in IEC 60793-2-10.
[f] These limits are consistent with IEC 60793-2-10/AMD1 ED7. For OM5, they are the same as previous versions of IEC 60793-2-10. OM3 and OM4 fibers compliant to previous versions of IEC 60793-2-10 are considered compliant for 100GBASE-VR1, 200GBASE-VR2, 400GBASE-VR4, 800GBASE-VR8, 100GBASE-SR1, 200GBASE-SR2, ~~and~~ 400GBASE-SR4, and 800GBASE-SR8 Physical Layer types.

167.10.3 Medium Dependent Interface (MDI)

Change 167.10.3 as follows:

The ~~100GBASE-VR1, 200GBASE-VR2, 400GBASE-VR4, 100GBASE-SR1, 200GBASE-SR2, or 400GBASE-SR4~~ PMD is coupled to the fiber optic cabling at the MDI. The MDI is the interface between the PMD and the "fiber optic cabling" (as shown in Figure 167–6). Examples of an MDI include the following:

a) PMD with a connectorized fiber pigtail plugged into an adapter;
b) PMD receptacle.

NOTE—Transmitter compliance testing is performed at TP2 as defined in 167.5.1, not at the MDI.

Insert new subclause 167.10.3.1a including Figure 167–8a as follows:

167.10.3.1a Optical lane assignments for 800GBASE-VR8 and 800GBASE-SR8

The eight transmit and eight receive optical lanes of 800GBASE-VR8 or 800GBASE-SR8 shall occupy the positions depicted in Figure 167–8a when looking into the MDI receptacle with the connector keyway feature on top.

The interface contains 16 active lanes within 16 total positions. The transmit optical lanes occupy the leftmost eight positions. The receive optical lanes occupy the rightmost eight positions.

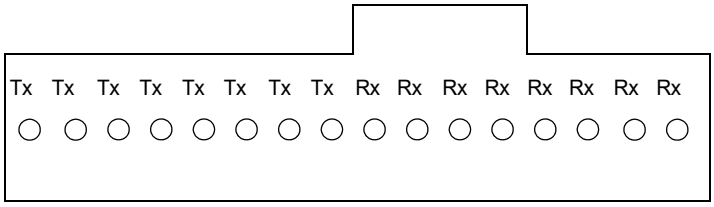


Figure 167–8a—Optical lane assignments for 800GBASE-VR8 and 800GBASE-SR8

Insert new subclause 167.10.3.4 after 167.10.3.3 as follows:

167.10.3.4 MDI requirements for 800GBASE-VR8 and 800GBASE-SR8

The MDI shall optically mate with the compatible plug on the optical fiber cabling. If the MDI is constructed with a connectorized fiber pigtail into an adapter, the connectorized pigtail shall meet the dimensional specifications of designation FOCIS 18 P-1x16-1-8-1-2-1 and the adapter shall meet the dimensional specifications of designation FOCIS 18 A-1-0 as defined in ANSI/TIA-604-18-A. If the MDI is constructed with a receptacle, it shall meet the dimensional specifications of designation FOCIS 18 R-1x16-1-8-1-2-2, as defined in ANSI/TIA-604-18-A. The plug terminating the optical fiber cabling that interconnects to either MDI configuration shall meet the dimensional specifications of designation FOCIS 18 P-1x16-1-8-2-2-1, as defined in ANSI/TIA-604-18-A. The MPO-16 female plug connector and MDI are structurally similar to those depicted in Figure 167–10, but with an angled end facet, 16 fibers, an offset keyway, and different pin diameters and locations. The MDI connection shall meet the interface performance specifications of IEC 63267-1 for performance grade Bm/1m.

Change the title of 167.11 as follows:

167.11 Protocol implementation conformance statement (PICS) proforma for Clause 167, Physical Medium Dependent (PMD) sublayer and medium, type 100GBASE-VR1, 200GBASE-VR2, 400GBASE-VR4, 800GBASE-VR8, 100GBASE-SR1, 200GBASE-SR2, ~~and~~ 400GBASE-SR4, and 800GBASE-SR8[10]

167.11.1 Introduction

Change the first paragraph in 167.11.1 as follows:

The supplier of a protocol implementation that is claimed to conform to Clause 167, Physical Medium Dependent (PMD) sublayer and medium, type 100GBASE-VR1, 200GBASE-VR2, 400GBASE-VR4, 800GBASE-VR8, 100GBASE-SR1, 200GBASE-SR2, ~~and~~ 400GBASE-SR4, and 800GBASE-SR8, shall complete the following protocol implementation conformance statement (PICS) proforma.

167.11.2 Identification

167.11.2.2 Protocol summary

Change the table in 167.11.2.2 as follows:

Identification of protocol standard	IEEE Std 802.3df-2024, Clause 167, Physical Medium Dependent (PMD) sublayer and medium, type 100GBASE-VR1, 200GBASE-VR2, 400GBASE-VR4, 800GBASE-VR8, 100GBASE-SR1, 200GBASE-SR2, ~~and~~ 400GBASE-SR4, and 800GBASE-SR8
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3df-2024.)	

Date of Statement	

[10] *Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

167.11.3 Major capabilities/options

Change the table in 167.11.3 as follows (some unchanged rows not shown):

Item	Feature	Subclause	Value/Comment	Status	Support
…					
*SR4	400GBASE-SR4 PMD	167.7	Device supports requirements for 400GBASE-SR4 PHY	O	Yes [ ] No [ ]
*VR8	800GBASE-VR8 PMD	167.7	Device supports requirements for 800GBASE-VR8 PHY	O	Yes [ ] No [ ]
*SR8	800GBASE-SR8 PMD	167.7	Device supports requirements for 800GBASE-SR8 PHY	O	Yes [ ] No [ ]
*INS	Installation / cable	167.10.1	Items marked with INS include installation practices and cable specifications not applicable to a PHY manufacturer	O	Yes [ ] No [ ]
…					

Change the title of 167.11.4 as follows:

167.11.4 PICS proforma tables for Physical Medium Dependent (PMD) sublayer and medium, type 100GBASE-VR1, 200GBASE-VR2, 400GBASE-VR4, 800GBASE-VR8, 100GBASE-SR1, 200GBASE-SR2, ~~and~~ 400GBASE-SR4, and 800GBASE-SR8

167.11.4.1 PMD functional specifications

Change the row for item F1 in the table in 167.11.4.1 as follows (unchanged rows not shown):

Item	Feature	Subclause	Value/Comment	Status	Support
F1	Compatible with 100GBASE-R, 200GBASE-R, ~~or~~ 400GBASE-R, or 800GBASE-R PCS and PMA	167.1		M	Yes [ ]
…					

167.11.4.6 Characteristics of the fiber optic cabling and MDI

Change the table in 167.11.4.6 as follows (unchanged rows not shown):

Item	Feature	Subclause	Value/Comment	Status	Support
…					
OC4	MDI layout for 400GBASE-VR2 and 400GBASE-SR2	167.10.3.1	Optical lane assignments per Figure 167–7	~~(VR2 or SR2)~~ VR2+SR2:M	Yes [ ] N/A [ ]
OC5	MDI layout for 400GBASE-VR4 and 400GBASE-SR4	167.10.3.1	Optical lane assignments per Figure 167–8	~~(VR4 or SR4)~~ VR4+SR4:M	Yes [ ] N/A [ ]
OC5a	MDI layout for 800GBASE-VR8 and 800GBASE-SR8	167.10.3.1a	Optical lane assignments per Figure 167–8a	VR8+SR8:M	Yes [ ] N/A [ ]
OC6	MDI mating, 100GBASE-VR1 and 100GBASE-SR1, with duplex optical fiber connector	167.10.3.2	MDI optically mates with plug on the cabling, performance grade Bm/2m	~~(VR1 or SR1)~~ VR1+SR1:M	Yes [ ] N/A [ ]
OC7	MDI requirements for 100GBASE-VR1 and 100GBASE-SR1, with duplex optical fiber connector	167.10.3.2	Per IEC 61753-1 and IEC 61753-022-2	~~(VR1 or SR1) and INS:M~~ INS* (VR1+SR1):M	Yes [ ] N/A [ ]
OC8	MDI mating, with multifiber connector	167.10.3.3	MDI optically mates with plug on the cabling, performance grade Bm/2m	~~(VR1, SR1, VR2, SR2, VR4, or SR4):!AFI:M~~ !AFI* (VR1+SR1 +VR2+SR2 +VR4+SR4):M	Yes [ ] N/A [ ]
OC9	MDI mating, with multifiber connector	167.10.3.3	MDI optically mates with plug on the cabling, performance grade Bm/1m	~~(VR1, SR1, VR2, SR2, VR4, or SR4):AFI:M~~ AFI* (VR1+SR1 +VR2+SR2 +VR4+SR4):M	Yes [ ] N/A [ ]
OC10	MDI dimensions, with multifiber connector	167.10.3.3	Per IEC 61754-7-1 interface 7-1-3 or interface 7-1-10	~~(VR1, SR1, VR2, SR2, VR4, or SR4):!AFI:M~~ !AFI* (VR1+SR1 +VR2+SR2 +VR4+SR4):M	Yes [ ] N/A [ ]

Item	Feature	Subclause	Value/Comment	Status	Support
OC11	MDI dimensions, with multifiber connector	167.10.3.3	Per IEC 61754-7-1 interface 7-1-3 or interface 7-1-9	~~(VR1, SR1, VR2, SR2, VR4, or SR4):AFI:M~~ AFI* (VR1+SR1 +VR2+SR2 +VR4+SR4):M	Yes [ ] N/A [ ]
OC12	Cabling connector dimensions, with multifiber connector	167.10.3.3	Per IEC 61754-7-1 interface 7-1-4	~~INS and (VR1, SR1, VR2, SR2, VR4, or SR4):!AFI:M~~ INS*!AFI* (VR1+SR1 +VR2+SR2 +VR4+SR4):M	Yes [ ] N/A [ ]
OC13	Cabling connector dimensions, with multifiber connector	167.10.3.3	Per IEC 61754-7-1 interface 7-1-1	~~INS and (VR1, SR1, VR2, SR2, VR4, or SR4):AFI:M~~ INS*AFI* (VR1+SR1 +VR2+SR2 +VR4+SR4):M	Yes [ ] N/A [ ]
OC14	MDI requirements, with multifiber connector	167.10.3.3	Per IEC 61753-1 and IEC 61753-022-2, performance grade Bm/2m	~~INS and (VR1, SR1, VR2, SR2, VR4, or SR4):!AFI:M~~ INS*!AFI* (VR1+SR1 +VR2+SR2 +VR4+SR4):M	Yes [ ] N/A [ ]
OC15	MDI requirements, with multifiber connector	167.10.3.3	Per IEC 63267-1, performance grade Bm/1m	~~INS and (VR1, SR1, VR2, SR2, VR4, or SR4):AFI:M~~ INS*AFI* (VR1+SR1 +VR2+SR2 +VR4+SR4):M	Yes [ ] N/A [ ]
OC16	MDI mating, with multifiber connector	167.10.3.4	MDI optically mates with plug on the cabling, performance grade Bm/1m	VR8+SR8:M	Yes [ ] N/A [ ]
OC17	MDI dimensions, with multifiber connector	167.10.3.4	Per ANSI/TIA-604-18-A designation FOCIS 18 P-1x16-1-8-1-2-1 and designation FOCIS 18 A-1-0 or designation FOCIS 18 R-1x16-1-8-1-2-2	VR8+SR8:M	Yes [ ] N/A [ ]
OC18	Cabling connector dimensions, with multifiber connector	167.10.3.4	Per ANSI/TIA-604-18-A designation FOCIS 18 P-1x16-1-8-2-2-1	INS* (VR8+SR8):M	Yes [ ] N/A [ ]
OC19	MDI requirements, with multifiber connector	167.10.3.4	Per IEC 63267-1, performance grade Bm/1m	INS* (VR8+SR8):M	Yes [ ] N/A [ ]

Insert new clauses Clause 169 to Clause 173 as follows:

169. Introduction to 800 Gb/s networks

169.1 Overview

169.1.1 Scope

This clause describes the general requirements for 800 Gigabit Ethernet.

800 Gigabit Ethernet uses the IEEE 802.3 MAC sublayer operating at a data rate of 800 Gb/s, coupled with any IEEE 802.3 800GBASE Physical Layer implementation and is defined for full duplex operation only.

169.1.2 Relationship of 800 Gigabit Ethernet to the ISO OSI reference model

800 Gigabit Ethernet couples the IEEE 802.3 MAC to a family of 800 Gb/s Physical Layer devices. The relationships among 800 Gigabit Ethernet, the IEEE 802.3 MAC, and the ISO Open System Interconnection (OSI) reference model are shown in Figure 169–1.

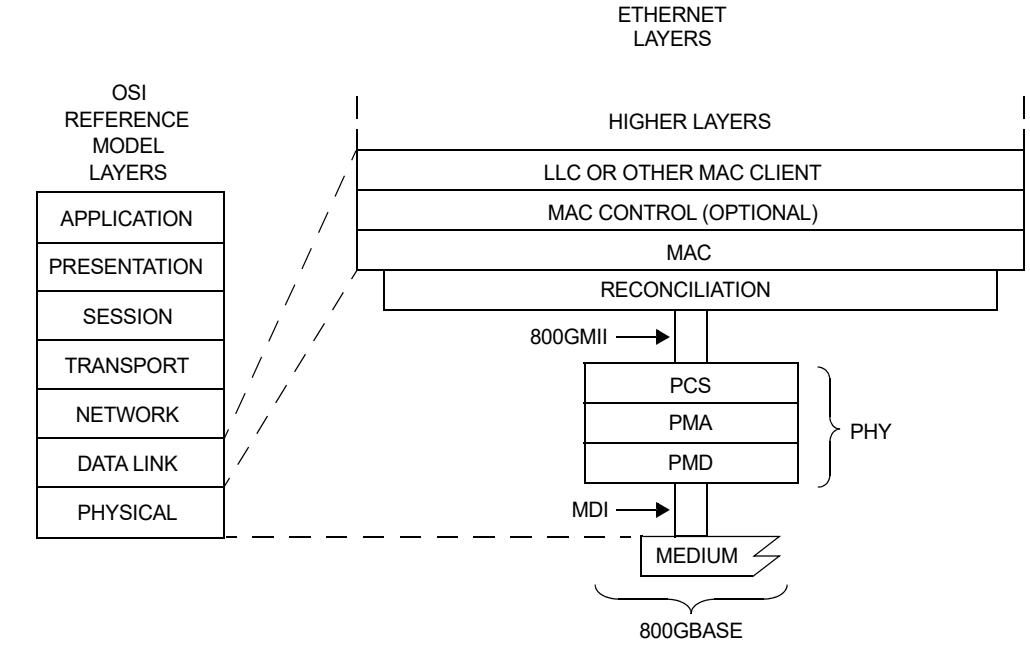


Figure 169–1—Architectural positioning of 800 Gigabit Ethernet

While this specification defines interfaces in terms of bits, octets, and frames, implementations may choose other data-path widths for implementation convenience. The only exceptions are as follows:

a) The 800GMII as specified in Clause 170, when implemented as a logical interconnection point between the MAC sublayer and the Physical Layer device (PHY), uses a 64-bit wide data path. Physical instantiations of this interface may use other data-path widths.

b) The management interface, when physically implemented as the MDIO/MDC (Management Data Input/Output and Management Data Clock) at an observable interconnection port, as specified in Clause 45, uses a bit-wide data path.

c) The PMA service interface, when physically implemented as 800GAUI-8 (800 Gb/s eight-lane Attachment Unit Interface) at an observable interconnection port, as specified in Annex 120F or Annex 120G, uses an 8-lane data path.

d) The MDI for each of the following PMDs uses an 8-lane data path:
   — 800GBASE-KR8 as specified in Clause 163
   — 800GBASE-CR8 as specified Clause 162
   — 800GBASE-VR8 and 800GBASE-SR8 as specified in Clause 167
   — 800GBASE-DR8 as and 800GBASE-DR8-2 as specified in Clause 124

169.1.3 Nomenclature

The nomenclature employed by the 800 Gb/s Physical Layer is explained as follows.

The alpha-numeric prefix 800GBASE in the port type (e.g., 800GBASE-R) represents a family of Physical Layer devices operating at a speed of 800 Gb/s.

The term 800GBASE-R represents a family of Physical Layer devices using the Physical Coding Sublayer (PCS) defined in Clause 172 for 800 Gb/s operation.

Physical Layer devices listed in Table 169–1 are defined for operation at 800 Gb/s.

Table 169–1—800 Gb/s PHYs

Name	Description
800GBASE-KR8	800 Gb/s PHY using 800GBASE-R encoding over eight lanes of an electrical backplane (see Clause 163)
800GBASE-CR8	800 Gb/s PHY using 800GBASE-R encoding over eight lanes of twinaxial copper cable (see 1.4.559 and Clause 162)
800GBASE-VR8	800 Gb/s PHY using 800GBASE-R encoding over eight multimode fibers in each direction with reach up to at least 50 m (see Clause 167)
800GBASE-SR8	800 Gb/s PHY using 800GBASE-R encoding over eight multimode fibers in each direction with reach up to at least 100 m (see Clause 167)
800GBASE-DR8	800 Gb/s PHY using 800GBASE-R encoding over eight single-mode fibers in each direction with reach up to at least 500 m (see Clause 124)
800GBASE-DR8-2	800 Gb/s PHY using 800GBASE-R encoding over eight single-mode fibers in each direction with reach up to at least 2 km (see Clause 124)

169.1.4 Physical Layer signaling systems

This standard specifies a family of Physical Layer implementations. Table 169–2 and Table 169–3 specify the correlation between PHY types and clauses. Implementations conforming to one or more PHY types meet the requirements of the corresponding clauses.

Table 169–2—PHY type and clause correlation (800GBASE copper)

PHY type	Clause[a]								
	73	170		171	172	173	120F	162	163
	Auto-Negotiation	RS	800GMII	800GMII Extender	800GBASE-R PCS	800GBASE-R PMA	800GAUI-8 C2C	800GBASE-CR8 PMD	800GBASE-KR8 PMD
800GBASE-KR8	M	M	O	O	M	M	O		M
800GBASE-CR8	M	M	O	O	M	M	O	M	

[a] O = Optional, M = Mandatory.

Table 169–3—PHY type and clause correlation (800GBASE optical)

PHY type	Clause[a]										
	170		171	172	173	120F	120G	124		167	
	RS	800GMII	800MII Extender	800GBASE-R PCS	800GBASE-R PMA	800GAUI-8 C2C	800GAUI-8 C2M	800GBASE-DR8 PMD	800GBASE-DR8-2 PMD	800GBASE-VR8 PMD	800GBASE-SR8 PMD
800GBASE-VR8	M	O	O	M	M	O	O			M	
800GBASE-SR8	M	O	O	M	M	O	O				M
800GBASE-DR8	M	O	O	M	M	O	O	M			
800GBASE-DR8-2	M	O	O	M	M	O	O		M		

[a] O = Optional, M = Mandatory.

169.2 Summary of 800 Gigabit Ethernet architecture

169.2.1 Reconciliation Sublayer (RS) and 800 Gb/s Media Independent Interface (800GMII)

The 800 Gb/s Media Independent Interface (800GMII) specified in Clause 170 provides a logical interconnection between the MAC sublayer and Physical Layer devices (PHYs). The 800GMII is not intended to be physically instantiated, rather it can logically connect layers within a device.

The 800GMII supports 800 Gb/s operation through its 64-bit-wide transmit and receive data paths. The Reconciliation Sublayer (RS) provides a mapping between the signals provided at the 800GMII and the MAC/PLS service definition.

While the 800GMII is an optional interface, it is used extensively in this standard as a basis for functional specification and it provides a common service interface for the Physical Coding Sublayer (Clause 172).

169.2.2 800GMII Extender and 800GMII Extender Sublayer (800GXS)

The optional 800GMII Extender (Clause 171) may be inserted between the Reconciliation Sublayer and the PHY to transparently extend the reach of the 800GMII.

The 800GMII Extender Sublayer (800GXS) is part of the 800GMII Extender. It is equivalent in function to the 800GBASE-R PCS in Clause 172 with the exceptions as defined in Clause 171.

169.2.3 Physical Coding Sublayer (PCS)

The PCS performs encoding of data from the 800GMII, applies FEC, distributes the data to multiple PCS lanes, and transfers the encoded data to the PMA.

The 800GBASE-R PCS is specified in Clause 172.

169.2.4 Physical Medium Attachment (PMA) sublayer

The PMA sublayer provides a medium-independent means to support the use of a range of physical media.

The 800GBASE-R PMA is specified in Clause 173.

169.2.5 Physical Medium Dependent (PMD) sublayer

The PMD sublayer is responsible for interfacing to the transmission medium. The PMD is located just above the Medium Dependent Interface (MDI).

The MDI, logically subsumed within each PMD subclause, is the actual medium attachment for the various supported media.

800GBASE-R PMDs, including the corresponding MDI and media, are specified in Clause 124, Clause 162, Clause 163, and Clause 167.

169.2.6 Auto-Negotiation

Auto-Negotiation provides a device with the capability to detect the abilities (modes of operation) supported by the device at the other end of the link, determine common abilities, and configure for joint operation.

Auto-Negotiation used by the 800 Gb/s backplane PHY (800GBASE-KR8) and the 800 Gb/s copper PHY (800GBASE-CR8) is specified in Clause 73.

169.2.7 Management interface (MDIO/MDC)

The optional MDIO/MDC management interface provides an interconnection between MDIO Manageable Devices (MMDs) and Station Management (STA) entities.

The MDIO/MDC management interface is specified in Clause 45.

169.2.8 Management

Managed objects, attributes, and actions are defined for all 800 Gigabit Ethernet components. These items are specified in Clause 30.

169.3 Service interface specification method and notation

The service interface specification for the 800GBASE-R Physical Layers is as per the definition in 1.2.2. Note that the 800GBASE-R inter-sublayer service interfaces use multiple scalar REQUEST and INDICATION primitives, to indicate the transfer of multiple independent streams of data units, as defined in 169.3.1 through 169.3.3.

169.3.1 Inter-sublayer service interface

The inter-sublayer service interface is described in an abstract manner and does not imply any particular implementation. The inter-sublayer service interface primitives are defined as follows:

IS_UNITDATA_*i*.request
IS_UNITDATA_*i*.indication
IS_SIGNAL.indication
IS_SIGNAL.request

The IS_UNITDATA_*i*.request (where $i = 0$ to $n - 1$, and n is the number of streams of data units) primitive is used to define the transfer of multiple streams of data units to a sublayer from the next higher (closer to the MAC) sublayer.

The IS_UNITDATA_*i*.indication (where $i = 0$ to $n - 1$, and n is the number of streams of data units) primitive is used to define the transfer of multiple streams of data units from a sublayer to the next higher sublayer.

The IS_SIGNAL.indication primitive is used to define the transfer of signal status from a sublayer to the next higher sublayer.

The IS_SIGNAL.request primitive is used to define the transfer of signal status to a sublayer from the next higher sublayer.

169.3.2 Instances of the inter-sublayer service interface

The inter-sublayer service interface may be instantiated between different sublayers, hence a prefix notation is defined to identify a specific instance of an inter-sublayer service interface. The following prefixes are defined:

— PMA:—for primitives issued on the interface between the PMA and the PCS or DTE 800GXS above called the PMA service interface.
— PHY_XS:—for primitives issued on the interface between the PHY 800GXS and the PMA above called the PHY 800GXS service interface.

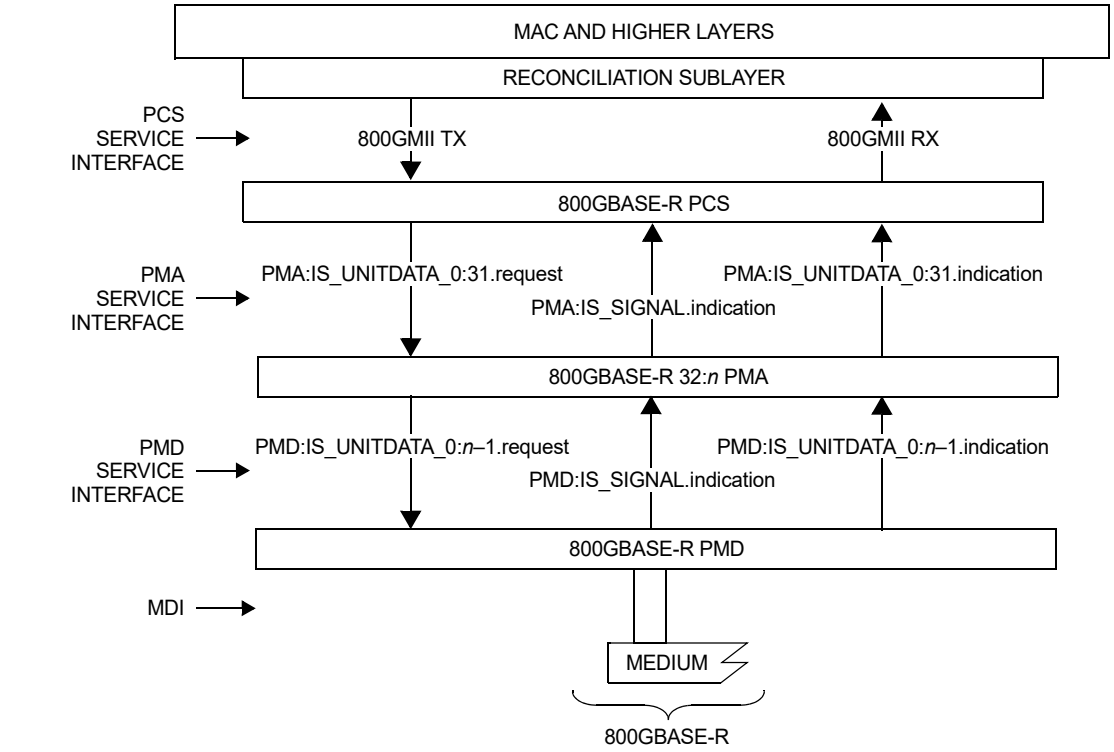
— PMD:—for primitives issued on the interface between the PMD and the PMA above called the PMD service interface.

As an example, the primitives for the PMD service interface are identified as follows:

PMD:IS_UNITDATA_*i*.request
PMD:IS_UNITDATA_*i*.indication
PMD:IS_SIGNAL.indication

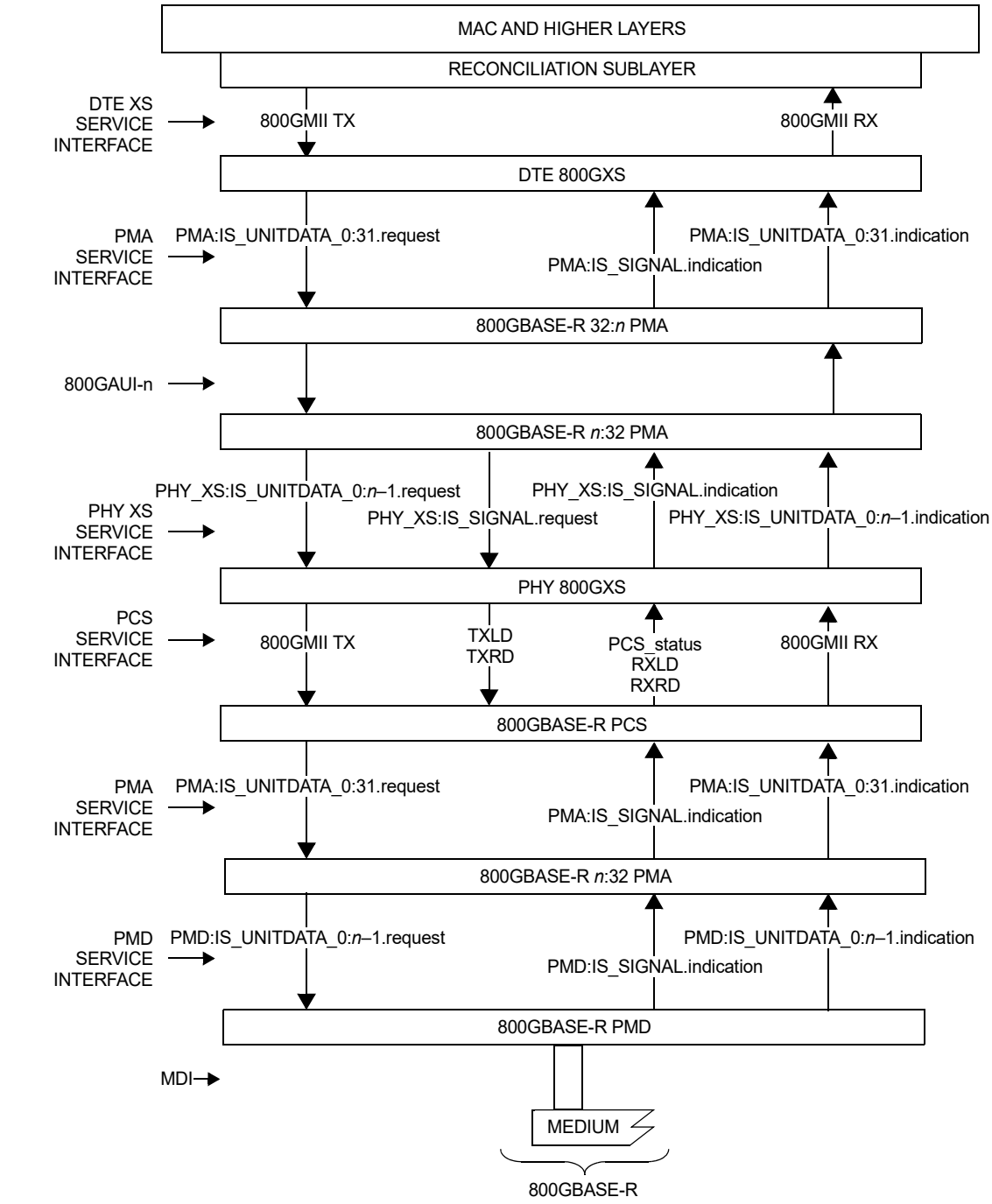
Examples of inter-sublayer service interfaces for 800GBASE-R with their corresponding instance names are illustrated in Figure 169–2 and Figure 169–3.

Primitives for other instances of inter-sublayer interfaces are represented in a similar manner.



800GMII = 800 Gb/s MEDIA INDEPENDENT INTERFACE
MAC = MEDIA ACCESS CONTROL
MDI = MEDIUM DEPENDENT INTERFACE
PCS = PHYSICAL CODING SUBLAYER
PMA = PHYSICAL MEDIUM ATTACHMENT
PMD = PHYSICAL MEDIUM DEPENDENT
n = NUMBER OF PARALLEL STREAMS OF DATA UNITS

Figure 169–2—800GBASE-R inter-sublayer service interfaces not including 800GMII Extender



800GAUI-n = 800 Gb/s ATTACHMENT UNIT INTERFACE
800GMII = 800 Gb/s MEDIA INDEPENDENT INTERFACE
800GXS = 800GMII EXTENDER SUBLAYER
DTE = DATA TERMINAL EQUIPMENT
MAC = MEDIA ACCESS CONTROL
MDI = MEDIUM DEPENDENT INTERFACE
PCS = PHYSICAL CODING SUBLAYER
PHY = PHYSICAL LAYER DEVICE
PMA = PHYSICAL MEDIUM ATTACHMENT
PMD = PHYSICAL MEDIUM DEPENDENT
XS = EXTENDER SUBLAYER
n = NUMBER OF PARALLEL STREAMS OF DATA UNITS

Figure 169–3—800GBASE-R inter-sublayer service interfaces including 800GMII Extender

169.3.3 Semantics of inter-sublayer service interface primitives

The semantics of the inter-sublayer service interface primitives for the 800GBASE-R sublayers are described in 116.3.3.1 through 116.3.3.3.

169.4 Delay constraints

Predictable operation of the MAC Control PAUSE operation (Clause 31, Annex 31B) demands that there be an upper bound on the propagation delays through the network. This implies that MAC, MAC Control sublayer, and PHY implementations conform to certain delay maxima, and that network planners and administrators conform to constraints regarding the cable topology and concatenation of devices. Table 169–4 contains the values of maximum delay (sum of transmit and receive delays at one end of the link) for each instance of a sublayer. If a PHY contains an Auto-Negotiation sublayer, the delay of the Auto-Negotiation sublayer is included within the delay of the PMD and medium. The delay for a set of sublayers within the same package may be constrained by the sum of constraints for the set of sublayers.

Table 169–4—Sublayer delay constraints

Sublayer	Maximum (bit time)[a]	Maximum (pause_quanta)[b]	Maximum (ns)	Notes[c]
800G MAC, RS, and MAC Control	196 608	384	245.76	See 170.1.4.
800GBASE-R PCS or 800GXS[d]	640 000	1250	800	See 172.5.
800GBASE-R 32:8 PMA or 8:32 PMA	36 864	72	46.08	See 173.5.4.
800GBASE-R 8:8 PMA	73 728	144	92.16	See 173.5.4.
800GBASE-KR8 PMD	32 768	64	40.96	Includes allocation of 14 ns for one direction through backplane medium. See 163.5.
800GBASE-CR8 PMD	32 768	64	40.96	Includes allocation of 14 ns for one direction through cable medium. See 162.5.
800GBASE-VR8 PMD	16 384	32	20.48	Includes 2 m of fiber. See 167.3.1.
800GBASE-SR8 PMD	16 384	32	20.48	Includes 2 m of fiber. See 167.3.1.
800GBASE-DR8 PMD	16 384	32	20.48	Includes 2 m of fiber. See 124.3.1.
800GBASE-DR8-2 PMD	16 384	32	20.48	Includes 2 m of fiber. See 124.3.1.

[a] For 800GBASE, 1 bit time (BT) is equal to 1.25 ps. (See 1.4.215 for the definition of bit time.)
[b] For 800GBASE, 1 pause_quantum is equal to 640 ps. (See 1.4.459 for the definition of pause_quanta.)
[c] Should there be a discrepancy between this table and the delay requirements of the relevant sublayer clause, the sublayer clause prevails.
[d] If an implementation includes the 800GMII Extender, the delay associated with the 800GMII Extender includes two 800GXS sublayers.

The physical medium interconnecting two optical PHYs introduces additional delay in a link.

See 80.4 for the calculation of bit time per meter of fiber or electrical cable.

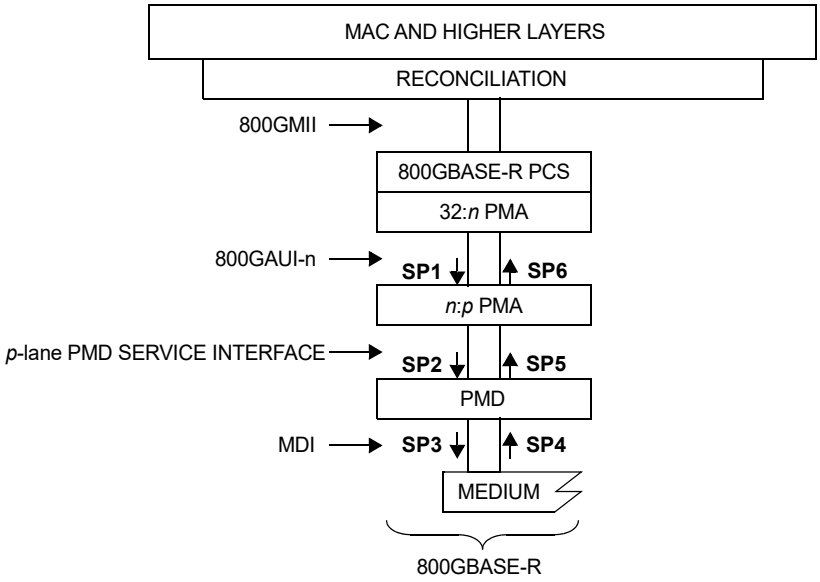
See 31B.3.7 for PAUSE reaction timing constraints for stations at operating speeds of 800 Gb/s.

169.5 Skew constraints

Skew (or relative delay) can be introduced between PCS lanes by both active and passive elements of an 800GBASE-R link. Skew is defined as the difference between the times of the earliest PCS lane and latest PCS lane for the one to zero transition of the alignment marker sync bits. The PCS deskew function (see 172.2.5.1) compensates for all lane-to-lane Skew observed at the receiver. The Skew between the PCS lanes is kept within limits as shown in Table 169–5 so that the transmitted information on the PCS lanes can be reassembled by the receive PCS.

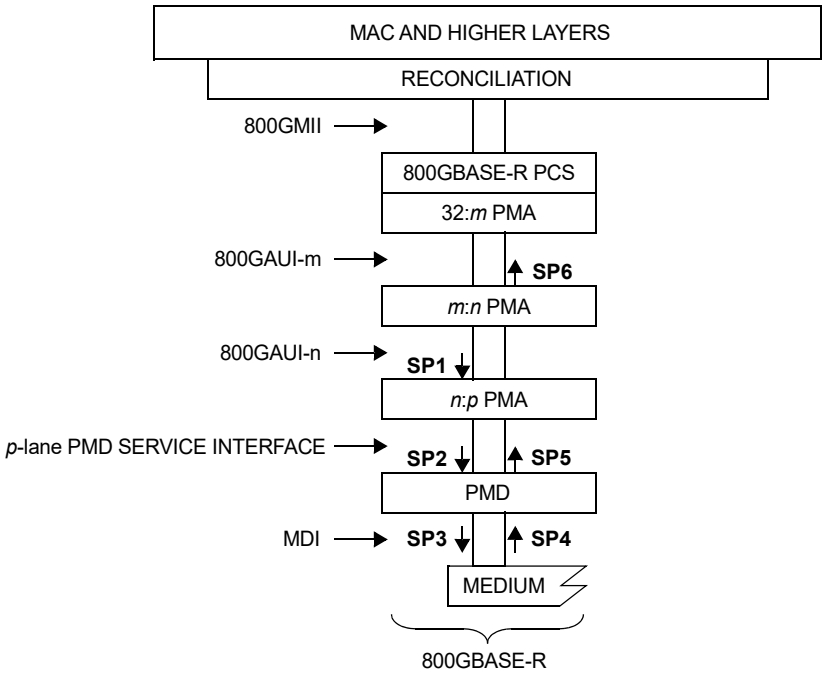
Skew Variation may be introduced due to variations in electrical, thermal. or environmental characteristics. Skew Variation is defined as the change in Skew between any PCS lane and any other PCS lane over the entire time that the link is in operation. From the time the link is brought up, Skew Variation is limited so that each PCS lane always traverses the same PCS lane between any pair of adjacent sublayers while the link remains in operation.

The maximum Skew and Skew Variation at physically instantiated interfaces is specified at Skew points SP1, SP2, and SP3 for the transmit direction and SP4, SP5, and SP6 for the receive direction as illustrated in Figure 169–4 for a PHY with one 800GAUI-n and Figure 169–5 for a PHY with two 800GAUI-n.



800GAUI-n = 800 Gb/s ATTACHMENT UNIT INTERFACE
800GMII = 800 Gb/s MEDIA INDEPENDENT INTERFACE
MAC = MEDIA ACCESS CONTROL
MDI = MEDIUM DEPENDENT INTERFACE
PCS = PHYSICAL CODING SUBLAYER
PMA = PHYSICAL MEDIUM ATTACHMENT
PMD = PHYSICAL MEDIUM DEPENDENT
n = 8
p = 8

Figure 169–4—800GBASE-R Skew points for a PHY with one 800GAUI-n



800GAUI-n = 800 Gb/s ATTACHMENT UNIT INTERFACE
800GMII = 800 Gb/s MEDIA INDEPENDENT INTERFACE
MAC = MEDIA ACCESS CONTROL
MDI = MEDIUM DEPENDENT INTERFACE
PCS = PHYSICAL CODING SUBLAYER
PMA = PHYSICAL MEDIUM ATTACHMENT
PMD = PHYSICAL MEDIUM DEPENDENT
m=8
n=8
p=8

Figure 169–5—800GBASE-R Skew points for a PHY with two 800GAUI-n

In the transmit direction, the Skew points are defined in the following locations:

— SP1 on the 800GAUI-n interface, at the input of the PMA closest to the PMD
— SP2 on the PMD service interface, at the input of the PMD
— SP3 at the output of the PMD, at the MDI

In the receive direction, the Skew points are defined in the following locations:

— SP4 at the MDI, at the input of the PMD
— SP5 on the PMD service interface, at the output of the PMD
— SP6 on the 800GAUI-n interface, at the output of the PMA closest to the PCS or DTE 800GXS

The allowable limits for Skew are shown in Table 169–5 and the allowable limits for Skew Variation are shown in Table 169–6.

The Skew and Skew Variation requirements for the PCS, PMA, and PMD sublayers are specified in the respective clauses as noted in Table 169–5 and Table 169–6.

Table 169–5—Summary of Skew constraints

Skew points	Maximum Skew (ns)[a]	Maximum Skew for 800GBASE-R PCS lane (UI)[b]	Notes[c]
SP1	16	≈ 425	See 173.5.3
SP2	25	≈ 664	See 173.5.3, 124.3.2.2, 162.6.3, 163.6.3, 167.3.2.2
SP3	36	≈ 956	See 173.5.3, 124.3.2.2, 162.6.3, 163.6.3, 167.3.2.2
SP4	116	≈ 3081	See 173.5.3, 124.3.2.2, 162.6.3, 163.6.3, 167.3.2.2
SP5	127	≈ 3373	See 173.5.3, 124.3.2.2, 162.6.3, 163.6.3, 167.3.2.2
SP6	145	≈ 3852	See 173.5.3
At PCS receive	152	≈ 4038	See 172.2.5.1

[a] The Skew limit includes 1 ns allowance for PCB traces that are associated with the Skew points.
[b] The symbol ≈ indicates approximate equivalent of maximum Skew in UI based on 1 UI equals 37.64706 ps at PCS lane signaling rate of 26.5625 GBd.
[c] Should there be a discrepancy between this table and the Skew requirements of the relevant sublayer clause, the sublayer clause prevails.

Table 169–6—Summary of Skew Variation constraints

Skew points	Maximum Skew Variation (ns)	Maximum Skew Variation for 53.125 GBd PMD lane (UI)[a]	Notes[b]
SP1	0.2	≈ 11	See 173.5.3
SP2	0.4	≈ 21	See 173.5.3, 124.3.2.2, 162.6.3, 163.6.3, 167.3.2.2
SP3	0.6	≈ 32	See 173.5.3, 124.3.2.2, 162.6.3, 163.6.3, 167.3.2.2
SP4	3.4	≈ 181	See 173.5.3, 124.3.2.2, 162.6.3, 163.6.3, 167.3.2.2
SP5	3.6	≈ 191	See 173.5.3, 124.3.2.2, 162.6.3, 163.6.3, 167.3.2.2
SP6	3.8	≈ 202	See 173.5.3
At PCS receive	4	≈ 213	See 173.5.3

[a] The symbol ≈ indicates approximate equivalent of maximum Skew Variation in UI based on 1 UI equals 18.82353 ps at PMD lane signaling rate of 53.125 GBd.
[b] Should there be a discrepancy between this table and the Skew requirements of the relevant sublayer clause, the sublayer clause prevails.

169.6 FEC Degrade

The FEC degrade feature provides the ability to detect and indicate a degrade condition at the RS-FEC decoder using FEC degrade detection, and to propagate the FEC degrade indication using FEC degrade signaling. The propagation of FEC degrade indications across PCS and XS is described in 116.6.

FEC degrade detection and signaling specifications for the 800GXS and 800GBASE-R PCS are summarized in 171.6 and 172.1.4, respectively.

169.7 State diagrams

State diagrams take precedence over text.

The conventions of 1.2 are adopted, along with the extensions listed in 21.5.

Multiple states of a function that have a transition to a common state utilizing different qualifiers (for example, multiple exit conditions to an IDLE or WAIT state) may be indicated by a shared arrow. An exit transition arrow connects to the shared arrow, and the qualifier is met prior to termination of the transition arrow on the shared arrow. The shared arrow has no qualifier.

169.8 Protocol implementation conformance statement (PICS) proforma

The supplier of a protocol implementation that is claimed to conform to any part of IEEE Std 802.3, Clause 170 through Clause 173, and related annexes demonstrates compliance by completing a protocol implementation conformance statement (PICS) proforma.

A completed PICS proforma is the PICS for the implementation in question. The PICS is a statement of which capabilities and options of the protocol have been implemented. A PICS is included at the end of each clause as appropriate. Each of the 800 Gigabit Ethernet PICS conforms to the notation and conventions used in 21.6.

170. Reconciliation Sublayer (RS) and Media Independent Interface for 800 Gb/s (800GMII)

170.1 Overview

This clause defines the characteristics of the Reconciliation Sublayer (RS) and the 800 Gb/s Media Independent Interface (800GMII) between Ethernet media access controllers and various 800 Gb/s PHYs. Figure 170–1 shows the relationship of the RS and 800GMII to the ISO/IEC OSI reference model.

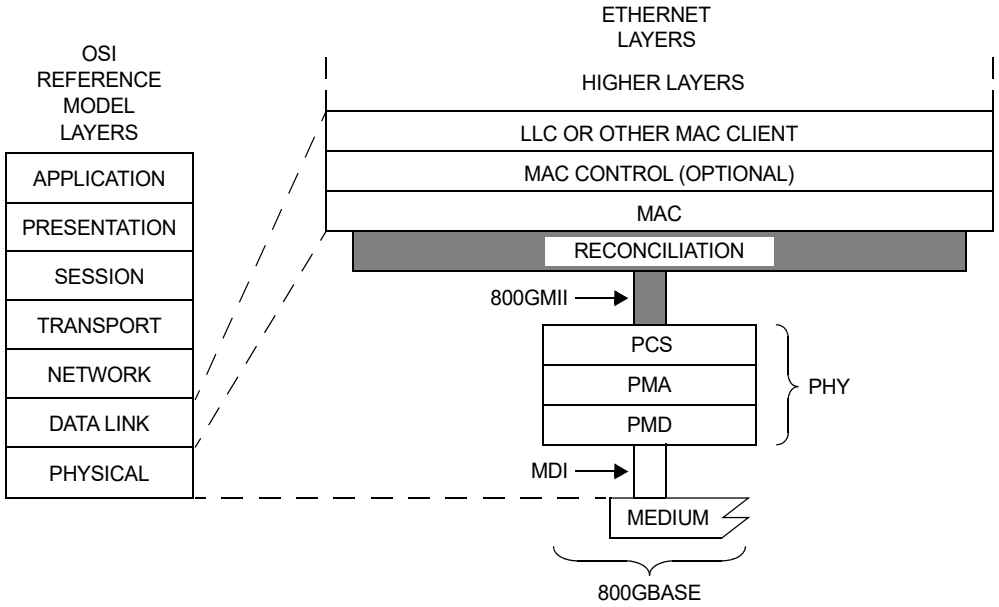


Figure 170–1—Relationship of the Reconciliation Sublayer and 800GMII to the ISO/IEC Open Systems Interconnection (OSI) reference model and IEEE 802.3 Ethernet model

The 800GMII is an optional logical interface between the MAC sublayer and the Physical Layer device (PHY). The 800GMII Extender may optionally be used to extend the 800GMII (see Clause 171).

The RS adapts the bit serial protocols of the MAC to the parallel format of the PCS service interface. Though the 800GMII is an optional interface, it is used in this standard as a basis for specification. The Physical Coding Sublayer (PCS) is specified to the 800GMII, so if not implemented, a conforming implementation shall behave functionally as if the RS and 800GMII were implemented.

The 800GMII has the following characteristics:

a) It supports a speed of 800 Gb/s.
b) Data and delimiters are synchronous to a clock reference.
c) It provides independent 64-bit wide transmit and receive data paths.
d) It supports full duplex operation only.

170.1.1 Summary of major concepts

The following are the major concepts of the 800GMII and RS:

— The 800GMII is functionally similar to other media independent interfaces that have been defined for lower speeds, as they all define an interface allowing independent development of MAC and PHY logic.
— The RS converts between the MAC serial data stream and the parallel data paths of the 800GMII.
— The RS maps the signal set provided at the 800GMII to the PLS service primitives provided at the MAC.
— Each direction of data transfer is independent and serviced by data, control, and clock signals.
— The RS generates continuous data or control characters on the transmit path and expects continuous data or control characters on the receive path.
— The RS participates in link fault detection and reporting by monitoring the receive path for status reports that indicate an unreliable link, and generating status reports on the transmit path to report detected link faults to the DTE on the remote end of the connecting link.

170.1.2 Application

This clause applies to the interface between the MAC and PHY, or between the PHY 800GXS and the PHY when the optional 800GMII Extender is used. This logical interface is used to provide media independence so that an identical media access controller may be used with supported PHY types.

170.1.3 Rate of operation

The 800GMII is specified to support 800 Gb/s operation.

170.1.4 Delay constraints

The maximum cumulative MAC Control, MAC, and RS delay (sum of transmit and receive delays at one end of the link) shall meet the values specified in Table 170–1. A description of overall system delay constraints and the definitions for bit times and pause_quanta can be found in 169.4 and its references.

Table 170–1—Delay constraints

Sublayer	Maximum (bit time)	Maximum (pause_quanta)	Maximum (ns)
800 Gb/s MAC, RS, and MAC Control	196 608	384	245.76

170.1.5 Allocation of functions

The allocation of functions at the 800GMII balances the need for media independence with interface simplicity. The 800GMII provides media independence by separating the Data Link and Physical Layers of the OSI seven-layer reference model.

170.1.6 800GMII structure

The 800GMII structure is identical to the CGMII structure specified in 81.1.6.

170.1.7 Mapping of 800GMII signals to PLS service primitives

The Reconciliation Sublayer (RS) shall map the signals provided at the 800GMII to the PLS service primitives defined in Clause 6. The PLS service primitives provided by the RS and described here behave in exactly the same manner as defined in Clause 6. Full duplex operation only is implemented at 800 Gb/s, therefore, PLS service primitives supporting CSMA/CD operation are not mapped through the RS to the 800GMII. This behavior and restrictions are the same as described in 22.2.1, with the details of the signaling described in 170.3.

The RS maps all primitives in an identical manner as the CGMII does and as specified in 81.1.7 except that EEE and LPI signaling are not supported.

170.2 800GMII data stream

The 800GMII data stream has the same characteristics as the CGMII data stream described in 81.2.

170.3 800GMII functional specifications

The 800GMII functions identically to the CGMII specified in 81.3 except that EEE and LPI signaling are not supported.

170.4 Protocol implementation conformance statement (PICS) proforma for Clause 170, Reconciliation Sublayer (RS) and Media Independent Interface for 800 Gb/s operation (800GMII)[11]

170.4.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Clause 170, Reconciliation Sublayer (RS) and Media Independent Interface for 800 Gb/s operation (800GMII), shall complete the following protocol implementation conformance statement (PICS) proforma.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

170.4.2 Identification

170.4.2.1 Implementation identification

Supplier[1]	
Contact point for inquiries about the PICS[1]	
Implementation Name(s) and Version(s)[1,3]	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)[2]	
NOTE 1—Required for all implementations. NOTE 2—May be completed as appropriate in meeting the requirements for the identification. NOTE 3—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

170.4.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3df-2024, Clause 170, Reconciliation Sublayer (RS) and Media Independent Interface for 800 Gb/s operation (800GMII)
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3df-2024.)	

Date of Statement	

[11] *Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

170.4.3 Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
*MII	PHY support of 800GMII	170.2, 170.3		O	Yes [ ] No [ ]

170.4.4 PICS proforma tables for Reconciliation Sublayer (RS) and Media Independent Interface for 800 Gb/s operation (800GMII)

170.4.4.1 General

Item	Feature	Subclause	Value/Comment	Status	Support
G1	Cumulative MAC Control, MAC and RS delay	170.1.4	Per Table 170–1	M	Yes [ ]
G2	Lane structure	170.1.6	Per Table 81–2	M	Yes [ ]

170.4.4.2 Mapping of PLS service primitives

Item	Feature	Subclause	Value/Comment	Status	Support
PL1	Mapping to Clause 6	170.1.7	RS implements mapping to Clause 6 PLS service primitives	MII:M	Yes [ ] N/A [ ]
PL2	Mapping of PLS_DATA.requests	170.1.7	In sequence TXD<0> to TXD<63>	MII:M	Yes [ ] N/A [ ]
PL3	Start control character creation	170.1.7	First octet of preamble converted to Start control character	MII:M	Yes [ ] N/A [ ]
PL4	TXD and TXC generation	170.1.7	For each 64 PLS_DATA.requests	MII:M	Yes [ ] N/A [ ]
PL5	Terminate control character creation	170.1.7	DATA_COMPLETE causes creation of Terminate control character in next lane in sequence	MII:M	Yes [ ] N/A [ ]
PL6	Mapping RXD to PLS_DATA.indications	170.1.7	Create PLS_DATA.indications in sequence from RXD<0> to RXD<63>	MII:M	Yes [ ] N/A [ ]
PL7	PLS_DATA.indication generation	170.1.7	Generate 64 PLS_DATA.indications for each RXD<63:0> until Terminate then generating 0, 8, 16, 24, 32, 40, 48, or 56	MII:M	Yes [ ] N/A [ ]
PL8	Start control character conversion	170.1.7	Convert valid Start control character to preamble before generating PLS_DATA.indications	MII:M	Yes [ ] N/A [ ]
PL9	Terminate control character	170.1.7	No PLS_DATA.indications generated	MII:M	Yes [ ] N/A [ ]

Item	Feature	Subclause	Value/Comment	Status	Support
PL10	PLS_DATA_VALID.indication generation	170.1.7	On change of value of DATA_VALID_STATUS	MII:M	Yes [ ] N/A [ ]
PL11	DATA_VALID_STATUS	170.1.7	Value of DATA_VALID on a lane 0 Start control character preceded by eight idles, a Sequence ordered set, or a Terminate character	MII:M	Yes [ ] N/A [ ]
PL12	DATA_VALID_STATUS	170.1.7	Value of DATA_NOT_VALID on any control character but Error	MII:M	Yes [ ] N/A [ ]
PL13	Frame not ending with Terminate control character	170.1.7	Ensure MAC detects CRC error	MII:M	Yes [ ] N/A [ ]

170.4.4.3 Data stream structure

Item	Feature	Subclause	Value/Comment	Status	Support
DS1	Frame transfer	170.2	Within 800GMII data stream	MII:M	Yes [ ] N/A [ ]
DS2	Bit mapping	170.2	Per Figure 81–4	MII:M	Yes [ ] N/A [ ]
DS3	Content of <data>	170.2	Consist of data octets	MII:M	Yes [ ] N/A [ ]
DS4	Recognition of <efd>	170.2	Terminate recognized in any lane	MII:M	Yes [ ] N/A [ ]

170.4.4.4 800GMII signal functional specifications

Item	Feature	Subclause	Value/Comment	Status	Support
FS1	TX_CLK active edge	170.3	TXD and TXC sampled on the rising edge of TX_CLK	MII:M	Yes [ ] N/A [ ]
FS2	TX_CLK frequency	170.3	One-sixty-fourth of the MAC transmit data rate	MII:M	Yes [ ] N/A [ ]
FS3	TXC assertion and de-assertion	170.3	De-asserted for data, asserted for control character	MII:M	Yes [ ] N/A [ ]
FS4	TXC clock	170.3	Synchronous to TX_CLK	MII:M	Yes [ ] N/A [ ]
FS5	TXD encoding	170.3	Per Table 81–3	MII:M	Yes [ ] N/A [ ]
FS6	TXD clock	170.3	Synchronous to TX_CLK	MII:M	Yes [ ] N/A [ ]
FS7	Start alignment	170.3	Start control character aligned to lane 0	MII:M	Yes [ ] N/A [ ]
FS8	RX_CLK active edge	170.3	RXD and RXC sampled on the rising edge of RX_CLK	MII:M	Yes [ ] N/A [ ]

Item	Feature	Subclause	Value/Comment	Status	Support
FS9	RX_CLK frequency	170.3	One-sixty-fourth of the MAC receive data rate	MII:M	Yes [ ] N/A [ ]
FS10	Loss of receive signal	170.3	Source RX_CLK from nominal clock	MII:M	Yes [ ] N/A [ ]
FS11	RXC assertion and de-assertion	170.3	De-asserted for data, asserted for control character	MII:M	Yes [ ] N/A [ ]
FS12	RXC clock	170.3	Synchronous to RX_CLK	MII:M	Yes [ ] N/A [ ]
FS13	RXD decoding	170.3	Per Table 81–4	MII:M	Yes [ ] N/A [ ]
FS14	RXD clock	170.3	Synchronous to RX_CLK	MII:M	Yes [ ] N/A [ ]
FS15	Received Error control character	170.3	RS cause MAC FrameCheckError	MII:M	Yes [ ] N/A [ ]
FS16	DATA_VALID assertion	170.3	RS not assert DATA_VALID unless Start control character in lane 0	MII:M	Yes [ ] N/A [ ]

170.4.4.5 Link fault signaling state diagram

Item	Feature	Subclause	Value/Comment	Status	Support
LF1	Link fault signaling state diagram	170.3	Implement per Figure 81–11	MII:M	Yes [ ] N/A [ ]
LF2	link_fault = OK and MAC frames	170.3	RS services MAC frame transmission requests	MII:M	Yes [ ] N/A [ ]
LF3	link_fault = OK and no MAC frames	170.3	In absence of MAC frames, RS transmits Idle control characters	MII:M	Yes [ ] N/A [ ]
LF4	link_fault = Local Fault	170.3	RS transmits continuous Remote Fault Sequence ordered sets	MII:M	Yes [ ] N/A [ ]
LF5	link_fault = Remote Fault	170.3	RS transmits continuous Idle control characters	MII:M	Yes [ ] N/A [ ]

171. 800GMII Extender and 800GMII Extender Sublayer (800GXS)

171.1 Overview

This clause defines the functional characteristics for the optional 800GMII Extender and 800GMII Extender Sublayer (800GXS).

The 800GMII Extender allows the extension of the 800GMII to the PCS via a physical instantiation. The 800GMII Extender is composed of a DTE 800GXS at the RS end and a PHY 800GXS at the PHY end, with one or two 800GAUI-n between them.

Physical Layer clauses associated with the 800GMII Extender are listed in Table 171–1.

Table 171–1— Physical Layer clauses associated with the 800GMII Extender

Associated Clause	800GMII Extender
170—800GMII	Required
171—DTE 800GXS	Required
171—PHY 800GXS	Required
173—800GBASE-R PMA	Required
120F—800GAUI-8 C2C	Optional[a]
120G—800GAUI-8 C2M	Optional[a]

[a] An 800GMII Extender includes at least one 800GAUI-8.

Figure 171–1 shows the relationship of the 800GMII Extender and 800GXS with other sublayers to the ISO Open System Interconnection (OSI) reference model.

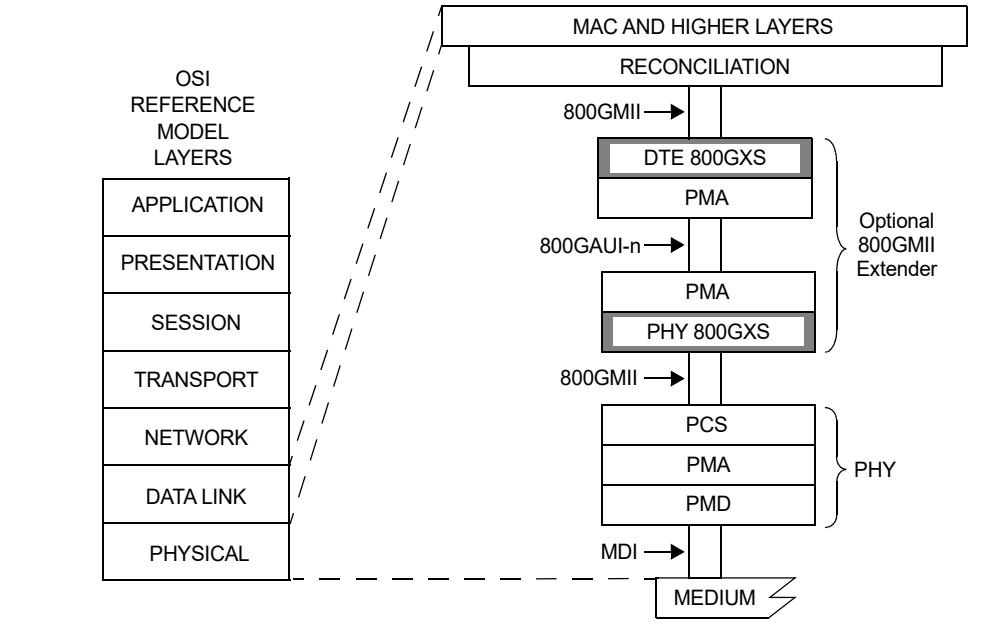


Figure 171–1—800GXS relationship to the ISO/IEC Open System Interconnection (OSI) reference model and the IEEE 802.3 Ethernet model

171.1.1 Summary of functions

The following is a list of the major functions of the 800GMII Extender:

- Simple signal mapping to the 800GMII
- The optional 800GMII Extender can be inserted between the Reconciliation Sublayer and the PHY to transparently extend the reach of the 800GMII
- Independent transmit and receive data paths
- Each 800GXS has the same functions as the 800GBASE-R PCS (see Clause 172)
- Each 800GXS connects to an 800GAUI-n as shown in Figure 171–1

171.2 DTE 800GXS

The DTE 800GXS shall be identical in function to the 800GBASE-R PCS (see Clause 172) with the exception that the FEC degrade signaling is defined in 171.6. Figure 172–2 provides a functional block diagram.

171.2.1 DTE 800GXS inter-sublayer interfaces

The service interfaces used by the DTE 800GXS are identical to those defined in 172.1.5.

171.3 PHY 800GXS

The PHY 800GXS shall be identical in function to an 800GBASE-R PCS (see Clause 172) with the following exceptions:

— The PCS is inverted with the transmit function used for the receive direction and vice versa.
— The service interface signals are remapped as defined in 171.3.2 and 171.3.3.
— FEC degrade signaling is defined in 171.6.

Figure 171–2 provides a functional block diagram of the PHY 800GXS.

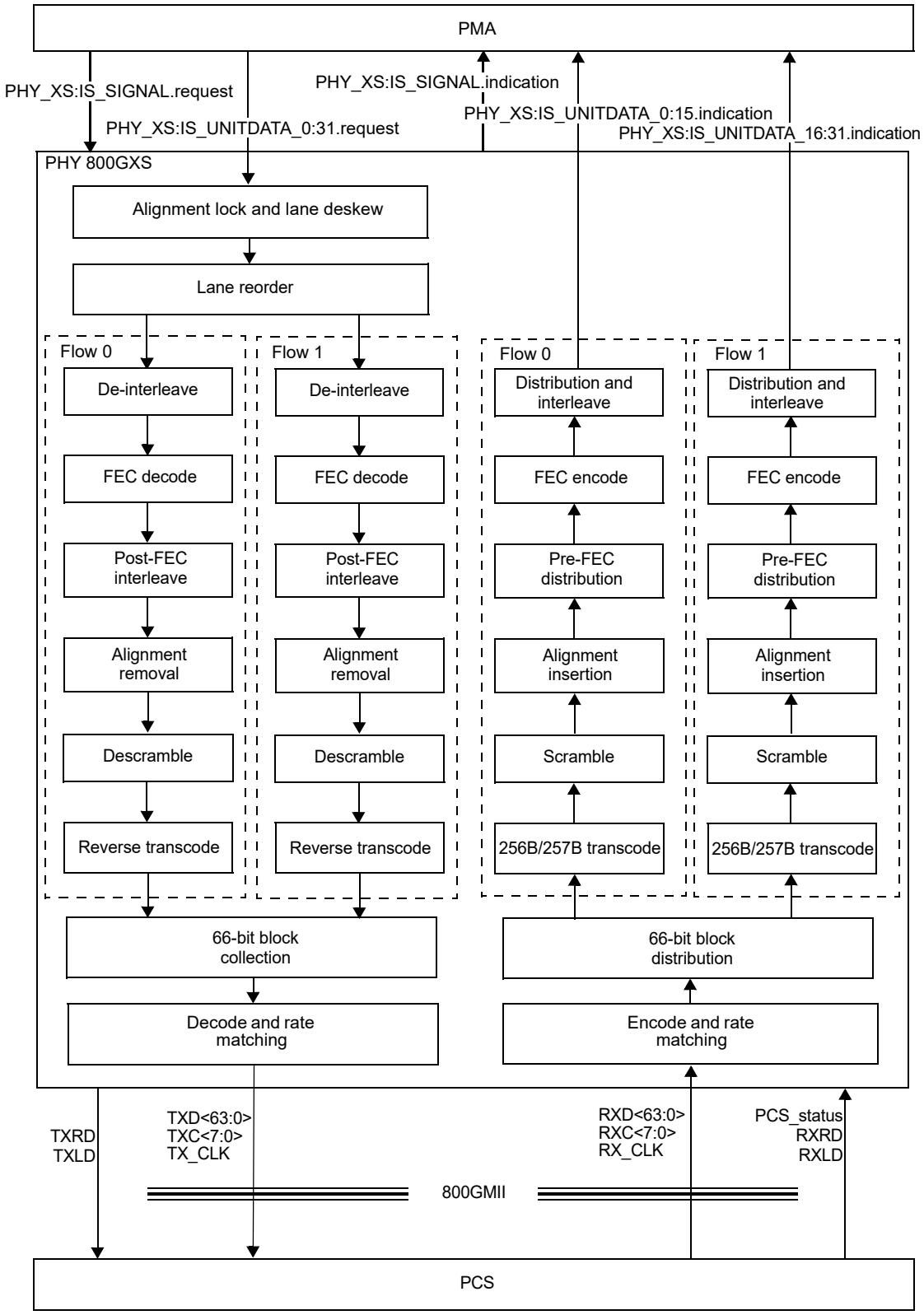


Figure 171–2—Functional block diagram for the PHY 800GXS

171.3.1 PHY 800GXS inter-sublayer interfaces

The PHY 800GXS inter-sublayer service interfaces are shown in Figure 169–3.

171.3.2 PHY 800GXS service interface

The PHY 800GXS service interface primitives are summarized as follows:

PHY_XS:IS_UNITDATA_*i*.request(tx_symbol)
PHY_XS:IS_UNITDATA_*i*.indication(rx_symbol)
PHY_XS:IS_SIGNAL.request(SIGNAL_OK)
PHY_XS:IS_SIGNAL.indication(SIGNAL_OK)

The primitives are defined for i = 0 to 31. In the transmit direction, the PHY 800GXS receives 32 parallel bit streams, each at a nominal signaling rate of 26.5625 Gb/s, from the PMA above. In the receive direction, the PHY 800GXS sends 32 parallel bit streams, each at a nominal signaling rate of 26.5625 Gb/s, to the PMA.

PHY_XS:IS_UNITDATA_*i*.request is the same as PMA:IS_UNITDATA_*i*.indication for the 32:8 PMA defined in 173.3.

PHY_XS:IS_UNITDATA_*i*.indication is the same as PMA:IS_UNITDATA_*i*.request for the 32:8 PMA defined in 173.3.

PHY_XS:IS_SIGNAL.request is the same as the PMA:IS_SIGNAL.indication for the 32:8 PMA defined in 173.3.

The PHY 800GXS provides signal status information to the PMA using the PHY_XS:IS_SIGNAL.indication(SIGNAL_OK) primitive (see Figure 171–2). The SIGNAL_OK parameter is set to OK when PCS_status (see 171.3.3) is true and is set to FAIL when PCS_status is false.

171.3.3 Service interface below the PHY 800GXS

The service interface below the PHY 800GXS allows the PHY 800GXS to transfer information to and from the PCS below.

The service interface below the PHY 800GXS is the 800GMII defined in Clause 170, with the following exceptions and additional signals:

- TX_CLK is used in place of RX_CLK, and vice versa
- TXD<63:0> is used in place of RXD<63:0>, and vice versa
- TXC<7:0> is used in place of RXC<7:0>, and vice versa
- Additional signals RXRD, RXLD, and PCS_status are provided in the receive direction (see 172.1.5.1)
- An additional signal TXRD indicates the state of the rx_rm_degraded variable (see 171.6.2) as detected by the PHY 800GXS in the transmit direction
- An additional signal TXLD indicates the state of the FEC_degraded_SER variable (see 171.6.2) as detected by the PHY 800GXS in the transmit direction

NOTE—In the transmit direction, if no idle control characters are inserted to compensate for the removal of alignment markers, the average data rate on the 800GMII will be reduced by approximately 49 ppm.

171.4 800GAUI-n

An 800GMII Extender may use any of the following electrical interfaces for the connection between its PMA sublayers, as shown in Figure 171–1:

— 800GAUI-8 chip-to-chip (Annex 120F)

— 800GAUI-8 chip-to-module (Annex 120G)

171.5 Link fault signaling in the receive direction

Link fault signaling generated by the local PHY or by the link partner is sent toward the Reconciliation Sublayer as ordered sets through the 800GMII Extender.

The PHY 800GXS provides signal status from the local PHY to the client PMA using the PHY_XS:IS_SIGNAL.indication(SIGNAL_OK) primitive (see 171.3.2 and Figure 171–2).

171.6 FEC degrade

The FEC degrade feature provides the ability to detect and indicate a degrade condition at the RS-FEC decoder using FEC degrade detection, and to propagate the FEC degrade indication using FEC degrade signaling. The propagation of FEC degrade indications across PCS and XS is described in 116.6.

FEC degrade detection is specified in 172.2.5.3. FEC degrade detection is optional.

FEC degrade signaling using the PCS alignment marker status field is specified for the DTE 800GXS and PHY 800GXS in 171.6.1 and 171.6.2, respectively.

FEC degrade signaling across the service interface below the PHY 800GXS is specified in 171.3.3.

171.6.1 DTE 800GXS FEC degrade signaling

The variable tx_am_sf is set as follows:

tx_am_sf<2:0> = {FEC_degraded_SER + rx_local_degraded,0,0}

where FEC_degraded_SER and rx_local_degraded are defined in 172.2.6.2.2 and + denotes logical OR.

171.6.2 PHY 800GXS FEC degrade signaling

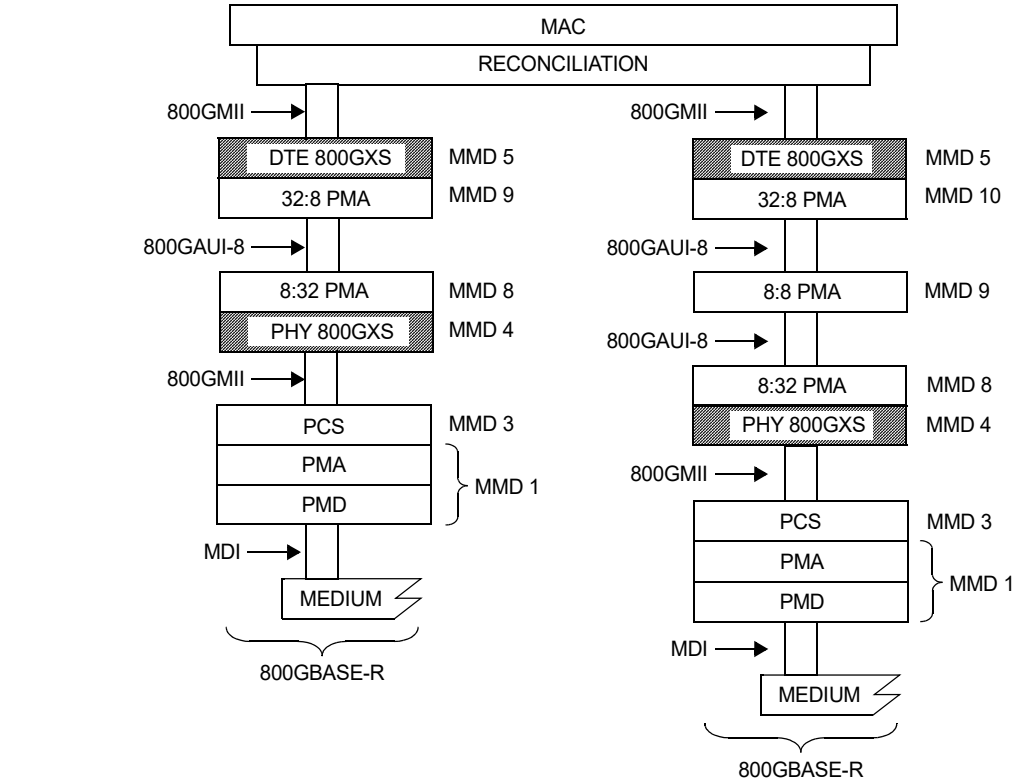
The variable tx_am_sf is set as follows:

tx_am_sf<2:0> = {RXRD, RXLD, 0}

where RXRD and RXLD are signals from the PCS on the PCS service interface (see 172.1.5.1).

171.7 800GXS partitioning example

Two partitioning examples and MMD numbering using the 800GXS are shown in Figure 171–3. Annex 173A shows additional examples of 800GXS partitioning and MMD numbering.



800GAUI = 800 Gb/s ATTACHMENT UNIT INTERFACE
800GMII = 800 Gb/s MEDIA INDEPENDENT INTERFACE
800GXS = 800GMII EXTENDER SUBLAYER
DTE = DATA TERMINAL EQUIPMENT
MAC = MEDIA ACCESS CONTROL
MDI = MEDIUM DEPENDENT INTERFACE
MMD = MDIO MANAGEABLE DEVICE
PCS = PHYSICAL CODING SUBLAYER
PHY = PHYSICAL LAYER DEVICE
PMA = PHYSICAL MEDIUM ATTACHMENT
PMD = PHYSICAL MEDIUM DEPENDENT

Figure 171–3—Example 800GBASE-R PMA layering with 800GXS

171.8 800GXS MDIO function mapping

The optional MDIO capability described in Clause 45 defines several registers that provide control and status information for and about the 800GXS. If MDIO is implemented, it shall map MDIO PHY 800GXS and DTE 800GXS control bits to Clause 172 control variables as shown in Table 171–2 and Table 171–4, respectively. Similarly, if MDIO is implemented, it shall map MDIO PHY 800GXS and DTE 800GXS status bits to Clause 172 status variables as shown in Table 171–3 and Table 171–5, respectively. MDIO registers relevant to the PHY 800GXS and DTE 800GXS are described in 45.2.4 and 45.2.5, respectively.

Table 171–2—MDIO PHY 800GXS to Clause 172 control variable mapping

MDIO control variable	PHY XS register name	Register/bit number	Clause 172 control variable
Loopback	PHY XS control 1 register	4.0.14	Loopback
Reset	PHY XS control 1 register	4.0.15	reset
Transmit test-pattern enable	BASE-R PHY XS test-pattern control register	4.42.3	tx_test_mode
PHY XS FEC bypass indication enable	PHY XS FEC control register	4.800.1	FEC_bypass_indication_enable
PHY XS FEC degraded SER enable	PHY XS FEC control register	4.800.2	FEC_degraded_SER_enable
PHY XS FEC degraded SER activate threshold	PHY XS FEC degraded SER activate threshold register	4.806, 4.807	FEC_degraded_SER_activate_threshold
PHY XS FEC degraded SER deactivate threshold	PHY XS FEC degraded SER deactivate threshold register	4.808, 4.809	FEC_degraded_SER_deactivate_threshold
PHY XS FEC degraded SER interval	PHY XS FEC degraded SER interval	4.810, 4.811	FEC_degraded_SER_interval

Table 171–3—MDIO PHY 800GXS to Clause 172 status variable mapping

MDIO status variable	PHY XS register name	Register/bit number	Clause 172 status variable
BASE-R PHY XS receive link status	BASE-R PHY XS status 1	4.32.12	PCS_status
PHY XS lane alignment status	Multi-lane BASE-R PHY XS alignment status 1	4.50.12	align_status
Lane 0 to 31 aligned	Multi-lane BASE-R PHY XS alignment status 3, 4, and 5	4.52.7:0 4.53.15:0 4.54.7:0	amps_lock<0:31>
FEC codeword counter	PHY XS RS-FEC codeword counter	4.300 to 4.302	FEC_cw_counter
FEC codeword error bin counter, 1 to 15	PHY XS RS-FEC codeword error bin, 1 to 15	4.340 to 4.369	FEC_codeword_error_bin_<1:15>
Lane 0 to 31 mapping	PHY XS lane mapping, lane 0 through lane 31	4.400 through 4.431	pcs_lane_mapping<0:31>
PHY XS FEC symbol errors, lane 0 to lane 31	PHY XS FEC symbol error counter, lane 0 to lane 31	4.600 to 4.663	FEC_symbol_error_counter <0:31>
PHY XS FEC bypass indication ability	PHY XS FEC status	4.801.1	FEC_bypass_indication_ability
PHY XS FEC high SER	PHY XS FEC status register	4.801.2	hi_ser_combined
PHY XS FEC degraded SER ability	PHY XS FEC status register	4.801.3	FEC_degraded_SER_ability

Table 171–3—MDIO PHY 800GXS to Clause 172 status variable mapping *(continued)*

MDIO status variable	PHY XS register name	Register/bit number	Clause 172 status variable
PHY XS FEC degraded SER	PHY XS FEC status register	4.801.4	FEC_degraded_SER
Remote degraded SER received	PHY XS FEC status register	4.801.5	rx_rm_degraded
Local degraded SER received	PHY XS FEC status register	4.801.6	rx_local_degraded
FEC corrected codewords	PHY XS FEC corrected codewords counter	4.802, 4.803	FEC_corrected_cw_counter
FEC uncorrected codewords	PHY XS FEC uncorrected codewords counter	4.804, 4.805	FEC_uncorrected_cw_ counter

Table 171–4—MDIO DTE 800GXS to Clause 172 control variable mapping

MDIO control variable	DTE XS register name	Register/bit number	Clause 172 control variable
Loopback	DTE XS control 1 register	5.0.14	Loopback
Reset	DTE XS control 1 register	5.0.15	reset
Transmit test-pattern enable	BASE-R DTE XS test-pattern control register	5.42.3	tx_test_mode
DTE XS FEC bypass indication enable	DTE XS FEC control register	5.800.1	FEC_bypass_indication_enable
DTE XS FEC degraded SER enable	DTE XS FEC control register	5.800.2	FEC_degraded_SER_enable
DTE XS FEC degraded SER activate threshold	DTE XS FEC degraded SER activate threshold register	5.806, 5.807	FEC_degraded_SER_activate_ threshold
DTE XS FEC degraded SER deactivate threshold	DTE XS FEC degraded SER deactivate threshold register	5.808, 5.809	FEC_degraded_SER_deactivate_ threshold
DTE XS FEC degraded SER interval	DTE XS FEC degraded SER interval	5.810, 5.811	FEC_degraded_SER_interval

Table 171–5—MDIO DTE 800GXS to Clause 172 status variable mapping

MDIO status variable	DTE XS register name	Register/bit number	Clause 172 status variable
BASE-R DTE XS receive link status	BASE-R DTE XS status 1	5.32.12	PCS_status
DTE XS lane alignment status	Multi-lane BASE-R DTE XS alignment status 1	5.50.12	align_status
Lane 0 to 31 aligned	Multi-lane BASE-R DTE XS alignment status 3,4, and 5	5.52.7:0 5.53.15:0 5.54.7:0	amps_lock<0:31>
FEC codeword counter	DTE XS RS-FEC codeword counter	5.300 to 5.302	FEC_cw_counter
FEC codeword error bin counter, 1 to 15	DTE XS RS-FEC codeword error bin, 1 to 15	5.340 to 5.369	FEC_codeword_error_bin_<1:15>
Lane 0 to 31 mapping	DTE XS lane mapping, lane 0 through lane 31	5.400 through 5.431	pcs_lane_mapping<0:31>
DTE XS FEC symbol errors, lane 0 to lane 31	DTE XS FEC symbol error counter, lane 0 to lane 31	5.600 to 5.663	FEC_symbol_error_counter <0:31>
DTE XS FEC bypass indication ability	DTE XS FEC status	5.801.1	FEC_bypass_indication_ability
DTE XS FEC high SER	DTE XS FEC status register	5.801.2	hi_ser_combined
DTE XS FEC degraded SER ability	DTE XS FEC status register	5.801.3	FEC_degraded_SER_ability
DTE XS FEC degraded SER	DTE XS FEC status register	5.801.4	FEC_degraded_SER
Remote degraded received	DTE XS FEC status register	5.801.5	rx_rm_degraded
Local degraded received	DTE XS FEC status register	5.801.6	rx_local_degraded
FEC corrected codewords	DTE XS FEC corrected codewords counter	5.802, 5.803	FEC_corrected_cw_counter
FEC uncorrected codewords	DTE XS FEC uncorrected codewords counter	5.804, 5.805	FEC_uncorrected_cw_counter

171.9 Protocol implementation conformance statement (PICS) proforma for Clause 171, 800GMII Extender and 800GMII Extender Sublayer (800GXS)[12]

171.9.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Clause 171, 800GMII Extender, and 800GMII Extender Sublayer (800GXS), shall complete the following protocol implementation conformance statement (PICS) proforma.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

171.9.2 Identification

171.9.2.1 Implementation identification

Supplier[1]	
Contact point for inquiries about the PICS[1]	
Implementation Name(s) and Version(s)[1,3]	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)[2]	
NOTE 1—Required for all implementations. NOTE 2—May be completed as appropriate in meeting the requirements for the identification. NOTE 3—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

171.9.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3df-2024, Clause 171, 800GMII Extender and 800GMII Extender Sublayer (800GXS)
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3df-2024.)	

Date of Statement	

[12]*Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

171.9.3 Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
MII	800GMII logical interface is supported	172.1.5.1		O	Yes [ ] No [ ]
*DTEXS	DTE 800GXS	171.2		O/2	Yes [ ] No [ ]
*PHYXS	PHY 800GXS	171.3		O/2	Yes [ ] No [ ]
*FDD	Support for FEC degrade detection	171.6		O	Yes [ ] No [ ]
*MD	MDIO	171.8		O	Yes [ ] No [ ]

171.9.4 PICS proforma tables for 800GMII Extender and 800GMII Extender Sublayer (800GXS)

171.9.4.1 Transmit function

Item	Feature	Subclause	Value/Comment	Status	Support
*SE	Uses stateless encoder	172.2.4.1.2		O	Yes [ ] No [ ]
TF1	Transmit 64B/66B encoder uses state diagram in Figure 119–14	172.2.4.1		!SE:M	Yes [ ] N/A [ ]
TF2	Transmit 64B/66B encoder uses stateless rules in Table 172–1	172.2.4.1.2		SE:M	Yes [ ] N/A [ ]
TF3	64B/66B to 256B/257B transcoder	172.2.4.4		M	Yes [ ]
TF4	Scrambler	172.2.4.5		M	Yes [ ]
TF5	Pad value	172.2.4.6		M	Yes [ ]
TF6	Alignment marker insertion	172.2.4.6		M	Yes [ ]
TF7	FEC degrade signaling	172.2.4.6		M	Yes [ ]
TF8	Pre-FEC distribution	172.2.4.7		M	Yes [ ]
TF9	Reed-Solomon encoder	172.2.4.8		M	Yes [ ]
TF10	Symbol distribution	172.2.4.9		M	Yes [ ]
TF11	Transmission bit ordering	172.2.4.10		M	Yes [ ]
TF12	Scrambled idle transmit test-pattern generator	172.2.4.11		M	Yes [ ]

171.9.4.2 Receive function

Item	Feature	Subclause	Value/Comment	Status	Support
*BI	Bypass indication supported	172.2.5.3		O	Yes [ ] No [ ]
*SD	Uses stateless decoder	172.2.5.9.2		O	Yes [ ] No [ ]
RF1	Alignment marker lock	172.2.5.1		M	Yes [ ]
RF2	PCS lane number is captured to an MDIO register	119.2.6.3		MD:M	Yes [ ] N/A [ ]
RF3	Deskew	172.2.5.1		M	Yes [ ]
RF4	Lane reorder and de-interleave	172.2.5.2		M	Yes [ ]
RF5	Reed-Solomon decoder corrects any combination of up to t=15 symbol errors in a codeword	172.2.5.3		M	Yes [ ]
RF6	Reed-Solomon decoder is capable of indicating when a codeword was not corrected	172.2.5.3		M	Yes [ ]
RF8	Error monitoring and assertion of hi_ser, while error indication is bypassed	172.2.5.3		BI:M	Yes [ ] N/A [ ]
RF9	Detect FEC degrade	172.2.5.3		FDD:M	Yes [ ] N/A [ ]
RF10	Alignment marker removal	172.2.5.5		M	Yes [ ]
RF11	Descrambler	172.2.5.6		M	Yes [ ]
RF12	256B/257B to 64B/66B transcoder	172.2.5.7		M	Yes [ ]
RF13	Receive 64B/66B decoder uses state diagram in Figure 119–15	172.2.5.9.1		!SD:M	Yes [ ] N/A [ ]
RF14	Receive 64B/66B decoder uses stateless rules in Table 172–4	172.2.5.9.2		SD:M	Yes [ ] N/A [ ]

171.9.4.3 64B/66B coding rules

Item	Feature	Subclause	Value/Comment	Status	Support
C1	Encoder (and ENCODE function) implements the code as specified	172.2.3, 172.2.6.2.3		M	Yes [ ]
C2	Decoder (and DECODE function) implements the code as specified	172.2.3, 172.2.6.2.3		M	Yes [ ]
C3	Only valid block types are transmitted	172.2.3		M	Yes [ ]
C4	Invalid block types are treated as an error	172.2.3		M	Yes [ ]

Item	Feature	Subclause	Value/Comment	Status	Support
C5	Only valid control characters are transmitted	172.2.3		M	Yes [ ]
C6	Invalid control characters are treated as an error	172.2.3		M	Yes [ ]
C7	Idles do not interrupt data	172.2.3		M	Yes [ ]
C8	IDLE control code insertion and deletion	172.2.3	Insertion or deletion in groups of 8 /I/s	M	Yes [ ]
C9	Sequence ordered set deletion	172.2.3	Only one whole ordered set of two consecutive sequence ordered sets may be deleted	M	Yes [ ]

171.9.4.4 Management

Item	Feature	Subclause	Value/Comment	Status	Support
M1	Equivalent access to XS management objects is provided	172.3		!MD:O	Yes [ ] No [ ] N/A [ ]
M2	Mapping of MDIO control bits and MDIO status bits for PHY 800GXS	171.8	See Table 118–1 and Table 118–2	MD*PHYXS:M	Yes [ ] N/A [ ]
M3	Mapping of MDIO control bits and MDIO status bits for DTE 800GXS	171.8	See Table 118–3 and Table 118–4	MD*DTEXS:M	Yes [ ] N/A [ ]

171.9.4.5 Loopback

Item	Feature	Subclause	Value/Comment	Status	Support
L1	Supports loopback	172.4		M	Yes [ ]
L2	When in loopback, transmits what it receives from the 800GMII	172.4		M	Yes [ ]
L3	When in loopback, ignore all data presented by the PMA	172.4		M	Yes [ ]

171.9.4.6 Delay constraints

Item	Feature	Subclause	Value/Comment	Status	Support
TIM1	800GXS delay constraint	172.5		M	Yes [ ]

172. Physical Coding Sublayer (PCS), type 800GBASE-R

172.1 Overview

172.1.1 Scope

This clause specifies the Physical Coding Sublayer (PCS) that is common to a family of Physical Layer implementations known as 800GBASE-R. The 800GBASE-R PCS is a sublayer of the 800 Gb/s PHYs listed in Table 169–1. The term 800GBASE-R is used when referring generally to Physical Layers using the PCS defined in this clause. Annex 172A provides examples of RS-FEC codewords constructed with the method specified in this clause.

172.1.2 Relationship of the 800GBASE-R PCS to other standards

Figure 172–1 shows the relationship of the 800GBASE-R PCS with other sublayers to the ISO Open System Interconnection (OSI) reference model.

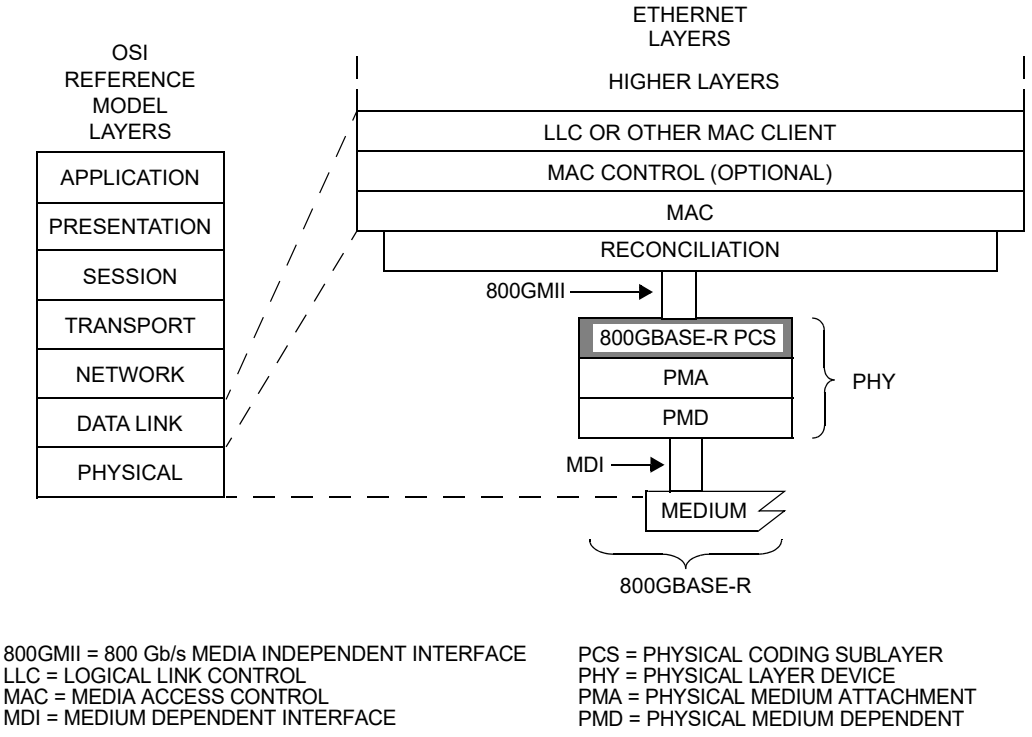


Figure 172–1—800GBASE-R PCS relationship to the ISO/IEC Open Systems Interconnection (OSI) reference model and IEEE 802.3 Ethernet model

172.1.3 Summary of functions

The PCS service interface is the 800 Gb/s Media Independent Interface (800GMII), which is defined in Clause 170. The 800GMII provides a uniform interface to the Reconciliation Sublayer for all 800 Gb/s PHY implementations.

The 800GBASE-R PCS is based on the 400GBASE-R PCS defined in Clause 119.

The 800GBASE-R PCS provide all services required by the 800GMII, including the following:

a) Encoding (decoding) of eight 800GMII data octets to (from) 66-bit blocks (64B/66B)
b) Transcoding from (to) 66-bit blocks to (from) 257-bit blocks (256B/257B)
c) Scrambling (descrambling) the 257-bit transcoded blocks
d) Alignment marker insertion and removal
e) Reed-Solomon encoding (decoding) the scrambled 257-bit blocks
f) Distribution of Reed-Solomon encoded data to (from) PCS lanes
g) Alignment marker lock, lane deskew and reordering of received PCS lanes
h) Transferring encoded data to (from) the PMA
i) Compensation for any rate differences caused by the insertion or deletion of alignment markers or due to any rate difference between the 800GMII and PMA through the insertion or deletion of idle control characters

172.1.4 FEC Degrade

The FEC degrade feature provides the ability to detect and indicate a degrade condition at the RS-FEC decoder using FEC degrade detection, and to propagate the FEC degrade indication using FEC degrade signaling. The propagation of FEC degrade indications across PCS and XS is described in 116.6.

FEC degrade detection is specified in 172.2.5.3. FEC degrade detection is optional.

FEC degrade signaling using the PCS alignment marker status field is specified for the PCS in 172.2.4.6.

FEC degrade signaling across the PCS service interface is specified in 172.1.5.1.

172.1.5 Inter-sublayer interfaces

The upper interface of the PCS connects to the Reconciliation Sublayer through the 800GMII. The lower interface of the PCS connects to the PMA to support a PMD. The 800GBASE-R PCS has a nominal rate at the PMA service interface of 26.5625 Gb/s on each of 32 PCS lanes, which provides capacity for the MAC data rate of 800 Gb/s.

While this specification defines interfaces in terms of bits, octets, and frames, implementations may choose other data-path widths for implementation convenience.

172.1.5.1 PCS service interface

The PCS service interface allows the 800GBASE-R PCS to transfer information to and from a PCS client. The PCS client is either the Reconciliation Sublayer or the PHY 800GXS.

When the client sublayer is the Reconciliation Sublayer, the PCS service interface is the 800GMII defined in Clause 170.

When the client sublayer is the PHY 800GXS, the PCS service interface is the 800GMII with additional signals TXRD, TXLD, RXRD, RXLD, and PCS_status.

The TXRD and TXLD signals indicate the state of the remote degrade and local degrade, respectively, as detected by the PHY 800GXS in the transmit direction (see 171.3.3).

The RXRD signal indicates the state of the rx_rm_degraded variable (see 172.2.6.2.2) as detected by the PCS in the receive direction.

The RXLD signal is the logical OR of the FEC_degraded_SER and rx_local_degraded variables (see 172.2.6.2.2) as detected by the PCS in the receive direction.

The PCS_status signal indicates the state of the PCS_status variable (see 119.2.6.2.2) as detected by the PCS in the receive direction.

172.1.5.2 Physical Medium Attachment (PMA) service interface

The PMA service interface supports the exchange of encoded data between the PCS and PMA. The PMA service interface is defined in 173.3 and is an instance of the inter-sublayer service interface definition in 169.3.

The PMA service interface for the PCS is described in an abstract manner and does not imply any particular implementation.

172.1.6 Functional block diagram

Figure 172–2 provides a functional block diagram of the 800GBASE-R PCS.

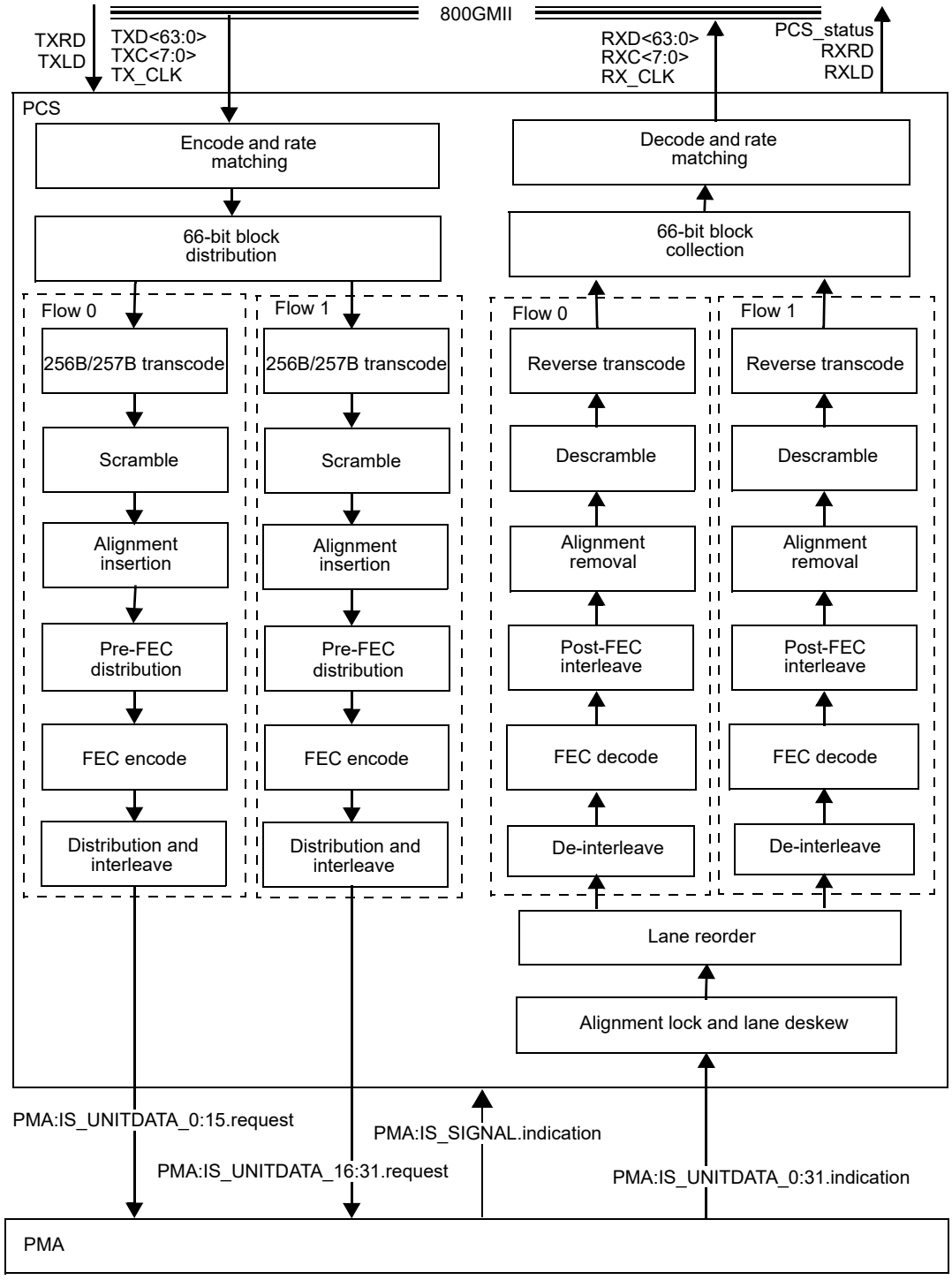


Figure 172–2—Functional block diagram

172.2 PCS functions

172.2.1 Overview

The 800GBASE-R PCS is composed of the PCS Transmit and PCS Receive processes. The PCS shields the Reconciliation Sublayer (and MAC) from the specific nature of the underlying channel.

When communicating with the 800GMII, the PCS uses an eight octet-wide, synchronous data path, with packet delineation being provided by transmit control signals (TXC<n> = 1) and receive control signals (RXC<n> = 1). When communicating with the PMA, the 800GBASE-R PCS uses 32 encoded bit streams also known as PCS lanes. Per direction (receive or transmit), the PCS lanes originate from a common clock but may vary in phase and skew dynamically. The PMA operates independently of block and packet boundaries. The PCS provides the functions necessary to map packets between the 800GMII format and the PMA service interface format.

The PCS transmit function can operate in normal mode or test-pattern mode.

When the transmit function is in normal mode, the PCS Transmit process continuously generates 66-bit blocks based on the TXD <63:0> and TXC <7:0> signals on the 800GMII. This takes place in the encode and rate matching function shown in Figure 172–2. The 66-bit blocks are then distributed between two parallel transmit functions, referred to as flow 0 and flow 1. Within each flow, the 66-bit blocks are transcoded to 257-bit blocks and scrambled. Alignment markers are periodically inserted into the data stream of each flow following the requirements specified in 172.2.4.6. For each flow, the data stream is distributed to two 5140-bit blocks and then FEC encoded. For each flow, the two FEC codewords are then interleaved before data is distributed to individual PCS lanes.

Transmit data units are sent to the service interface via the PMA:IS_UNITDATA_0:31.request primitive.

When the transmit function is in test-pattern mode, a test pattern is packed into the transmit data units that are sent to the PMA service interface via the PMA:IS_UNITDATA_0:31.request primitive.

In the receive direction, the PCS Synchronization process continuously monitors PMA:IS_SIGNAL.indication(SIGNAL_OK). When SIGNAL_OK indicates OK, then the PCS synchronization process accepts data units via the PMA:IS_UNITDATA_0:31.indication primitive. It attains alignment marker lock based on the common marker (CM) portion of the alignment markers that are periodically transmitted on every PCS lane and identifies individual PCS lanes using the unique marker (UM) portion of the alignment marker. The PCS lanes are then reordered and deskewed, and the align_status flag is set. Note that a particular transmit PCS lane can be received on any receive lane of the service interface due to the skew and multiplexing that occurs in the path.

The PCS Receive process separates the reordered PCS lanes into two sets of 16 PCS lanes belonging to each flow. Within a flow, the data from the 16 PCS lanes is de-interleaved, processed by the FEC decoder, and re-interleaved on a 10-bit basis to form a single data stream. The alignment markers are removed, the data is descrambled and reverse transcoded back to 66-bit blocks. A 66-bit block collection function merges the 66-bit blocks from the two flows into a single stream of blocks that are then 64B/66B decoded.

172.2.2 Use of 66-bit blocks

The PCS maps 800GMII signals into 66-bit blocks, and vice versa, using a 64B/66B coding scheme. The PCS functions ENCODE and DECODE generate, manipulate, and interpret 66-bit blocks as defined in 172.2.3.

172.2.3 64B/66B code

The 64B/66B code is identical to that specified in 119.2.3 with the following exceptions:

— 200GMII/400GMII is replaced with 800GMII.
— 200GBASE-R/400GBASE-R is replaced with 800GBASE-R.
— EEE and Low Power Idle are not supported.

172.2.4 Transmit function

172.2.4.1 64B/66B encoder

The transmit PCS generates 66-bit blocks based on the TXD<63:0> and TXC<7:0> signals received from the 800GMII. Each 800GMII transfer is encoded into one 66-bit block. The contents of each 66-bit block are contained in a vector tx_coded<65:0> with tx_coded<1:0> containing the sync header and the remainder of the bits the payload. The transmit PCS shall use the encoding method defined in either 172.2.4.1.1 or 172.2.4.1.2.

172.2.4.1.1 State-diagram encoder

The state-diagram encoder generates 66-bit blocks based on the TXD<63:0> and TXC<7:0> signals received from the 800GMII as specified by the transmit state diagram shown in Figure 119–14.

172.2.4.1.2 Stateless encoder

The stateless encoder generates 66-bit blocks based only on the current and preceding 800GMII transfers. Each 800GMII transfer is mapped into a 72-bit vector tx_raw<71:0> (see 172.2.6.2.2). The encoder shall encode each tx_raw<71:0> to a 66-bit block tx_coded<65:0> according to the rules in Table 172–1. Constants LBLOCK_T and EBLOCK_T are defined in 172.2.6.2.1. Variables reset, tx_raw, and tx_coded are defined in 172.2.6.2.2. Functions T_TYPE and ENCODE, and the block types, are defined in 172.2.6.2.3.

Table 172–1—PCS stateless encoder rules

reset	T_TYPE(tx_raw_{i-1})[a]	T_TYPE(tx_raw_i)[b]	Resulting tx_coded
1	any block type	any block type	LBLOCK_T
0	C or T	C	ENCODE(tx_raw_i)
0	C or T	S	ENCODE(tx_raw_i)
0	S or D	D	ENCODE(tx_raw_i)
0	S or D	T	ENCODE(tx_raw_i)
0	any combination not listed above		EBLOCK_T

[a] tx_raw_{i-1} is the 72-bit vector that immediately precedes tx_raw_i.
[b] tx_raw_i is the 72-bit vector that is being encoded.

172.2.4.2 Rate matching

The transmit PCS may remove idle control characters or sequence ordered sets to compensate for the insertion of alignment markers. The transmit PCS may remove idle control characters or sequence ordered

sets or may insert idle control characters to compensate for different clock domains on the 800GMII and the PMA service interface. See 119.2.3.5 and 119.2.3.8 for the deletion and insertion rules.

172.2.4.3 Block distribution

The 66-bit blocks are distributed to the two flows in an alternating fashion by the block distribution function such that the first 66-bit block is sent to flow 0, the second 66-bit block is sent to flow 1, the third 66-bit block is sent to flow 0, and subsequent 66-bit blocks continue the distribution procedure across the two flows.

172.2.4.4 64B/66B to 256B/257B transcoder

The 64B/66B to 256B/257B transcoder in each flow is identical to that specified in 119.2.4.2.

NOTE—The two streams of 257-bit blocks generated by this process, together with the FEC_degraded_SER and rx_local_degraded bits should be used as the reference signal for mapping to OTN. The details of how to combine the two streams of 257-bit blocks into a single stream are outside the scope of this document.

172.2.4.5 Scrambler

The scrambler in each flow is identical to that specified in 119.2.4.3. Although there is no requirement on the initial value of each scrambler, if an implementation sets the scrambler state to a fixed value (e.g., when reset is asserted), the two scramblers should be set to different states.

NOTE— If the two scramblers have the same state and the same input (e.g., encoded Remote Fault signal), their outputs will be identical. In that case, specific choices of input lanes in the PMA bit-multiplexing function can create atypical sequences on the PMA output.

172.2.4.6 Alignment marker mapping and insertion

The alignment marker mapping and insertion in each flow is identical to the 400GBASE-R alignment marker and insertion function specified in 119.2.4.4 with the following exceptions:

- Alignment marker encoding values for flow 0 are specified in Table 172–2.
- Alignment marker encoding values for flow 1 are specified in Table 172–3 and the variable *x* in 119.2.4.4.2 takes the values of PCS lane number minus 16.
- The alignment marker insertion within each flow shall occur at the same point relative to the original stream of 66-bit blocks before block distribution. This requirement is illustrated in Figure 172–3 where the alignment marker group is inserted prior to the 257-bit block containing the 66-bit block *k* for flow 0 and prior to the 257-bit block containing the 66-bit block *k*+1 for flow 1.
- When the client sublayer is the Reconciliation Sublayer, tx_am_sf<2:0> is assigned as follows:
  tx_am_sf<2:0> = {FEC_degraded_SER + rx_local_degraded, 0, 0}
  where FEC_degraded_SER and rx_local_degraded are defined in 172.2.6.2.2 and + denotes logical OR.
- When the client sublayer is the PHY 800GXS, tx_am_sf<2:0> is assigned as follows:
  tx_am_sf<2:0> = {TXRD, TXLD, 0}
  where TXRD and TXLD are signals from the PHY 800GXS on the PCS service interface (see 172.1.5.1).

The alignment marker format for each PCS lane is shown in Figure 119–4. There is a portion that is common across all alignment markers (designated as CM0 to CM5), a unique portion per PCS lane (designated as UM0 to UM5), and a unique pad per PCS lane within a flow (designated as UP0 to UP2). The pad in PCS lane *j* is the same as that in PCS lane *j* + 16 where *j* takes values from 0 to 15.

NOTE—A text file containing the alignment marker patterns, as shown in Table 172–2 and Table 172–3, is available at https://standards.ieee.org/downloads/802.3/.

Table 172–2—800GBASE-R flow 0 alignment marker encodings

PCS lane number	Encoding[a]														
	CM0	CM1	CM2	UP0	CM3	CM4	CM5	UP1	UM0	UM1	UM2	UP2	UM3	UM4	UM5
0	0x9A	0x4A	0x26	0xB6	0x65	0xB5	0xD9	0xD9	0xFE	0x71	0xF3	0x26	0x01	0x8E	0x0C
1				0x04				0x67	0xA5	0xDE	0x7E	0x98	0x5A	0x21	0x81
2				0x46				0xFE	0xC1	0xF3	0x56	0x01	0x3E	0x0C	0xA9
3				0x5A				0x84	0x79	0x80	0xD0	0x7B	0x86	0x7F	0x2F
4				0xE1				0x19	0xD5	0x51	0xF2	0xE6	0x2A	0xAE	0x0D
5				0xF2				0x4E	0xED	0x4F	0xD1	0xB1	0x12	0xB0	0x2E
6				0x3D				0xEE	0xBD	0x9C	0xA1	0x11	0x42	0x63	0x5E
7				0x22				0x32	0x29	0x76	0x5B	0xCD	0xD6	0x89	0xA4
8				0x60				0x9F	0x1E	0x73	0x75	0x60	0xE1	0x8C	0x8A
9				0x6B				0xA2	0x8E	0xC4	0x3C	0x5D	0x71	0x3B	0xC3
10				0xFA				0x04	0x6A	0xEB	0xD8	0xFB	0x95	0x14	0x27
11				0x6C				0x71	0xDD	0x66	0x38	0x8E	0x22	0x99	0xC7
12				0x18				0x5B	0x5D	0xF6	0x95	0xA4	0xA2	0x09	0x6A
13				0x14				0xCC	0xCE	0x97	0xC3	0x33	0x31	0x68	0x3C
14				0xD0				0xB1	0x35	0xFB	0xA6	0x4E	0xCA	0x04	0x59
15				0xB4				0x56	0x59	0xBA	0x79	0xA9	0xA6	0x45	0x86

[a] Each octet is transmitted LSB to MSB.

Table 172–3—800GBASE-R flow 1 alignment marker encodings

PCS lane number	Encoding[a]														
	CM0	CM1	CM2	UP0	CM3	CM4	CM5	UP1	UM0	UM1	UM2	UP2	UM3	UM4	UM5
16	0x9A	0x4A	0x26	0xB6	0x65	0xB5	0xD9	0xD9	0x01	0x8E	0x0C	0x26	0xFE	0x71	0xF3
17				0x04				0x67	0x5A	0x21	0x81	0x98	0xA5	0xDE	0x7E
18				0x46				0xFE	0x3E	0x0C	0xA9	0x01	0xC1	0xF3	0x56
19				0x5A				0x84	0x86	0x7F	0x2F	0x7B	0x79	0x80	0xD0
20				0xE1				0x19	0x2A	0xAE	0x0D	0xE6	0xD5	0x51	0xF2
21				0xF2				0x4E	0x12	0xB0	0x2E	0xB1	0xED	0x4F	0xD1
22				0x3D				0xEE	0x42	0x63	0x5E	0x11	0xBD	0x9C	0xA1
23				0x22				0x32	0xD6	0x89	0xA4	0xCD	0x29	0x76	0x5B
24				0x60				0x9F	0xE1	0x8C	0x8A	0x60	0x1E	0x73	0x75
25				0x6B				0xA2	0x71	0x3B	0xC3	0x5D	0x8E	0xC4	0x3C
26				0xFA				0x04	0x95	0x14	0x27	0xFB	0x6A	0xEB	0xD8
27				0x6C				0x71	0x22	0x99	0xC7	0x8E	0xDD	0x66	0x38
28				0x18				0x5B	0xA2	0x09	0x6A	0xA4	0x5D	0xF6	0x95
29				0x14				0xCC	0x31	0x68	0x3C	0x33	0xCE	0x97	0xC3
30				0xD0				0xB1	0xCA	0x04	0x59	0x4E	0x35	0xFB	0xA6
31				0xB4				0x56	0xA6	0x45	0x86	0xA9	0x59	0xBA	0x79

[a] Each octet is transmitted LSB to MSB.

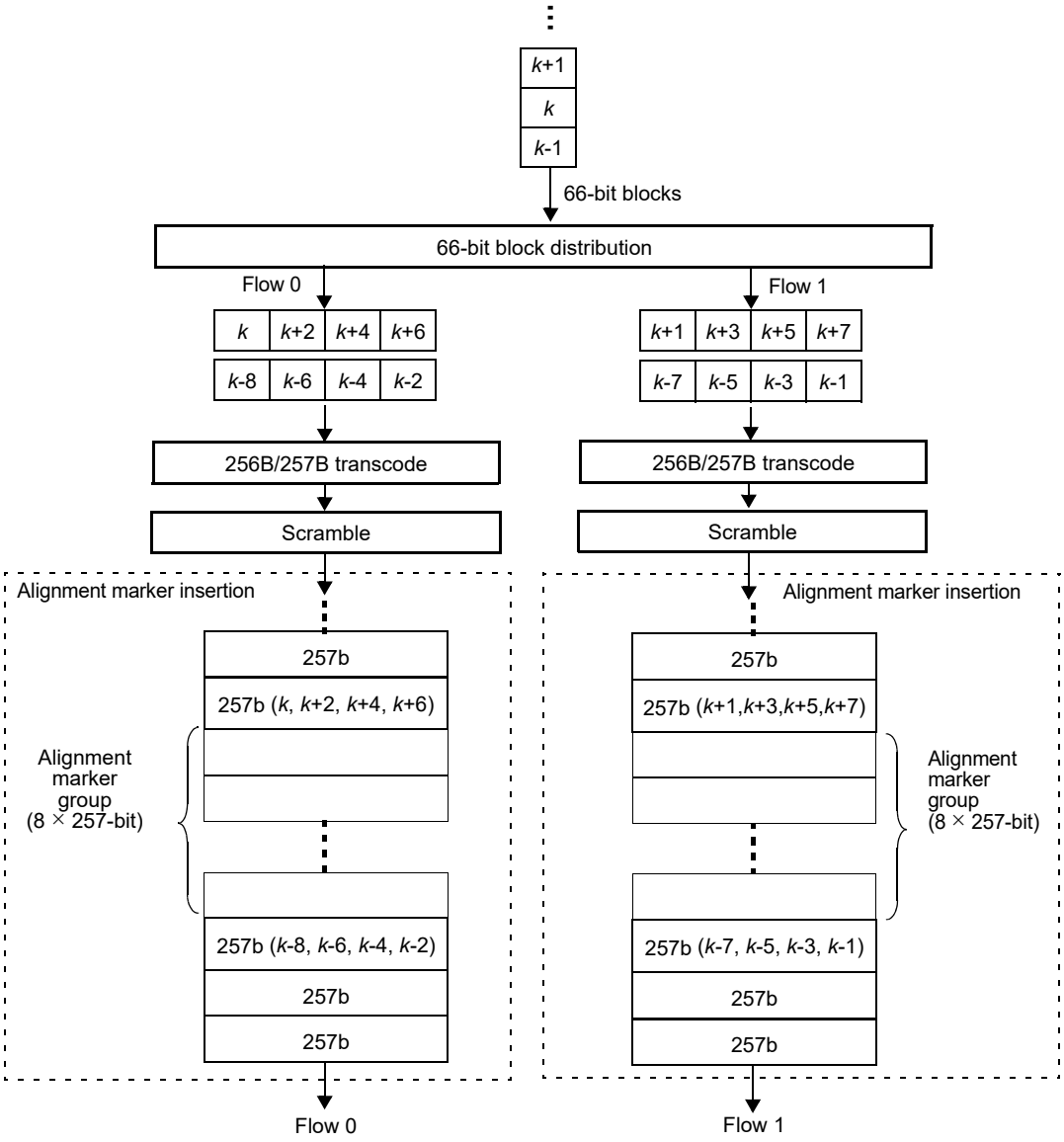


Figure 172–3—800GBASE-R PCS alignment marker insertion

172.2.4.7 Pre-FEC distribution

The pre-FEC distribution in each flow is identical to that specified in 119.2.4.5.

172.2.4.8 Reed-Solomon encoder

The Reed-Solomon encoder in each flow is identical to that specified in 119.2.4.6. Examples of RS-FEC codewords are provided in Annex 172A.

172.2.4.9 Symbol distribution

The symbol distribution in each flow is identical to the symbol distribution of the 400GBASE-R PCS in 119.2.4.7.

172.2.4.10 Transmit bit ordering and distribution

The transmit bit ordering and distribution is illustrated in Figure 172–4. The transmit bit ordering and distribution in "Flow 0 transmit function" and "Flow 1 transmit function" are identical to the 400GBASE-R transmit bit ordering and distribution in Figure 119–11 with the following exceptions:

— The "66-bit block distribution" of Figure 172–4 directly feeds into the "64B/66B to 256B/257B transcoder" in each flow's transmit function shown in Figure 119–11, and the functional blocks above the "64B/66B to 256B/257B transcoder" in each flow are not used.

— For flow 1, the PMA service interface lane numbers 0:15 are replaced with 16:31, respectively.

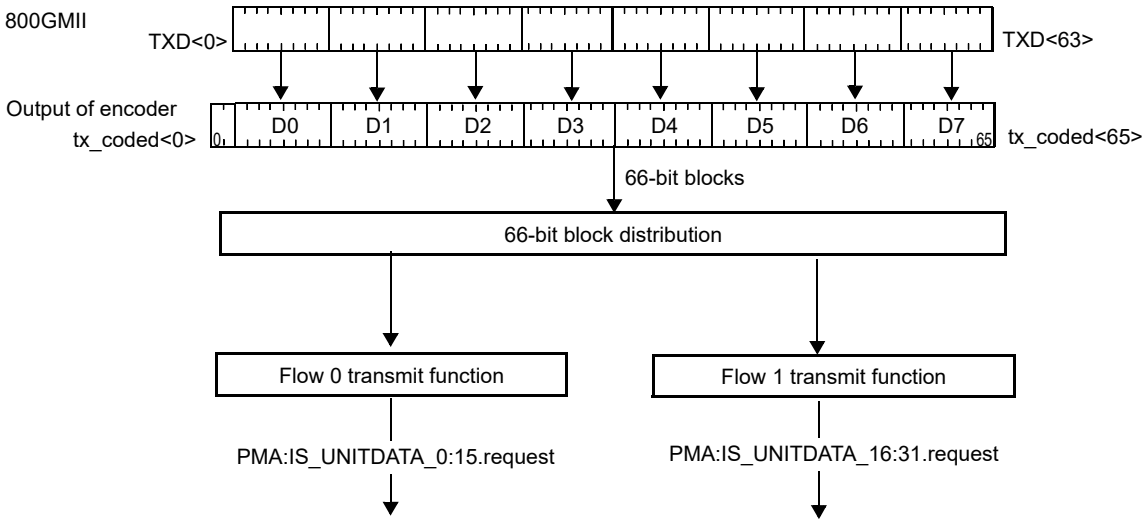


Figure 172–4—800GBASE-R PCS transmit bit ordering and distribution

172.2.4.11 Test-pattern generator

The PCS shall have the ability to generate a scrambled idle test pattern, which is suitable for receiver tests and for certain transmitter tests. When test pattern generation is enabled (tx_test_mode is 1), the scrambled idle test pattern is generated by the PCS. The scrambled idle test pattern is the output of the PCS when the input to the PCS at the 800GMII is composed only of idle control characters.

If a Clause 45 MDIO is implemented, then the tx_test_mode variable is accessible through the register as shown in Table 172–5.

172.2.5 Receive function

172.2.5.1 Alignment lock and deskew

The alignment lock and deskew is identical to that specified in 119.2.5.1 with the following exceptions:

— $n = 32$

— Figure 119–13 is replaced with Figure 172–5 and Figure 172–6.

— The maximum Skew is changed from 180 ns to 152 ns.

172.2.5.2 Lane reorder and de-interleave

The PCS lanes might be received in any order on the PMA service interface lanes. The PCS receive function shall order the PCS lanes according to the PCS lane number. The PCS lane number is defined by the unique portion (UM_0 to UM_5) of the alignment marker that is mapped to each PCS lane (see 172.2.4.6).

After all 32 PCS lanes are aligned, deskewed, and reordered, they are separated into two sets of 16 PCS lanes belonging to each flow. PCS lanes 0 to 15 are sent to flow 0 and PCS lanes 16 to 31 are sent to flow 1. Within a flow, the data from the 16 PCS lanes is de-interleaved to reconstruct the original two streams of FEC codewords.

172.2.5.3 Reed-Solomon decoder

The Reed-Solomon decoder is identical to that specified in 119.2.5.3, with the following exceptions:

— FEC_degraded_SER in flow 0 and flow 1 are mapped to FEC_degraded_SER_0 and FEC_degraded_SER_1, respectively.

— hi_ser in flow 0 and flow 1 are mapped to hi_ser_0 and hi_ser_1, respectively.

The FEC degrade detection is optional.

172.2.5.4 Post-FEC interleave

The post-FEC interleave in each flow is identical to that specified in 119.2.5.4.

172.2.5.5 Alignment marker removal

The alignment marker removal in each flow is identical to that of the 400GBASE-R PCS in 119.2.5.5.

172.2.5.6 Descrambler

The descrambler in each flow is identical to that specified in 119.2.5.6.

172.2.5.7 256B/257B to 64B/66B transcoder

The 256B/257B to 64B/66B transcoder in each flow is identical to that specified in 119.2.5.7.

172.2.5.8 Block collection

The block collection reverses the block distribution done in the transmitter (see 172.2.4.3) by combining the 66-bit blocks from the two flows in an alternating fashion to form a single stream of 66-bit blocks. The first 66-bit block after the alignment marker group from flow 0 shall be followed by the first 66-bit block after the alignment marker group from flow 1.

172.2.5.9 64B/66B decoder

The receive PCS decodes 66-bit blocks to produce RXD<63:0> and RXC<7:0> for transmission to the 800GMII. One 800GMII transfer is decoded from each 66-bit block. The receive PCS shall use one of the two decoding methods that are defined in 172.2.5.9.1 and 172.2.5.9.2.

172.2.5.9.1 State-diagram decoder

The state-diagram decoder decodes 66-bit blocks to produce RXD<63:0> and RXC<7:0> for transmission to the 800GMII as specified by the receive state diagram shown in Figure 119–15.

172.2.5.9.2 Stateless decoder

The stateless decoder generates 800GMII transfers based only on the current and preceding 66-bit blocks. The decoder shall decode each 66-bit block rx_coded<65:0> to a 72-bit vector rx_raw<71:0> (see 172.2.6.2.2) according to the rules in Table 172–4. Constants LBLOCK_R and EBLOCK_R are defined in 172.2.6.2.1. Variables reset, rx_raw, and rx_coded are defined in 172.2.6.2.2. Functions R_TYPE and DECODE, and the block types, are defined in 172.2.6.2.3.

Table 172–4—PCS stateless decoder rules

reset	R_TYPE(rx_coded$_{i-1}$)[a]	R_TYPE(rx_coded$_i$)[b]	Resulting rx_raw
1	any block type	any block type	LBLOCK_R
0	any block type	E	EBLOCK_R
0	E	any block type	EBLOCK_R
0	any combination not listed above		DECODE(rx_coded$_i$)

[a] rx_coded$_{i-1}$ is the 66-bit block that immediately precedes rx_coded$_i$.
[b] rx_coded$_i$ is the 66-bit block that is being decoded.

172.2.5.10 Rate matching

The receive PCS may insert idle control characters to compensate for the deletion of alignment markers. The receive PCS may remove idle control characters or sequence ordered sets or may insert idle control characters to compensate for different clock domains on the PMA service interface and the 800GMII. See 119.2.3.5 and 119.2.3.8 for the deletion and insertion rules.

NOTE—If no idle control characters are inserted to compensate for the removal of alignment markers, the average data rate on the 800GMII will be reduced by approximately 49 ppm.

172.2.6 Detailed functions and state diagrams

172.2.6.1 State diagram conventions

The body of this subclause is composed of state diagrams, including the associated definitions of variables, functions, and counters. Should there be a discrepancy between a state diagram and descriptive text, the state diagram prevails.

The notation used in the state diagrams follows the conventions of 21.5. The notation ++ after a counter or integer variable indicates that its value is to be incremented by 1.

172.2.6.2 State variables

172.2.6.2.1 Constants

The constants are the same as those specified in 119.2.6.2.1 with the following exception:

— 200GMII/400GMII is replaced with 800GMII.

172.2.6.2.2 Variables

The variables are the same as those specified in 119.2.6.2.2 with the following exceptions:

— 200GMII/400GMII is replaced with 800GMII.

— Some variables are modified or added as follows.

The following variable definitions are used in place of those defined in 119.2.6.2.2.

amps_lock<*x*>
: Same behavior as in 119.2.6.2.2 with *x* = 0:31.

current_pcsl
: Same behavior as in 119.2.6.2.2 with the exception that the unique marker bits are defined in Table 172–2 and Table 172–3.

pcs_alignment_valid
: Same behavior as 119.2.6.2.2 with the exception that the unique alignment markers are defined in 172.2.4.6.

restart_lock
: Boolean variable that is set by the PCS synchronization process to restart the alignment marker lock process on all PCS lanes. It is set to true in the DESKEW_FAIL state or if either restart_lock<*y*> are true. It is set to false upon entry into the LOSS_OF_ALIGNMENT state.

rx_local_degraded
: Boolean variable that is set to true when the receiver in either flow detects rx_am_sf<1> asserted for two consecutive alignment marker periods. It is deasserted when rx_am_sf<1> is deasserted for two consecutive alignment marker periods in both flows. If a Clause 45 MDIO is implemented, this variable is mapped per Table 172–6.

rx_rm_degraded
: Boolean variable that is set to true when the receiver in either flow detects rx_am_sf<2> asserted for two consecutive alignment marker periods. It is deasserted when rx_am_sf<2> is deasserted for two consecutive alignment marker periods in both flows. If a Clause 45 MDIO is implemented, this variable is mapped per Table 172–6.

The following variable definitions are added to those defined in 119.2.6.2.2.

FEC_degraded_SER
: Boolean variable that is the logical OR of FEC_degraded_SER_0 and FEC_degraded_SER_1 (see 172.2.5.3). If a Clause 45 MDIO is implemented, the status of this variable is mapped per Table 172–6.

hi_ser_combined

Boolean variable that is the logical OR of hi_ser_0 and hi_ser_1 (see 172.2.5.3). If a Clause 45 MDIO is implemented, the status of this variable is mapped per Table 172–6.

restart_lock<*y*>

Per flow Boolean variable that is set to true after 3 consecutive uncorrected codewords are received (3_BAD state) by the RS-FEC decoder of flow *y*, where *y* is 0 or 1.

172.2.6.2.3 Functions

The functions are the same as those specified in 119.2.6.2.3 with the following exceptions:

— 200GMII/400GMII is replaced with 800GMII.
— EEE and Low Power Idle are not supported.

172.2.6.2.4 Counters

The counters are the same as those specified in 119.2.6.2.4 for the 400GBASE-R PCS with the following exception:

amp_counter

This counter counts the interval of 16 384 FEC codewords containing alignment marker payload sequences for the 800GBASE-R PCS.

172.2.6.3 State diagrams

The state diagrams are identical to those specified in 119.2.6.3 with the following exceptions:

— The 800GBASE-R PCS implements 32 alignment marker lock processes (Figure 119–12).
— The PCS lane mapping registers are found in MDIO registers 3.400 to 3.431 (see 172.3.1).
— The PCS synchronization process is depicted in Figure 172–5 and Figure 172–6, instead of in Figure 119–13.
— The monitor for three consecutive uncorrectable FEC codewords (see Figure 172–6) is done independently within each flow.

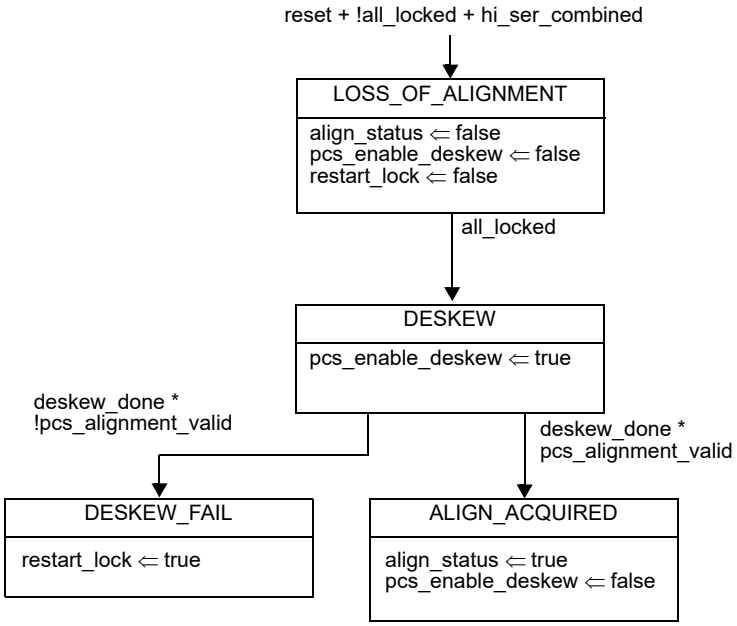


Figure 172–5—PCS synchronization state diagram

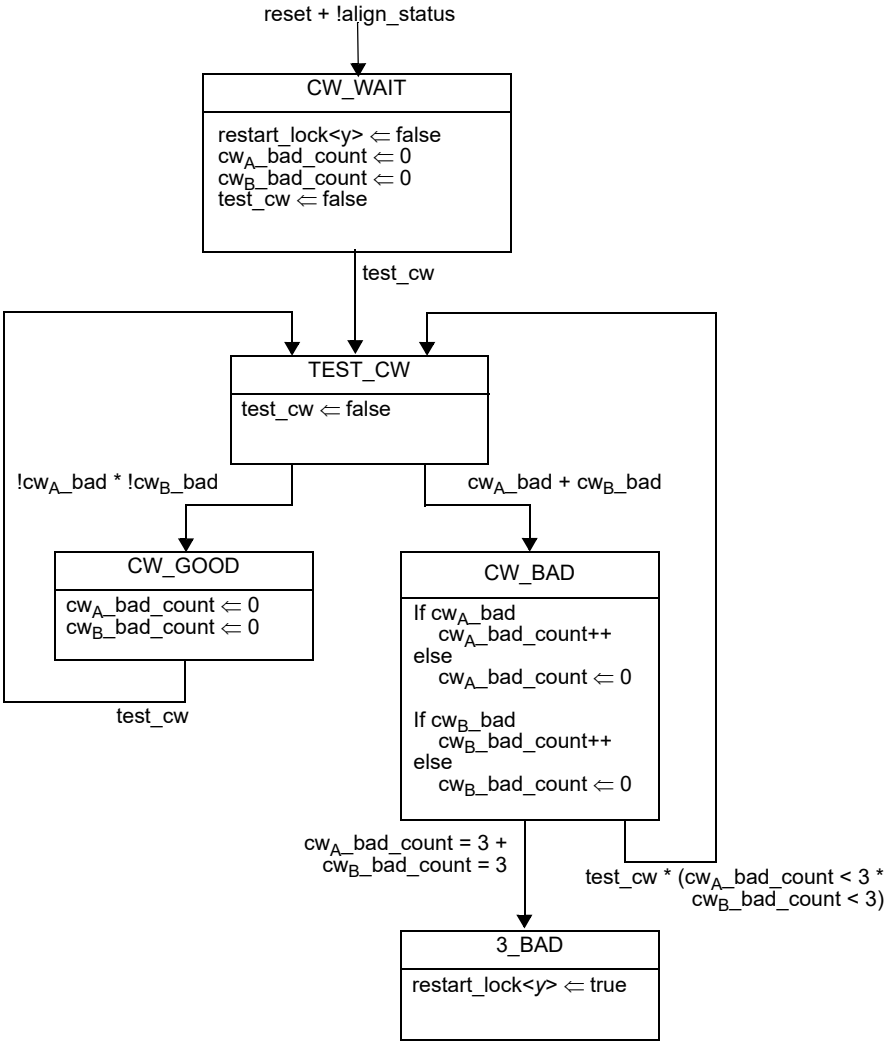


Figure 172–6—PCS per-flow codeword monitor state diagram

172.3 PCS management

The following objects apply to PCS management. If an MDIO Interface is provided (see Clause 45), they are accessed via that interface. If not, it is recommended that an equivalent access is provided.

172.3.1 PCS MDIO function mapping

The optional MDIO capability described in Clause 45 defines several registers that provide control and status information for and about the PCS. If MDIO is implemented, it shall map MDIO control bits to PCS control variables, as shown in Table 172–5, and MDIO status bits to PCS status variables, as shown in Table 172–6. MDIO registers relevant to the 800GBASE-R PCS are described in 45.2.3.

Table 172–5—MDIO/PCS control variable mapping

MDIO control variable	PCS register name	Register/bit number	PCS control variable
Loopback	PCS control 1 register	3.0.14	Loopback
Reset	PCS control 1 register	3.0.15	reset
Transmit test-pattern enable	BASE-R PCS test-pattern control register	3.42.3	tx_test_mode
PCS FEC bypass indication enable	PCS FEC control register	3.800.1	FEC_bypass_indication_enable
PCS FEC degraded SER enable	PCS FEC control register	3.800.2	FEC_degraded_SER_enable
PCS FEC degraded SER activate threshold	PCS FEC degraded SER activate threshold register	3.806, 3.807	FEC_degraded_SER_activate_ threshold
PCS FEC degraded SER deactivate threshold	PCS FEC degraded SER deactivate threshold register	3.808, 3.809	FEC_degraded_SER_deactivate_ threshold
PCS FEC degraded SER interval	PCS FEC degraded SER interval	3.810, 3.811	FEC_degraded_SER_interval

Table 172–6—MDIO/PCS status variable mapping

MDIO status variable	PCS register name	Register/bit number	PCS status variable
BASE-R and MultiGBASE-T receive link status	BASE-R and MultiGBASE-T PCS status 1 register	3.32.12	PCS_status
PCS lane alignment status	Multi-lane BASE-R PCS alignment status 1 register	3.50.12	align_status
Lane 0 to 31 aligned	Multi-lane BASE-R PCS alignment status registers	3.52.7:0 3.53.15:0 3.54.7:0	amps_lock<0:31>
FEC codeword counter	PCS FEC codeword counter register	3.300 to 3.302	FEC_cw_counter
FEC codeword error bin counter, 1 to 15	PCS FEC codeword error bin, 1 to 15	3.340 to 3.369	FEC_codeword_error_bin_ <1:15>
Lane 0 to 31 mapping	Lane *x* mapping register	3.400 through 3.431	pcs_lane_mapping<0:31>
PCS FEC symbol errors, PCS lanes 0 to 31	PCS FEC symbol error counter register, lanes 0 to 31	3.600 to 3.663	FEC_symbol_error_counter _<0:31>
PCS FEC bypass indication ability	PCS FEC status register	3.801.1	FEC_bypass_indication_ ability
PCS FEC high SER	PCS FEC status register	3.801.2	hi_ser_combined
PCS FEC degraded SER ability	PCS FEC status register	3.801.3	FEC_degraded_SER_ability
PCS FEC degraded SER	PCS FEC status register	3.801.4	FEC_degraded_SER

Table 172–6—MDIO/PCS status variable mapping *(continued)*

MDIO status variable	PCS register name	Register/bit number	PCS status variable
Remote degraded SER received	PCS FEC status register	3.801.5	rx_rm_degraded
Local degraded SER received	PCS FEC status register	3.801.6	rx_local_degraded
PCS FEC corrected codewords	PCS FEC corrected codewords counter register	3.802, 3.803	FEC_corrected_cw_counter
PCS FEC uncorrected codewords	PCS FEC uncorrected codewords counter register	3.804, 3.805	FEC_uncorrected_cw_ counter

172.3.2 FEC_corrected_cw_counter

The FEC_corrected_cw_counter is identical to 119.3.2 with the clarification that the count includes both flows.

172.3.3 FEC_uncorrected_cw_counter

The FEC_uncorrected_cw_counter is identical to 119.3.3 with the clarification that the count includes both flows.

172.3.4 FEC_symbol_error_counter_*i*

FEC_symbol_error_counter_*i* (where *i*=0 to 31 for the 800GBASE-R PCS) are 32-bit counters that count once for each 10-bit symbol corrected on PCS lane *i* when align_status is true. These variables are mapped to the registers defined in Table 172–6.

172.3.5 FEC_cw_counter

The FEC_cw_counter is an optional 48-bit counter that counts once for each FEC codeword received when align_status is true. This variable is mapped to the registers defined in 45.2.3.48a (3.300 to 3.302).

172.3.6 FEC_codeword_error_bin_*i*

FEC_codeword_error_bin_*i*, where *i*=1 to 15, are optional 32-bit counters. While align_status is true, for each codeword received with exactly *i* correctable 10-bit symbols, FEC_codeword_error_bin_*i* is incremented. For example, if a codeword has exactly five errored 10-bit symbols, then fec_codeword_error_bin_5 is incremented. These variables are mapped to registers defined in 45.2.3.48b (3.340 to 3.369).

172.4 Loopback

Loopback is identical to that specified in 119.4.

172.5 Delay constraints

The maximum delay contributed by the 800GBASE-R PCS (sum of transmit and receive delays at one end of the link) shall be no more than 640 000 BT (1250 pause_quanta or 800 ns). A description of overall system delay constraints and the definitions for bit times and pause_quanta can be found in 169.4 and its references.

172.6 Auto-Negotiation

The following requirements apply to a PCS used with an 800GBASE-CR8 or 800GBASE-KR8 PMD where support for the Auto-Negotiation process defined in Clause 73 is mandatory. The PCS shall support the AN_LINK.indication(link_status) primitive (see 73.9). The parameter link_status shall take the value FAIL when PCS_status=false and the value OK when PCS_status=true. The primitive shall be generated when the value of link_status changes.

172.7 Protocol implementation conformance statement (PICS) proforma for Clause 172, Physical Coding Sublayer (PCS), type 800GBASE-R[13]

172.7.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Clause 172, Physical Coding Sublayer (PCS), type 800GBASE-R, shall complete the following protocol implementation conformance statement (PICS) proforma.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

172.7.2 Identification

172.7.2.1 Implementation identification

Supplier[1]	
Contact point for inquiries about the PICS[1]	
Implementation Name(s) and Version(s)[1,3]	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)[2]	
NOTE 1—Required for all implementations. NOTE 2—May be completed as appropriate in meeting the requirements for the identification. NOTE 3—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

172.7.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3df-2024, Clause 172, Physical Coding Sublayer (PCS), type 800GBASE-R
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3df-2024.)	

Date of Statement	

[13] *Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

172.7.3 Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
MII	800GMII logical interface is supported	172.1.5.1		O	Yes [ ] No [ ]
*MD	MDIO	172.3.1		O	Yes [ ] No [ ]
*FDD	Support for FEC degrade detection	172.2.5.3		O	Yes [ ] No [ ]

172.7.4 PICS proforma tables for Physical Coding Sublayer (PCS), type 800GBASE-R

172.7.4.1 Transmit function

Item	Feature	Subclause	Value/Comment	Status	Support
*SE	Uses stateless encoder	172.2.4.1.2		O	Yes [ ] No [ ]
TF1	Transmit 64B/66B encoder uses state diagram in Figure 119–14	172.2.4.1.1		!SE:M	Yes [ ] N/A [ ]
TF2	Transmit 64B/66B encoder uses stateless rules in Table 172–1	172.2.4.1.2		SE:M	Yes [ ] N/A [ ]
TF3	64B/66B to 256B/257B transcoder	172.2.4.4		M	Yes [ ]
TF4	Scrambler	172.2.4.5		M	Yes [ ]
TF5	Pad value	172.2.4.6		M	Yes [ ]
TF6	Alignment marker insertion	172.2.4.6		M	Yes [ ]
TF7	FEC degrade signaling	172.2.4.6		M	Yes [ ]
TF8	Pre-FEC distribution	172.2.4.7		M	Yes [ ]
TF9	Reed-Solomon encoder	172.2.4.8		M	Yes [ ]
TF10	Symbol distribution	172.2.4.9		M	Yes [ ]
TF11	Transmission bit ordering	172.2.4.10		M	Yes [ ]
TF12	Scrambled idle transmit test-pattern generator	172.2.4.11		M	Yes [ ]

172.7.4.2 Receive function

Item	Feature	Subclause	Value/Comment	Status	Support
*BI	Bypass indication supported	172.2.5.3		O	Yes [ ] No [ ]
*SD	Uses stateless decoder	172.2.5.9.2		O	Yes [ ] No [ ]
RF1	Alignment marker lock	172.2.5.1		M	Yes [ ]
RF2	PCS lane number is captured to an MDIO register	172.2.6.3		MD:M	Yes [ ] N/A [ ]
RF3	Deskew	172.2.5.1		M	Yes [ ]
RF4	Lane reorder and de-interleave	172.2.5.2		M	Yes [ ]
RF5	Reed-Solomon decoder corrects any combination of up to t=15 symbol errors in a codeword	172.2.5.3		M	Yes [ ]
RF6	Reed-Solomon decoder is capable of indicating when a codeword was not corrected	172.2.5.3		M	Yes [ ]
RF7	Error monitoring and assertion of hi_ser, while error indication is bypassed	172.2.5.3		BI:M	Yes [ ] N/A [ ]
RF8	Detect FEC degrade	172.2.5.3		FDD:M	Yes [ ] N/A [ ]
RF9	Alignment marker removal	172.2.5.5		M	Yes [ ]
RF10	Descrambler	172.2.5.6		M	Yes [ ]
RF11	256B/257B to 64B/66B transcoder	172.2.5.7		M	Yes [ ]
RF12	Receive 64B/66B decoder uses state diagram in Figure 119–15	172.2.5.9.1		!SD:M	Yes [ ] N/A [ ]
RF13	Receive 64B/66B decoder uses stateless rules in Table 172–4	172.2.5.9.2		SD:M	Yes [ ] N/A [ ]

172.7.4.3 64B/66B coding rules

Item	Feature	Subclause	Value/Comment	Status	Support
C1	Encoder (and ENCODE function) implements the code as specified	172.2.3, 172.2.6.2.3		M	Yes [ ]
C2	Decoder (and DECODE function) implements the code as specified	172.2.3, 172.2.6.2.3		M	Yes [ ]
C3	Only valid block types are transmitted	172.2.3		M	Yes [ ]
C4	Invalid block types are treated as an error	172.2.3		M	Yes [ ]
C5	Only valid control characters are transmitted	172.2.3		M	Yes [ ]
C6	Invalid control characters are treated as an error	172.2.3		M	Yes [ ]
C7	Idles do not interrupt data	172.2.3		M	Yes [ ]
C8	IDLE control code insertion and deletion	172.2.3	Insertion or deletion in groups of 8 /I/s	M	Yes [ ]
C9	Sequence ordered set deletion	172.2.3	Only one whole ordered set of two consecutive sequence ordered sets may be deleted	M	Yes [ ]

172.7.4.4 Management

Item	Feature	Subclause	Value/Comment	Status	Support
M1	Equivalent access to PCS management objects is provided	172.3		!MD:O	Yes [ ] No [ ] N/A [ ]
M2	Mapping of MDIO control bits and MDIO status bits	172.3.1		MD:M	Yes [ ] N/A [ ]

172.7.4.5 Loopback

Item	Feature	Subclause	Value/Comment	Status	Support
L1	Supports loopback	172.4		M	Yes [ ]
L2	When in loopback, transmits what it receives from the 800GMII	172.4		M	Yes [ ]
L3	When in loopback, ignore all data presented by the PMA	172.4		M	Yes [ ]

172.7.4.6 Delay constraints

Item	Feature	Subclause	Value/Comment	Status	Support
TIM1	PCS delay constraint	172.5		M	Yes [ ]

172.7.4.7 Auto-Negotiation

Item	Feature	Subclause	Value/Comment	Status	Support
*AN	Support for use with an 800GBASE-CR8 or 800GBASE-KR8 PMD	172.6	AN technology dependent interface described in Clause 73	O	Yes [ ] No [ ]
AN1	AN_LINK.indication primitive	172.6	Support of the AN_LINK.indication(link_status) primitive	AN:M	Yes [ ] N/A [ ]
AN2	link_status parameter	172.6	Takes the value OK or FAIL	AN:M	Yes [ ] N/A [ ]
AN3	Generation of AN_LINK.indication primitive	172.6	Generated when the value of link_status changes	AN:M	Yes [ ] N/A [ ]

173. Physical Medium Attachment (PMA) sublayer, type 800GBASE-R

173.1 Overview

173.1.1 Scope

This clause specifies the Physical Medium Attachment (PMA) sublayer for the family of 800 Gb/s Physical Layer implementations, known as 800GBASE-R. The PMA allows the PCS (specified in Clause 172) to connect in a media-independent way with a range of physical media, or for the DTE 800GXS to connect to the PHY 800GXS (specified in Clause 171). The 800GBASE-R PMA(s) can support any of the 800 Gb/s PMDs in Table 169–1.

Three types of the 800GBASE-R PMA are defined: 32:8 PMA, 8:32 PMA, and 8:8 PMA.

173.1.2 Position of the PMA in the 800GBASE-R sublayers

Figure 173–1 shows the relationship of the PMA sublayer with other sublayers to the ISO Open System Interconnection (OSI) reference model.

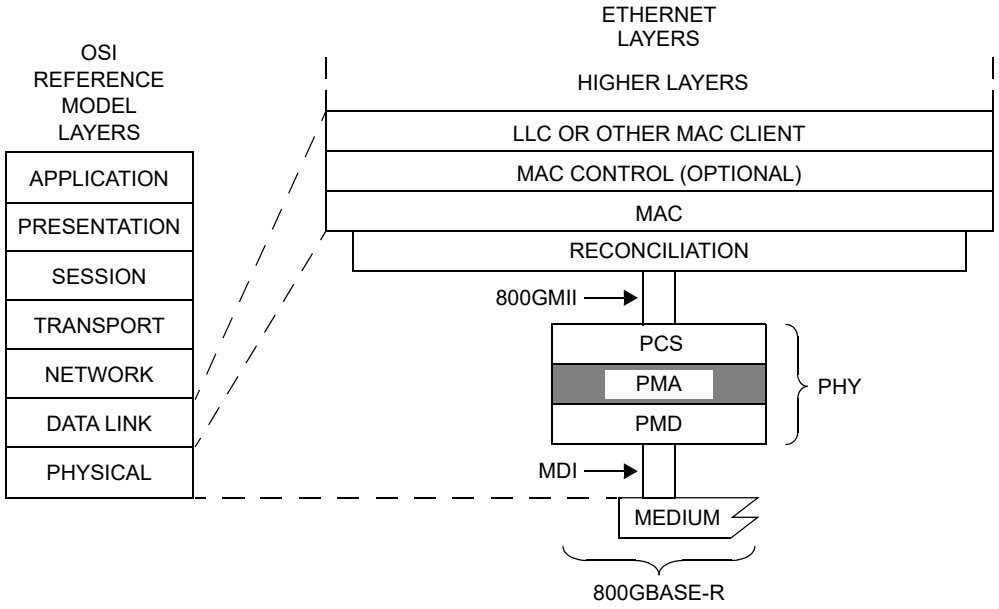


Figure 173–1—800GBASE-R PMA relationship to the ISO/IEC Open Systems Interconnection (OSI) reference model and IEEE 802.3 Ethernet model

173.1.3 Summary of functions

The following is a summary of the principal functions implemented (when required) by the PMA in both the transmit and receive directions:

- Adapt the PCS lane (PCSL) formatted signal to the appropriate number of abstract or physical lanes
- Provide per input-lane clock and data recovery
- Provide bit-level multiplexing
- Provide clock generation
- Provide signal drivers
- Optionally provide local loopback to/from the PMA service interface
- Optionally provide remote loopback to/from the PMD service interface
- Optionally provide test-pattern generation and detection
- Tolerate Skew Variation
- Perform PAM4 encoding and decoding
- Provide signal status information

173.1.4 PMA sublayer positioning

An implementation may use one or more PMA sublayers to adapt the number and rate of the PCSLs to the number and rate of the PMD lanes. The number of PMA sublayers required depends on the partitioning of functionality for a particular implementation.

Figure 173–2 shows examples of the PMA sublayer positioning for implementations with an 800GMII Extender and for implementations without an 800GMII Extender. Additional examples are illustrated in Annex 173A.

A 32:8 PMA sublayer is required in the following cases:

- In an 800GBASE-R PHY between the 800GBASE-R PCS and an 800GAUI-8
- In an 800GBASE-R PHY between the 800GBASE-R PCS and an 8-lane 800GBASE-R PMD
- In an 800GMII Extender between the DTE 800GXS and an 800GAUI-8

An 8:32 PMA sublayer is required in the following case:

- In an 800GMII Extender between an 800GAUI-8 and the PHY 800GXS

An 8:8 PMA sublayer is required in the following cases:

- In an 800GBASE-R PHY between an 800GAUI-8 and an 8-lane 800GBASE-R PMD
- In an 800GBASE-R PHY between two 800GAUI-8
- In an 800GMII Extender between two 800GAUI-8

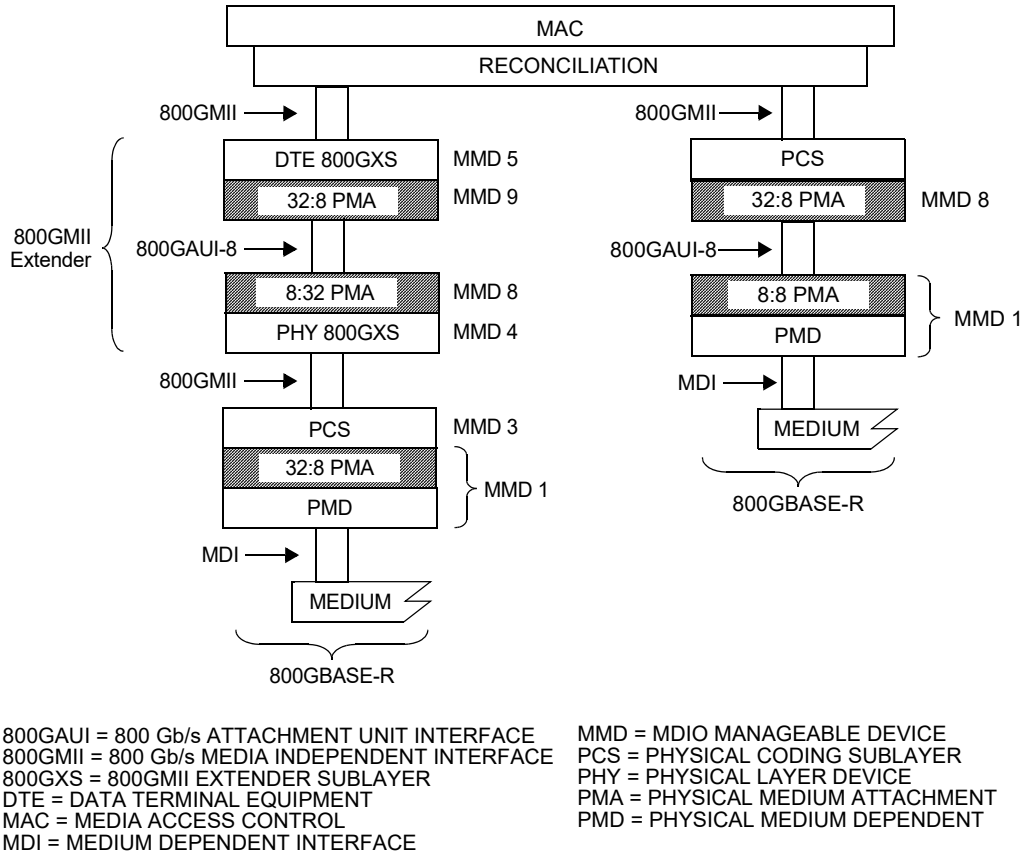


Figure 173–2—Examples of 800GBASE-R PMA layering

Management Data Input/Output (MDIO) Manageable Device (MMD) addresses 1, 8, 9, 10, and 11 are available for addressing multiple instances of PMA sublayers (see Table 45–1 for MMD device addresses). If the PMA sublayer that is closest to the PMD is packaged with the PMD, it shares MMD 1 with the PMD. More addressable instances of PMA sublayers, each one separated from lower addressable instances by chip-to-chip interfaces, may be implemented and addressed allocating MMD addresses to PMAs in increasing numerical order going from the PMD toward the MAC. A maximum of four PMA sublayers are addressable as MDIO MMDs.

173.2 PMA service interface

The PMA service interface for 800GBASE-R is an instance of the inter-sublayer service interface defined in 169.3.1. The PMA service interface primitives (when applicable) are summarized as follows:

PMA:IS_UNITDATA_*i*.request(tx_symbol)
PMA:IS_UNITDATA_*i*.indication(rx_symbol)
PMA:IS_SIGNAL.indication(SIGNAL_OK)

For a 32:8 PMA (see Figure 173–3), the primitives are defined for $i = 0$ to 31. In the transmit direction, the PMA receives 32 parallel bit streams from either the 800GBASE-R PCS or the DTE 800GXS, each at a nominal signaling rate of 26.5625 Gb/s. In the receive direction, the PMA sends 32 parallel bit streams to the PMA client, each at a nominal signaling rate of 26.5625 Gb/s. The 32:8 PMA also provides signal status

information to the PMA client using the PMA:IS_SIGNAL.indication service interface primitive (see 173.5.8.1).

For the 8:32 and 8:8 PMAs (see Figure 173–4 and Figure 173–5), the service interface primitives are defined for *i* = 0 to 7. In the transmit direction, the PMA receives 8 parallel PAM4 symbol streams from the PMA client, each operating at a nominal signaling rate of 53.125 GBd. In the receive direction, the PMA sends 8 parallel PAM4 symbol streams to the PMA client, each at a nominal signaling rate of 53.125 GBd.

The 8:32 and 8:8 PMAs may optionally provide signal status information to the PMA client as described in 173.5.8.2 and 173.5.8.3.

173.3 Service interface below PMA

There are several different sublayers that may appear below a PMA, including the PMD, an Extender Sublayer, or another PMA. The variable *inst* represents whichever sublayer appears below the PMA (e.g., another PMA or a PMD).

The sublayer below the PMA utilizes the inter-sublayer service interface defined in 169.3.1. The service interface primitives provided to the PMA (when applicable) are summarized as follows:

inst:IS_UNITDATA_*i*.request(tx_symbol)
inst:IS_UNITDATA_*i*.indication(rx_symbol)
inst:IS_SIGNAL.indication(SIGNAL_OK)
PHY_XS:IS_SIGNAL.request(SIGNAL_OK)

For the 32:8 PMA and 8:8 PMA (see Figure 173–3 and Figure 173–5), the *inst*:IS_UNITDATA_*i* primitives are defined for *i* = 0 to 7 and *inst* is either PMA or PMD. In the transmit direction, the PMA sends 8 parallel PAM4 symbol streams to the sublayer below the PMA, each operating at a nominal signaling rate of 53.125 GBd. In the receive direction, the PMA receives 8 parallel PAM4 symbol streams from the sublayer below the PMA, each at a nominal signaling rate of 53.125 GBd. Electrical and timing specifications of the service interface below the PMA are defined if the interface is physically instantiated (e.g., 800GAUI-8), otherwise the service interface is specified only abstractly. If the sublayer below the PMA is a PMD, then the PMA also receives a PMD:IS_SIGNAL.indication primitive indicating the status of the signal from the PMD (see 173.5.8.1 and 173.5.8.3).

For the 8:8 PMA, if the sublayer below the PMA is another PMA, the 8:8 PMA may optionally provide signal status information to the sublayer below as described in 173.5.8.3.

For the 8:32 PMA (see Figure 173–4) the *inst*:IS_UNITDATA_*i* primitives are defined for *i* = 0 to 31 and *inst* is always PHY_XS. In the transmit direction, the PMA sends 32 parallel bit streams to the PHY 800GXS, each at a nominal signaling rate of 26.5625 Gb/s. In the receive direction, the PMA receives 32 parallel bit streams from the PHY 800GXS, each at a nominal signaling rate of 26.5625 Gb/s. The PMA provides signal status information to the PHY 800GXS using the PHY_XS:IS_SIGNAL.request service interface primitive (see 173.5.8.2). The PMA also receives a PHY_XS:IS_SIGNAL.indication primitive indicating the status of the signal from the PHY 800GXS (see 173.5.8.2).

173.4 PMA types

Three different types of the 800GBASE-R PMA are defined in this clause: 32:8 PMA, 8:32 PMA, and 8:8 PMA. These PMA types are all based upon the 400GBASE-R PMA defined in Clause 120.

173.4.1 32:8 PMA

Figure 173–3 provides the functional block diagram of the 32:8 PMA. The features of a 32:8 PMA include the following:

— 32 input and output lanes for the PMA service interface

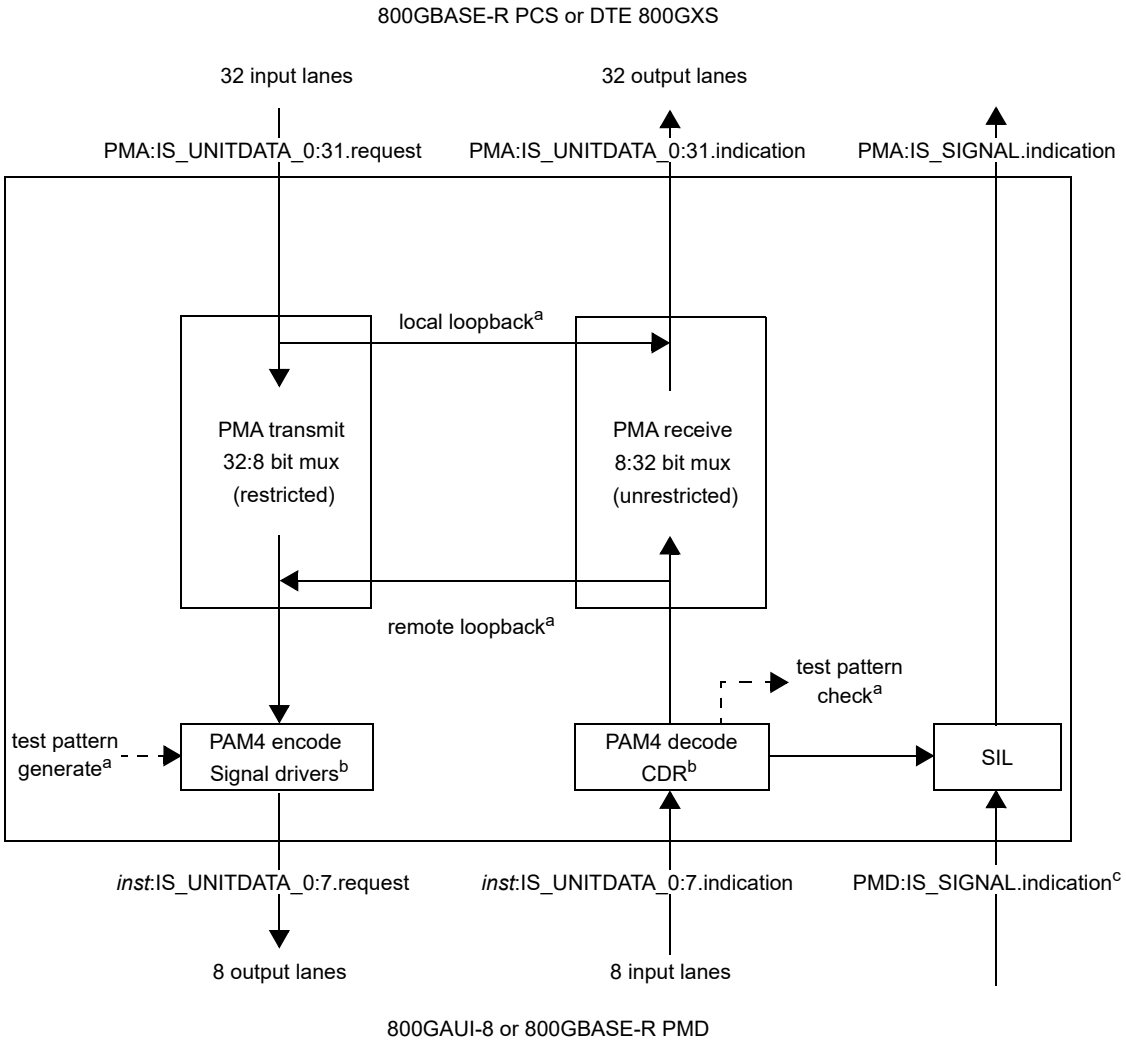
— 8 input and output lanes for the service interface below the PMA

— In the transmit direction, restricted bit-level multiplexing between the 32 input lanes and the 8 output lanes (see 173.5.2.1)

— In the receive direction, unrestricted bit-level multiplexing between the 8 input lanes and the 32 output lanes (see 173.5.2.1)

— The interface above the PMA (32 lanes) connects with either an 800GBASE-R PCS or a DTE 800GXS

— The interface below the PMA (8 lanes) connects with either a PMD or a physically instantiated interface (800GAUI-8)



inst: PMA[b] or PMD[c]
SIL: signal indication logic

[a] Optional.
[b] If an 800GAUI-8 is below the PMA.
[c] If the sublayer below the PMA is a PMD.

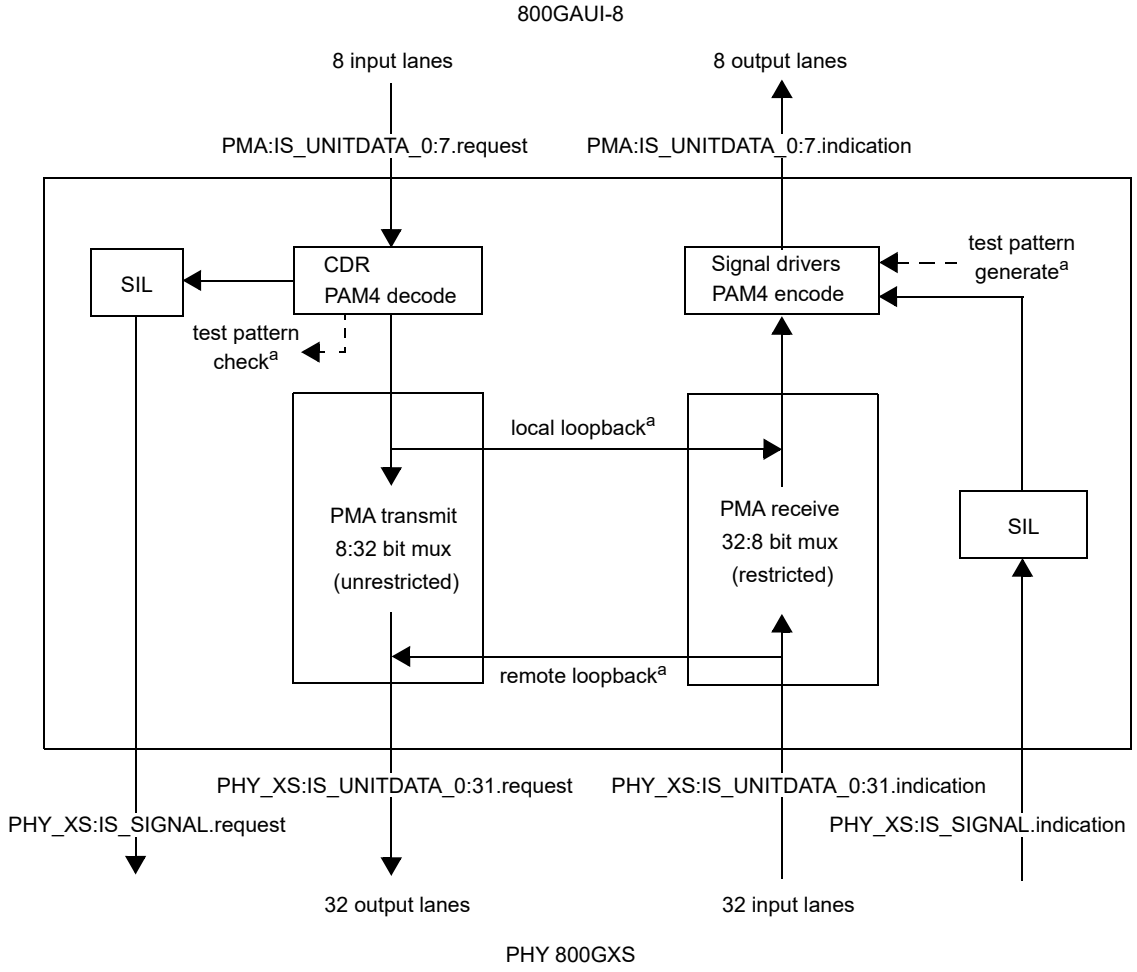
Figure 173–3—32:8 PMA functional block diagram

173.4.2 8:32 PMA

Figure 173–4 provides the functional block diagram of the 8:32 PMA. The features of an 8:32 PMA include the following:

— 8 input and output lanes for the PMA service interface
— 32 input and output lanes for the service interface below the PMA
— In the transmit direction, unrestricted bit-level multiplexing between the 8 input lanes and the 32 output lanes (see 173.5.2.2)
— In the receive direction, restricted bit-level multiplexing between the 32 input lanes and the 8 output lanes (see 173.5.2.2)

— The interface above the PMA (8 lanes) connects with a physically instantiated interface (800GAUI-8)
— The interface below the PMA (32 lanes) connects with a PHY 800GXS



SIL: signal indication logic

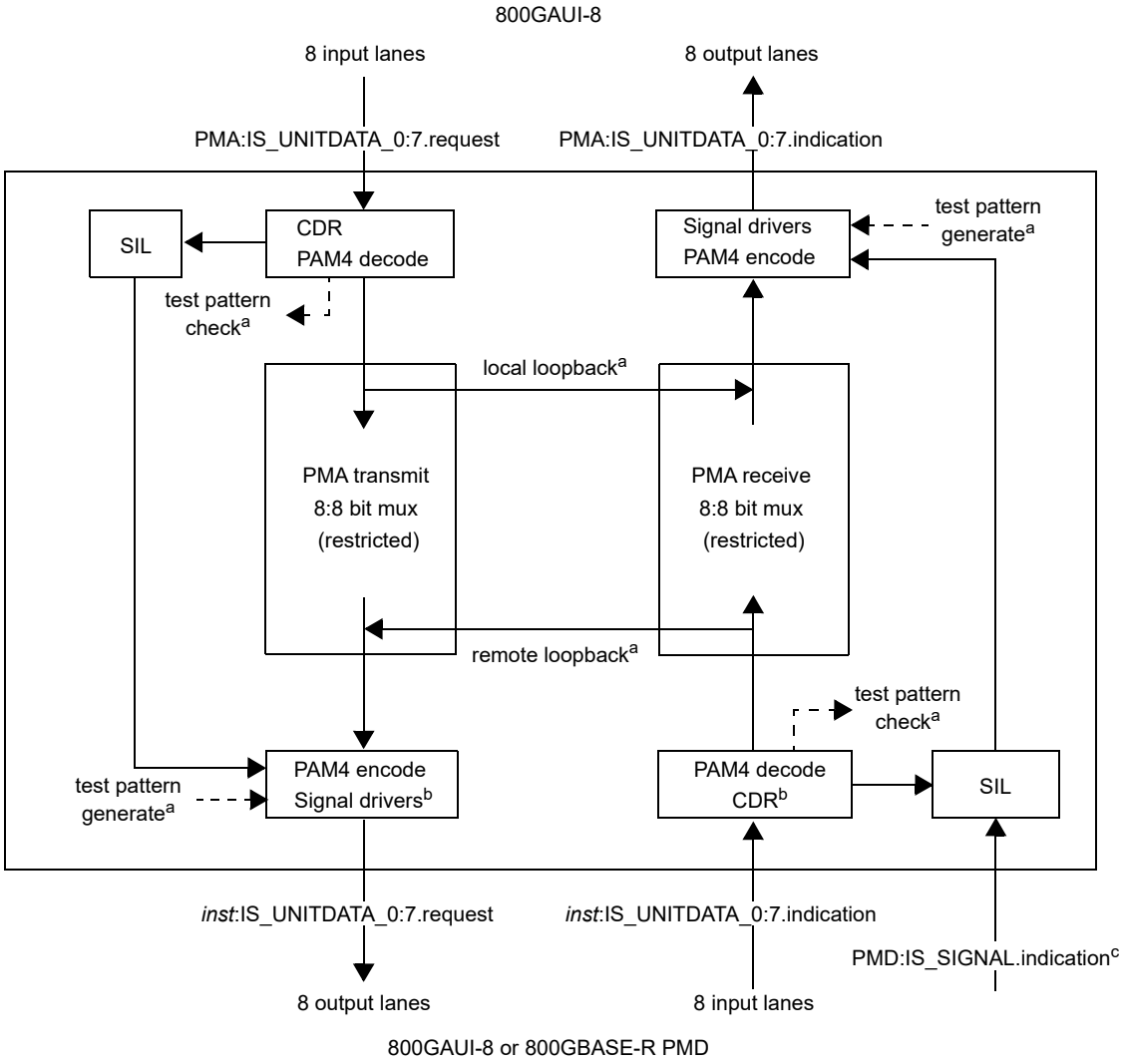
[a] Optional.

Figure 173–4—8:32 PMA functional block diagram

173.4.3 8:8 PMA

Figure 173–5 provides the functional block diagram of the 8:8 PMA. The features of an 8:8 PMA include the following:

— 8 input and output lanes for the PMA service interface
— 8 input and output lanes for the service interface below the PMA
— In the transmit and receive directions, restricted bit-level multiplexing between the 8 input lanes and the 8 output lanes (see 173.5.2.3)
— The interface above the PMA connects with a physically instantiated interface (800GAUI-8)
— The interface below the PMA connects with either a PMD or a physically instantiated interface (800GAUI-8)



inst: PMA[b] or PMD[c]
SIL: signal indication logic

[a] Optional.
[b] If an 800GAUI-8 is below the PMA.
[c] If the sublayer below the PMA is a PMD.

Figure 173–5—8:8 PMA functional block diagram

173.5 Functions within the PMA

173.5.1 Per input-lane clock and data recovery (CDR)

If the interface above the PMA is physically instantiated as 800GAUI-8, the PMA shall meet the electrical and timing specifications in Annex 120F or Annex 120G, as appropriate, at the PMA service interface.

If the interface below the PMA is physically instantiated as 800GAUI-8, the PMA shall meet the electrical and timing specifications in Annex 120F or Annex 120G, as appropriate, at the service interface below the PMA.

173.5.2 Bit-level multiplexing

The PMA provides bit-level multiplexing of PCSLs in both the transmit and receive directions.

The bit-level multiplexing functions are different amongst the 32:8, 8:32, and 8:8 PMAs.

173.5.2.1 32:8 PMA bit-level multiplexing

The 32:8 PMA provides bit-level multiplexing in both the transmit and receive directions.

In the transmit direction, the bit-level multiplexing function is performed among the PCSLs received from the PMA client via the PMA:IS_UNITDATA_*i*.request primitives (for PMA client lanes $i = 0$ to 31) with the result sent to the service interface below the PMA using the *inst*:IS_UNITDATA_*i*.request primitives (for service interface lanes $i = 0$ to 7), as shown in Figure 173–3. This is a restricted bit-level multiplexing function that is identical to the bit-level multiplexing function specified in 120.5.2 with the number of PCSLs *z* equal to 32 and with the following exception:

— The bit-level multiplexing function has an additional constraint that each of the 8 output lanes carries two PCSLs from PMA client lanes $i = 0$ to 15 and two PCSLs from PMA client lanes $i = 16$ to 31. Bits from the four PCSLs are multiplexed in temporal order with one bit from each of two lanes from PMA client lanes $i = 0$ to 15 followed by one bit from each of two lanes from PMA client lanes $i = 16$ to 31.

In the receive direction, the bit-level multiplexing function is performed among the PCSLs received from the service interface below the PMA using the *inst*:IS_UNITDATA_*i*.request primitives (for service interface lanes $i = 0$ to 7) with the result sent to the PMA client via the PMA:IS_UNITDATA_*i*.request primitives (for PMA client lanes $i = 0$ to 31), as shown in Figure 173–3. This is an unrestricted bit-level multiplexing function that is identical to that specified in 120.5.2 with the number of PCSLs *z* equal to 32.

173.5.2.2 8:32 PMA bit-level multiplexing

The 8:32 PMA provides bit-level multiplexing in both the transmit and receive directions.

In the transmit direction, the bit-level multiplexing function is performed among the PCSLs received from the PMA client via the PMA:IS_UNITDATA_*i*.request primitives (for PMA client lanes $i = 0$ to 7) with the result sent to the service interface below the PMA using the *inst*:IS_UNITDATA_*i*.request primitives (for service interface lanes $i = 0$ to 31), as shown in Figure 173–4. This is an unrestricted bit-level multiplexing function that is identical to the bit-level multiplexing function specified in 120.5.2 with the number of PCSLs *z* equal to 32.

In the receive direction, the bit-level multiplexing function is performed among the PCSLs received from the service interface below the PMA using the PHY_XS:IS_UNITDATA_*i*.indication primitives (for service interface lanes $i = 0$ to 31) with the result sent to the PMA client via the PMA:IS_UNITDATA_*i*.indication primitives (for PMA client lanes $i = 0$ to 7), as shown in Figure 173–4. This is a restricted bit-level multiplexing function that is identical to that specified in 120.5.2 with the number of PCSLs *z* equal to 32 and with the following exception:

— The bit-level multiplexing function has an additional constraint that each of the 8 output lanes carries two PCSLs from PHY 800GXS service interface lanes $i = 0$ to 15 and two PCSLs from PHY 800GXS service interface lanes $i = 16$ to 31. Bits from the four PCSLs are multiplexed in temporal order with one bit from each of two lanes from PHY 800GXS service interface lanes $i = 0$ to 15 followed by one bit from each of two lanes from PHY 800GXS service interface lanes $i = 16$ to 31.

173.5.2.3 8:8 PMA bit-level multiplexing

The 8:8 PMA provides bit-level multiplexing in both the transmit and receive directions.

In the transmit direction, the bit-level multiplexing function is performed among the PCSLs received from the PMA client via the PMA:IS_UNITDATA_*i*.request primitives (for PMA client lanes *i* = 0 to 7) with the result sent to the service interface below the PMA using the *inst*:IS_UNITDATA_*i*.request primitives (for service interface lanes *i* = 0 to 7), as shown in Figure 173–5.

In the receive direction, the bit-level multiplexing function is performed among the PCSLs received from the service interface below the PMA using the *inst*:IS_UNITDATA_*i*.request primitives (for service interface lanes *i* = 0 to 7) with the result sent to the PMA client via the PMA:IS_UNITDATA_*i*.request primitives (for PMA client lanes *i* = 0 to 7), as shown in Figure 173–5.

In both the transmit and receive directions, this is a restricted bit-level multiplexing function that is identical to the bit-level multiplexing function specified in 120.5.2 with the number of PCSLs *z* equal to 32 and with the following exception:

— The 4 PCSLs received on an input lane shall be mapped to an output lane such that the Gray mapped PAM4 symbol sequence on the output lane is either identical to the Gray mapped PAM4 symbol sequence on the input lane, or is the result of reversing the order of each pair of bits {A, B} to {B, A} in the Gray mapping function (see 173.5.7.1).

173.5.3 Skew and Skew Variation

The Skew (relative delay) between the PCSLs is kept within limits so that the information on the lanes can be reassembled by the PCS.

Any PMA that combines PCSLs from different input lanes onto the same output lane is required to tolerate Skew Variation between the input lanes without changing the PCSL positions on the output. Skew and Skew Variation at physically instantiated interfaces are specified at Skew points SP1 and SP2 in the transmit direction and SP5 and SP6 in the receive direction. Skew, Skew Variation, and Skew points are defined in 169.5. Skew points are illustrated in Figure 169–4 and Figure 169–5.

173.5.3.1 Skew generation toward SP1

In an implementation with one or more physically instantiated 800GAUI-8 interfaces, at the output of the PMA that sends data in the transmit direction toward the 800GAUI-8 that is closest to the PMD (SP1 in Figure 169–4 and Figure 169–5) there shall be no more than 16 ns of Skew between PCSLs and no more than 200 ps of Skew Variation between output lanes towards the 800GAUI-8.

173.5.3.2 Skew tolerance at SP1

In an implementation with one or more physically instantiated 800GAUI-8 interfaces, the PMA that receives data in the transmit direction from the 800GAUI-8 (SP1 in Figure 169–4 and Figure 169–5) shall tolerate the maximum amount of Skew Variation allowed at SP1 (200 ps) between input lanes while maintaining the bit ordering and position of each PCSL on each PMA lane in the transmit direction (toward the PMD).

173.5.3.3 Skew generation toward SP2

If the PMD service interface is physically instantiated so that the Skew at SP2 can be measured, at the output of the PMA adjacent to the PMD service interface there shall be no more than 25 ns of Skew between PCLs, and no more than 400 ps of Skew Variation between output lanes toward the PMD service interface (SP2 in Figure 169–4 and Figure 169–5). In an implementation with one or more physically instantiated 800GAUI-8

interfaces, the Skew measured at the input to the PMA adjacent to the PMD service interface (SP1 in Figure 169–4 and Figure 169–5) is limited to no more than 16 ns of Skew and no more than 200 ps of Skew Variation.

173.5.3.4 Skew tolerance at SP5

If the PMD service interface is physically instantiated so that the Skew at SP5 can be measured, the PMA adjacent to the PMD service interface (SP5) shall tolerate the maximum amount of Skew Variation allowed at SP5 (3.6 ns) between output lanes from the PMD service interface while maintaining the bit ordering and position of each PCSL on each PMA lane in the receive direction (toward the MAC).

173.5.3.5 Skew generation at SP6

In an implementation with one or more physically instantiated 800GAUI-8 interfaces, at SP6 (the receive direction of the 800GAUI-8 closest to the PCS), at the output of the PMA or group of PMAs between the PMD and the 800GAUI-8 closest to the PCS there shall be no more than 145 ns of Skew between PCSLs, and no more than 3.8 ns of Skew Variation between output lanes toward the 800GAUI-8 in the receive direction.

If there is a physically instantiated PMD service interface that allows the Skew to be measured, the Skew measured at SP5 is limited to no more than 127 ns of Skew and no more than 3.6 ns of Skew Variation. If there is no physically instantiated PMD service interface, the Skew measured at SP4 is limited to no more than 116 ns of Skew, and no more than 3.4 ns of Skew Variation.

173.5.3.6 Skew tolerance at SP6

In an implementation with one or more physically instantiated 800GAUI-8 interfaces, the PMA between the 800GAUI-8 closest to the PCS and the PCS shall tolerate the maximum amount of Skew Variation allowed at SP6 (3.8 ns) between input lanes while maintaining the bit order and position of PCSLs on lanes sent in the receive direction towards the MAC.

173.5.4 Delay constraints

There may be up to four instances of the 800GBASE-R PMA within a Physical Layer, which is composed of an 800GBASE-R PHY and, optionally, an 800GMII Extender. The maximum delay (sum of transmit and receive delays) contributed by each instance of an 800GBASE-R PMA shall meet the values specified in Table 173–1. A description of overall system delay constraints and the definitions for bit times and pause_quanta can be found in 169.4 and its references.

NOTE—Although the PMD service interface definition implies otherwise, the delay allocation for the majority of the clock and data recovery function is allocated to the PMA adjacent to the PMD, rather than to the PMD.

Table 173–1—Delay constraints

Sublayer	Maximum (bit time)	Maximum (pause_quanta)	Maximum (ns)
800GBASE-R 8:32 PMA or 32:8 PMA	36 864	72	46.08
800GBASE-R 8:8 PMA	73 728	144	92.16

173.5.5 Clocking architecture

A PMA with *m* input lanes and *n* output lanes shall clock the output lanes such that the bit rate of the output lanes is *m*/*n* times the bit rate of the input lanes. For input or output lanes encoded as PAM4 the symbol rate is half of the bit rate. This applies in both the transmit and receive directions of transmission.

NOTE—There is no requirement that all output lanes use a common clock. For example in an 8:8 PMA, each output lane may use a separate clock derived from its corresponding input.

Details of the clocking architecture are outside the scope of this standard.

173.5.6 Signal drivers

For a case where there is a physically instantiated interface, the PMA provides electrical signal drivers. The electrical and jitter/timing specifications for these interfaces appear in:

— Annex 120F, which specifies the 800GAUI-8 interface for chip-to-chip applications
— Annex 120G, which specifies the 800GAUI-8 interface for chip-to-module applications

173.5.7 PAM4 Encoding

173.5.7.1 Gray mapping

The Gray mapping for PAM4 encoded lanes is identical to that specified in 120.5.7.1.

173.5.7.2 Precoding

The precoding specifications in this subclause apply to the input and output lanes of a PMA that are connected to the service interface of an 800GBASE-CR8 or 800GBASE-KR8 PMD, or are part of an 800GAUI-8 C2C link.

The PMA shall provide 1/(1+D) mod 4 precoding capability on each transmit lane and may optionally provide 1/(1+D) mod 4 decoding capability on each receive lane. Precoding is implemented as specified in 135.5.7.2.

The precoder is enabled independently on the Tx output, Rx input, Rx output, and Tx input on each lane. Precoding is enabled and disabled using variables precoder_tx_out_enable_*i*, precoder_rx_in_enable_*i*, precoder_rx_out_enable_*i*, and precoder_tx_in_enable_*i* (where *i* is in the range 0 to 7). If a Clause 45 MDIO is implemented, these variables are accessible through registers as shown in Table 173–2.

If the PMA is connected to the service interface of an 800GBASE-CR8 or 800GBASE-KR8 PMD and training is enabled by the management variable mr_training_enable (see 136.7), then precoder_tx_out_enable_*i* and precoder_rx_in_enable_*i* shall be set as determined by the PMD control function in the LINK_READY state on lane *i* (see 136.8.11.7.5 and Figure 136–7). The method by which the PMD control function affects these variables is implementation dependent.

If the PMA is connected to the service interface of an 800GBASE-CR8 or 800GBASE-KR8 PMD and training is disabled by the management variable mr_training_enable, or if the PMA is part of an 800GAUI-8 link, then precoder_tx_out_enable_*i*, precoder_rx_in_enable_*i*, precoder_rx_out_enable_*i*, and precoder_tx_in_enable_*i* are set as required by the implementation. The method described in 135F.3.2.1 may be used for 800GAUI-8 C2C.

173.5.8 Signal status

173.5.8.1 32:8 PMA signal status

In the receive direction, the 32:8 PMA provides signal status information to the PMA client (800GBASE-R PCS or DTE 800GXS) using the PMA:IS_SIGNAL.indication(SIGNAL_OK) service interface primitive (see 173.2 and Figure 173–3):

The SIGNAL_OK parameter is set to OK when all of the following conditions are met:

- Data is being received on all 8 input lanes (*inst*:IS_UNITDATA_0:7.indication)
- The received data is being sent on all 32 output lanes (PMA:IS_UNITDATA_0:31.indication)
- The SIGNAL_OK parameter of the PMD:IS_SIGNAL.indication primitive is set to OK, if there is a PMD immediately below the PMA

Otherwise SIGNAL OK is set to FAIL.

173.5.8.2 8:32 PMA signal status

In the transmit direction, the 8:32 PMA provides signal status information to the PHY 800GXS using the PHY_XS:IS_SIGNAL.request(SIGNAL_OK) service interface primitive (see 173.3 and Figure 173–4). The SIGNAL_OK parameter is set to OK when data is being received on all 8 input lanes (PMA:IS_UNITDATA_0:7.request) and the received data is being sent on all 32 output lanes (PHY_XS:IS_UNITDATA_0:31.request). Otherwise SIGNAL OK is set to FAIL.

In the receive direction, the 8:32 PMA optionally provides signal status information to the client PMA by disabling (squelching) one or more output lanes (PMA:IS_UNITDATA_0:7.indication) when the PHY_XS:IS_SIGNAL.indication SIGNAL_OK parameter (see 173.3 and Figure 173–4) is FAIL.

173.5.8.3 8:8 PMA signal status

In the transmit direction, the 8:8 PMA optionally provides signal status to the sublayer below (see 173.3 and Figure 173–5) by disabling (squelching) one or more output lanes (*inst*:IS_UNITDATA_0:7.request) when data is not being received on all 8 input lanes (PMA:IS_UNITDATA_0:7.request).

In the receive direction, the 8:8 PMA optionally provides signal status to the client PMA by disabling (squelching) one or more output lanes (PMA:IS_UNITDATA_0:7.indication) when the PMD:IS_SIGNAL.indication SIGNAL_OK parameter (see 173.3 and Figure 173–5) is FAIL or when data is not being received on all 8 input lanes (*inst*:IS_UNITDATA_0:7.indication).

173.5.9 PMA local loopback mode (optional)

The PMA local loopback mode functions identically to that specified in 120.5.9.

173.5.10 PMA remote loopback mode (optional)

The PMA remote loopback mode functions identically to that specified in 120.5.10.

173.5.11 PMA test patterns (optional)

Where the lanes of the PMA are connected to a physically instantiated interface 800GAUI-8 or the PMD service interface, the PMA may optionally generate and detect test patterns. These test patterns are used to test adjacent layer interfaces for an individual PMA sublayer or to perform testing between a physically instantiated interface of a PMA and external testing equipment.

The test pattern functionality is identical to that defined for PAM4 encoded signals in 120.5.11.2.

173.6 PMA MDIO function mapping

The optional MDIO capability described in Clause 45 describes several variables that provide control and status information for and about the PMA. Since a given implementation may employ more than one PMA sublayer, the PMA control and status information is organized into multiple addressable instances, one for each possible PMA sublayer. See 45.2.1 and 173.1.4 for the allocation of MMD addresses to PMA sublayers. Control and status registers for MMD 8, 9, and 10 use the Extended PMA control and status registers at identical locations to those for MMD 1. Annex 173A provides additional examples of mapping MMD addresses to sublayers.

Mapping of MDIO control variables to PMA control variables is shown in Table 173–2. Mapping of MDIO status variables to PMA status variables is shown in Table 173–3. Mapping of MDIO counter to PMA counters is shown in Table 173–4. These tables provide the register and bit numbers for the PMA addressed as MMD 1. For implementations with multiple PMA sublayers, additional PMA sublayers use the corresponding register and bit numbers in MMDs 8, 9, 10, and 11 as necessary.

Table 173–2—MDIO/PMA control variable mapping

MDIO variable	PMA/PMD register name	Register/ bit number	PMA control variable
PMA remote loopback	PMA/PMD control 1	1.0.1	Remote_loopback_enable
PMA local loopback	PMA/PMD control 1	1.0.0	Local_loopback_enable
Lane 0 to 7 Tx output precoder enable	PMA precoder control Tx output	1.600.0 to 1.600.7	precoder_tx_out_enable_<0:7>
Lane 0 to 7 Rx input precoder enable	PMA precoder control Rx input	1.601.0 to 1.601.7	precoder_rx_in_enable_<0:7>
Lane 0 to 7 Rx output precoder enable	PMA precoder control Rx output	1.602.0 to 1.602.7	precoder_rx_out_enable_<0:7>
Lane 0 to 7 Tx input precoder enable	PMA precoder control Tx input	1.603.0 to 1.603.7	precoder_tx_in_enable_<0:7>
PRBS31Q pattern enable	PRBS pattern testing control	1.1501.13	PRBS31Q_pattern_enable
SSPRQ pattern enable	PRBS pattern testing control	1.1501.14	SSPRQ_pattern_enable
Tx generator enable	PRBS pattern testing control	1.1501.3	PRBS_Tx_gen_enable
Tx checker enable	PRBS pattern testing control	1.1501.2	PRBS_Tx_check_enable
Rx generator enable	PRBS pattern testing control	1.1501.1	PRBS_Rx_gen_enable
Rx checker enable	PRBS pattern testing control	1.1501.0	PRBS_Rx_check_enable
Lane 0 to 7 SW enable	Square wave testing control	1.1510.0 to 1.1510.7	Square_wave_enable_<0:7>
Lane 0 to 7 PRBS9Q enable	PRBS9Q testing control	1.1511.0 to 1.1511.7	PRBS9Q_enable_<0:7>
Lane 0 to 7 PRBS13Q enable	PRBS13Q testing control	1.1512.0 to 1.1512.7	PRBS13Q_enable_<0:7>

Table 173–3—MDIO/PMA status variable mapping

MDIO status variable	PMA/PMD register name	Register/bit number	PMA status variable
PMA remote loopback ability	800G PMA/PMD extended ability register	1.73.15	800G_Remote_loopback_ability
PMA local loopback ability	PMA/PMD status 2 register	1.8.0	Local_loopback_ability
Tx input precoder request flag	PMA precoder request flag	1.604.1	precoder_rx_in_request_flag
Rx input precoder request flag	PMA precoder request flag	1.604.0	precoder_rx_in_request_flag
Lane 0 to 7 Rx input precoder request status	PMA precoder request Rx input status	1.605.0 to 1.605.7	precoder_rx_in_request_<0:7>
Lane 0 to 7 Tx input precoder request status	PMA precoder request Tx input status	1.606.0 to 1.606.7	precoder_tx_in_request_<0:7>
Square wave test ability	Test-pattern ability register	1.1500.12	Square_wave_ability
PRBS13Q Tx generator ability	Test-pattern ability register	1.1500.11	PRBS13Q_gen_Tx_ability
PRBS13Q Rx generator ability	Test-pattern ability register	1.1500.10	PRBS13Q_gen_Rx_ability
PRBS31Q Tx generator ability	Test-pattern ability register	1.1500.9	PRBS31Q_gen_Tx_ability
PRBS31Q Rx generator ability	Test-pattern ability register	1.1500.7	PRBS31Q_gen_rx_ability
PRBS31Q Tx checker ability	Test-pattern ability register	1.1500.8	PRBS31Q_Tx_checker_ability
PRBS31Q Rx checker ability	Test-pattern ability register	1.1500.6	PRBS31Q_Rx_checker_ability
SSPRQ Tx generator ability	Test-pattern ability register	1.1500.13	SSPRQ_gen_Tx_ability
PRBS9Q Rx generator ability	Test-pattern ability register	1.1500.14	PRBS9Q_gen_Rx_ability
PRBS9Q Tx generator ability	Test-pattern ability register	1.1500.15	PRBS9Q_gen_Tx_ability

Table 173–4—MDIO/PMA counters mapping

MDIO variable	PMA/PMD register name	Register/bit number	PMA status variable
Error counter Tx, lane 0 to 7	PRBS Tx pattern testing error counter, lane 0 to lane 7	1.1600 to 1.1607	Ln<0:7>_PRBS_Tx_test_err_ counter
Error counter Rx, lane 0 to 7	PRBS Rx pattern testing error counter, lane 0 to lane 7	1.1700 to 1.1707	Ln<0:7>_PRBS_Rx_test_err_ counter

173.7 Protocol implementation conformance statement (PICS) proforma for Clause 173, Physical Medium Attachment (PMA) sublayer, type 800GBASE-R[14]

173.7.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Clause 173, Physical Medium Attachment (PMA) sublayer, type 800GBASE-R shall complete the following protocol implementation conformance statement (PICS) proforma.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

173.7.2 Identification

173.7.2.1 Implementation identification

Supplier[1]	
Contact point for inquiries about the PICS[1]	
Implementation Name(s) and Version(s)[1,3]	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)[2]	
NOTE 1—Required for all implementations. NOTE 2—May be completed as appropriate in meeting the requirements for the identification. NOTE 3—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

173.7.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3df-2024, Clause 173, Physical Medium Attachment (PMA) sublayer, type 800GBASE-R
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3df-2024.)	

Date of Statement	

[14] *Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

173.7.3 Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
*P328	32:8 PMA	173.4		O/1	Yes [ ] No [ ]
*P832	8:32 PMA	173.4		O/1	Yes [ ] No [ ]
*P88	8:8 PMA	173.4		O/1	Yes [ ] No [ ]
*C2CA	AUI C2C above PMA (toward MAC)	173.2		P832+P88:O/2	Yes [ ] No [ ] N/A [ ]
*C2MA	AUI C2M above PMA (toward MAC)	173.2		P832+P88:O/2	Yes [ ] No [ ] N/A [ ]
*C2CB	AUI C2C below PMA (toward PMD)	173.3		P328+P88:O/3	Yes [ ] No [ ] N/A [ ]
*C2MB	AUI C2M below PMA (toward PMD)	173.3		P328+P88:O/3	Yes [ ] No [ ] N/A [ ]
*PMDE	800GBASE-CR8 or 800GBASE-KR8 PMD below PMA	173.3		P328+P88:O/3	Yes [ ] No [ ] N/A [ ]
*PMDO	800GBASE-VR8, 800GBASE-SR8, 800GBASE-DR8, or 800GBASE-DR8-2 PMD below PMA	173.3		P328+P88:O/3	Yes [ ] No [ ] N/A [ ]
*PSID	PMA connected to a physically instantiated PMD service interface	173.3		O	Yes [ ] No [ ]
*MD	MDIO	173.6	Registers and interface supported	O	Yes [ ] No [ ]

173.7.4 Skew generation and tolerance

Item	Feature	Subclause	Value/Comment	Status	Support
S1	Skew generation toward SP1 in transmit direction	173.5.3.1	≤ 16 ns	C2CB+C2MB:M	Yes [ ] N/A [ ]
S2	Skew Variation generation toward SP1 in transmit direction	173.5.3.1	≤ 200 ps	C2CB+C2MB:M	Yes [ ] N/A [ ]
S3	Skew Variation tolerance at SP1	173.5.3.2	Minimum 200 ps	C2CA+C2MA:M	Yes [ ] N/A [ ]
S4	Skew generation toward SP2 in transmit direction	173.5.3.3	≤ 25 ns	PSID:M	Yes [ ] N/A [ ]

Item	Feature	Subclause	Value/Comment	Status	Support
S5	Skew Variation generation toward SP2 in transmit direction	173.5.3.3	≤ 400 ps	PSID:M	Yes [ ] N/A [ ]
S6	Skew Variation tolerance at SP5	173.5.3.4	Minimum 3.6 ns	PSID:M	Yes [ ] N/A [ ]
S7	Skew generation toward SP6 in receive direction	173.5.3.5	≤ 145 ns	C2CA+C2MA:M	Yes [ ] N/A [ ]
S8	Skew Variation generation toward SP6 in receive direction	173.5.3.5	≤ 3.8 ns	C2CA+C2MA:M	Yes [ ] N/A [ ]
S9	Skew Variation tolerance at SP6	173.5.3.6	Minimum 3.8 ns	C2CB+C2MB:M	Yes [ ] N/A [ ]

173.7.5 Delay constraints

Item	Feature	Subclause	Value/Comment	Status	Support
D1	PMA delay constraint	173.5.4		M	Yes [ ]

173.7.6 Test patterns

Item	Feature	Subclause	Value/Comment	Status	Support
T1	Send PRBS13Q Tx	120.5.11.2.1		C2CB+C2MB+ PMDO+PMDE:O	Yes [ ] No [ ] N/A [ ]
T2	Send PRBS13Q Rx	120.5.11.2.1		C2CA+C2MA:O	Yes [ ] No [ ] N/A [ ]
T3	Send PRBS31Q Tx	120.5.11.2.2		C2CB+C2MB+ PMDO+PMDE:O	Yes [ ] No [ ] N/A [ ]
T4	Send PRBS31Q Rx	120.5.11.2.2		C2CA+C2MA:O	Yes [ ] No [ ] N/A [ ]
T5	Check PRBS31Q Tx	120.5.11.2.2		C2CA+C2MA:O	Yes [ ] No [ ] N/A [ ]
T6	Check PRBS31Q Rx	120.5.11.2.2		C2CB+C2MB+ PMDO+PMDE:O	Yes [ ] No [ ] N/A [ ]
T7	Send SSPRQ Tx	120.5.11.2.3		PMDO:O	Yes [ ] No [ ] N/A [ ]
T8	Send square wave (quaternary) Tx	120.5.11.2.4		PMDO:O	Yes [ ] No [ ] N/A [ ]

173.7.7 Loopback

Item	Feature	Subclause	Value/Comment	Status	Support
LB1	PMA local loopback	173.5.9	Meets the requirements of 173.5.9	O	Yes [ ] No [ ]
LB2	PMA remote loopback	173.5.10	Meets the requirements of 173.5.10	O	Yes [ ] No [ ]

173.7.8 Precoding

Item	Feature	Subclause	Value/Comment	Status	Support
P1	PMA transmit output supports precoding	173.5.7.2		PMDE+ C2CB:M	Yes [ ] N/A [ ]
P2	PMA receive output supports precoding	173.5.7.2		C2CA:M	Yes [ ] N/A [ ]
P3	PMA transmit input supports precoding	173.5.7.2		C2CA:O	Yes [ ] No [ ] N/A [ ]
P4	PMA receive input supports precoding	173.5.7.2		PMDE+ C2CB:O	Yes [ ] No [ ] N/A [ ]

173.7.9 Signal status

Item	Feature	Subclause	Value/Comment	Status	Support
SS1	Signal status for 32:8 PMA	173.5.8.1		P328:O	Yes [ ] No [ ] N/A [ ]
SS2	Signal status for 8:32 PMA	173.5.8.2		P832:O	Yes [ ] No [ ] N/A [ ]
SS3	Signal status for 8:8 PMA	173.5.8.3		P88:O	Yes [ ] No [ ] N/A [ ]
SS4	Signal status by disabling (squelching) output lanes for 8:32 PMA	173.5.8.2		P832:O	Yes [ ] No [ ] N/A [ ]
SS5	Signal status by disabling (squelching) output lanes for 8:8 PMA	173.5.8.3		P88:O	Yes [ ] No [ ] N/A [ ]

173.7.10 Electrical

Item	Feature	Subclause	Value/Comment	Status	Support
E1	Interface above meets 800GAUI-8 C2C requirements in Annex 120F	173.5.1, 173.5.6		C2CA:M	Yes [ ] N/A [ ]
E2	Interface above meets 800GAUI-8 C2M requirements in Annex 120G	173.5.1, 173.5.6		C2MA:M	Yes [ ] N/A [ ]
E3	Interface below meets 800GAUI-8 C2C requirements in Annex 120F	173.5.1, 173.5.6		C2CB:M	Yes [ ] N/A [ ]
E4	Interface below meets 800GAUI-8 C2M requirements in Annex 120G	173.5.1, 173.5.6		C2MB:M	Yes [ ] N/A [ ]

NOTE—This annex is numbered in correspondence to its associated clause; i.e., Annex 4A corresponds to Clause 4.

Annex 4A

(normative)

Simplified full duplex media access control

4A.4 Specific implementations

4A.4.2 MAC parameters

Change Note 4 in 4A.4.2 as follows:

NOTE 4—For 40 Gb/s, 50 Gb/s, 100 Gb/s, 200 Gb/s, ~~and~~ 400 Gb/s, and 800 Gb/s operation, the received interpacket gap (the spacing between two packets, from the last bit of the FCS field of the first packet to the first bit of the Preamble of the second packet) can have a minimum value of 8 BT (bit times), as measured at the XLGMII, 50GMII, CGMII, 200GMII, ~~or~~ 400GMII, or 800GMII receive signals at the DTE due to clock tolerance and lane alignment requirements.

Annex 31B

(normative)

MAC Control PAUSE operation

31B.3 Detailed specification of PAUSE operation

31B.3.7 Timing considerations for PAUSE operation

Insert the following paragraph into 31B.3.7 after the "At operating speeds of 400 Gb/s, …") paragraph:

At operating speeds of 800 Gb/s, a station shall not begin to transmit a (new) frame more than 1810 pause_quanta after the reception of a valid PAUSE frame that contains a non-zero value of pause_time, as measured at the MDI.

Insert a new paragraph at the end of 31B.3.7 as follows:

800 Gb/s – max_overrun = 115840 + frame_length.

31B.4 Protocol implementation conformance statement (PICS) proforma for MAC Control PAUSE operation[15]

31B.4.3 Major capabilities/options

Insert a new row at the end of the table in 31B.4.3 as follows (unchanged rows not shown):

Item	Feature	Subclause	Value/Comment	Status	Support
…					
*MIIp	At operating speeds of 800 Gb/s.	31B.3.7	N/A	O	Yes [ ] No [ ]

31B.4.6 PAUSE command MAC timing considerations

Insert a new row at the end of the table in 31B.4.6 as follows (unchanged rows not shown):

Item	Feature	Subclause	Value/Comment	Status	Support
…					
TIM17	Measurement point for station at 800 Gb/s	31B.3.7	Delay at MDI ≤ 1810 pause_quanta[a]	MIIp: M	Yes [ ] N/A [ ]

[a] Delay from receiving valid PAUSE command, with nonzero value for pause_time, to cessation of transmission.

[15] *Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this annex so that it can be used for its intended purpose and may further publish the completed PICS.

Annex 90A was added by IEEE Std 802.3cx-2023.

Annex 90A

(informative)

Timestamping accuracy considerations

90A.3 Considerations for use of different data delay measurement points

Change Table 90A–1 as follows:

Table 90A–1—Magnitude of potential timestamp accuracy impairments

Ethernet rate	Magnitude of potential timestamp accuracy impairments per transmit or receive port (ns)			
	Mismatched data delay measurement point [a]	Idle insertion / removal [b,c]	Alignment marker/ codeword marker insertion / removal [c]	PCS lane distribution / merging
10M	800	400	N/A	N/A
100M	80	40		N/A
1G	8	16[d], 8[e]		0 [e], N/A[d]
2.5G	3.2	12.8		N/A [g]
5G	1.6	6.4		N/A [g]
10G	0.8	3.2		N/A [d, f, g], 0 [e]
25G	0.32	1.28	10.24	N/A
40G	0.2	1.6	6.4	4.8
50G	0.16	1.28	5.12	3.84
100G	0.08	0.64	12.8	12.16
200G	0.04	0.32	2.56	N/A [g]
400G	0.02	0.16	2.56	N/A [g]
800G	0.01	0.08	2.56	N/A [g]

[a] The value shown only accounts for the time between the two data delay measurement point options when they are adjacent. See 90A.3 for other factors that can affect some of these values.
[b] The value shown corresponds to the effect of a single Idle insertion/removal.
[c] The path data delay of a packet can be affected when its data delay measurement point occurs after an alignment marker, codeword marker, or Idle insertion/removal event.
[d] For 1000BASE-X or 10GBASE-R
[e] For 1000BASE-T or 10GBASE-X
[f] For 10GBASE-T
[g] For PHYs including FEC, the lane distribution/merging operation belongs only to the forward error correction (FEC) function. The FEC lane distribution/merging operation is not subject to potential timestamp accuracy impairments because its path data delay determination was already clearly defined, and not subject to implementation flexibilities.

Annex 93A

(normative)

Specification methods for electrical channels

93A.1 Channel Operating Margin

Insert three new rows at the end of Table 93A–2 (as amended by IEEE Std 802.3ck-2022) as follows (unchanged rows not shown):

Table 93A–2—Physical Layer specifications that employ COM

Physical Layer	Parameter values
…	
800GBASE-CR8 (Clause 162)	Table 162–20
800GBASE-KR8 (Clause 163)	Table 163–11
800GAUI-8 C2C (Annex 120F)	Table 120F–8

Change the title of Annex 120F (added by IEEE Std 802.3ck-2022) as follows:

Annex 120F

(normative)

Chip-to-chip Attachment Unit Interfaces 100GAUI-1 C2C, 200GAUI-2 C2C, 400GAUI-4 C2C, and 800GAUI-8 C2C ~~100 Gb/s one-lane Attachment Unit Interface (100GAUI-1 C2C), 200 Gb/s two-lane Attachment Unit Interface (200GAUI-2 C2C), 400 Gb/s four-lane Attachment Unit Interface (400GAUI-4 C2C)~~

120F.1 Overview

Change the text in 120F.1 as follows:

This annex defines the functional and electrical characteristics for the optional chip-to-chip 100 Gb/s one-lane Attachment Unit Interface (100GAUI-1 C2C), 200 Gb/s two-lane Attachment Unit Interface (200GAUI-2 C2C), ~~and~~ 400 Gb/s four-lane Attachment Unit Interface (400GAUI-4 C2C), and 800 Gb/s eight-lane Attachment Unit Interface (800GAUI-8 C2C). ~~The 100GAUI-1 C2C, 200GAUI-2 C2C, and 400GAUI-4 C2C~~ These interfaces provide electrical characteristics and associated compliance points, which can optionally be used when designing systems with electrical interconnect of approximately 25 cm in length.

100GAUI-1 C2C, 200GAUI-2 C2C, ~~and~~ 400GAUI-4 C2C, and 800GAUI-8 C2C are physical instantiations of the PMA service interface between the FEC (for 100GBASE-P PHYs) or PCS (for 200GBASE-R, ~~and~~ 400GBASE-R, and 800GBASE-R PHYs) and the PMD, as described in 135.1.4, ~~and~~ 120.1.4, and 173.1.4. Figure 120F–1 shows example relationships of the ~~100GAUI-1 C2C, 200GAUI-2 C2C, and 400GAUI-4~~ C2C interfaces to the ISO/IEC Open System Interconnection (OSI) reference model.

The sublayers, including PCS and FEC (for 100GBASE-P PHYs), for each PHY that can optionally include a 100GAUI-1 C2C, 200GAUI-2 C2C, ~~or~~ 400GAUI-4 C2C, or 800GAUI-8 C2C are summarized in the tables in 80.1.5, ~~and~~ 116.1.4, and 169.1.4, and are specified in the corresponding PMD clause. The positioning of the ~~100GAUI-1 C2C, 200GAUI-2 C2C, or 400GAUI-4~~ C2C interfaces relative to other sublayers is shown in 135.1, ~~and~~ 120.1, and 173.1, with further examples in Annex 135A, ~~and~~ Annex 120A, and Annex 173A.

The ~~100GAUI-1, 200GAUI-2, or 400GAUI-4~~ C2C bidirectional link is described in terms of a C2C transmitter, a C2C channel, and a C2C receiver. Figure 120F–2 depicts a typical C2C application. The C2C components at both ends of the link have connected ground references.

The C2C interface is composed of independent data paths in each direction. Each 100GAUI-1 C2C, 200GAUI-2 C2C, ~~or~~ 400GAUI-4 C2C, or 800GAUI C2C data path contains one, two, ~~or~~ four, or eight, respectively, differential lanes, which are AC-coupled.

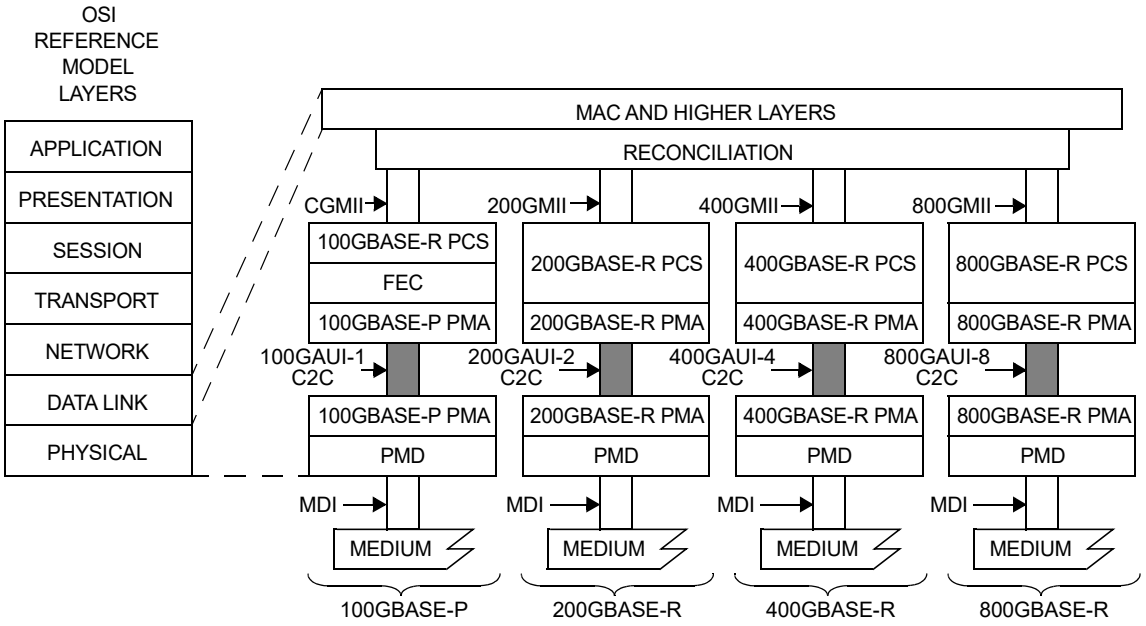
The ~~100GAUI-1, 200GAUI-2, and 400GAUI-4~~ C2C transmitter and receiver use PAM4 signaling. The highest differential level corresponds to the tx_symbol or rx_symbol value three, and the lowest differential level corresponds to the tx_symbol or rx_symbol value zero. The nominal signaling rate for each lane is 53.125 GBd.

The ~~100GAUI-1, 200GAUI-2, and 400GAUI-4~~ C2C channel is specified in 120F.4.

The ~~100GAUI-1, 200GAUI-2, and 400GAUI-4~~ C2C transmitter on each end of the link is adjusted to an appropriate setting, which may be based on channel knowledge. If implemented, the transmitter equalization feedback mechanism described in 120F.3.2.6 may be used to identify an appropriate setting of the link partner transmitter. The adaptive or adjustable receiver performs the remainder of the equalization.

The ~~100GAUI-1, 200GAUI-2, and 400GAUI-4~~ C2C transmitter supports 1/(1+D) mod 4 precoding, as specified in 135.5.7.2, ~~and~~ 120.5.7.2, and 173.5.7.2, that may be enabled or disabled as required. The ~~100GAUI-1, 200GAUI-2, and 400GAUI-4~~ C2C receiver may support 1/(1+D) mod 4 precoding, as specified in 135.5.7.2, ~~and~~ 120.5.7.2, and 173.5.7.2. Precoding may be enabled and disabled using the precoder request mechanism specified in 135F.3.2.1.

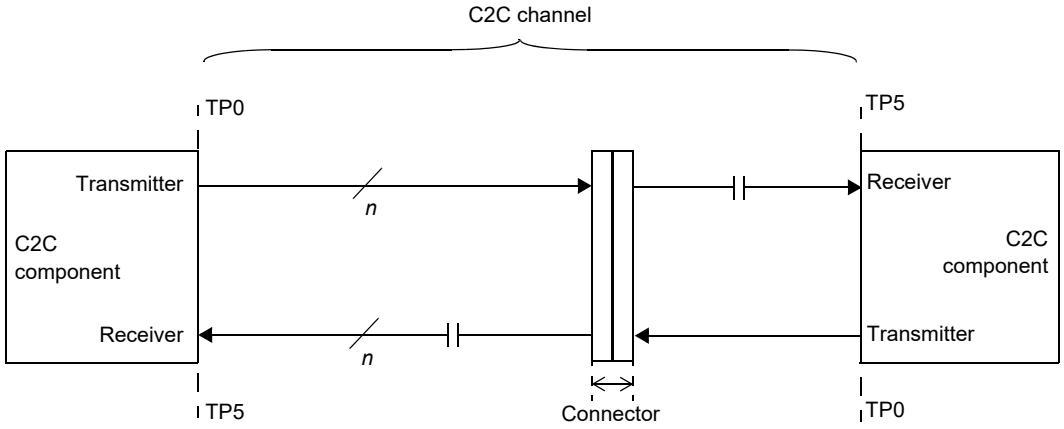
Replace Figure 120F–1 with the following figure:



100GAUI-1 = 100 Gb/s ONE-LANE ATTACHMENT UNIT INTERFACE
200GAUI-2 = 200 Gb/s TWO-LANE ATTACHMENT UNIT INTERFACE
200GMII = 200 Gb/s MEDIA INDEPENDENT INTERFACE
400GAUI-4 = 400 Gb/s FOUR-LANE ATTACHMENT UNIT INTERFACE
400GMII = 400 Gb/s MEDIA INDEPENDENT INTERFACE
800GMII = 800 Gb/s MEDIA INDEPENDENT INTERFACE
800GAUI-8 = 800 Gb/s EIGHT-LANE ATTACHMENT UNIT INTERFACE
CGMII = 100 Gb/s MEDIA INDEPENDENT INTERFACE
FEC = FORWARD ERROR CORRECTION
MAC = MEDIA ACCESS CONTROL
MDI = MEDIUM DEPENDENT INTERFACE
PCS = PHYSICAL CODING SUBLAYER
PMA = PHYSICAL MEDIUM ATTACHMENT
PMD = PHYSICAL MEDIUM DEPENDENT

Figure 120F–1—Example 100GAUI-1, 200GAUI-2, 400GAUI-4, and 800GAUI-8 C2C relationship to the ISO/IEC Open System Interconnection (OSI) reference model and the IEEE 802.3 Ethernet model

Change the title and NOTE in Figure 120F–2 as follows:



NOTE—The number of lanes *n* is equal to 1 for 100GAUI-1, 2 for 200GAUI-2, ~~and~~ 4 for 400GAUI-4, and 8 for 800GAUI-8.

Figure 120F–2—Typical ~~100GAUI-1, 200GAUI-2, and 400GAUI-4~~ C2C application

120F.2 Compliance points

Change 120F.2 as follows:

The electrical characteristics for the ~~100GAUI-1 C2C, 200GAUI-2 C2C, and 400GAUI-4~~ C2C interfaces are defined at test points as described in 163.9.2.1 and 163.9.3.2.

120F.3 Electrical characteristics

120F.3.1 Transmitter electrical characteristics

Change the first paragraph of 120F.3 as follows:

A ~~100GAUI-1 C2C, 200GAUI-2 C2C, and 400GAUI-4~~ C2C transmitter shall meet the specifications given in Table 120F–1.

Change footnote a of Table 120F–1 as follows (unchanged rows and footnotes not shown):

Table 120F–1—Transmitter electrical characteristics at TP0v

Parameter	Reference	Value	Units
Signaling rate, each lane (range)		53.125 ± 50 ppm[a]	GBd
…			

[a] For 100GAUI-1, 200GAUI-2, or 400GAUI-4 C2C with a PMA in the same package as the PCS sublayer or for any 800GAUI-8 C2C. In other cases, the signaling rate is derived from the signaling rate presented to the input lanes (see Figure 135–3 and Figure 120–3) by the adjacent PMD, PMA, or FEC sublayers.

120F.3.2 Receiver characteristics

Change Table 120F–4 as follows (most unchanged rows not shown):

Table 120F–4—Receiver characteristics at TP5v

Parameter	Reference	Value	Units
Signaling rate, each lane (range) 100GAUI-1, 200GAUI-2, 400GAUI-4 800GAUI-8	120F.3.2.1	 53.125 ± 100 ppm 53.125 ± 50 ppm	 GBd GBd
…			
Jitter tolerance	120F.3.2.5	Table 162–17	—
NOTE—For 100GAUI-1, 200GAUI-2, or 400GAUI-4, although the C2C transmitter is specified with a signaling rate range of ±50 ppm when in the same package as the PCS, the signaling rate range may be ±100 ppm when derived from an intermediate interface (e.g., 100GAUI-4).			

120F.3.2.1 Receiver signaling rate

Change 120F.3.2.1 as follows:

The receiver shall comply with the requirements of 120F.3.2.4 and 120F.3.2.5 for any signaling rate in the range specified in Table 120F–4 ~~53.125 GBd ± 100 ppm~~.

120F.4 Channel characteristics

Change the first paragraph of 120F.4 as follows:

Table 120F–7 provides a summary of the channel characteristics ~~for 100GAUI-1 C2C, 200GAUI-2 C2C, and 400GAUI-4 C2C interfaces,~~ and references to the subclauses addressing each parameter.

Change the title of 120F.5 as follows:

120F.5 Protocol implementation conformance statement (PICS) proforma for Annex 120F, Chip-to-chip Attachment Unit Interfaces 100GAUI-1 C2C, 200GAUI-2 C2C, 400GAUI-4 C2C, and 800GAUI-8 C2C ~~100 Gb/s one-lane Attachment Unit Interface (100GAUI-1 C2C), 200 Gb/s two-lane Attachment Unit Interface (200GAUI-2 C2C), and 400 Gb/s four-lane Attachment Unit Interface (400GAUI-4 C2C)~~[16]

120F.5.1 Introduction

Change the first paragraph of 120F.5.1 as follows:

The supplier of a protocol implementation that is claimed to conform to Annex 120F, Chip-to-chip Attachment Unit Interfaces 100GAUI-1 C2C, 200GAUI-2 C2C, 400GAUI-4 C2C, and 800GAUI-8 C2C ~~100 Gb/s one-lane Attachment Unit Interface (100GAUI-1 C2C), 200 Gb/s two-lane Attachment Unit Interface (200GAUI-2 C2C), and 400 Gb/s four-lane Attachment Unit Interface (400GAUI-4 C2C)~~, shall complete the following protocol implementation conformance statement (PICS) proforma.

120F.5.2 Identification

120F.5.2.2 Protocol summary

Change the table in 120F.5.2.2 as follows:

Identification of protocol standard	IEEE Std 802.3df-2024, Annex 120F, Chip-to-chip Attachment Unit Interfaces 100GAUI-1 C2C, 200GAUI-2 C2C, 400GAUI-4 C2C, and 800GAUI-8 C2C ~~100 Gb/s one-lane Attachment Unit Interface (100GAUI-1 C2C), 200 Gb/s two-lane Attachment Unit Interface (200GAUI-2 C2C), and 400 Gb/s four-lane Attachment Unit Interface (400GAUI-4 C2C)~~
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3df-2024.)	

Date of Statement	

[16] *Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this ~~subclause~~ annex so that it can be used for its intended purpose and may further publish the completed PICS.

120F.5.3 Major capabilities/options

Change item NOL in the table in 120F.5.3 as follows (unchanged rows not shown):

Item	Feature	Subclause	Value/Comment	Status	Support
NOL	Number of differential AC-coupled lanes	120F.1	One independent data path in each direction for 100GAUI-1 C2C, two independent data paths in each direction for 200GAUI-2 C2C, ~~and~~ four independent data paths in each direction for 400GAUI-4 C2C, or eight independent data paths in each direction for 800GAUI-8 C2C	M	Yes [ ]
…					

Change the title of 120F.5.4 as follows:

120F.5.4 PICS proforma tables for Chip-to-chip Attachment Unit Interfaces 100GAUI-1 C2C, 200GAUI-2 C2C, 400GAUI-4 C2C, and 800GAUI-8 C2C ~~100 Gb/s one-lane Attachment Unit Interface (100GAUI-1 C2C), 200 Gb/s two-lane Attachment Unit Interface (200GAUI-2 C2C), and 400 Gb/s four-lane Attachment Unit Interface (400GAUI-4 C2C)~~

Change the title of Annex 120G (added by IEEE Std 802.3ck-2022) as follows:

Annex 120G

(normative)

Chip-to-module Attachment Unit Interfaces 100GAUI-1 C2M, 200GAUI-2 C2M, 400GAUI-4 C2M, and 800GAUI-8 C2M

~~100 Gb/s one-lane Attachment Unit Interface (100GAUI-1 C2M), 200 Gb/s two-lane Attachment Unit Interface (200GAUI-2 C2M), and 400 Gb/s four-lane Attachment Unit Interface (400GAUI-4 C2M)~~

120G.1 Overview

Change the text in 120G.1 as follows:

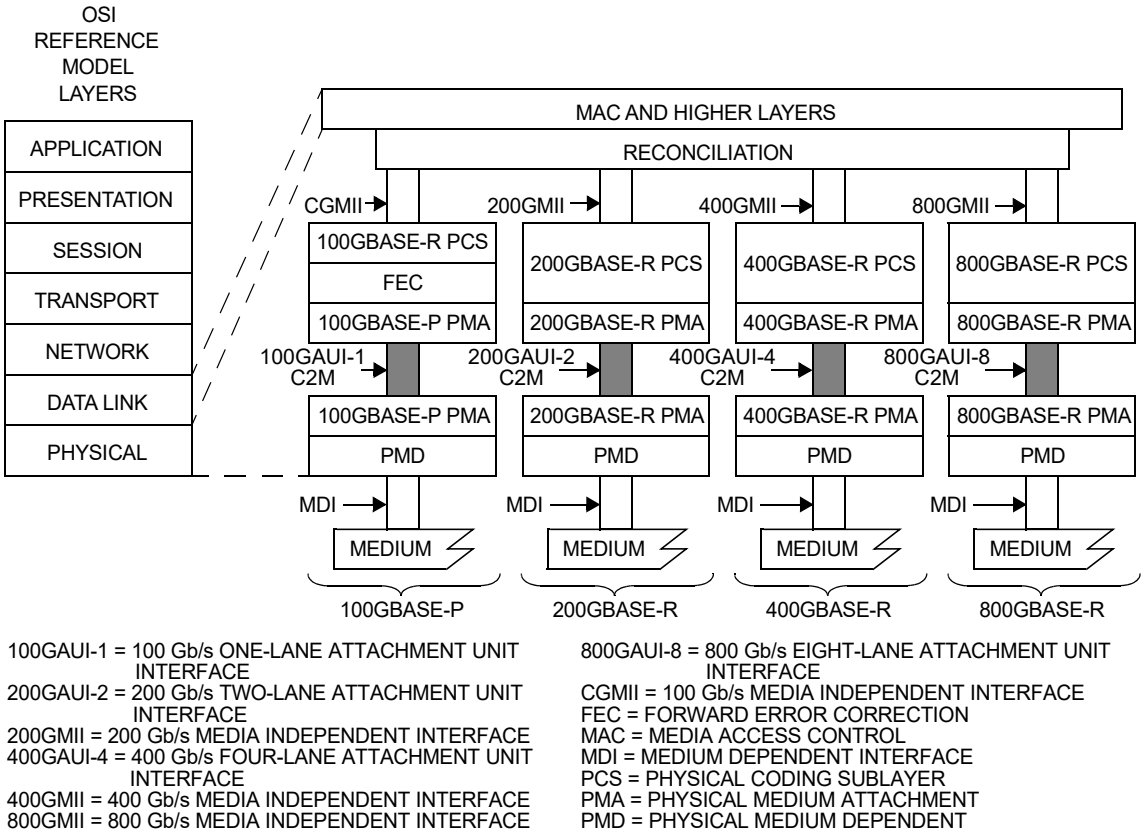
This annex defines the functional and electrical characteristics for the optional chip-to-module (C2M) 100 Gb/s one-lane Attachment Unit Interface (100GAUI-1 C2M), 200 Gb/s two-lane Attachment Unit Interface (200GAUI-2 C2M), ~~and~~ 400 Gb/s four-lane Attachment Unit Interface (400GAUI-4 C2M), and 800 Gb/s eight-lane Attachment Unit Interface (800GAUI-8 C2M). Figure 120G–1 shows the relationship of the ~~100GAUI-1, 200GAUI-2, and 400GAUI-4~~ C2M interface~~s~~ to the ISO/IEC Open System Interconnection (OSI) reference model. The C2M interface provides electrical characteristics and associated compliance points, which can optionally be used when designing systems with pluggable module interfaces.

The sublayers, including PCS and FEC (for 100GBASE-P PHYs), for each PHY that can optionally include a 100GAUI-1 C2M, 200GAUI-2 C2M, ~~or~~ 400GAUI-4 C2M, or 800GAUI-8 C2M interface are summarized in the tables in 80.1.5, ~~and~~ 116.1.4, and 169.1.4, and are specified in the corresponding PMD clause. The positioning of the ~~100GAUI-1 C2M, 200GAUI-2 C2M, or 400GAUI-4~~ C2M interfaces relative to other sublayers is shown in 135.1, ~~and~~ 120.1, and 173.1, with further examples in Annex 135A, ~~and~~ Annex 120A, and Annex 173A.

The C2M link is described in terms of a host C2M component, a C2M channel with associated insertion loss (ILdd), and a module C2M component. The host C2M component and module C2M component have connected ground references. Figure 120G–2 depicts a typical C2M application and summarizes the ILdd budget associated with the C2M application. The ILdd budget reflects the highest ILdd intended to be supported and is characterized by Equation (120G–5) and illustrated in Figure 120G–12. The C2M interface comprises independent data paths in each direction. Each 100GAUI-1, 200GAUI-2, ~~and~~ 400GAUI-4, or 800GAUI-8 C2M data path contains one, two, ~~or~~ four, or eight differential lanes, respectively, using PAM4 signaling, where the highest differential level corresponds to the symbol three and the lowest level corresponds to the symbol zero. Each lane is AC-coupled within the module.

The nominal signaling rate for each lane is 53.125 GBd.

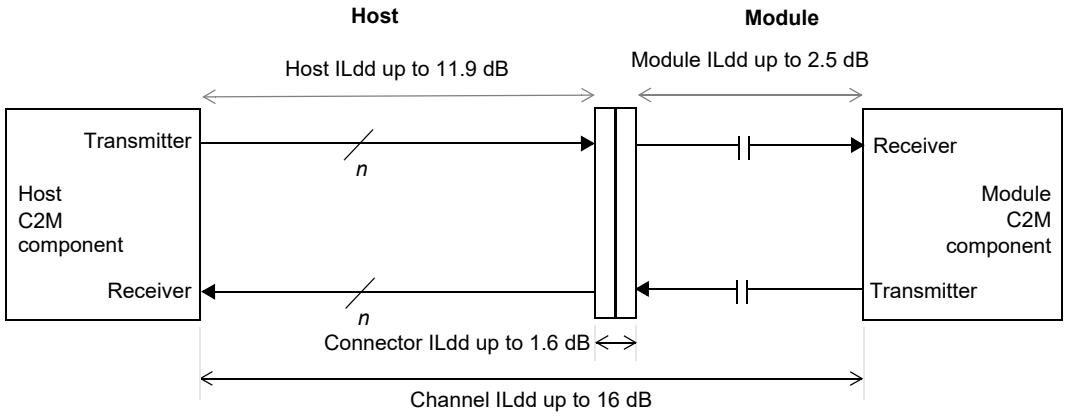
Replace Figure 120G–1 with the following figure:



100GAUI-1 = 100 Gb/s ONE-LANE ATTACHMENT UNIT INTERFACE
200GAUI-2 = 200 Gb/s TWO-LANE ATTACHMENT UNIT INTERFACE
200GMII = 200 Gb/s MEDIA INDEPENDENT INTERFACE
400GAUI-4 = 400 Gb/s FOUR-LANE ATTACHMENT UNIT INTERFACE
400GMII = 400 Gb/s MEDIA INDEPENDENT INTERFACE
800GMII = 800 Gb/s MEDIA INDEPENDENT INTERFACE
800GAUI-8 = 800 Gb/s EIGHT-LANE ATTACHMENT UNIT INTERFACE
CGMII = 100 Gb/s MEDIA INDEPENDENT INTERFACE
FEC = FORWARD ERROR CORRECTION
MAC = MEDIA ACCESS CONTROL
MDI = MEDIUM DEPENDENT INTERFACE
PCS = PHYSICAL CODING SUBLAYER
PMA = PHYSICAL MEDIUM ATTACHMENT
PMD = PHYSICAL MEDIUM DEPENDENT

Figure 120G–1—Example 100GAUI-1, 200GAUI-2, 400GAUI-4, and 800GAUI-8 C2M relationship to the ISO/IEC Open System Interconnection (OSI) reference model and the IEEE 802.3 Ethernet model

Change the title and NOTE in Figure 120G–2 as follows:



NOTE—The number of lanes *n* is equal to 1 for 100GAUI-1, 2 for 200GAUI-2, ~~and~~ 4 for 400GAUI-4, and 8 for 800GAUI-8.

Figure 120G–2—100GAUI-1, 200GAUI-2, ~~and~~ 400GAUI-4, and 800GAUI-8 C2M insertion loss budget at 26.56 GHz

120G.1.1 Bit error ratio

Change 120G.1.1 as follows:

The bit error ratio (BER) when processed by the PMA according to Clause 135 for 100GAUI-1 C2M, ~~or~~ according to Clause 120 for 200GAUI-2 or 400GAUI-4 C2M, or according to Clause 173 for 800GAUI-8 C2M, shall be less than 10^{-5}.

120G.2 Compliance point definitions

Change the text in 120G.2 as follows:

The electrical characteristics for the ~~100GAUI-1, 200GAUI-2, and 400GAUI-4~~ C2M interfaces are defined at compliance points for the host and module. Reference test fixtures, called compliance boards, are used to access the electrical specification parameters.

Figure 120G–3 depicts the location of compliance points for each lane when measuring ~~100GAUI-1, 200GAUI-2, or 400GAUI-4~~ C2M host compliance. The output of the Host Compliance Board (HCB) is used to verify the host electrical output signal at TP1a. The input of the HCB at TP4a is used to verify the host input compliance.

Figure 120G–4 depicts the location of compliance points for each lane when measuring ~~100GAUI-1, 200GAUI-2, or 400GAUI-4~~ C2M module compliance. The output of the Module Compliance Board (MCB) is used to verify the module electrical output signal at TP4. The input of the MCB at TP1 is used to verify the module input compliance.

Additional details on the requirements for the MCB and HCB are given in 120G.5.4.

Replace Figure 120G–3 with the following figure:

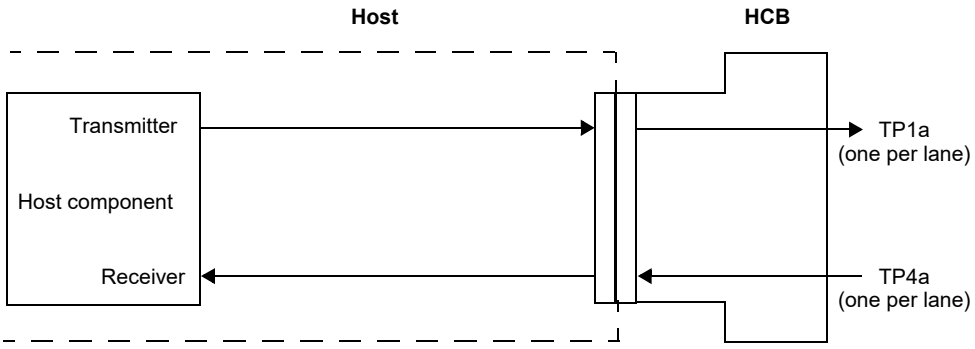


Figure 120G–3—Host compliance points

Replace Figure 120G–4 with the following figure:

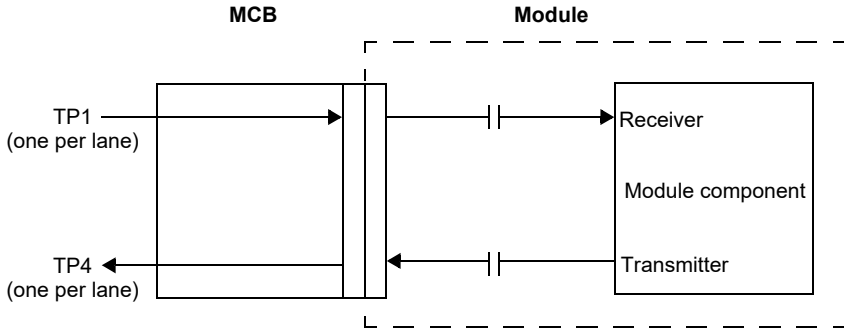


Figure 120G–4—Module compliance points

120G.3 Electrical characteristics

120G.3.1 Host output characteristics

Change footnote a in Table 120G–1 as follows (unchanged rows and footnotes not shown):

Table 120G–1—Host output characteristics at TP1a

Parameter	Reference	Value	Units
Signaling rate, each lane (range)		53.125 ± 50 ppm[a]	GBd
…			

[a] For 100GAUI-1, 200GAUI-2, or 400GAUI-4 C2M with a PMA in the same package as the PCS sublayer or for any 800GAUI-8 C2M. In other cases, the signaling rate is derived from the signaling rate presented to the PMA input lanes (see Figure 135–3 and Figure 120–3) by the adjacent PMA or FEC sublayers.

120G.3.1.5 Host output eye height and vertical eye closure (VEC)

Change the second paragraph of 120G.3.1.5 as follows:

All counter-propagating signals are asynchronous to the co-propagating signals using the PRBS13Q[17] (see 120.5.11.2.1) or PRBS31Q[18] (see 120.5.11.2.2) pattern, or a valid 100GBASE-R, 200GBASE-R, ~~or~~ 400GBASE-R, or 800GBASE-R signal. For the case where PRBS13Q or PRBS31Q are used with a common clock, there is at least 31 UI delay between the patterns on one lane and any other lane, so that the symbols on each lane are not correlated. The crosstalk generator is calibrated at TP4 using a test system with a response as defined in 120G.3.1, rather than the reference receiver of 120G.5.2, with target differential peak-to-peak voltage of 845 mV and transition time (see 120G.3.1.4) of 8.5 ps.

[17] PRBS13Q is also referred to as Pattern 4 for some PAM4 optical PMDs (e.g., see Table 121–9).
[18] PRBS31Q is also referred to as Pattern 3 for some PAM4 optical PMDs (e.g., see Table 121–9).

120G.3.2 Module output characteristics

Change the row for "Differential peak-to-peak output voltage (max)" in Table 120G-3 as follows (unchanged rows not shown):

Table 120G–3—Module output characteristics at TP4

Parameter	Reference	Value	Units
…			
Differential peak-to-peak output voltage (max) Short mode Long mode Disabled	120G.5.1	 600 845 35	 mV mV mV
…			

120G.3.2.1 Module output modes

Change Table 120G–4 as follows:

Table 120G–4—Module output mode mapping

IEEE 802.3 interface type	Module output mode	Host electrical interface
100GAUI-1 C2M	short	100GAUI-1-S C2M
100GAUI-1 C2M	long	100GAUI-1-L C2M
200GAUI-2 C2M	short	200GAUI-2-S C2M
200GAUI-2 C2M	long	200GAUI-2-L C2M
400GAUI-4 C2M	short	400GAUI-4-S C2M
400GAUI-4 C2M	long	400GAUI-4-L C2M
800GAUI-8 C2M	short	800GAUI-8-S C2M
800GAUI-8 C2M	long	800GAUI-8-L C2M

120G.3.2.2 Module output eye height and VEC

Change the second paragraph of 120G.3.2.2 as follows:

All counter-propagating signals are asynchronous to the co-propagating signals using the PRBS13Q[19] (see 120.5.11.2.1) or PRBS31Q[20] (120.5.11.2.2) pattern, or a valid 100GBASE-R, 200GBASE-R, ~~or~~ 400GBASE-R, or 800GBASE-R signal. For the case where PRBS13Q or PRBS31Q are used with a common clock, there is at least 31 UI delay between the patterns on one lane and any other lane, so that the symbols on each lane are not correlated. The crosstalk generator is calibrated at TP1a using a test system with a response as defined in 120G.3.1, rather than the reference receiver of 120G.5.2, with target

[19] PRBS13Q is also referred to as Pattern 4 for some PAM4 optical PMDs (e.g., see Table 121–9).
[20] PRBS31Q is also referred to as Pattern 3 for some PAM4 optical PMDs (e.g., see Table 121–9).

differential peak-to-peak voltage of 750 mV and transition time (see 120G.3.1.4) of 10 ps for short mode and 15 ps for long mode.

120G.3.3 Host input characteristics

Change the first row of Table 120G–7 as follows (unchanged rows not shown):

Table 120G–7—Host input characteristics

Parameter	Reference	Test point	Value	Units
Signaling rate, each lane (range) 100GAUI-1, 200GAUI-2, 400GAUI-4 800GAUI-8	120G.3.3.1	TP4a	53.125 ± 100 ppm 53.125 ± 50 ppm	GBd GBd
…				

120G.3.3.5 Host stressed input tolerance

120G.3.3.5.2 Host stressed input test calibration

Change item e) in the lettered list in 120G.3.3.5.2 as follows:

e) The counter-propagating crosstalk signals are calibrated at TP1a using a test system with a response as defined in 120G.3.1, rather than the reference receiver of 120G.5.2, to the differential peak-to-peak voltage and transition time (see 120G.3.1.4) specified in Table 120G–8. The crosstalk signal transition time and amplitude are calibrated with a PRBS13Q pattern. The crosstalk pattern is changed to PRBS31Q (see 120.5.11.2.2), scrambled idle (see 82.2.11, ~~and~~ 119.2.4.9, or 172.2.4.11), or another valid 100GBASE-R, 200GBASE-R, ~~or~~ 400GBASE-R, or 800GBASE-R signal for stressed signal calibration (see step g)). If the PRBS31Q pattern is used with a common clock, there is at least 31 UI delay between the PRBS31Q patterns on one lane and any other lane.

120G.3.3.5.3 Host stressed input test procedure

Change the first three paragraphs of 120G.3.3.5.3 as follows:

After the stress has been calibrated, the pattern generator is set to generate PRBS31Q, scrambled idle, or another valid 100GBASE-R, 200GBASE-R, ~~or~~ 400GBASE-R, or 800GBASE-R sequence. The HCB is unplugged from the MCB and is plugged into the host under test. The host electrical output is enabled on all lanes with any of the patterns above. The test is repeated with sinusoidal jitter set to each of the six cases in Table 162–17.

If the test is performed with PRBS31Q, the BER for the AUI under test may be calculated using the bit error counter in the PMA test pattern checker (see 120.5.11.2.2) as the number of bit errors divided by the number of received bits. The BER for the AUI under test is the average of the BER of each of its lanes.

If the test is performed with scrambled idle or another valid 100GBASE-R, 200GBASE-R, ~~or~~ 400GBASE-R, or 800GBASE-R sequence, the BER for the AUI under test may be calculated using the FEC decoder error counters (see 91.6, ~~and~~ 119.3.1, and 172.3.1), as the number of FEC symbol errors divided by the number of received bits.

120G.3.4 Module input characteristics

Change the first row in Table 120G–9 as follows (unchanged rows not shown):

Table 120G–9—Module input characteristics

Parameter	Reference	Test point	Value	Units
Signaling rate, each lane (range) 100GAUI-1, 200GAUI-2, 400GAUI-4 800GAUI-8	120G.3.4.1	TP1	53.125 ± 100 ppm 53.125 ± 50 ppm	GBd GBd
…				

120G.3.4.3 Module stressed input tolerance

120G.3.4.3.2 Module stressed input test calibration

Change item e) in the lettered list in 120G.3.4.3.2 as follows:

e) The counter-propagating crosstalk signals are calibrated at TP4 using a test system with a response as defined in 120G.3.1, rather than the reference receiver of 120G.5.2, to the differential peak-to-peak voltage and transition time (see 120G.3.1.4) specified in Table 120G–10. The crosstalk signal transition time and amplitude are calibrated with a PRBS13Q pattern. The crosstalk pattern is changed to PRBS31Q (see 120.5.11.2.2), scrambled idle (see 82.2.11, 119.2.4.9, or 172.2.4.11), or another valid 100GBASE-R, 200GBASE-R, ~~or~~ 400GBASE-R, or 800GBASE-R signal for stressed signal calibration (see step g)). If the PRBS31Q pattern is used with a common clock, there is at least 31 UI delay between the PRBS31Q patterns on one lane and any other lane.

120G.3.4.3.3 Module stressed input test procedure

Change the first three paragraphs of 120G.3.4.3.3 as follows:

After the stress has been calibrated, the pattern generator is set to generate PRBS31Q, scrambled idle, or another valid 100GBASE-R, 200GBASE-R,~~ or~~ 400GBASE-R, or 800GBASE-R sequence. The HCB is unplugged from the MCB and the module under test is plugged into the MCB. The module electrical output is enabled on all lanes with any of the patterns above. The test is repeated with sinusoidal jitter set to each of the six cases in Table 162–17.

If the test is performed with PRBS31Q, the BER for the AUI under test may be calculated using the bit error counter in the PMA test pattern checker (see 120.5.11.2.2) as the number of bit errors divided by the number of received bits. The BER for the AUI under test is the average of the BER of each of its lanes.

If the test is performed with scrambled idle or another valid 100GBASE-R, 200GBASE-R, ~~or~~ 400GBASE-R, or 800GBASE-R sequence, the BER for the AUI under test may be calculated by placing the module under test into local loopback (see 120.5.9) and feeding the module output into a compliant host or its equivalent. The BER for the AUI under test is calculated using the FEC decoder error counters (see 91.6, ~~and~~ 119.3.1, and 172.3.1), as the number of FEC symbol errors divided by the number of received bits.

Change the title of 120G.6 as follows:

120G.6 Protocol implementation conformance statement (PICS) proforma for Annex 120G, Chip-to-module Attachment Unit Interfaces 100GAUI-1 C2M, 200GAUI-2 C2M, 400GAUI-4 C2M, and 800GAUI-8 C2M ~~100 Gb/s one-lane Attachment Unit Interface (100GAUI-1 C2M), 200 Gb/s two-lane Attachment Unit Interface (200GAUI-2 C2M), and 400 Gb/s four-lane Attachment Unit Interface (400GAUI-4 C2M)~~[21]

120G.6.1 Introduction

Change the first paragraph of 120G.6.1 as follows:

The supplier of a protocol implementation that is claimed to conform to Annex 120G, Chip-to-module Attachment Unit Interfaces 100GAUI-1 C2M, 200GAUI-2 C2M, 400GAUI-4 C2M, and 800GAUI-8 C2M ~~100 Gb/s one-lane Attachment Unit Interface (100GAUI-1 C2M), 200 Gb/s two-lane Attachment Unit Interface (200GAUI-2 C2M), and 400 Gb/s four-lane Attachment Unit Interface (400GAUI-4 C2M)~~, shall complete the following protocol implementation conformance statement (PICS) proforma.

120G.6.2 Identification

120G.6.2.2 Protocol summary

Change the table in 120G.6.2.2 as follows:

Identification of protocol standard	IEEE Std 802.3df-2024, Annex 120G, Chip-to-module Attachment Unit Interfaces 100GAUI-1 C2M, 200GAUI-2 C2M, 400GAUI-4 C2M, and 800GAUI-8 C2M ~~100 Gb/s one-lane Attachment Unit Interface (100GAUI-1 C2M), 200 Gb/s two-lane Attachment Unit Interface (200GAUI-2 C2M), and 400 Gb/s four-lane Attachment Unit Interface (400GAUI-4 C2M)~~
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3df-2024.)	

Date of Statement	

[21] *Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this annex so that it can be used for its intended purpose and may further publish the completed PICS.

120G.6.3 Major capabilities/options

Change item NOL in the table in 120G.6.3 as follows (unchanged rows not shown):

Item	Feature	Subclause	Value/Comment	Status	Support
NOL	Number of differential AC-coupled lanes	120G.1	One, two, ~~or~~ four, or eight independent data paths in each direction for 100GAUI-1, 200GAUI-2, ~~and~~ 400GAUI-4, and 800GAUI-8 C2M, respectively	M	Yes [ ]
…					

Change the title of 120G.6.4 as follows:

120G.6.4 PICS proforma tables for Chip-to-module Attachment Unit Interfaces 100GAUI-1 C2M, 200GAUI-2 C2M, 400GAUI-4 C2M, and 800GAUI-8 C2M ~~100 Gb/s one-lane Attachment Unit Interface (100GAUI-1 C2M), 200 Gb/s two-lane Attachment Unit Interface (200GAUI-2 C2M), and 400 Gb/s four-lane Attachment Unit Interface (400GAUI-4 C2M)~~

Change the title of Annex 162A (added by IEEE Std 802.3ck-2022) as follows:

Annex 162A

(informative)

Transmitter, receiver, and channel parameters associated with test points TP0 and TP5 for 100GBASE-CR1, 200GBASE-CR2, ~~and~~ 400GBASE-CR4, and 800GBASE-CR8

162A.1 Overview

Change the text in 162A.1 as follows:

This annex provides information on transmitter, receiver, and channel parameters associated with test points TP0 and TP5, which might not be testable in an implemented system. TP0 and TP5 test points are illustrated in the 100GBASE-CR1, 200GBASE-CR2, ~~and~~ 400GBASE-CR4, and 800GBASE-CR8 link block diagram of Figure 162–2. This annex also provides information on channel characteristics.

162A.6 Channel effective return loss (ERL)

Change the text in 162A.6 as follows:

The ~~100GBASE-CR1, 200GBASE-CR2 and 400GBASE-CR4 channels are~~ channel is recommended to meet the ERL specified in 163.10.3.

Change the title of Annex 162B (added by IEEE Std 802.3ck-2022) as follows:

Annex 162B

(normative)

Test fixtures for 100GBASE-CR1, 200GBASE-CR2, 400GBASE-CR4, 800GBASE-CR8, 100GAUI-1 C2M, 200GAUI-2 C2M, ~~and~~ 400GAUI-4 C2M, and 800GAUI-8 C2M

162B.1 Test fixtures

Change 162B.1 as follows:

Transmitter and receiver measurements at TP2 or TP3 for the 100GBASE-CR1, 200GBASE-CR2, ~~and~~ 400GBASE-CR4, and 800GBASE-CR8 hosts (see Annex 162D) and at TP1a or TP4a for the 100GAUI-1, 200GAUI-2, ~~and~~ 400GAUI-4, and 800GAUI-8 C2M hosts (see Annex 120G), are made utilizing the test fixture specified in 162B.2. Cable assembly measurements for the cable assembly types (see Annex 162D) are made between TP1 and TP4 with test fixtures as specified in 162B.3 on both ends. The test fixtures are specified in a mated state to enable connections to measurement equipment. The reference insertion loss of the mated test fixtures is 6.6 dB at 26.56 GHz using Equation (162B–5). The requirements in the referenced subclauses are not the MDI connector specifications for an implemented design.

Change the title of 162B.5 as follows:

162B.5 Protocol implementation conformance statement (PICS) proforma for Annex 162B, Test fixtures for 100GBASE-CR1, 200GBASE-CR2, 400GBASE-CR4, 800GBASE-CR8, 100GAUI-1 C2M, 200GAUI-2 C2M, ~~and~~ 400GAUI-4 C2M, and 800GAUI-8 C2M[22]

162B.5.1 Introduction

Change the first paragraph of 162B.5.1 as follows:

The supplier of a protocol implementation that is claimed to conform to Annex 162B, Test fixtures for 100GBASE-CR1, 200GBASE-CR2, 400GBASE-CR4, 800GBASE-CR8, 100GAUI-1 C2M, 200GAUI-2 C2M, ~~and~~ 400GAUI-4 C2M, and 800GAUI-8 C2M, shall complete the following protocol implementation conformance statement (PICS) proforma.

162B.5.2 Identification

162B.5.2.2 Protocol summary

Change the table in 162B.5.2.2 as follows:

Identification of protocol standard	IEEE Std 802.3df-2024, Annex 162B, Test fixtures for 100GBASE-CR1, 200GBASE-CR2, 400GBASE-CR4, 800GBASE-CR8, 100GAUI-1 C2M, 200GAUI-2 C2M, ~~and~~ 400GAUI-4 C2M, and 800GAUI-8 C2M
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3df-2024.)	

Date of Statement	

Change the title of 162.B.5.4 as follows:

162B.5.4 PICS proforma tables for test fixtures for ~~Test fixtures for~~ 100GBASE-CR1, 200GBASE-CR2, 400GBASE-CR4, 800GBASE-CR8, 100GAUI-1 C2M, 200GAUI-2 C2M, ~~and~~ 400GAUI-4 C2M, and 800GAUI-8 C2M

[22] *Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this annex so that it can be used for its intended purpose and may further publish the completed PICS.

Change the title of Annex 162C (added by IEEE Std 802.3ck-2022) as follows:

Annex 162C

(normative)

MDIs for 100GBASE-CR1, 200GBASE-CR2, ~~and~~ 400GBASE-CR4, and 800GBASE-CR8

162C.1 Overview

Change the first paragraph of 162C.1 as follows:

This annex defines the Media Dependent Interface (MDI) for 100GBASE-CR1, 200GBASE-CR2, ~~and~~ 400GBASE-CR4, and 800GBASE-CR8. The MDI couples the PMD (specified in 162.8 and 162.9) to the cable assembly (specified in 162.11). The PMDs supportable for each MDI connector type are given in Table 162C–1. The SFP-DD112, DSFP, QSFP112, QSFP-DD800, and OSFP are also referred to as multi-lane connectors.

Change Table 162C–1 as follows:

Table 162C–1—Number of PMDs supportable for each connector type

MDI types	100GBASE-CR1	200GBASE-CR2	400GBASE-CR4	800GBASE-CR8	Reference
SFP112	1	—	—	—	162C.2.1
SFP-DD112	1,2	1	—	—	162C.2.2
DSFP	1, 2	1	—	—	162C.2.3
QSFP112	1, 2, 4	1, 2	1	—	162C.2.4
QSFP-DD800	1, 2, 4, 8	1, 2, 4	1, 2	1	162C.2.5
OSFP	1, 2, 4, 8	1, 2, 4	1, 2	1	162C.2.6

Insert the following paragraph after the fourth paragraph of 162C.1:

For 800GBASE-CR8, the mechanical interface between the PMD and the cable assembly is a mated pair of connectors meeting the requirements of 162C.2.5 (QSFP-DD800) or 162C.2.6 (OSFP). The plug connector is used on the cable assembly and the receptacle is used on the PMD. The cable assembly connector shall be the MDI connector plug. The PMD connector shall be the MDI connector receptacle.

Change Table 162C–2 as follows:

Table 162C–2—PMD to connector signal assignments

PMD signal <PMD number>:<PMD signal>				Connector signal
100GBASE-CR1	**200GBASE-CR2**	**400GBASE-CR4**	**800GBASE-CR8**	
0:DL0n	0:DL0n	0:DL0n	0:DL0n	DL0n
0:DL0p	0:DL0p	0:DL0p	0:DL0p	DL0p
1:DL0n	0:DL1n	0:DL1n	0:DL1n	DL1n
1:DL0p	0:DL1p	0:DL1p	0:DL1p	DL1p
2:DL0n	1:DL0n	0:DL2n	0:DL2n	DL2n
2:DL0p	1:DL0p	0:DL2p	0:DL2p	DL2p
3:DL0n	1:DL1n	0:DL3n	0:DL3n	DL3n
3:DL0p	1:DL1p	0:DL3p	0:DL3p	DL3p
4:DL0n	2:DL0n	1:DL0n	0:DL4n	DL4n
4:DL0p	2:DL0p	1:DL0p	0:DL4p	DL4p
5:DL0n	2:DL1n	1:DL1n	0:DL5n	DL5n
5:DL0p	2:DL1p	1:DL1p	0:DL5p	DL5p
6:DL0n	3:DL0n	1:DL2n	0:DL6n	DL6n
6:DL0p	3:DL0p	1:DL2p	0:DL6p	DL6p
7:DL0n	3:DL1n	1:DL3n	0:DL7n	DL7n
7:DL0p	3:DL1p	1:DL3p	0:DL7p	DL7p
0:SL0n	0:SL0n	0:SL0n	0:SL0n	SL0n
0:SL0p	0:SL0p	0:SL0p	0:SL0p	SL0p
1:SL0n	0:SL1n	0:SL1n	0:SL1n	SL1n
1:SL0p	0:SL1p	0:SL1p	0:SL1p	SL1p
2:SL0n	1:SL0n	0:SL2n	0:SL2n	SL2n
2:SL0p	1:SL0p	0:SL2p	0:SL2p	SL2p
3:SL0n	1:SL1n	0:SL3n	0:SL3n	SL3n
3:SL0p	1:SL1p	0:SL3p	0:SL3p	SL3p
4:SL0n	2:SL0n	1:SL0n	0:SL4n	SL4n
4:SL0p	2:SL0p	1:SL0p	0:SL4p	SL4p
5:SL0n	2:SL1n	1:SL1n	0:SL5n	SL5n
5:SL0p	2:SL1p	1:SL1p	0:SL5p	SL5p
6:SL0n	3:SL0n	1:SL2n	0:SL6n	SL6n

Table 162C–2—PMD to connector signal assignments *(continued)*

PMD signal <PMD number>:<PMD signal>				Connector signal
100GBASE-CR1	**200GBASE-CR2**	**400GBASE-CR4**	**800GBASE-CR8**	
6:SL0p	3:SL0p	1:SL2p	0:SL6p	SL6p
7:SL0n	3:SL1n	1:SL3n	0:SL7n	SL7n
7:SL0p	3:SL1p	1:SL3p	0:SL7p	SL7p

162C.2.5 QSFP-DD800

Change the first paragraph of 162C.2.5 as follows:

For 100GBASE-CR1, 200GBASE-CR2, ~~or~~ 400GBASE-CR4, or 800GBASE-CR8, the mechanical interface between the PMD and the cable assembly may be a mated pair of connectors ~~as defined~~ as defined in the QSFP-DD800 MSA. QSFP-DD800 supports up to eight lanes.

162C.2.6 OSFP

Change the first paragraph of 162C.2.6 as follows:

For 100GBASE-CR1, 200GBASE-CR2, ~~or~~ 400GBASE-CR4, or 800GBASE-CR8, the mechanical interface between the PMD and the cable assembly may be a mated pair of connectors as defined in the OSFP MSA. OSFP supports up to eight lanes.

Change the title of 162C.3 as follows:

162C.3 Protocol implementation conformance statement (PICS) proforma for Annex 162C, MDIs for 100GBASE-CR1, 200GBASE-CR2, ~~and~~ 400GBASE-CR4, and 800GBASE-CR8[23]

162C.3.1 Introduction

Change the first paragraph of 162C.3.1 as follows:

The supplier of a protocol implementation that is claimed to conform to Annex 162C, MDIs for 100GBASE-CR1, 200GBASE-CR2, ~~and~~ 400GBASE-CR4, and 800GBASE-CR8, shall complete the following protocol implementation conformance statement (PICS) proforma.

162C.3.2 Identification

162C.3.2.2 Protocol summary

Change the table in 162C.3.2.2 as follows:

Identification of protocol standard	IEEE Std 802.3df-2024, Annex 162C, MDIs for 100GBASE-CR1, 200GBASE-CR2, ~~and~~ 400GBASE-CR4, and 800GBASE-CR8
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3df-2024.)	

Date of Statement	

Change the title of 162C.3.4 as follows:

162C.3.4 PICS proforma tables for MDIs for 100GBASE-CR1, 200GBASE-CR2, ~~and~~ 400GBASE-CR4, and 800GBASE-CR8

[23] *Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this annex so that it can be used for its intended purpose and may further publish the completed PICS.

Change the title of Annex 162D (added by IEEE Std 802.3ck-2022) as follows:

Annex 162D

(informative)

Cable assemblies and hosts for 100GBASE-CR1, 200GBASE-CR2, ~~and~~ 400GBASE-CR4, and 800GBASE-CR8

162D.1 Overview

Change the text of 162D.1 as follows:

This annex describes cable assembly types specified in 162.11 for hosts with 100GBASE-CR1, 200GBASE-CR2,~~ or~~ 400GBASE-CR4, or 800GBASE-CR8 Physical Layers. The six MDI connector receptacles specified are given in Table 162D–1. This enables multiple cable assembly types with different combinations of the plug connectors at each end.

162D.1.1 Cable assembly types

Change the text of 162D.1.1 as follows:

Cable assembly types, denoted as 100GBASE-CR1, 200GBASE-CR2,~~ and~~ 400GBASE-CR4, and 800GBASE-CR8, have a common set of electrical parameters specified in 162.11, enabling a 2 m length. Cable assembly types with different combinations of the plug connectors for compatible host receptacles and supportable number of PMDs are given in Table 162D–2 for 100GBASE-CR1, Table 162D–3 for 200GBASE-CR2, ~~and~~ Table 162D–4 for 400GBASE-CR4, and Table 162D–5 for 800GBASE-CR8; other combinations are possible.

Insert Table 162D–5 after Table 162D–4 as follows:

Table 162D–5—800GBASE-CR8 cable assembly types and supportable PMDs

One end		Other end(s)		Supportable PMDs
Receptacle/Plug	Number	Receptacle/Plug	Number	Number
QSFP-DD800	1	QSFP-DD800	1	1
QSFP-DD800	1	OSFP	1	1
OSFP	1	OSFP	1	1

Insert new annex Annex 172A corresponding to Clause 172 as follows:

Annex 172A

(informative)

800GBASE-R PCS FEC codeword examples

This annex provides example PCS FEC codewords produced by the 64B/66B to 256B/257B transcoding, scrambling, pre-FEC distribution, and Reed-Solomon encoding defined in 172.2.4. This annex presents data in a tabular form. The contents of the tables are hexadecimal representations of the data and are transmitted to the symbol distribution function from left to right within each row starting from the top row and ending at the bottom row. The most significant bit of each hex symbol is transmitted first.

A constant transmission of idle control characters is sent to the 256B/257B transcoder in each flow of the 800GBASE-R PCS resulting in a continuous stream of 257-bit blocks per flow, tx_xcoded<0:256>, shown in hex:

tx_xcoded<0:256> = 0070000000000000078000000000000007800000000000000780000000000000

In this example, an alignment marker is due for insertion in each flow. The scrambler seed [see Equation (49–1)] just before the 257-bit block was scrambled is as follows, for each of the two flows:

For flow 0, the scrambler seed is S<0:57> = 24E6959D0FA5DBD

For flow 1, the scrambler seed is S<0:57> = 1FB58857D81624F

In each flow, after scrambling and inserting the alignment marker group am_mapped, the variable tx_scrambled_am is produced as shown in Table 172A–1 for flow 0 and Table 172A–2 for flow 1. In these tables, italicized characters are alignment markers and bold characters are padding for the alignment markers. In each flow, just prior to insertion, the seed of the PRBS9 generator used for padding is P<0:8> = 0x100.

NOTE 1—A text file containing the patterns in Table 172A–1 and Table 172A–2 is available at https://standards.ieee.org/downloads/802.3/.

In each flow, after distributing into two message blocks and PCS FEC encoding, codewords c_A and c_B are produced. For each flow, c_A and c_B may be illustrated as two 5440-bit representations cx_A and cx_B as follows:

For all i=0 to 543:

$cx_A <(10i+9):(10i)> = c_A<i>$

$cx_B <(10i+9):(10i)> = c_B<i>$

The expanded codewords are shown in Table 172A–3 and Table 172A–4 for flow 0, and in Table 172A–5 and Table 172A–6 for flow 1 (bold characters are parity).

NOTE 2—A text file containing the patterns in Table 172A–3 through Table 172A–6 is available at https://standards.ieee.org/downloads/802.3/.

For both flows, the example codewords have tx_am_sf<2:0> = {0,0,0}.

Table 172A–1—Example tx_scrambled_am with alignment marker group for 800GBASE-R PCS flow 0

Index <*i*:*j*>	tx_scrambled_am<*i*:*j*>
<0:256>	*0B2ACAB2ACAB2ACAB2ACAB2ACAB2ACAB2ACAB2ACA9324C9324C9324C9324C9324*
<257:513>	*1926499264992649 91B421184592144D2F445014D517435064290242CA669AA6A*
<514:770>	*1374DD314C5354D5354DD314C5334DD356D5B56D5B56D5B56D5B56D5B56D5B56D*
<771:1027>	*0B6ADAB66F9B96C9B76DDB96D1B76D1BF6E1B26CDBD6D9B8B7DA9F80678A8AD7B*
<1028:1284>	*1E4B2F2B80AF5D571B9B5D4CBDF1D00F9FF9714372729199DB35AFF4CDF2E9BF9*
<1285:1541>	*1D7E1AA0BD3D8BA16DAAB83C86F1C6A4C3D959E995921E601CD49D736213A81A3*
<1542:1798>	*028FD1912A2AD9283950E183FA3B0196372399DBC94932C982990B4102985E84A*
<1799:2055>	*15D1B04967A30D5178CE48F0569849A***00846139561BD37228569FB24B7E4D4CC0**
<2056:2312>	08CCD177010357E8DAB65B6F9160968075341AC958CFC828D8372DC66242646D8
<2313:2569>	026FEAA09736E915DD54C5F7E600ECFCBD7D7C207941C5D7182D8B95FE412ED12
<2570:2826>	014CCE446415F10CDC7BBAFB1CC4B442EF5737AFB4F3BED48D240C9095F5FD3A6
<2827:3083>	10219FBE135EDE0B73C15238C150007886562E30A50CB27DF341954DB8CA1C564
<3084:3340>	16598EAD3C229838CB9BEE7F793139EE1F89FDAD9071687CBEDF89B4E527A03CD
<3341:3597>	1C2044F260A85EE6EB506C25E7C1196298548B4B3576F1B084C83F2E3CB5FC5F6
<3598:3854>	1C9D40EF27471536FE9EB5E3BC3870D46755080EA6D29F09CF8FA697A738DD3EC
<3855:4111>	193FA8A7675CE03706A49019B93544E19DD66CE78E6A94BEBD07ECCAE7DF2076D
<4112:4368>	081919F234C00959E5AFFC9F83C909805378B5F3F2E4917F3E48B5DE4758CEA42
<4369:4625>	1D378C193CDD3D0F781ABC3529BF76A66B7C73A7230B517D96DAFF6A39F9EA9B6
<4626:4882>	05E852B6917E9D1410B6509E778629A516FB2BCEABA79F12241DBC94CDAFFFF02
<4883:5139>	1D98F5991744C9FC5393EFD6299558CB4F28DF3BF3C8636DBA505E3A296C7BD2E
<5140:5396>	00FAACFBFDBC1C29CED046C73C9AAAFE3DE8849ADAD16E864814846BB8CB889AD
<5397:5653>	04D11BFE0E8DEF5ECFDBE45D1EE4607B4B44DF874F8E976DD828FCFD38158A8FF
<5654:5910>	00EE28B635049BA9506024BA13862A1D6BAE22D0DB5DDB1F4DBE0F80E9EDBBCC6
<5911:6167>	1CD0769BC76446DA04136E7C6D19905DFB81AC3BFD931426901028D729E529F5A
<6168:6424>	14C3FF33243D7D2B5137B63359FD25B82CDE769D0F10D2E60A0386E60820BE8F4
<6425:6681>	1993F1FE2D6C60459F26A74BD0265C2959899E4C5B24196AFD51DB241CFCF9091
<6682:6938>	18EE61EA5A0D584DE8AC602618874BBA60A907115513BC960F6BE32C68F1F2458
<6939:7195>	042251FD6EF16662F5C99D9779B20B865B1401C96034C99550401BCB2792E5638
<7196:7452>	0CE3AE06476B769F33E5577CE4BA6D62071CABE3EA9561D6077FD23909568A25A
<7453:7709>	1BBC46AC3DF26A5BB0EA4FDBCBFB42738A84007619C594E24AB396AFB5F05FBFF
<7710:7966>	076C96A407E106D494AA6B0C5168E1F335B812D7BC530CE8C6FC13F6C54EC2165
<7967:8223>	056CC06AFE2BD2A9894C4D1AD9E632F861208AD3894EFF0DE8B0291C486EA3281
<8224:8480>	094534A897031E6307E32C1906C85E99CD4696FC818D2B5EAF26A576DE149AE12
<8481:8737>	085AE9048EDDC5401827FAA937411FF35C10287236FFDC87E7E7E334B038EE3F9
<8738:8994>	014179E0E2359D3B961A1302FA4B7AC384F0564B15D7504DADBE3C65EE8F6F13A
<8995:9251>	08D40F4B092621CCA4919E81D0C15014204622D41814894DBE389C149E5E2257A
<9252:9508>	0E4772C6718DA5361ABFAAD60F5C32D304740DE671045CDAD6617125F4BBF457D
<9509:9765>	071A7D2B02B41F13971A22FE8A29F0A03C1CEC43CA0411D7872F18D12E0A2BD06
<9766:10022>	1344403844B360B4A61968D045941FF821511C2E95455C300EED811D314AD7018
<10023:10279>	0275A5C4A36F6B8B13AFAFFFCDFDBD9B13F00488494886CDEB13B31FC9F7941CF

Table 172A–2—Example tx_scrambled_am with alignment marker group for 800GBASE-R PCS flow 1

Index <*i*:*j*>	tx_scrambled_am<*i*:*j*>
<0:256>	*0B2ACAB2ACAB2ACAB2ACAB2ACAB2ACAB2ACA9324C9324C9324C9324C9324*
<257:513>	*1926499264992649 91B421184592144D2F445014D517435064290242CA669AA6A*
<514:770>	*1374DD314C5354D5354DD314C5334DD356D5B56D5B56D5B56D5B56D5B56D5B56D*
<771:1027>	*0B6ADAB66F9B96C9B76DDB96D1B76D1BF6E1B26CDBD6D9B8B8196F7C588549274*
<1028:1284>	*063530AC615723489C7AA533420E2FF060068EBC8D8D6E6624CA500B320D16406*
<1285:1541>	*0181256F4EC1749EA25944C3B93E35583CE696199A91DE9020DB9EB3922FA719F*
<1542:1798>	*036FA98F2DAB3957C6AF1E7C05C4FE69C8DC662436B6CD367D66F4BEFD67A17B5*
<1799:2055>	*0A2E4FB6985CF2AE8731B70FA967B65***00846139561BD37228569FB24B7E4D4CC0**
<2056:2312>	1F86712D0B9C5715BC0B73ECCC6DD388DCC420940ACD6A761E9DBFD65F67A6F80
<2313:2569>	17D275B453FCD8EE9BBA94A522014E8FA3612BD59F1561BF74F4DFA4BBB186627
<2570:2826>	08F114445112D312B36734B261D20AC5BA8E888DFFF7AC7FBFDDCC270294A477B
<2827:3083>	129C411094B7035E81B92A2390C3A5F42EEB0FAFD8B4AB14E2F282A004EF203DF
<3084:3340>	1922EC8280625B274A3BE4165602BE1AA5D500E9B5E42CA8A1ABF23428487DCC0
<3341:3597>	05283BE31434B6768BA691A9E03AD081BDE41FD90DCFE850CC9C6993D2632CE00
<3598:3854>	010D455AB1946A8AF1B27E7970F9C64099FE6DD0BF426CFDD965F0F62B29F497B
<3855:4111>	0A24DCC7CA2E026301236DF64D82DE1BA3C0782F57F00618A931EBD9CD53E5FDF
<4112:4368>	1FB0A3715E0D9FB90914C768F175C7CC935331B3C4575547B4C4C25B9ABCD8698
<4369:4625>	0C7BDEACF874C37E408742B8E1B1D1155793CD9A46DB62CED7FED0542B774E155
<4626:4882>	0FB5F72DEEF86145B1203BB9357A111B3DE41A6F68FF8EFBA05764C7C8A310219
<4883:5139>	14E0EFA4D7E1D11276142A97DC986CC8AD33952EB7415501160BC907D27957D78
<5140:5396>	1ADD66B6629E510BDC1C913AB02C7BD575C4165BA1F57D71C1C67C129EDCD0885
<5397:5653>	09357A0D4F3A2EDE5040F70E722B367A0B5995F07EDB2DA93118CA44E4A95BD8C
<5654:5910>	1F87871D3792E369DC0EE28B3700C7B21256A342A41541C21760FA2A817EB1718
<5911:6167>	1A08EF85796CA9198F49380C6834D413CD1E6AB22AAF3826244FF2FAE786966CE
<6168:6424>	0C17672A70D318BD56B86CAD4E6B5F8CF307FDEC8331ECC71F7918F94245C3F62
<6425:6681>	19F56BAEFA5211C1272E4F9D16CA2CD6F63E731C1F67495BB02209956EB212FF2
<6682:6938>	04CE02FCA580E394CD4BBEEE49A2724E89FCFF76F58F6A5C9554C369DAF03EA38
<6939:7195>	0D7A7417F605A52B76F10EB7D784A8C0D46CA4A46082E97C54682CCAD8128F4C8
<7196:7452>	1F062F513B79AA19647D271AECA27C172D10824306C524CFC5AD1A882EC269C47
<7453:7709>	16464DB070D86EA6F6F2DCC17BF64C0439C0DCC6F5E080B7FA5CF0BC17D4941FE
<7710:7966>	1E570C5B95F6A1EF2568FBA6A3E2AA3E10F92CFC848B7DDDC0C229DA995EF3238
<7967:8223>	0B019680216F92EFC7A77F2D846BF50FB5571C8B0597EDD4444C0D1ACD73ED0B2
<8224:8480>	0D4342D2956C0316F27A6CA376E43165DFF6E0BF72B3B4B684DD48B5C1E497305
<8481:8737>	19D3C8BC33383FBF0B145F73B019C77C25F7EF62FE3A30D7BF87ACDE21F33AB65
<8738:8994>	1B21A3FA20EB18693BA928B8E8B1481F9C1B4CAA136A317E5575FEE62626B4689
<8995:9251>	0217E9C2B11E1B9B07184C9B7188D658F7703770D3DB76533A2A6AD850A9C01B3
<9252:9508>	1407CB283808020B5602DA0A14AC8761931FDB8BE807E7D3D7A6ED35A656B92F8
<9509:9765>	059FC0379557A8410F5AA2B5D7F4A506BA87443FF05C4F26D9B1B7625AA0AAD8A
<9766:10022>	11C1338632F6EE337BA90C50DB4CDEC64C758D8B5FAF5A880C5C3C62FBCE1A7BD
<10023:10279>	0581091408463FFB4FD2C97DE7105B4108FC7FCF460728BDA613FD80FA8608928

Table 172A–3—RS(544,514) codeword A for 800GBASE-R PCS flow 0

Index <*i*:*j*>	cx_A<*i*:*j*>
<5439:5120>	A6A9AA6A9AA6A9AA6A9A6499264992649926499264992D886284BD280BA2609026519565D946559565196
<5119:4800>	6D5B56D5B56D5B56D5B57D936ED8B62D876CD9B6FB41F547DE7A6A07575BDEA014FDD8C499B97EE9
<4799:4480>	BCD56BC9A11D7D8256A6A999E2B1B315CA3131AA380C3B8A34339492684C810BD2EA92C331E3C619
<4479:4160>	401C8F61447E7EDCCA66077D56AFED4815C9AFE6D8B691236C7F7A4894AA7ECDCEBC10380639D209
<4159:3840>	48B9904D84BBDC645B57BEBEE96049F5CB27E7ACB40A8A0DE01AA509342C6CB8534AAEA22633BD93
<3839:3520>	3BFF204FC2FD8E502D0F4F285D750D83E51D13AB0DB043C68F7267B51CBF8F70ECC40896DC8CBE72
<3519:3200>	F95FC9B807959988ABB99CD56F5F37EFB6EC4E58D4BEB0FF21F679F490F9DD635A10C7B3FC2D5A52
<3199:2880>	56CFB4E62BB695B79D1BA97F4050533DD2C9BEAB1F1C1653FF6E99AC88A3FDE99B4FB1F3F6C82945
<2879:2560>	F7BE0EFB07B9C6CACB8F9096B308258EF228B01FF7AFCBA189D2C7E71EED3F207F163B58EEC0C02E
<2559:2240>	A8EEB169DD65CF86F319B82E36DAC8D8E09077DCA3009AC4A7569FFE11A96F735ED0F685E96028CE
<2239:1920>	E8265F8CDA9A39540A509936869A2A8267CE3ABC560BD80F08CBB0415749FACB149C42AFE68EBE9B
<1919:1600>	135A6E02C0AA5807906AE384CB74F99F6CB700FA5480D25D52D208FBC295570F642C546E2685255A
<1599:1280>	0FBFFD27F056F2A147C33B6F561BB1DF9B994E0351D95C8F9B7D104470FF3463815D28A958106069
<1279:960>	9B3324B302D6AC9DB6B2A10823B86055E0BACC50F6F847E434C7414E0DCD0D206DA50E4D75DB65E3
<959:640>	2EE470AD0DE1092E04A8812B44A3DB0E7A77A9DCC7194FEA0DA61C433F4435891EE97DBE750C8D16
<639:320>	51543380F0881388B114962019A6962D0D13FC4552E1D6EE5CD6A408EAF6237F5FECD980292CD9C8
<319:0>	4FC29**D9798C2C55370750272E393736FF6D38A3DF36A7A93002B47850A96CDE76854DA59062AD1B3**

Table 172A–4—RS(544,514) codeword B for 800GBASE-R flow 0

Index <*i*:*j*>	cx_B<*i*:*j*>
<5439:5120>	A6A9AA6A9AA6A9AA6A9A6499264992649926499264992109A2C8A22ACAC250B426599565D946559765197
<5119:4800>	6D5B56D5B56D5B56D5B59DBB69DBB6FD936BD87695B98B52933A9D73B19571FCF51E72733ADF67EC
<4799:4480>	1FBD07455B4F238F0D7912780AE4841617E2A693857F8C049DEDD92A0C5A0CAA40D9798A89C6A164
<4479:4160>	621AAEC9A824EC9203458118BB4F4402C1635209D83314CA401576CEEBA30193FFAE9EAE9B4FEB74
<4159:3840>	940447D476FAE46BA3D97965681352E5E1087DED3CC7100984C74C2FBEA631DA8335E5832CEDFCE4
<3839:3520>	3F1ADD1FE9B232567A2041A7782A7AA62A1348F6C874FEB76F8145CB65AF1ED61554AE7CA3EF4B63
<3519:3200>	999453AC3B093278719A71F4AE09D404C0A9F0014F09F279005A3A7FD289C4EB9B2C98F2C1EB0EFD
<3199:2880>	599CE431BEFD79C6542F4B572684F2A32D19EBCB2267BAD81FF1BA2F93274686A4F37361176C78DA
<2879:2560>	749AAB7CA1415E7EA8BD6B3B4026B13A65AF6317DEA7DDE1E0C8B2EBA5412FD1A83DA29055292039
<2559:2240>	5C08E6DB1B3EEE0EEECED94892079D98BEE35A6F6410294FE5866667D64598E5F680B711C33C3A08
<2239:1920>	E2FC9D1E0693FD2E999AC9C24FD4DBFCC90338B490C6AC33A5A8111EE5E0A631E0D229F75199927B
<1919:1600>	1D0A36924C20B4F749870EAB79F355A4E35A72BE70FF713A8B76B5693CDDFC9FD73802E6072736DF
<1599:1280>	7EADC1281094A1A8B599A41478B9075190836BD54BCA458B19862D4729EC9418414E51D233C8FC4C
<1279:960>	F41597EE58EAF5250E435D7710ABE4B27F820C4EEFFE7B331C27F3D623B942CBE1AC1E46815EDB4C
<959:640>	B784B2F192531E6308A04606029071929114E71AB62C36A9D71958111ED9D0D7D45D8E353823A7F4
<639:320>	E53C08DE057AD8F1D0BD114438370C05B05422875160140E51C056BC5075F5CFFBDBF211044D7A33
<319:0>	EFBCE**3BC2198756E3F23CE3783B4D1085B12943E924B87EF67FED64D92E66AE99B5E579C0F8B1BCB**

Table 172A–5—RS(544,514) codeword A for 800GBASE-R PCS flow 1

Index <*i*:*j*>	cx_A<*i*:*j*>
<5439:5120>	A6A9AA6A9AA6A9AA6A9A6499264992649926499264992D886284BD280BA2609026519565D946559565196
<5119:4800>	6D5B56D5B56D5B56D5B57D936ED8B62D876CD9B6077EFA842E86550894AB215FEB02273B66468116
<4799:4480>	831A98355E22B271AA5959A5EDB273E5F63E326AC7F3C475CBCC6B6D97B37EF42D156D3CCE1C39E6
<4479:4160>	401C8F61447E7EDCC8C3859D481E6F5DA7648166C37FB37C3EE4B28719774A5CA6C6AF6A8BB5FA37
<4159:3840>	E4544116469CC326A38AF61AF7FB21A50EF20AD25E949C26FA35DBF354F40144F4FC262325C13C0D
<3839:3520>	AC015D6EA6EAE85DF128C7F4BD15625C360F80EC0A18E4BDCD612ADAC6C73CDCF321DB85DDF1F66A
<3519:3200>	D27244FA401226FED3C5D040F547D72AFBF284F5EFE5178BC75679B5765BD227A0C9EFE1DFB2E21C
<3199:2880>	88B272591BFE8A82EFAA9DCFBB46E0D5AC404CB7EE3507C446CB25FE1EE45519344E9CBB40AF40BE
<2879:2560>	FAB6B3694F1DF911A1D5341F0C77CCBCA21AC8AC7448270F35D07EADB725531491BCF0D9763E0668
<2559:2240>	C612485954D0A2FFD0C7DC69E6249258C2BE2C4D73E247D1619CDCD5857AB0CE58FFC109A6FF7D3E
<2239:1920>	1D2685D529483C9369ACE7FE0A91106A921645FAE0199EFA2C2E7F935DD2656DCAF9EBFA25ADBAD7
<1919:1600>	486B0494108FB4106F2F307912AFC4AC7C85A4485187EAC46E11C980E15D4F7A0324E7630415FF43
<1599:1280>	2BDFE61FD4EF38B8AE2A3E09F7D981B73BD43969DA3F7FBA21C28EA837B7C8B58DF1645A06D7B66C
<1279:960>	3B74D3B69D695761D5D2B9CF4C1F43EFA6043FDFC7FAC5E211D5C268BCC6BB8E8519CFA66B64FFFD
<959:640>	8C8B1FA0D47618EB66B1BBCEEB6DCCD59503627C0E208A010A70B19E8CFCF5D96B503E03EAA82156
<639:320>	EB829E17FFF236646D41150E6DEB666116DC6CD7F58AD747A3B0DA5A2462CB69323882F8C62F47C8
<319:0>	7C110**1E2E9D7DE149660AA91354E2A473CF6434EB00C349782F3FF0E85F3DDEDEF69F4DBED4633BD**

Table 172A–6—RS(544,514) codeword B for 800GBASE-R PCS flow 1

Index <*i*:*j*>	cx_B<*i*:*j*>
<5439:5120>	A6A9AA6A9AA6A9AA6A9A6499264992649926499264992109A2C8A22ACAC250B426599565D946559765197
<5119:4800>	6D5B56D5B56D5B56D5B59DBB69DBB6FD936BD8766986849163C6A27C72658E030AE18D8CC5209813
<4799:4480>	2072F4B9A470EC7CF186E24405E744E62BEDA5537A8073FB621226D5F3A5F355BF26867576395E9B
<4479:4160>	621AAEC9A824EC9F024773AD49DB1923A11A072B72D35CBFE8B6B3F65D29011F1520F9F632F74A61
<4159:3840>	788445A59A69497ED2227FFFC9DE81710E590B03D83115C1D05F0B472905722F0E880A9B6E24D3EA
<3839:3520>	748B884C2889C90065C10A2E65947942E7B26D7F4CC993180051531A8BC98744C3FFA19B0D3379F2
<3519:3200>	56CCE74431B6C6CD8780EAE188C8E6A7EFF1D8D8213715D09919911C5591B3B0D78F350C9027538D
<3199:2880>	AA9B36DB732DED4A1F5BBD90C2453B42F79B2FFE2EE4D28B08707AC888A1BE8D8CB5D2A81A209279
<2879:2560>	1EB3528E842706A7BD1DBB5F57064167550179CF9EEF0139E666BE06D188C89A9FCF1CA4F72A381D
<2559:2240>	26CAD128708342A46816A1D4DF18072C0F256555643FCE759AD072A31AB56A56B9E7DF1987131121
<2239:1920>	DFAAF7DF88D38B9D146FE32E63759035CFF03B4A4E3A59389CFCADDB7952B601E0E0B906F5208FAF
<1919:1600>	314D86265D6294C14BC45E8F6D3325A6F4121306649AD820B29BCDB86EF6CEEFD083B0EBED0CEA83
<1599:1280>	0A54FED0AD524BBA3D0F9A624DDE884C89980D0049D78B4FF5ADC4EE988AB03ACD096152860BCB62
<1279:960>	187FDFA2E642E894F1064F0CCF7E28372E3BEB46315FDECCCFE9B8BB812CA4A2EC09B042918754CE
<959:640>	6B112395E20D8C818C69C0F2CA6D51A180E05CA6023560B5A930EDF02E5FECB2D93B9A7B15EBC2D4
<639:320>	4BDD608BA0D92D8569B541D8C3BABB85366192367AE021E27BEF020103FF4BDEFDA3C4F3D386586F
<319:0>	61452**68031843B34748CF604A47A190AAF03AEB9CC367B9364FAEC90878D81980D1B802A4F52995A**

Insert new annex Annex 173A corresponding to Clause 173 as follows:

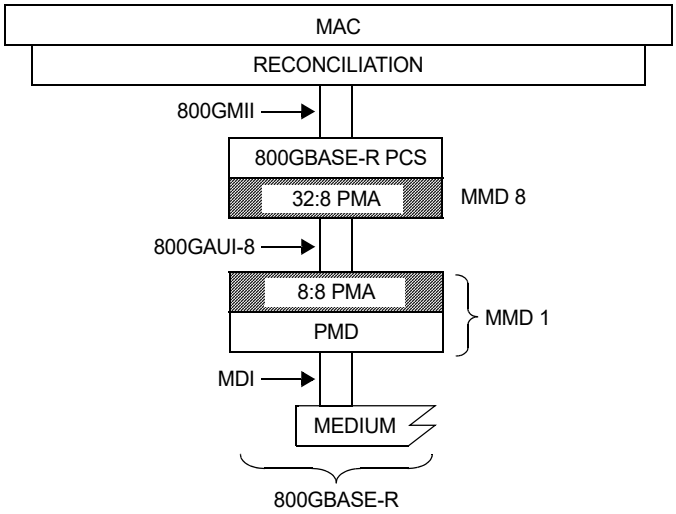
Annex 173A

(informative)

800 Gb/s PMA sublayer partitioning examples

This annex provides various partitioning examples. Partitioning guidelines and MMD numbering conventions are described in 173.1.4.

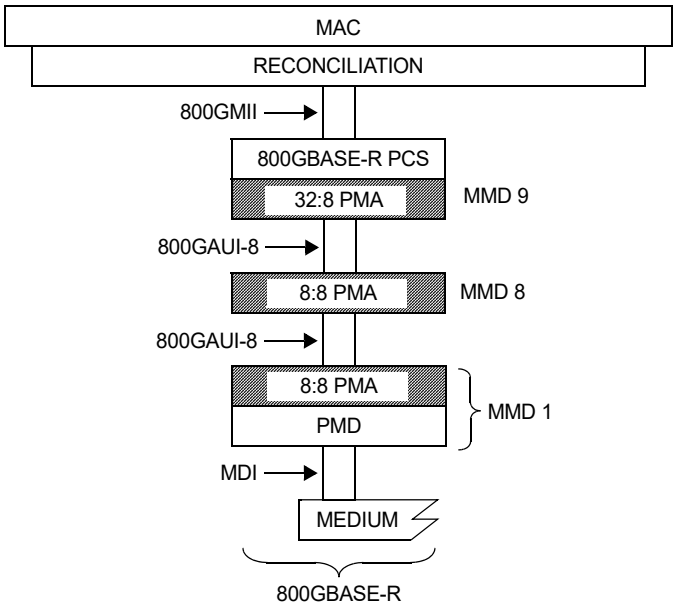
Figure 173A–1 depicts an example of PMA layering with an eight-lane PMD and one 800GAUI-8.



800GAUI = 800 Gb/s ATTACHMENT UNIT INTERFACE
800GMII = 800 Gb/s MEDIA INDEPENDENT INTERFACE
MAC = MEDIA ACCESS CONTROL
MDI = MEDIUM DEPENDENT INTERFACE
MMD = MDIO MANAGEABLE DEVICE
PCS = PHYSICAL CODING SUBLAYER
PHY = PHYSICAL LAYER DEVICE
PMA = PHYSICAL MEDIUM ATTACHMENT
PMD = PHYSICAL MEDIUM DEPENDENT

Figure 173A–1—Example PMA layering with eight-lane PMD and single 800GAUI-8

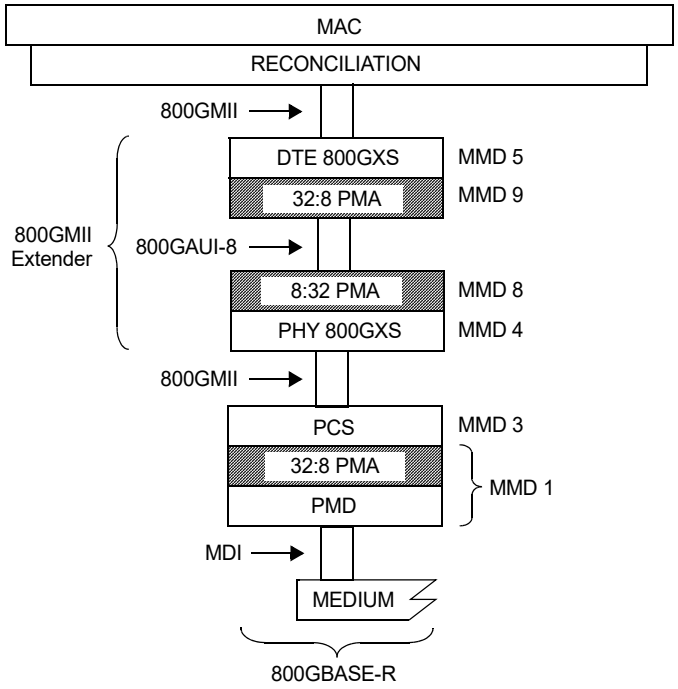
Figure 173A–2 depicts an example of PMA layering with an eight-lane PMD and two 800GAUI-8.



800GAUI = 800 Gb/s ATTACHMENT UNIT INTERFACE
800GMII = 800 Gb/s MEDIA INDEPENDENT INTERFACE
MAC = MEDIA ACCESS CONTROL
MDI = MEDIUM DEPENDENT INTERFACE
MMD = MDIO MANAGEABLE DEVICE
PCS = PHYSICAL CODING SUBLAYER
PHY = PHYSICAL LAYER DEVICE
PMA = PHYSICAL MEDIUM ATTACHMENT
PMD = PHYSICAL MEDIUM DEPENDENT

Figure 173A–2—Example PMA layering with an eight-lane PMD and two 800GAUI-8

Figure 173A–3 depicts an example of PMA layering with an eight-lane PMD, 800GMII Extender, and one 800GAUI-8.



800GAUI = 800 Gb/s ATTACHMENT UNIT INTERFACE
800GMII = 800 Gb/s MEDIA INDEPENDENT INTERFACE
800GXS = 800GMII EXTENDER SUBLAYER
DTE = DATA TERMINAL EQUIPMENT
MAC = MEDIA ACCESS CONTROL
MDI = MEDIUM DEPENDENT INTERFACE
MMD = MDIO MANAGEABLE DEVICE
PCS = PHYSICAL CODING SUBLAYER
PHY = PHYSICAL LAYER DEVICE
PMA = PHYSICAL MEDIUM ATTACHMENT
PMD = PHYSICAL MEDIUM DEPENDENT

Figure 173A–3—Example PMA layering with an eight-lane PMD, 800GMII Extender, and one 800GAUI-8

Figure 173A–4 depicts two examples of PMA layering with an eight-lane PMD, 800GMII Extender, and two 800GAUI-8.

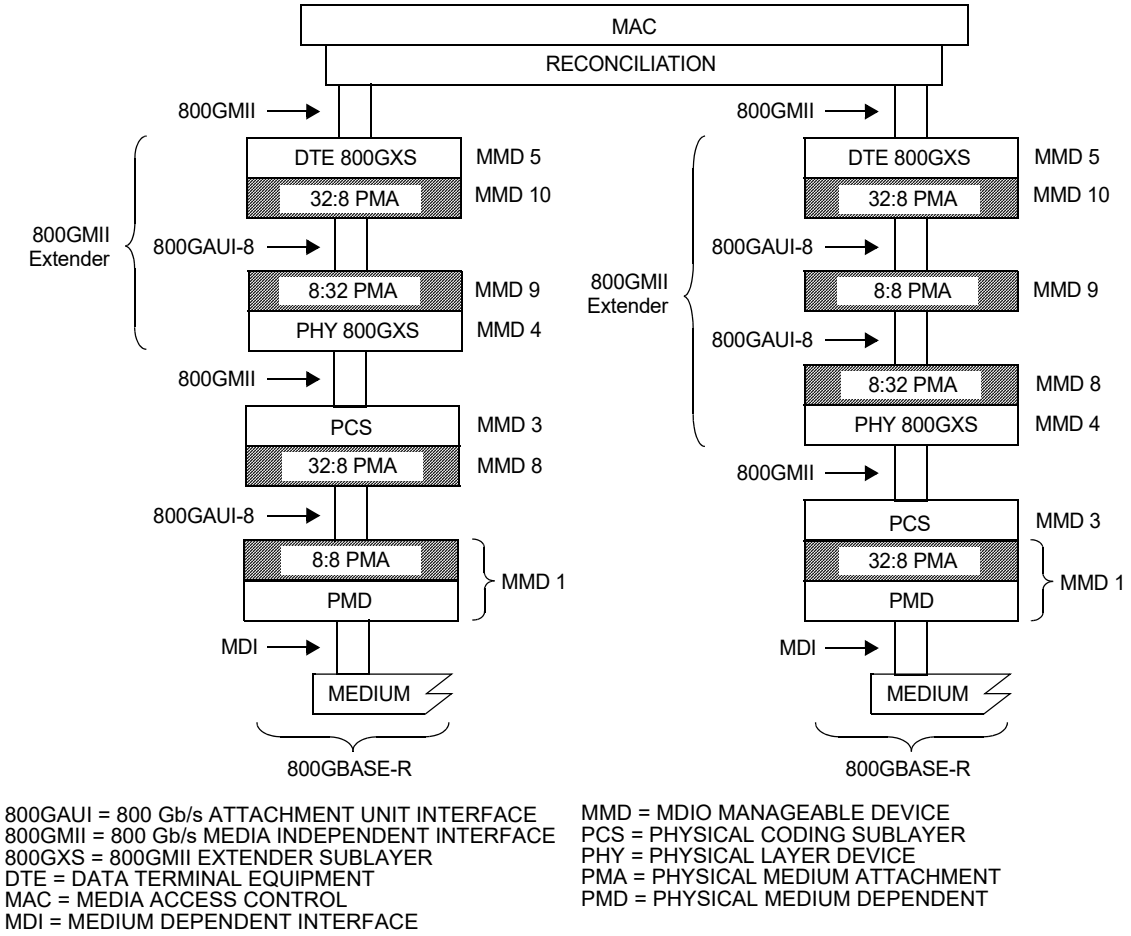


Figure 173A–4—Example PMA layering with an eight-lane PMD, 800GMII Extender, and two 800GAUI-8

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