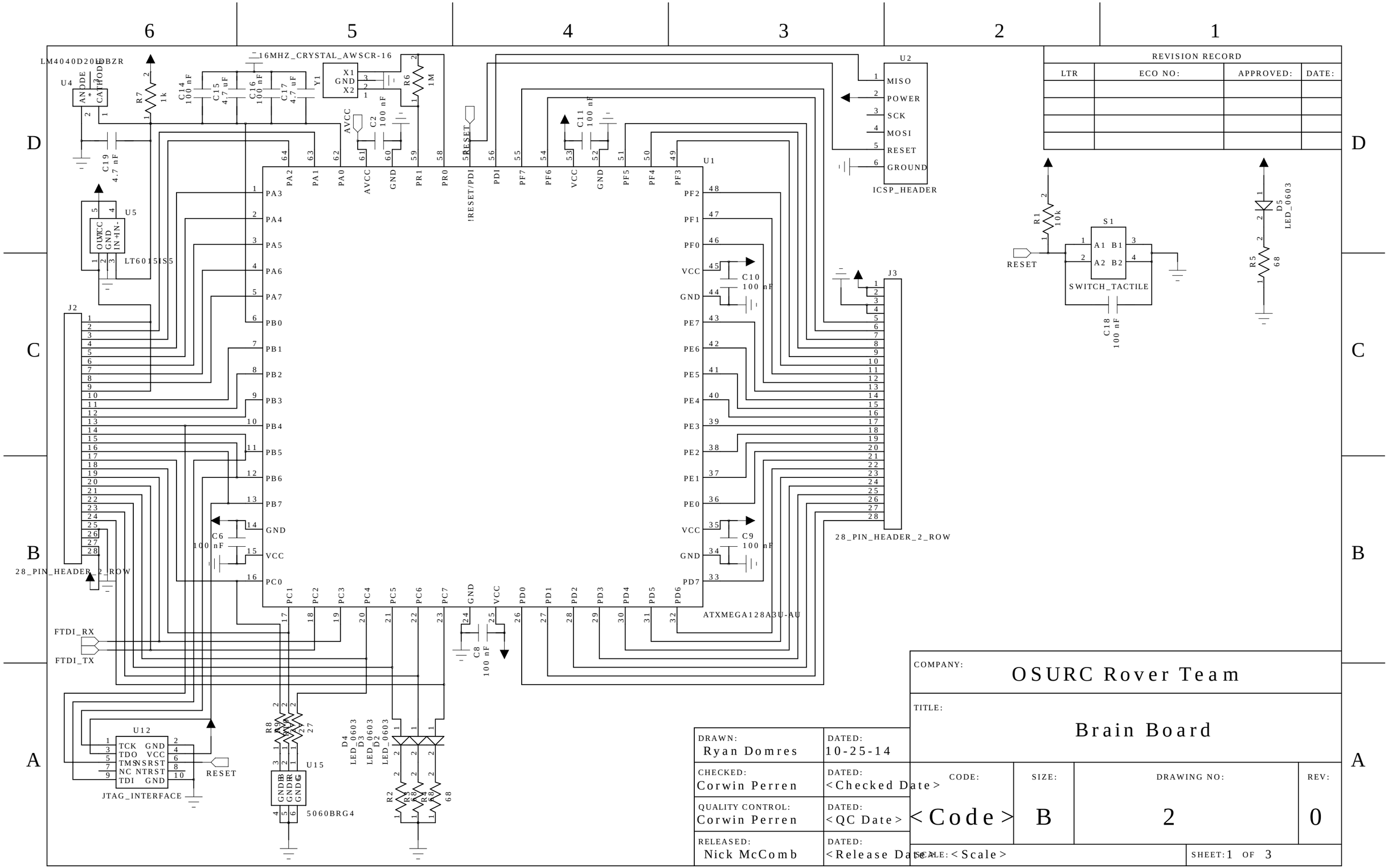
6
5
4
3
2
1
D
C
B
A
LM4040D20IDBZR
U4
ANODE
CATHODE
R7
1k
C14
100 nF
C15
4.7 uF
C16
100 nF
C17
4.7 uF
16MHZ_CRYSTAL_AWSCR-16
Y1
X1
GND
X2
R6
1M
C19
4.7 nF
U5
OUT
VCC
GND
IN+
IN-
LT6015IS5
AVCC
C2
100 nF
!RESET
C11
100 nF
U2
MISO
POWER
SCK
MOSI
RESET
GROUND
ICSP_HEADER
U1
PA2
PA1
PA0
AVCC
GND
PR1
PR0
!RESET/PDI
PDI
PF7
PF6
VCC
GND
PF5
PF4
PF3
PA3
PA4
PA5
PA6
PA7
PB0
PB1
PB2
PB3
PB4
PB5
PB6
PB7
GND
VCC
PC0
PF2
PF1
PF0
VCC
GND
PE7
PE6
PE5
PE4
PE3
PE2
PE1
PE0
VCC
GND
PD7
C10
100 nF
C9
100 nF
C6
100 nF
J2
28_PIN_HEADER_2_ROW
J3
28_PIN_HEADER_2_ROW
PC1
PC2
PC3
PC4
PC5
PC6
PC7
GND
VCC
PD0
PD1
PD2
PD3
PD4
PD5
PD6
ATXMEGA128A3U-AU
C8
100 nF
FTDI_RX
FTDI_TX
U12
TCK
TDO
TMS
NC
TDI
GND
VCC
SRST
NTRST
GND
JTAG_INTERFACE
RESET
R8
R9
R10
R11
27
U15
GND
GND
GND
5060BRG4
D4
LED_0603
D3
LED_0603
D2
LED_0603
R2
R3
R4
R5
68
R1
10k
RESET
S1
A1
B1
A2
B2
SWITCH_TACTILE
C18
100 nF
D5
LED_0603
R5
68
REVISION RECORD
LTR
ECO NO:
APPROVED:
DATE:
DRAWN:
Ryan Domres
DATED:
10-25-14
CHECKED:
Corwin Perren
DATED:
<Checked Date>
QUALITY CONTROL:
Corwin Perren
DATED:
<QC Date>
RELEASED:
Nick McComb
DATED:
<Release Date>
COMPANY:
OSURC Rover Team
TITLE:
Brain Board
CODE:
<Code>
SIZE:
B
DRAWING NO:
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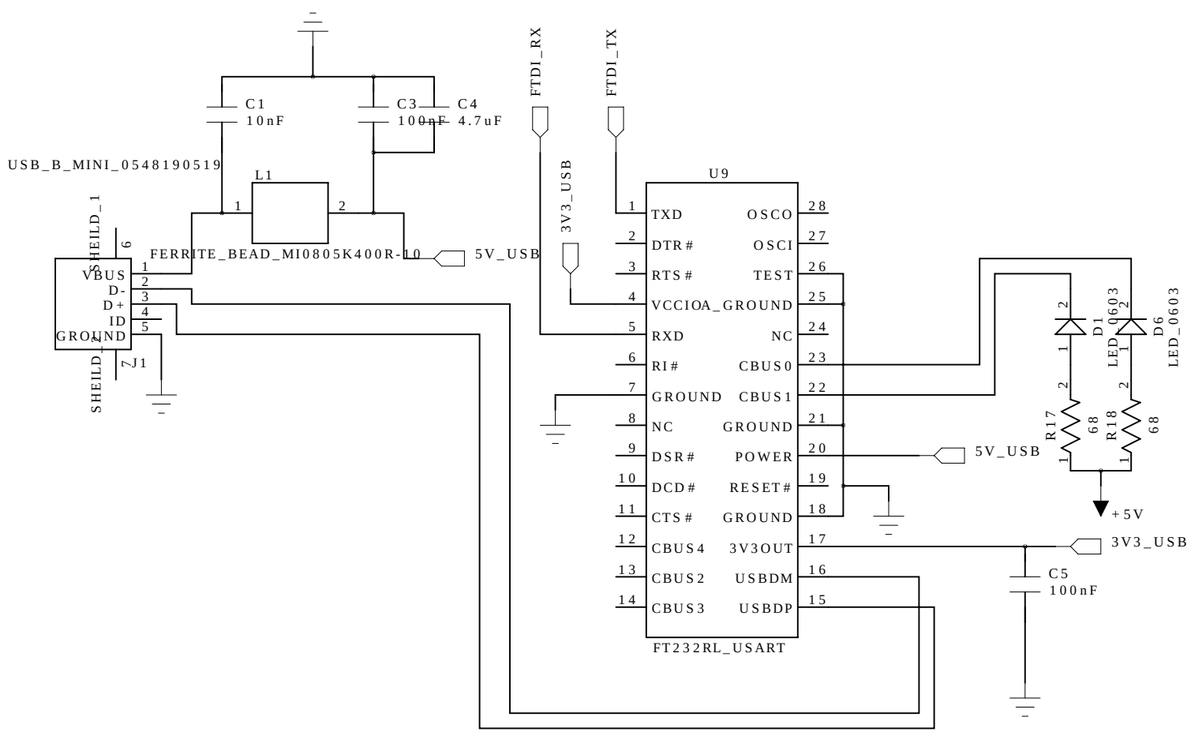
REV:
0
SCALE: <Scale>
SHEET: 1 OF 3

REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:



COMPANY: OSURC Rover Team			
TITLE: Brain Board			
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SCALE: <Scale>		SHEET: 2 OF 3	

DRAWN: Ryan Domres	DATED: 10-25-14
CHECKED: Corwin Perren	DATED: <Checked Date>
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RELEASED: Nick McComb	DATED: <Release Date>

REVISION RECORD			
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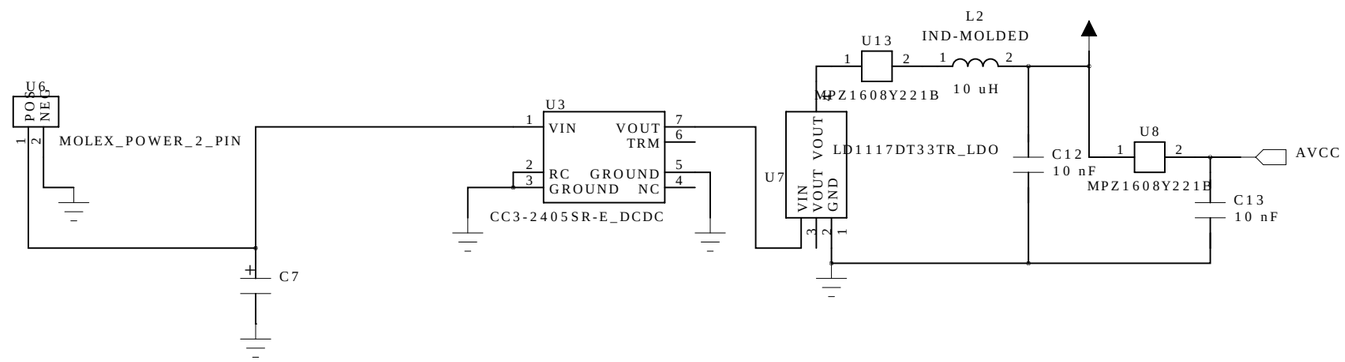

DRAWN: Ryan Domres	DATED: 10-25-14	COMPANY: OSURC Rover Team	
CHECKED: Corwin Perren	DATED: <Checked Date>	TITLE: Brain Board	
QUALITY CONTROL: Corwin Perren	DATED: <QC Date>	CODE: <Code>	SIZE: B
RELEASED: Nick McComb	DATED: <Release Date>	DRAWING NO: 2	REV: 0
		SCALE: <Scale>	SHEET: 3 OF 3