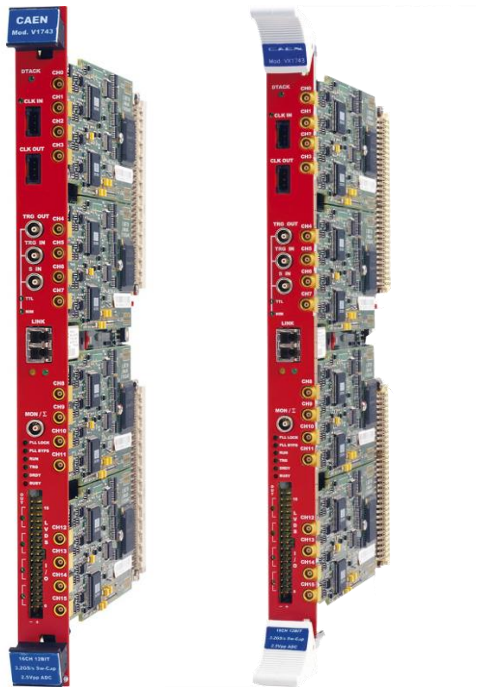
CAEN
Tools for Discovery

Electronic Instrumentation



User Manual UM2750

V1743 & VX1743

16 Channel 12bit 3.2 GS/s Switched Capacitor Digitizer

Rev. 0 - 06 March 2015

Purpose of this Manual

This User Manual contains the full description of the V1743 and VX1743 Digitizers.
For any reference to registers in this user manual, please refer to document [RD2] at the digitizer web page.

Change Document Record

Date	Revision	Changes
06 March 2015	00	Initial release

Symbols, abbreviated terms and notation

DLL	Delay Line Loop
INL	Integral Non Linearity
LVDS	Low Voltage Digital Signal
PLL	Phase-Locked Loop
TDC	Time to Digital Converter
USB	Universal Serial Bus

Reference Documents

[RD1] GD2512 – CAENUpgrader QuickStart Guide

[RD2] V1743 Registers Description

[RD3] AN2086 – Synchronization of a multi-board acquisition system with CAEN digitizers

[RD4] UM1935 - CAENDigitizer User & Reference Manual

[RD5] UM1934 - CAENComm User & Reference Manual

[RD6] UM2754 - WaveCatcher User Manual

All documents can be downloaded at: http://www.caen.it/csite/LibrarySearch.jsp

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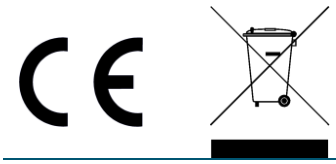

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Safety Notices

CAUTION: this product needs proper cooling.

USE ONLY CRATES WITH FORCED COOLING AIR FLOW SINCE OVERHEAT MAY DEGRADE THE MODULE PERFORMANCES!

V1743/VX1743 CANNOT BE OPERATED WITH CAEN CRATES VME8001/8002/8004!

CAUTION: this product needs proper handling.

ALL CABLES MUST BE REMOVED FROM THE FRONT PANEL BEFORE EXTRACTING THE BOARD FROM THE CRATE!

1 Introduction

The Mod. V1743 is a VME 6U module housing a 16-channel, 12-bit, 3.2 GS/s Switched Capacitor Digitizer, issued from the collaboration with CEA/IRFU & CNRS/IN2P3/LAL and based on the SAMLONG chip.

The input dynamic range is 2.5 V_{pp} (DC coupled) on single ended MCX coaxial connectors. The DC offset is adjustable in the ±1.25 V range via a 16-bit DAC on each channel (see § **Analog Input Stage**).

Considering the sampling frequency and the number of bits, it is well suited for very fast signals like those coming from fast scintillators coupled to PMTs, Silicon Photomultipliers, APD, Diamond detectors and others.

The analog input signals are continuously sampled inside the SAMLONG chips in a circular analog memory buffer (1024 cells) at the default sampling frequency of 3.2 GS/s (312.5 ps of sampling period); frequencies of 1.6 GS/s, 0.8 and 0.4 GS/s are also software selectable. As a trigger signal arrives, all analog memory buffers are frozen and subsequently digitized with a resolution of 12 bits into a digital memory buffer with independent read and write access. Up to 7 full events per channel (1 event = 1024 * 12 bits) can be stored consecutively.

Each input channel is equipped with a discriminator with a 16-bit programmable threshold, which generates trigger requests. Requests from all channels are processed by the board to generate a common trigger causing all the channels to acquire an event simultaneously. The common board trigger can also be provided externally by software command, or by the front panel TRG-IN input, or by any combination of the channel discriminators and/or the TRG-IN.

During analog to digital conversion process, the V1743 cannot handle other triggers, thus generating a Dead Time (maximum 125 µs, decreasing proportionally with the recording depth thanks to the configurable record length).

Each input channel is equipped with an individual hit rate monitor based on its own discriminator and on two counters giving the number of hits which cross the programmed discriminator threshold (also during the Dead Time) and the time elapsed with a 1-MHz clock (see § **Hit Rate Monitor**). This permits among others measuring the hit rate with respect to the signal amplitude.

Each input channel is equipped with a digital programmable charge integrator which permits a high rate measurement in charge mode (see § **Running in Charge Mode**).

Each pair of channels is equipped with a 40-bit TDC (counter) tagging the trigger with the clock delivered to the SAMLONG chips (200 MHz down to 25 MHz depending on the selected sampling frequency).

V1743 houses a fixed amplitude pulser on each analog input, which permits an easy complete functionality test and the use of the module in reflectometer mode (see § **Test Pattern Pulser**).

The module features a front panel CLK-IN connector as well as an internal PLL for clock synthesis from internal/external references. Multi-board synchronization is supported, so all SAMLONG chips can be synchronized with a common clock source and ensuring Trigger Time Stamps alignment (*please, contact CAEN for details*). Once synchronized, all data will be aligned and coherent between multiple V1743 boards. CLK-IN / CLK-OUT connectors allow for a Daisy-chained clock distribution.

16 general purpose LVDS I/Os also FPGA-controlled can be programmed for Busy, Data Ready, Memory Full or Individual Trig-Out management. An Input Pattern (external signal) can be provided on the LVDS I/Os to be latched to each trigger as an event marker (see § **Front Panel LVDS I/Os**).

An analog output (MON/Σ) from internal 12-bit 100-MHz DAC controlled by the FPGA allows to provide out four types of information: Trigger Majority, Test Pulses, Memory Occupancy, Voltage Level (see § **Analog Monitor**).

V1743 is equipped with a VME64 interface (VM64X in case of VX1743) where the data readout can be performed in Single Data Transfer (D32), 32/64-bit Block Transfer (BLT, MBLT, 2eVME. 2eSST) and 32/64-bit Chained Block Transfer (CBLT).

The module houses Optical Link interface supporting transfer rate of 80 MB/s and offers Daisy chain capability. Therefore, it is possible to connect up to 8 ADC modules to a single A2818 Optical Link Controller, or up to 32 using a A3818 (4-link version).

Board Models	Description	Product Code
V1743	V1743 - 16 Ch. 12 bit 3.2GS/s Switched-Capacitor Digitizer: 7 events/ch (1kS/event), EP3C16, SE	WV1743XAAAAA
VX1743	VX1743 - 16 Ch. 12 bit 3.2GS/s Switched-Capacitor Digitizer: 3 events/ch (1kS/event), EP3C16, SE	WVX1743XAAAA
Related Products	**Description**	**Product Code**
A2818	A2818 – PCI Optical Link (Rhos compliant)	WA2818XAAAAA
A3818A	A3818A – PCIe 1 Optical Link	WA3818AXAAAA
A3818B	A3818B – PCIe 2 Optical Link	WA3818BXAAAA
A3818C	A3818C – PCIe 4 Optical Link	WA3818CXAAAA
V1718	V1718 - VME-USB 2.0 Bridge	WV1718XAAAAA
V1718LC	V1718LC - VME-USB 2.0 Bridge (Rohs Compliant)	WV1718LCXAAA
VX1718	VX1718 - VME-USB 2.0 Bridge	WVX1718XAAAA
VX1718LC	VX1718LC - VME-USB 2.0 Bridge (Rohs Compliant)	WV1718LCXAAA
V2718	V2718 - VME-PCI Bridge	WV2718XAAAAA
V2718LC	V2718LC - VME-PCI Bridge (Rohs compliant)	WV2718LCXAAA
VX2718	VX2718 - VME-PCI Bridge	WVX2718XAAAA
VX2718LC	VX2718LC - VME-PCI Bridge	WVX2718LCXAA
V2718LC KIT	V2718KITLC - VME-PCI Bridge (V2718)+PCI Optical Link (A2818)+Optical Fibre 5m duplex (AY2705) (Rohs)	WK2718LCXAAA
V2718 KIT	V2718KIT - VME-PCI Bridge (V2718) + PCI OpticalLink (A2818) + Optical Fibre 5m duplex (AY2705)	WK2718XAAAAA
V2718 KIT-B	V2718KITB - VME-PCI Bridge (V2718) + PCIe Optical Link (A3818A) + Optical Fibre 5m duplex (AY2705)	WK2718XBAAAA
VX2718LC KIT	VX2718KITLC - VME-PCI Bridge (VX2718)+PCI Optical Link (A2818)+Optical Fibre 5m duplex (AY2705) (Rohs)	WKX2718LCXAA
VX2718 KIT	VX2718KIT - VME-PCI Bridge (VX2718) + PCI OpticalLink (A2818) + Optical Fibre 5m duplex (AY2705)	WKX2718XAAAA
VX2718 KIT-B	VX2718KITB - VME-PCI Bridge (VX2718) + PCIe Optical Link (A3818A) + Optical Fibre 5m duplex (AY2705)	WKX2718XBAAA
Accessories	**Description**	**Product Code**
A317	Clock Distribution Cable	WA317XAAAAAA
A654	Single Channel MCX to LEMO Cable Adapter	WA654XAAAAAA
A654 KIT4	4 MCX TO LEMO Cable Adapter	WA654K4AAAAA
A654 KIT8	8 MCX TO LEMO Cable Adapter	WA654K8AAAAA
A659	A659 - Single Channel MCX to BNC Cable Adapter	WA659XAAAAAA
A659 KIT4	4 MCX TO BNC Cable Adapter	WA659K4AAAAA
A659 KIT8	8 MCX TO BNC Cable Adapter	WA659K8AAAAA
AI2730	Optical Fibre 30 m simplex	WAI2730XAAAA
AI2720	Optical Fibre 20 m simplex	WAI2720XAAAA
AI2705	Optical Fibre 5 m simplex	WAI2705XAAAA
AI2703	Optical Fibre 30 cm simplex	WAI2703XAAAA
AY2730	Optical Fibre 30 m duplex	WAY2730XAAAA
AY2720	Optical Fibre 20 m duplex	WAY2720XAAAA
AY2705	Optical Fibre 5 m duplex	WAY2705XAAAA

Tab. 1.1: Table of models and related items

2 Block Diagram

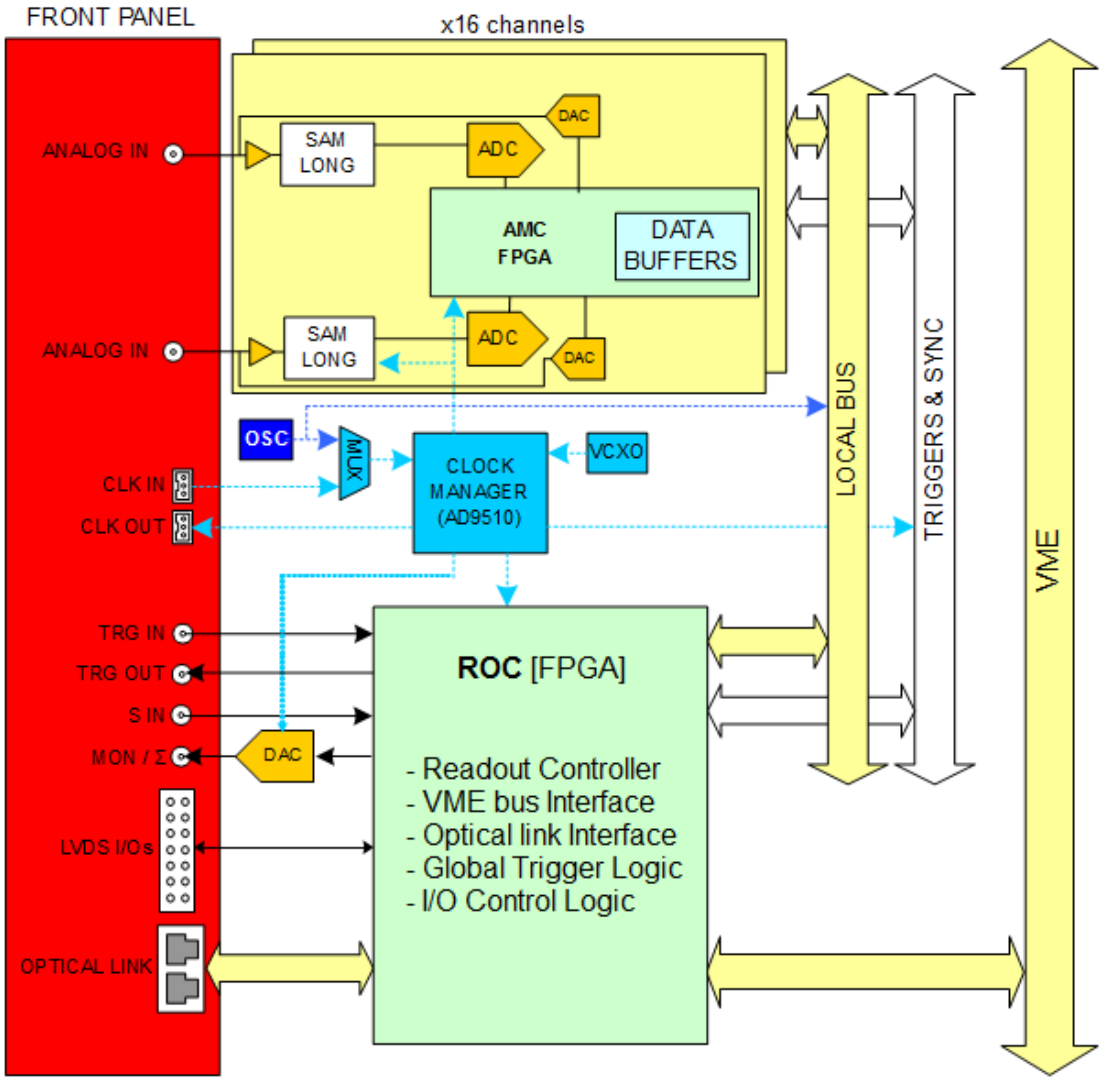


Fig. 2.1: Block Diagram

3 Technical Specifications

GENERAL	**Form Factor** 1-unit wide, 6U VME64 (V1743) and VME64X (VX1743)		
ANALOG INPUT	**Channels** 16 channels Single ended **Impedance** Zin: 50 Ω	**Connector** MCX **Full Scale Range** 2.5 Vpp DC coupled	**Bandwidth** 500 MHz **Offset** Programmable 16-bit DAC for DC offset adjustment on each channel. Range: ±1.25 V
TEST FUNCTIONALITY	One pulser per channel with programmable 16-bit pattern (fixed amplitude)		
DIGITAL CONVERSION	**Analog Memory (Switched Capacitor Array)** SAMLONG Fast Analog Memory chip 2 channels, 1024 storage cells/ch 320 ns minimum recorded time/event **Sampling Rate** 3.2/1.6 /0.8/0.4 GS/s SW selectable	**Dead Time (Event A/D Conversion)** 125 µs (max. @ 1024 samples) **Note:** value decreasing proportionally with the depth recording (configurable record length) **Resolution** 12 bits	
TIMING RESOLUTION	< 20 ps RMS before time calibration < 5 ps RMS after time calibration **Note:** obtained with factory calibration and dual-pulse timing measurement with pulse generator. Test conditions: periodic input pulses with 1V Amplitude, 1kHz Frequency, rise time of 0.8 / 1.6 / 2.5 ns. The resolution does not change significantly when varying the delay Δt between the two pulses		
NOISE LEVEL	0.75 mV RMS		
CLOCK GENERATION	Synchronization clock source: internal/external On-board PLL provides generation of the main board clocks from an internal (50 MHz loc. oscillator) or external (front panel CLK-IN connector) reference		
DIGITAL I/O	**CLK-IN (AMP Modu II)** AC coupled differential input clock LVDS, ECL, PECL, LVPECL, CML (single ended NIM/TTL available) Jitter<100ppm requested **TRG-IN (LEMO)** External trigger digital input NIM/TTL, Zin = 50 Ω	**CLK-OUT (AMP Modu II)** DC coupled differential LVDS clock output locked at ADC sampling clock (Freq.: 500 MHz) **TRG-OUT (LEMO)** Trigger digital output NIM/TTL, Rt = 50 Ω	**S-IN (LEMO)** SYNC/START front panel digital input, NIM/TTL, Zin = 50 Ω
DIGITAL MEMORY	7 event/ch Multi-Event Buffer (1024 samples per event)		
TRIGGER	**TRG-IN (LEMO)** External trigger digital input NIM/TTL, Zin = 50 Ω	**TRG-OUT (LEMO)** Trigger digital output NIM/TTL, Rt = 50 Ω	
SYNCHRONIZATION	**Clock Propagation** • *Daisy chain*: through CLK-IN/CLK-OUT connectors (AC coupled differential input clock: LVDS, ECL, PECL, LVPECL, CML on AMP MODU II connector) • *One-to-many*: clock distribution from an external clock source on CLK-IN connector Clock Cable delay compensation	**Acquisition Synchronization** • Sync Start/Stop through TRG-IN or S-IN input, TRG-OUT output • External Trigger Time Stamp reset **Trigger Time Stamps Alignment** By S-IN input connector	
ADC & MEMORY CONTR.	Altera Cyclone EP3C16 (1 FPGA serves 4 channels)		
COMMUNICATION INTERFACE	**Optical Link** CAEN CONET proprietary protocol Up to 80 MB/s transfer rate Daisy chainable: it is possible to connect up to to 8 or 32 ADC modules to a single Optical Link Controller (respectively A2818 or A3818)	**VME** VME 64X compliant Data transfer mode: BLT32, MBLT64 (70 MB/s using CAEN Bridge), CBLT32/64, 2eVME, 2eSST (up to 200 MB/s)	
ANALOG MONITOR	12-bit / 125MHz DAC FPGA controlled; four operating modes: - Test pulses: 1Vpp ramp generator - Majority signal: proportional to the nr. of channels under/over threshold (steps of 125 mV) - Memory Occupancy signal: proportional to the Multi Event Buffer Occupancy (1 buffer ~ 1mV) - Voltage level: programmable output voltage level.		
LVDS I/O	16 general purpose LVDS I/O controlled by the FPGA: Busy, Data Ready, Memory full, Individual Trig-Out and other functions can be programmed. An Input Pattern from the LVDS I/O can be associated to each trigger as an event marker		

DIGITAL PULSE PROCESSING	Software selectable embedded Charge Mode for input pulse high rate charge integration and fast histogramming		
FIRMWARE UPGRADE	Firmware can be upgraded via VME*bus*/Optical Link		
SOFTWARE	General purpose C libraries and configuration tools(Windows and Linux support); WaveCatcher readout software (Windows only)		
POWER CONSUMPTIONS	@ +5V	@ +12 V *(Not used)*	@ -12V
	5 A (max.)	-	1 A (max.)

Tab. 3.1: Specifications table

4 Packaging and Compliancy

The module is a 1-unit wide, 6U VME64/VME64X board.

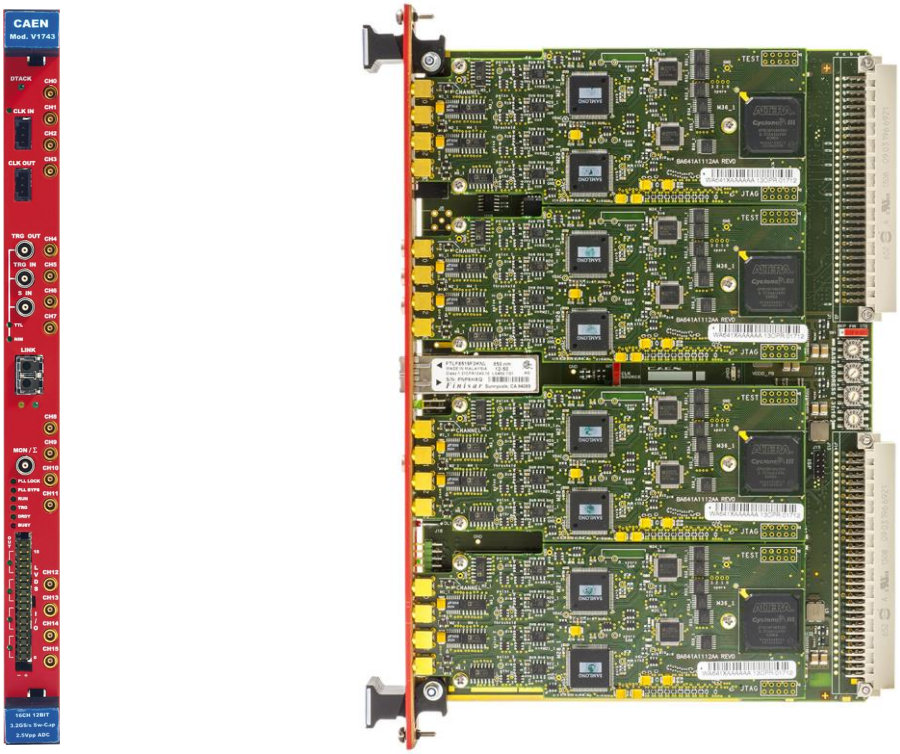


Fig. 4.1: V1743 view

CAUTION: to manage the product, consult the operating instructions provided.

A POTENTIAL RISK EXISTS IF THE OPERATING INSTRUCTIONS ARE NOT FOLLOWED!

CAUTION: this product needs proper cooling.

USE ONLY CRATES WITH FORCED COOLING AIR FLOW SINCE OVERHEAT MAY DEGRADE THE MODULE PERFORMANCES!

V1743/VX1743 CANNOT BE OPERATED WITH CAEN CRATES VME8001/8002/8004!

CAUTION: this product needs proper handling.

ALL CABLES MUST BE REMOVED FROM THE FRONT PANEL BEFORE EXTRACTING THE BOARD FROM THE CRATE!

CAEN provides the specific document "Precautions for Handling, Storage and Installation", available in the documentation tab of the product's web page, that the user is mandatory to read before to operate with CAEN equipment.

5 Power Requirements

The table below resumes the V1743/VX1743 power consumptions per relevant power supply rail.

SUPPLY VOLTAGE	CONSUMPTIONS
+5 V	5 A (max.)
+12 V	*Not used*
-12 V	1 A (max.)

Tab. 5.1: Power requirements t able

6 Panels Description

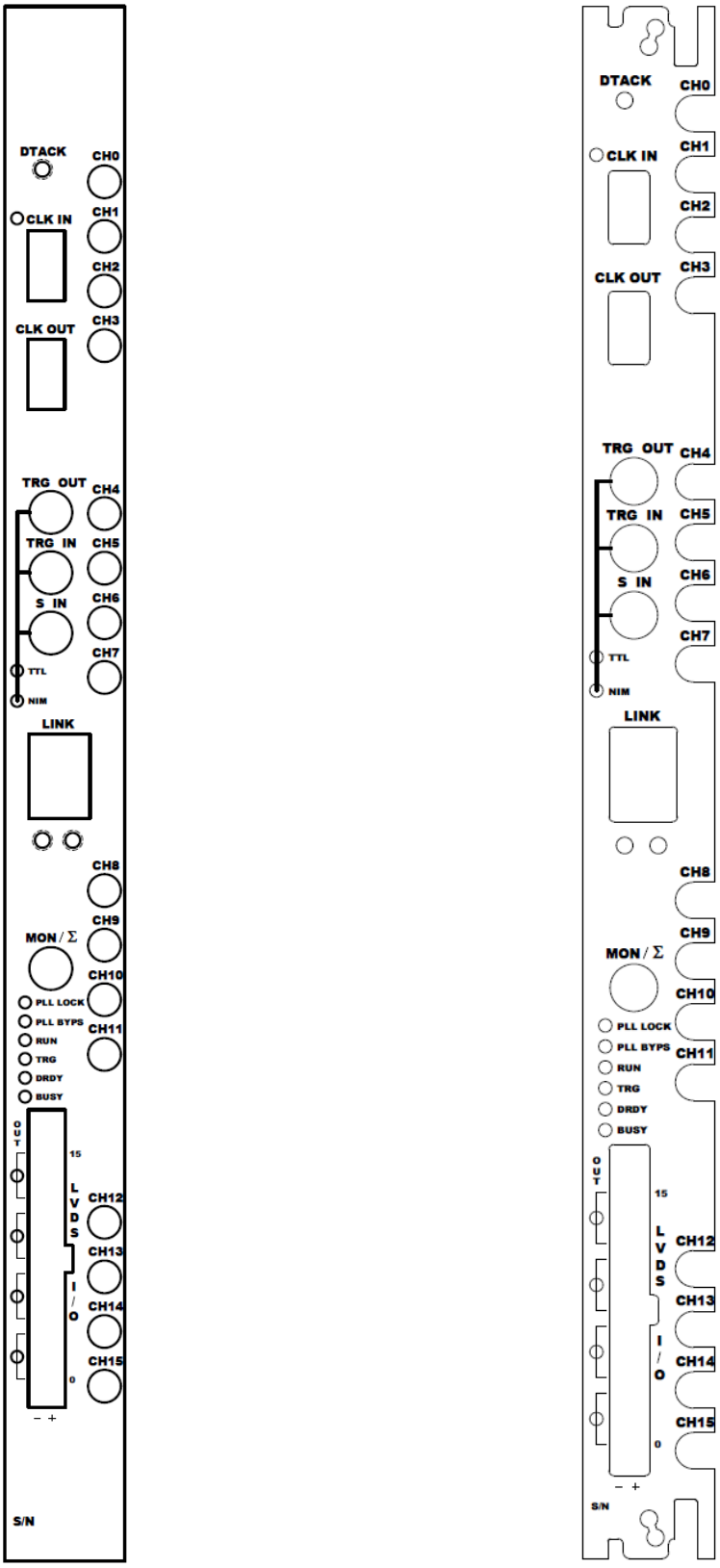


Fig. 6.1: V1743(sx)/VX1743(dx) front panel view

Front Panel

ANALOG INPUT

FUNCTION

Input connectors (CH0 to CH15) receiving the input analog signals.

ELECTRICAL SPECS

Input dynamics: 2.5 V_{pp}.

Input impedance (Z_{in}): 50 Ω.

MECHANICAL SPECS

Series: MCX connectors.

Type: CS 85MCX-50-0-16.

Manufacturer: SUHNER

Suggested plug: MCX-50-2-16 type.

Suggested cable: RG174 type.

CLK IN / CLK OUT

FUNCTION

Input and output connectors for the external clock.

ELECTRICAL SPECS

Sign. type: differential (LVDS, ECL, PECL, LVPECL, CML).

Coupling: AC.

Z_{diff}: 100 Ω.

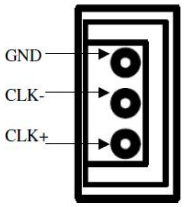
MECHANICAL SPECS

Series: AMPMODU connectors.

Type: 3-102203-4 (3-pin).

Manufacturer: AMP Inc.

PINOUT



CLK IN LED (GREEN): indicates the external clock is enabled.

TRG IN / TRG OUT / S IN

FUNCTION

External trigger digital input and output connectors;

SYNC/START/STOP digital input connector. Configurable as reset of the time stamp or to start/stop the acquisition

ELECTRICAL SPECS

Signal level: NIM or TTL.

Input impedance (Z_{in}): 50 Ω.

MECHANICAL SPECS

Series: 101 A 004 connectors.

Type: DLP 101 A 004-28.

Manufacturer: FISCHER.

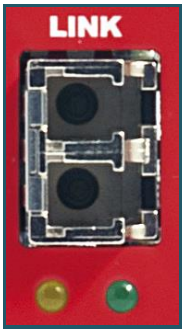
Alternatively:

Type: EPL 00 250 NTN.

Manufacturer: LEMO.

TTL (GREEN), NIM (GREEN): indicate the standard TTL or NIM is set for TRG-OUT, TRG-IN, S-IN.

OPTICAL LINK PORT



FUNCTION

Optical LINK connector for data readout and flow control. Daisy chainable. Compliant to Multimode 62.5/125µm cable featuring LC connectors on both sides.

ELECTRICAL SPECS

Transfer rate: up to 80 MB/s.

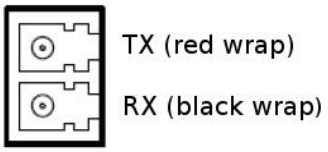
MECHANICAL SPECS

Series: SFF Transceivers.

Type: FTLF8519F-2KNL (LC connectors).

Manufacturer: FINISAR.

PINOUT



LINK LEDs (GREEN/YELLOW): right LED (GREEN) indicates the network presence, while left LED (YELLOW) signals the data transfer activity.

MON / Σ

FUNCTION

Analog Monitor output connector with 4 programmable modes:

- Trigger Majority
- Test Pulses
- Memory Occupancy
- Voltage Level

ELECTRICAL SPECS

12-bit (100 MHz) DAC output, $1V_{pp}$ on R_t=50 Ω

MECHANICAL SPECS

Series: 101 A 004 connectors.

Type: DLP 101 A 004-28.

Manufacturer: FISCHER.

Alternatively:

Type: EPL 00 250 NTN.

Manufacturer: LEMO

DIAGNOSTICS LEDs

PLL LOCK (GREEN): indicates the PLL is locked to the reference clock;

PLL BYPS (GREEN): indicates the PLL drives directly the ADCs. PLL circuit is switched off and PLL LOCK LED is turned off;

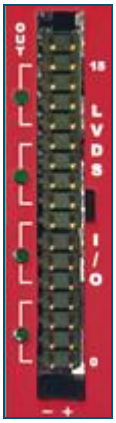
RUN (GREEN): indicates the acquisition is running (data taking). Please, refer to the *ACQUISITION STATUS* register description in **[RD2]**)

TRG (GREEN): indicates the trigger is accepted.

DRDY (GREEN): indicates the event/data is present in the Output Buffer.

BUSY (RED): indicates all the buffers are full for at least one channel.

LVDS I/Os CONNECTOR



FUNCTION

16-pin connector with programmable general purpose LVDS I/O signals organized in 4 independent signal groups: 0÷3; 4÷7; 8÷11; 12÷15.

In/Out direction is software controlled.

Different selectable modes:

- Busy
- Memory Full
- Data Ready
- Individual Trig-Out
- Pattern

ELECTRICAL SPECS

Level: differential LVDS

Z_{diff}: 100 Ω

MECHANICAL SPECS

Series : TE - AMPMODU Mod II Series

Type: 5-826634-0 (lead spacing: 2.54mm; row pitch: 2.54mm)

Manufacturer: AMP Inc.

LABELS

Two blue labels on each insertion/extraction handle on the VME front panel report:

- Manufacturer name and board's model
- -Brief functional description of the moduel

A little silver label, on the bottom of the VME board's front panel, reports:

- 4-digit Serial Number (S/N)

7 Internal Components

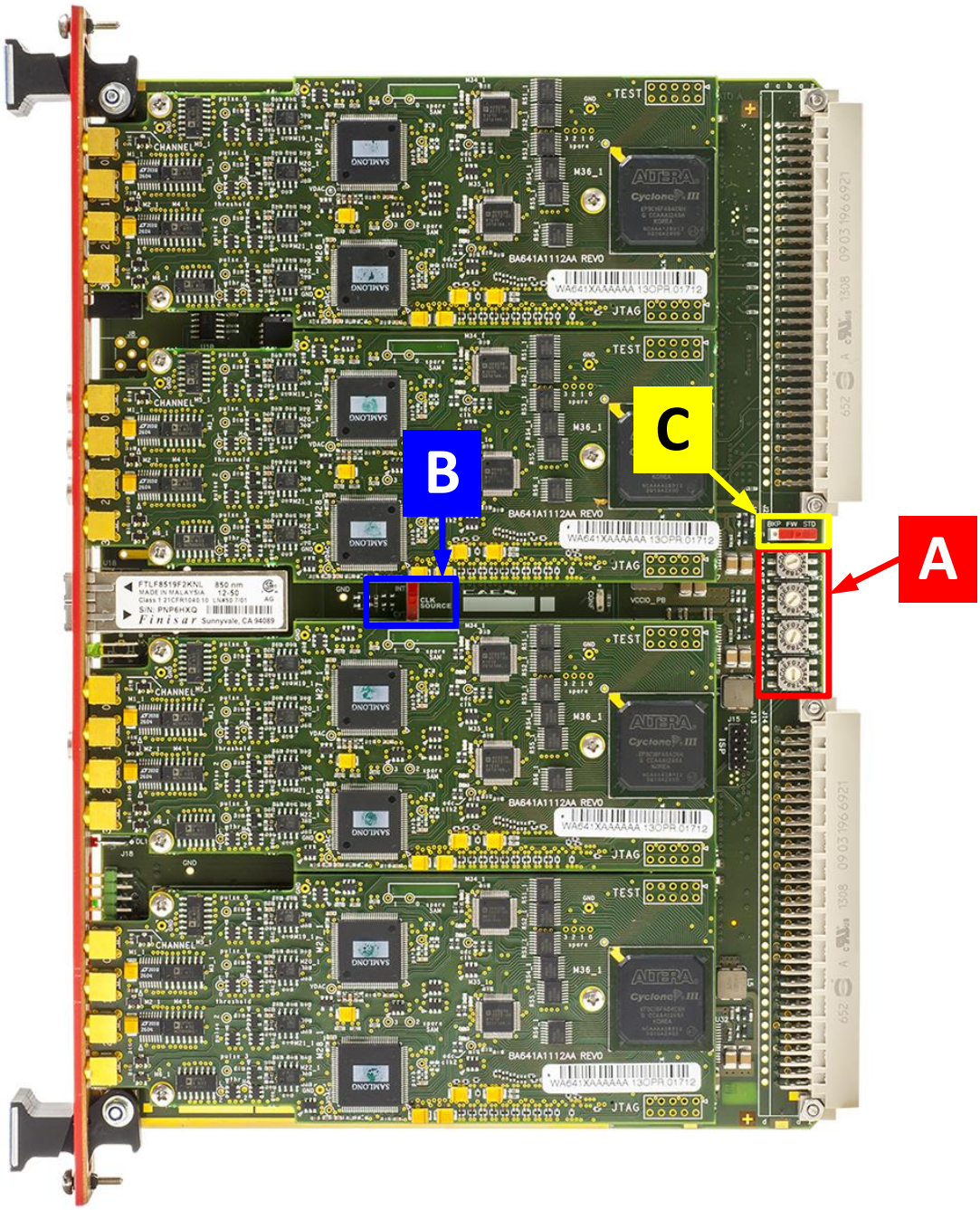


Fig. 7.1: Rotary and dip switches location

A	**SW2,4,5,6: "Base Address [31:16]"**	**Type:** Rotary Switches	**Function:** Set the VME Base Address of the module
B	**SW3: "CLOCK SOURCE" INT/EXT**	**Type:** Dip Switch	**Function:** Selects the clock source (External or Internal)
C	**SW1: "FW" BKP/STD**	**Type:** Dip Switch	**Function:** Selects between the "Standard" (STD) or the "Backup" (BKP) FLASH page firmware copy to be loaded on the FPGAs at power-on (default position: STD)

8 Functional Description

Analog Input Stage

Input dynamics is 2.5 V_{pp} on single ended MCX coaxial connectors (see § **6**). A 16-bit DAC allows to add up to a ±1.25 V DC offset in order to preserve the full dynamic range also in the extreme case of unipolar, positive or negative input signal. The input bandwidth ranges from DC to 500 MHz (@3dB).

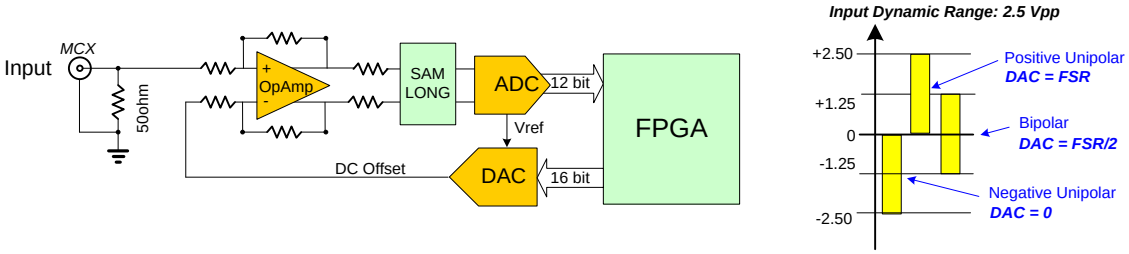


Fig. 8.1: Analog Input Diagram

Setting the DC offset requires a write access to the *Group n DAC SPI DATA* register (address 0x1n54).

Sampling in the Analog Memory

The analog input signals from each pair of channels are continuously sampled into one SAMLONG chip, which consists of a matrix of Delay Line Loops (DLLs) generating a 3.2 GS/s sampling frequency from an input clock of 200 MHz; 1.6 GS/s, 0.8 and 0.4 GS/s frequencies can be also programmed (see § **Changing the Sampling Frequency**).

Signals produced by the DLLs simultaneously open write switches in both sampling channels, where the differential input signals are sampled (1024 sampling capacitance cells per channel).

After being started by the so-called "Run" signal (corresponding to the WRITE signal on **Fig. 8.2**) going high, the DLLs run continuously in a circular fashion (after reaching the end of the matrix, samples are over written) until decoupled from the write switches when the Run signal goes down. This actually takes place after the arrival of a trigger signal synchronously delayed by the so-called post-trigger delay (set in the *Group n POSTTRIGGER* register; address 0x1n30), which finally provokes the freezing of the currently stored signal in the sampling capacitance cells.

Subsequently, the cells are multiplexed into the 12-bit ADCs whose output are stored by the FPGA into the Digital Memory Buffer and made ready for readout in the shape of events data.

A 16-bit DAC allows to add up a ±1.25 V DC offset in order to preserve the full dynamic range also in the extreme case of unipolar positive or negative input signals (see § **Analog Input Stage**).

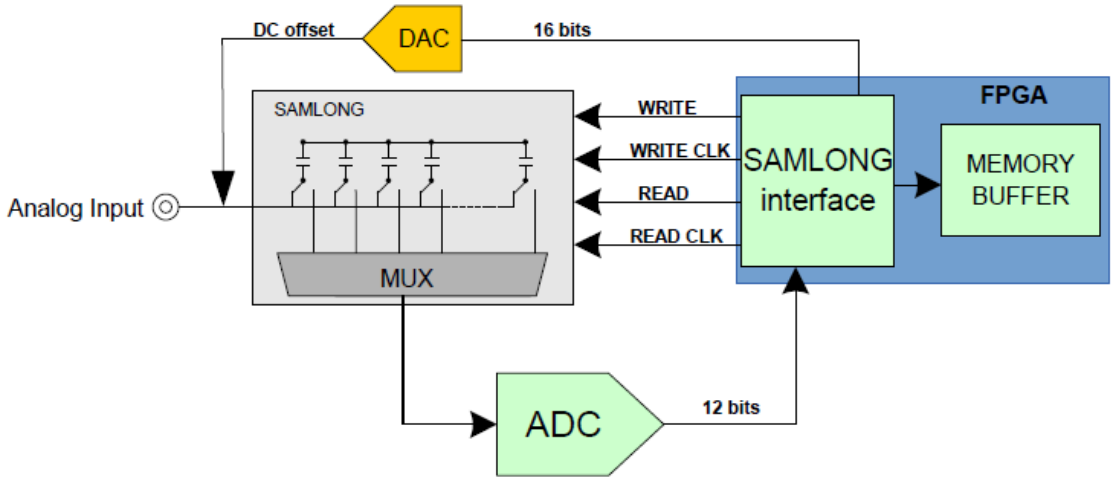


Fig. 8.2: Input Diagram

Detailed documentation of the SAMLONG chip is available at:

http://electronique.lal.in2p3.fr/echanges/USBWaveCatcher/Documentation/Boards&Chips/doc_SAMLONG_rev1.pdf

(in case the active link above doesn't work, copy and paste it on the internet browser)

Clock Distribution

The module features a PLL for clock synthesis with a selectable internal or external reference clock source.

Multi-board synchronization can be performed by driving a clock on CLOCK-IN input, allowing all SAMLONGs to run synchronously with this external reference. All analog inputs will be sampled at the same time without time drift, allowing high resolution timing and time analysis across multiple modules.

The module clock is provided by OSC-CLK and REF-CLK.

OSC-CLK is a fixed 50 MHz clock provided by an on board oscillator; it handles Optical Link, USB and Local Bus (communication between motherboard and mezzanine boards; see red traces in **Fig. 8.3**).

REF-CLK handles trigger logic, acquisition logic (samples storage into RAM, buffer freezing on trigger) through a clock chain. Such domain can use either an external (via the front panel signal) or an internal (via the local oscillator) source; in the latter case OSC-CLK and REF-CLK will be synchronous (the operating mode remains the same anyway).

REF-CLK is processed by an AD9510 device, which delivers 200 MHz clock signals directly to SAMLONG chips (WRITE_CLK on **Fig. 8.2** Wr_Clk on **Fig. 8.3**) and to the front-end FPGA. The latter will divide it to produce a 10 MHz clock (ADC_Clk on **Fig. 8.3**) used both for the readout of the SAMLONG chips (READ_CLK on **Fig. 8.2**) and for driving the ADC conversion. The AD9510 device also provides a 100 MHz clock to the trigger logics.

Refer to the AD9510 data sheet for more details:

http://www.analog.com/static/imported-files/data_sheets/AD9510.pdf

(in case the active link above doesn't work, copy and paste it on the internet browser)

When running with the reduced sampling frequencies, the 200 MHz clock is divided inside the front-end FPGA before being sent to the SAMLONG chips via the clock multiplexer as shown in **Fig. 8.3**.

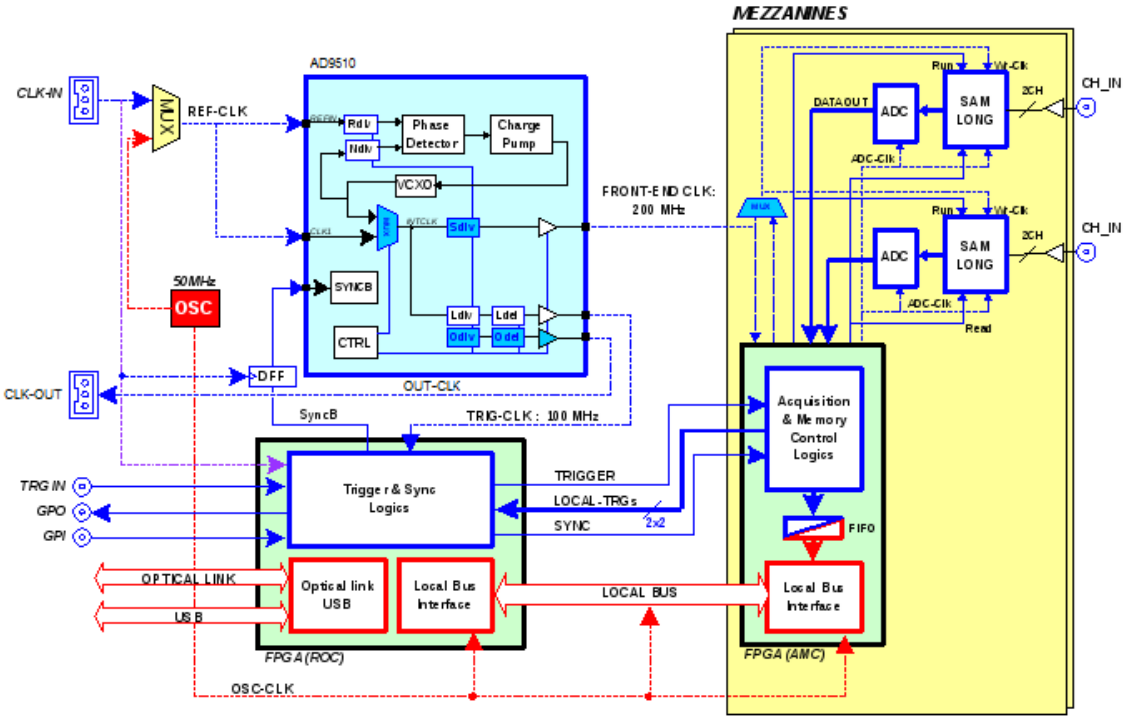


Fig. 8.3: Clock Distribution Diagram

PLL Mode

The Phase Detector within the AD9510 device allows to couple REF-CLK with a VCXO providing out the nominal operating frequency (3.2 GHz by default).

As introduced in § **Clock Distribution**, the source of the REF-CLK signal can be external (see **Fig. 8.2**) on CLK-IN front panel connector or internal from the 50 MHz local oscillator. Programming the REF-CLK source internal or external can be performed by acting on the on-board dip switch SW3 (see **Fig. 7.1**). The following options are allowed:

1. 50 MHz internal clock source – It's the standard operating mode, where the default AD9510 configuration doesn't require to be changed. OSC-CLK = REF-CLK.
2. 50 MHz external clock source – In this case it is not required to reprogram the AD9510 dividers, as the external clock reference is identical to the frequency of the internal oscillator. CLK-IN = OSC-CLK = REF-CLK.
3. External clock source different from 50 MHz – In this case, the user is required to program the AD9510 dividers in order to lock the VCXO to REF-CLK in order to provide out the admitted value of the sampling frequency. CLK-IN = REF-CLK. **Please, contact CAEN for more information on the allowed external frequencies (see § 13).**

Changing the Sampling Frequency

The sampling frequency of the SAMLONG chips can be programmed by software by accessing the *Group n SAMPLING FREQUENCY* register, address 0x1n40 (*n* refers to a channel pair; *n* = 0 to 7). The admitted values are:

3.2 GS/s (default)

1.6 GS/s

0.8 GS/s

0.4 GS/s

Output Clock

The AD9510 output can be available on the front panel CLK-OUT connector (see § **Front Panel**). The signal needs to be enabled by the user in the CAENUpgrader "PLL Upgrade" GUI (refer to **[RD1]**).

Data Correction

Different types of data correction are required, in order to compensate for unavoidable construction differences among the SAMLONG chips. The data correction is not applied at FPGA level, but must be implemented runtime/offline at software level by the user. All boards are factory calibrated during production test and calibration parameters are saved on-board. Application software provided by CAEN, automatically recovers the calibration parameters and runs them in order to correct the stored data events (refer to **[RD4]** and **[RD6]**).

The different data correction types are:

- **Line Offset Calibration:** this calibration permits reducing the baseline noise down to ~ 0.95 mV RMS. With this sole calibration performed, waveform data is already directly usable with a dynamic range of 11.5 bits and a sampling time precision of ~ 20 ps RMS.
- **Individual Pedestal Calibration:** this calibration permits reducing the baseline noise down to ~ 0.75 mV RMS, thus increasing the dynamic range to 11.7 bits.

Note: The user is recommended to perform the Individual Pedestal Calibration once he has his setup ready.

- **Time INL Calibration:** this calibration compensates the fixed time dispersion along the sampling matrix. The eventual sampling time precision scales down to ~ 5 ps RMS. The factory calibration parameters cannot be modified by the user
- **Trigger Threshold DAC Offset Calibration:** this calibration is necessary to obtain the best precision for small signals on the trigger threshold for the channel input discriminator. The factory calibration parameters cannot be modified by the user

Note: The user is not allowed to store his own calibration parameters on the board, except for the Individual Pedestal Calibration.

Line Offset Correction

The SAMLONG structure is a matrix of 16 lines and 64 columns. Whereas this structure guarantees a very stable time base, it also has the characteristic that each line is equipped with its own buffer, which provokes an offset modulo 16 in the baseline pattern. Nevertheless, this offset remains very stable. Thus, in order to compensate for it, each line of the chip is equipped with individual correction DACs.

The raw waveform before any correction (vertical scale is 20 mV/div) is shown in **Fig. 8.4**, while **Fig. 8.5** displays a zoom on one channel where the fixed pattern modulo 16 linked to the matrix structure can be distinguished.

Fig. 8.6 displays the sampled waveform after line offset correction with the same vertical scale (20 mV/div) and **Fig. 8.7** shows the same plot as **Fig. 8.6** but with a vertical scale of 2 mV/div.

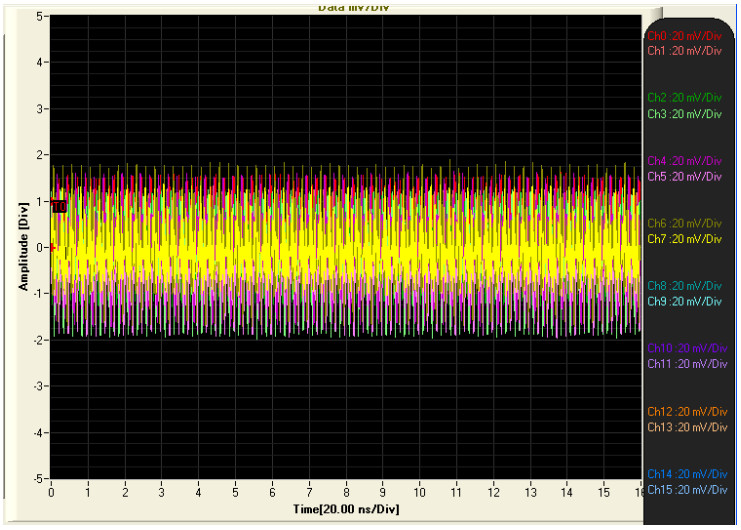


Fig. 8.4: Sampled waveform before line offset correction

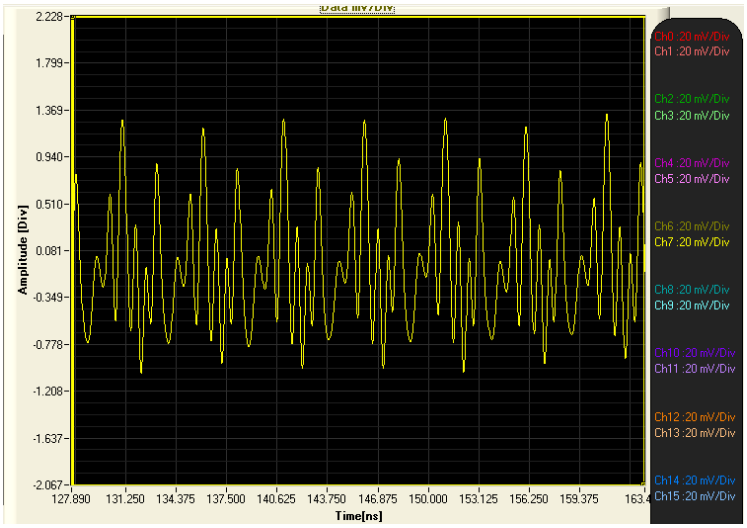


Fig. 8.5: Zoom on the sampled waveform before line offset correction

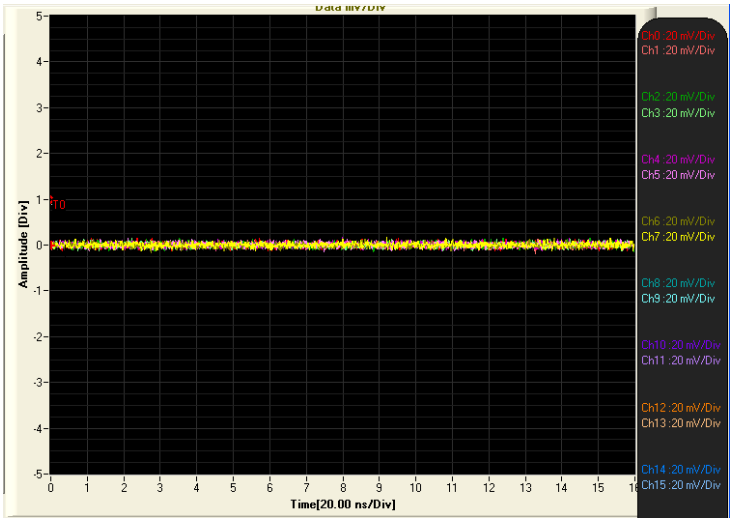


Fig. 8.6: Sampled waveform after line offset correction

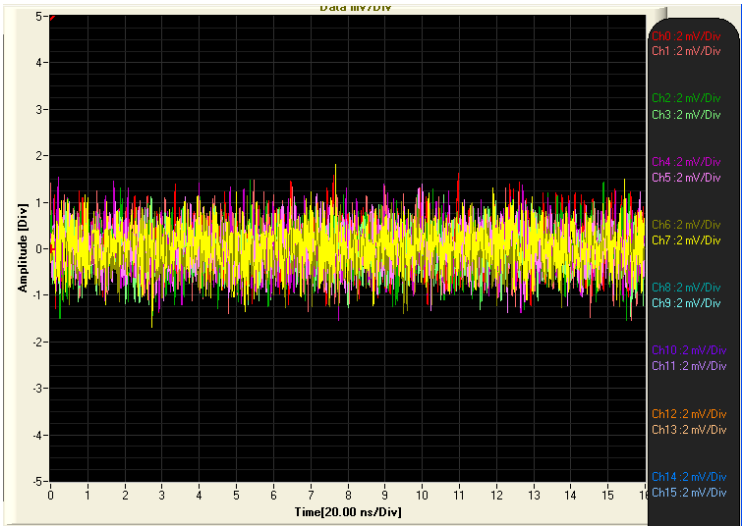


Fig. 8.7: Zoom on the sampled waveform after line offset correction

Individual Pedestal Correction

After the Line Offset correction, there is still a small residual individual offset distribution remaining on the baseline. This calibration will remove it. **Fig. 8.8** displays the waveform after this residual pedestal correction.

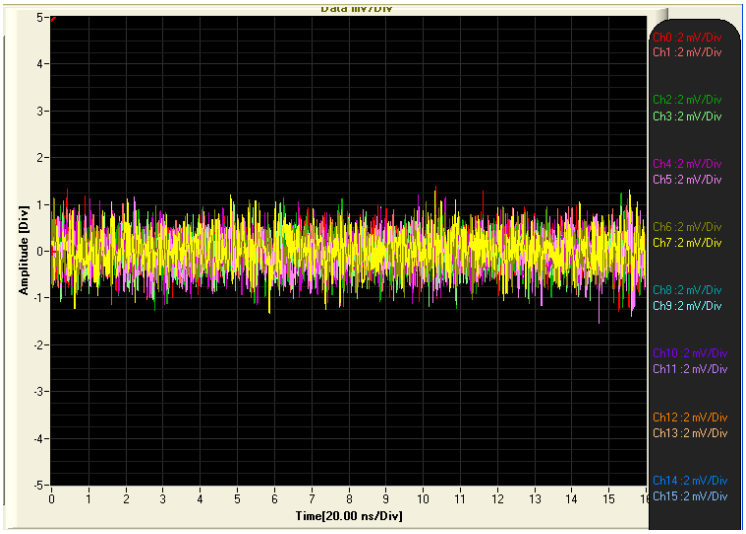


Fig. 8.8: Sampled waveform after individual pedestal correction

Individual pedestal calibration can be performed through the WaveCatcher software (see § **10**) in the following conditions:

- All the board channels must be disconnected

- Calibration must be done after the board is at its thermal regime

- Calibration must be done each time the temperature conditions vary significantly

Please, consult the software User Manual (**[RD6]**) for the specific calibration operations.

Time INL Correction

The sampling sequence is handled by SAMLONG through 1024 physical delay elements spread over the sampling matrix; the unavoidable construction differences between such delay elements can be compensated through a time calibration. The following figures show an example of the integral non linearity (INL) time profile of SAMLONG chips, before and after correction. Note the extremely low residual value on **Fig. 8.10**.

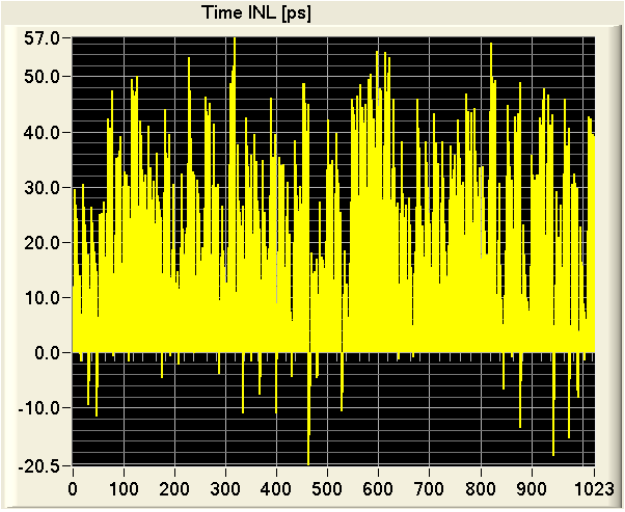


Fig. 8.9: Example of INL before time correction

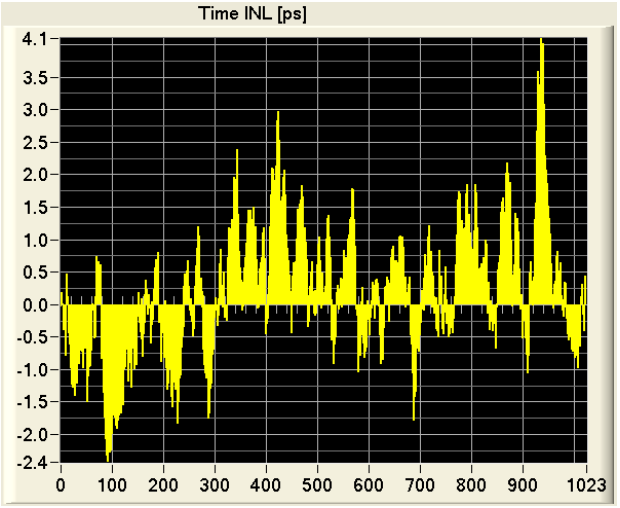


Fig. 8.10: Example of INL after time correction

Trigger Threshold DAC Offset Correction

The latter calibration permits setting the zero of the trigger discriminator threshold with a high precision, thus allowing triggering efficiently on very small signals around zero (a few mV).

Acquisition Run/Stop

The acquisition can be started and stopped in different ways, according to bits[1:0] setting of *ACQUISITION CONTROL* register (address 0x8100) and bit[2] of the same register:

- SW CONTROLLED (bits[1:0] = 00): Start and Stop take place by software command. Bit[2] = 0 means stopped, while bit[2] = 1 means running.
- S-IN CONTROLLED (bits[1:0] = 01): bit[2] = 1 arms the acquisition and the Start is issued as the S-IN signal is set high and the Stop occurs when it is set low. If bit[2] = 0 (disarmed), the acquisition is always off.
- FIRST TRIGGER CONTROLLED (bits[1:0] = 10): bit[2] = 1 arms the acquisition and the Start is issued on the first trigger pulse (rising edge) on the TRG-IN connector. This pulse is not used as a trigger; actual triggers start from the second pulse on TRG-IN. The Stop acquisition must be SW controlled (i.e. reset of bit[2]).
- LVDS I/Os CONTROLLED: this mode acts like the S-IN CONTROLLED (bits[1:0] = 01), but using the configurable features of the signals on the LVDS I/Os connector (see § **Front Panel LVDS I/Os**).

Running in Charge Mode

V1743 features an embedded Charge Mode which permits using the FPGA to calculate the charge comprised within a predefined part of each event. As the calculation is performed by the firmware, the acquisition rate can raise up to 7 kHz for full events (depending on the signal input rate). The system will start the summation at a predefined cell value (REF_CELL_FOR_CHARGE). It will last until a total number N (CHARGE_LENGTH) of cells have been summed. Then the result will be stored in a dedicated FIFO (CHARGE_FIFO) together with the physical position of the column where REF_CELL_FOR_CHARGE is located, in order to allow the concerned cells to have their pedestal corrected if necessary. The storage into the FIFO might optionally be filtered by a programmable threshold set on the charge result (CHARGE_THRESHOLD).

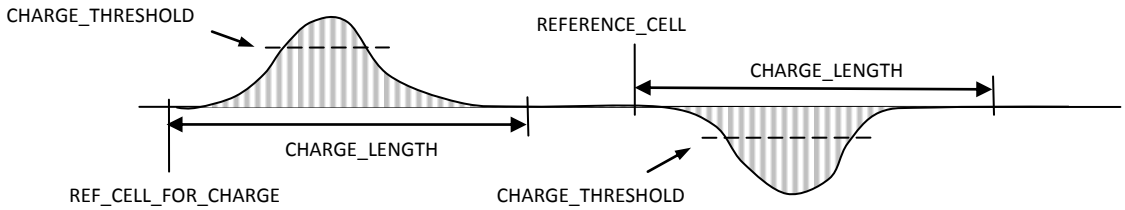


Fig. 8.11: Parameters used for the charge measurement mode

Fig. 8.11 describes the meaning of the different parameters quoted here above, for the integration of both a positive and a negative signal.

These operations are performed in parallel and independently on all channels. The event is readout only when the charge FIFOs will get full (they contain 256 events). To this end, the board front-end is automatically restarted as long as this doesn't happen.

As the number of words might be different in both channels in specific trigger modes, the charge and cell position will get forced to zero when the corresponding read FIFO is empty.

Event Structure

The event can be readout either via VMEbus or Optical Link as:

- **Header** (four 32-bit words)
- **Data** (variable size and format)

Data format is 32-bit long word (**Fig. 8.12**).

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HEADER	1	0	1	0	TOTAL EVENT SIZE (LWORDS)																											
	BOARD ID					BF	RES.	PATTERN																		G.MSK						
	RESERVED										EVENT COUNTER																					
	EVENT TIME TAG																															
GROUP 0	GROUP HEADER								GROUP 0 CHANNEL DATA first word																							
	GROUP 0 information								GROUP 0 CHANNEL DATA																							
	GROUP TRAILER								GROUP 0 CHANNEL DATA last word																							
GROUP 1	GROUP HEADER								GROUP 1 CHANNEL DATA first word																							
	GROUP 1 information								GROUP 1 CHANNEL DATA																							
	GROUP TRAILER								GROUP 1 CHANNEL DATA last word																							
GROUP 2	GROUP HEADER								GROUP 2 CHANNEL DATA first word																							
	GROUP 2 information								GROUP 2 CHANNEL DATA																							
	BLOCK TRAILER								GROUP 2 CHANNEL DATA last word																							
. . .	. . .								. . .																							
GROUP 7	GROUP HEADER								GROUP 7 CHANNEL DATA first word																							
	GROUP 7 information								GROUP 7 CHANNEL DATA																							
	GROUP TRAILER								GROUP 7 CHANNEL DATA last word																							

Fig. 8.12: Event Format

Note: A group is composed by 2 adjacent analog channels (GROUP 0 = channels 0 - 1, GROUP 1 = channels 2 - 3, GROUP 2 = channels 4 - 5, …, GROUP 7 = channels 14 - 15).

Header

Header is composed of four (4) words including the following information:

- **TOTAL EVENT SIZE (1st header word)**: size of the event (number of 32-bit long words);
- **BOARD ID (GEO) (2nd header word)**;
- **BOARD FAIL FLAG (Bit[26] of 2nd header word):** this bit is set to "1" in consequence of a hardware problem (e.g. PLL unlocking). The user can investigate the problem by the available *BOARD FAIL STATUS* register (refer to **[RD2]**) or contact CAEN Support Service (see § **13**);
- **PATTERN (2nd header word):** 16-bit pattern latched on the LVDS I/O as one trigger arrives;
- **G.MSK (2nd header word):** the mask of the groups participating in the event (e.g. GROUP 0 and GROUP 1 participating → G.MSK = 0x3; this information must be used by the software to acknowledge what group the samples are coming from; the first event contains the samples from the group with the lowest number);
- **EVENT COUNTER (3rd header word):** it is the trigger counter; it can count either accepted triggers only, or all triggers (bit[3] of the *ACQUISITION CONTROL* register).
- **EVENT TIME TAG (4th header word):** it is a 31-bit counter + 1 bit as roll over flag, which is reset when the acquisition starts and is incremented at each trigger clock hit (10 ns @100MHz). It is the trigger time reference.

Data

Data are the stored information from each enabled group; data from masked groups are not read. The part of an event related to each group presents the format described in **Fig. 8.13** (example based on GROUP 0).

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GROUP HEADER = 0x69								ADC DATA CHANNEL 1 SAMPLE 0												ADC DATA CHANNEL 0 SAMPLE 0											
HIT_COUNTER CH0 LSB								ADC DATA CHANNEL 1 SAMPLE 1												ADC DATA CHANNEL 0 SAMPLE 1											
HIT_COUNTER CH0 MSB								ADC DATA CHANNEL 1 SAMPLE 2												ADC DATA CHANNEL 0 SAMPLE 2											
TIME_COUNTER CH0 LSB								ADC DATA CHANNEL 1 SAMPLE 3												ADC DATA CHANNEL 0 SAMPLE 3											
TIME_COUNTER CH0 MSB								ADC DATA CHANNEL 1 SAMPLE 4												ADC DATA CHANNEL 0 SAMPLE 4											
HIT_COUNTER CH1 LSB								ADC DATA CHANNEL 1 SAMPLE 5												ADC DATA CHANNEL 0 SAMPLE 5											
HIT_COUNTER CH1 MSB								ADC DATA CHANNEL 1 SAMPLE 6												ADC DATA CHANNEL 0 SAMPLE 6											
TIME_COUNTER CH1 LSB								ADC DATA CHANNEL 1 SAMPLE 7												ADC DATA CHANNEL 0 SAMPLE 7											
TIME_COUNTER CH1 MSB								ADC DATA CHANNEL 1 SAMPLE 8												ADC DATA CHANNEL 0 SAMPLE 8											
SAMPLING_FREQUENCY								ADC DATA CHANNEL 1 SAMPLE 9												ADC DATA CHANNEL 0 SAMPLE 9											
EVENT_ID								ADC DATA CHANNEL 1 SAMPLE 10												ADC DATA CHANNEL 0 SAMPLE 10											
FCR LSB								ADC DATA CHANNEL 1 SAMPLE 11												ADC DATA CHANNEL 0 SAMPLE 11											
FCR MSB								ADC DATA CHANNEL 1 SAMPLE 12												ADC DATA CHANNEL 0 SAMPLE 12											
TDC Byte 0 (LSB)								ADC DATA CHANNEL 1 SAMPLE 13												ADC DATA CHANNEL 0 SAMPLE 13											
TDC Byte 1								ADC DATA CHANNEL 1 SAMPLE 14												ADC DATA CHANNEL 0 SAMPLE 14											
TDC Byte 2								ADC DATA CHANNEL 1 SAMPLE 15												ADC DATA CHANNEL 0 SAMPLE 15											
TDC Byte 3								ADC DATA CHANNEL 1 SAMPLE 16												ADC DATA CHANNEL 0 SAMPLE 16											
TDC Byte 4 (MSB)								ADC DATA CHANNEL 1 SAMPLE 17												ADC DATA CHANNEL 0 SAMPLE 17											
DUMMY								ADC DATA CHANNEL 1 SAMPLE 18												ADC DATA CHANNEL 0 SAMPLE 18											
DUMMY …								ADC DATA …												ADC DATA …											
BLOCK TRAILER = 0x96								ADC DATA CHANNEL 1 SAMPLE N-1												ADC DATA CHANNEL 0 SAMPLE N-1											

Fig. 8.13: Group Data Format

In the group data described above, the number of words directly corresponds to the number of columns read in the SAMLONG chips multiplied by 16 (fixed number of lines). Bits 0 to 23 always correspond to digitized event data. Both channels are grouped inside the same word. Bits 24 to 31 are used for header, trailer, and event information.

- For each channel, HIT_COUNTER and TIME_COUNTER are 16-bit counters used to calculate the hit rate linked to the activity on the channel since the last event. HIT_COUNTER counts the number of times the input discriminator has be toggling since the last event, whereas TIME_COUNTER counts the time in units of 1 µs. The first counter saturating blocks the other. Taking care of memorizing this information long enough in the software, this measurement can range from 0.1 Hz to > ~400 MHz (see § **Hit Rate Monitor**).

- SAMPLING_FREQUENCY is common to all channels. It is coded on 2 bits as follows:

  0 => 3.2 GS/s

  1 => 1.6 GS/s

  2 => 0.8 GS/s

  3 => 0.4 GS/s

- EVENT_ID corresponds to the 8 lower significant bits of the event number since the beginning of the run.

- FCR is the address of the First Cell Read in the SAMLONG chip for the current event. It is coded on 10 bits (which corresponds to the 1024 cells).

- TDC is the value of the individual channel counter and is coded over 40 bits. The corresponding counter runs with the SAMLONG clock, thus covering a minimum of 1h30 at 200 MHz. It is reset at the RUN acquisition, but it is also possible to program the S-IN input connector to reset it when an external signal is fed in.

In case of charge readout mode (see § **Running in Charge Mode**), the part of an event related to each group presents the format as in **Fig. 8.14** (example of GROUP 0):

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	REF CELL COLUMN						1	CHARGE CHANNEL 0 EVENT 1																						
0	0	REF CELL COLUMN						1	CHARGE CHANNEL 1 EVENT 1																						
0	0	REF CELL COLUMN						1	CHARGE CHANNEL 0 EVENT 2																						
0	0	REF CELL COLUMN						1	CHARGE CHANNEL 1 EVENT 2																						
-	-	…						-	…																						
0	0	REF CELL COLUMN						1	CHARGE CHANNEL 0 EVENT 256																						
0	0	REF CELL COLUMN						1	CHARGE CHANNEL 1 EVENT 256																						

Fig. 8.14: Group Data Format in Charge Mode

In the group data described above, the number of words (512) corresponds to twice the charge FIFO depth per channel (256 words). Charge data is coded in two's complement over 23 bits. REF CELL COLUMN corresponds to the number of the physical column where the charge calculation started inside the SAMLONG chip (0 to 63). It is necessary for optional software correction purpose.

Acquisition Synchronization

Each pair of input channels share a SRAM memory in the channel FPGA (see **Fig. 2.1**) that is organized into buffers able to store up to 7 full events per channel, that is to say 7 kS/ch (1 event = 1024 samples or 1024 * 12 bits). When the trigger occurs, the acquisition takes place as described in § **Sampling in the Analog Memory**.

When the Digital Memory Buffer is filled, the board is considered FULL: no trigger is accepted and the acquisition stops. As soon as at least one buffer is readout, the board exits the FULL condition and acquisition restarts.

In some cases, the BUSY propagation from the digitizer to other parts of the system has some latency and it can happen that one or more triggers occur while the digitizer is already FULL and unable to accept those triggers. This condition causes event loss and it is particularly unsuitable when there are multiple digitizers running synchronously, because the triggers accepted by one board and not by other boards cause event misalignment.

In this cases, it is possible to program the BUSY signal to be asserted when the digitizer is close to FULL condition, but it has still some free buffers (Almost FULL condition). In this mode, the digitizer remains able to accept some more triggers even after the BUSY assertion and the system can tolerate a delay in the inhibit of the trigger generation. When the Almost FULL condition is enabled by setting the Almost FULL level (*Memory Almost FULL Level* register, address 0x816C) to X, the BUSY signal is asserted as soon as X buffers are filled, although the board still goes FULL (and rejects triggers) when all the buffers are filled

In case of multi-board setup, the BUSY signal can be propagated among boards through the front panel LVDS I/O connectors (see § **Front Panel LVDS I/Os**).

Trigger Management

All the channels in a board share the same trigger (common board trigger), that is to say they acquire an event simultaneously and in the same way (a determined number of samples and position with respect to the trigger).

The common board trigger is generated based on different trigger sources:

- **Software trigger:** produced via a software command.
- **External trigger:** received via the front panel TRG-IN signal.
- **Self-trigger:** generated by the individual discriminator, with programmable threshold, placed on each analog channel. The self-triggers from each couple of adjacent channel then generate a single trigger request. The trigger request finally contribute to the common board trigger generation.
- **Coincidence** between any of the latter (*t.b.d.*).
- **Programmable majority** of the latter (*t.b.d.*).

As a common board trigger is issued, the analog buffers related to that trigger are frozen, then digitized by the 12-bit ADCs, then stored into the digital memory buffer and are available for readout (refer to § **Sampling in the Analog Memory**).

The analog to digital conversion process is affected by a dead time during which the module cannot handle other triggers. This dead time depends on the number of samples to be digitized (13 µs + ($N_{samples}$ / 16) * 1.75 µs). The V1743 features a maximum dead time of 125 µs (@ 1024 samples recording).

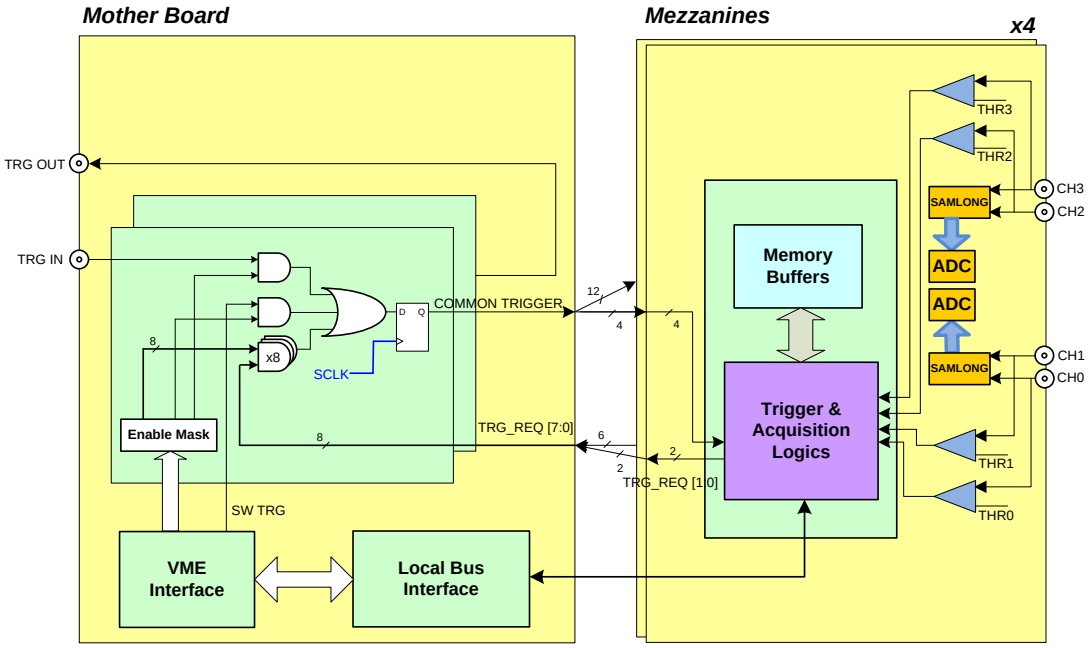


Fig. 8.15: Trigger Management block diagram

Software Trigger

Software triggers are internally produced via a software command (write access to the *SW TRIGGER* register) through VMEbus or Optical Linkbus

External Trigger

External signal received via the front panel TRG-IN connector, that can be TTL/NIM (configurable through the *FRONT PANEL I/O CONTROL* register). The external trigger is synchronized with the internal 100 MHz trigger clock.

Self-Trigger

V1743 is equipped with a discriminator with a 16-bit programmable threshold on each channel, which permits generating a self-trigger signal when the digitized input pulse exceeds the threshold value (configurable through the *Group n DAC SPI DATA* register). The self-triggers of each couple of adjacent channels are then processed to provide out a single trigger request. The trigger requests are propagated to the central trigger logic to produce the board common trigger, which is finally distributed back to all channels causing the event acquisition (see **Fig. 8.15**). **Fig. 8.16** schematizes the self-trigger generation, the trigger request and common trigger logic.

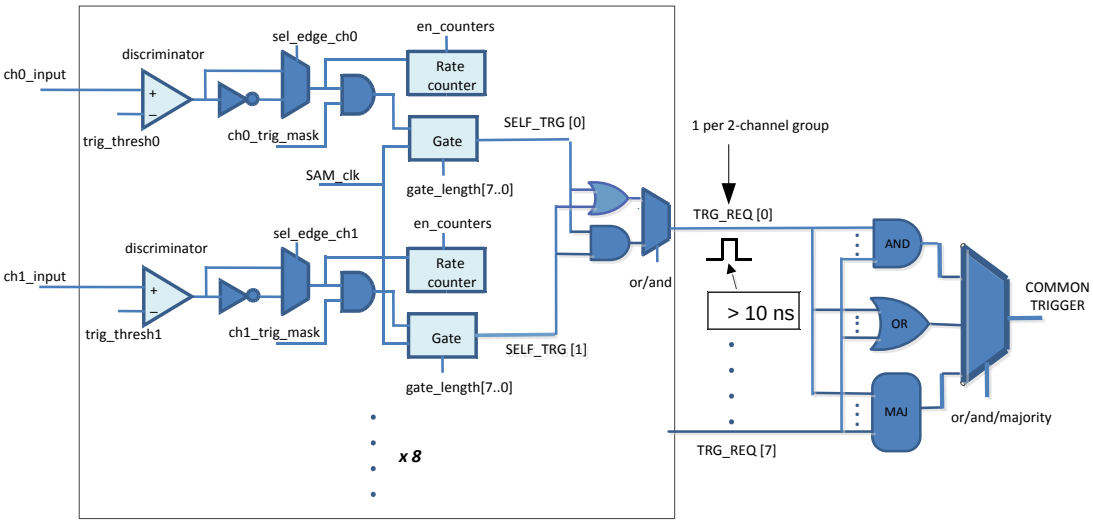


Fig. 8.16: Self-Trigger generation, Trigger Request and Common Trigger logic

Tab. 8.1 shows the registers involved in the self-trigger management

Signal/Function	Reference Register Address	Bit(s)
sel_edge_ch0	0x1n3C	Bit[5]
ch0_trig_mask	0x1n3C	Bit[4]
sel_edge_ch1	0x1n3C	Bit[7]
ch1_trig_mask	0x1n3C	Bit[6]
en_counters	0x1n70	Bit[3]
gate_length[7..0]	0x1n38	
or/and	0x003C	Bit[3]
or/and/majority	0x810C	Bits[9:8]

Tab. 8.1: Map of available FPGA registers for the self-trigger management

The FPGA, through the *Group n TRIGGER GATE* register (address 0x1n38), can be programmed in order the self-trigger to be a pulse of configurable width (see **Fig. 8.17**).

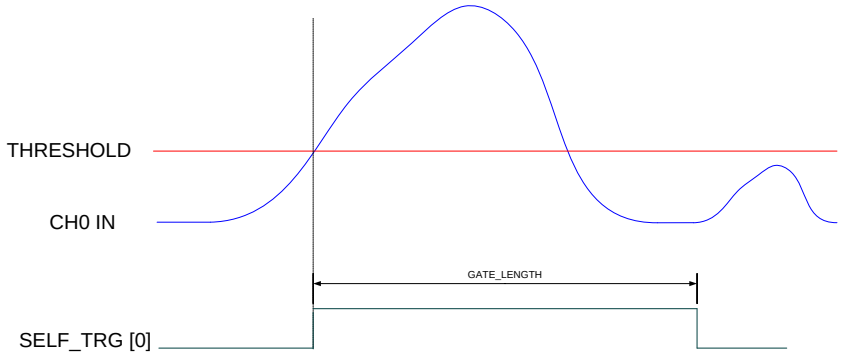


Fig. 8.17: Self-trigger generation

The FPGA, through the *Group n TRIGGER* register (address 0x1n3C), can be programmed in order the trigger request for a couple of adjacent channels to be the AND or OR of the levant self-trigger signals (see **Fig. 8.16**).

The FPGA, through the *TRIGGER SOURCE ENABLE MASK* register (address 0x810C), can be programmed in order The common trigger can be the OR, the AND or the Majority of the enabled trigger requests (see **Fig. 8.16**).

Default Conditions: by firmware default, the FPGA is programmed so that:

- All the channels are disabled to generate trigger requests, while the external trigger and software trigger are enabled.
- Each trigger request is the OR of two pulses whose width is fixed by default depending on the board operating frequency: 15 ns (@3.2 GS/s); 20 ns (@1.6 GS/s); 30 ns (@0.8 GS/s); 50 ns (@0.4 GS/s).
- The common trigger is generated as the OR of the enabled trigger requests.

Trigger Coincidence Level

T.b.d.

Majority Level

T.b.d.

Trigger Distribution

In the default configuration, the OR of all the enabled trigger sources is synchronized with the internal clock, then becomes the common trigger of the board and is fed in parallel to all channels, which consequently provokes the capture of an event.

A Trigger Out is also generated on the relevant front panel TRG-OUT connector (NIM or TTL), and allows to extend the trigger signal to other boards: set bits[17:16] = 00 in *FRONT PANEL I/O CONTROL* register and enable the desired trigger sources in *FRONT PANEL TRIGGER OUT ENABLE MASK* register.

For example, in order to start the acquisition on all the channels of the boards, as one of the channels crosses its threshold, the trigger request from the channel must be enabled as Trigger Out signal, the Trigger Out must then be fed to a Fan Out unit; the obtained signal has to be fed to the external trigger input TRG-IN of all the boards in the chain (including the board which generated the Trigger Out signal).

Multi-Board Synchronization

When multi-board systems are involved in an experiment, it is necessary to synchronize different boards. In this way the user can acquire from N boards with Y channel each, like if they were just one board with (N x Y) channels.

The main issue in the synchronization of a multi-board system is to propagate the sampling clock among the boards. This is made through input/output daisy chain connections among the digitizers. One board has to be chosen to be the "master" board that propagates its own clock to the others. A programmable phase shift can adjust possible delays in the clock propagation. This allows to have both the same ADC sampling clock, and the same time reference for all boards. Having the same time reference means that the acquisition starts/stops at the same time, and that the time stamps of different boards is aligned to the same absolute time.

There are several ways to implement the trigger logic. The synchronization tool allows to propagate the trigger to all boards and acquire the events accordingly. Moreover, in case of busy state of one or more boards, the acquisition is inhibited for all boards.

Documentation reference **[RD3]** provides detailed guidelines on how to synchronize CAEN VME digitizers.

Note: This document must be referenced to approach the synchronization concept with CAEN VME digitizers (cabling, clock, trigger and run management different cases), while the frequency setting and software support need to be tailored to 743 series by the user. **Please, contact CAEN for details specific for the V1743 (see§ 13)**.

Front Panel LVDS I/Os

The V1743 is provided with 16 general purpose programmable LVDS I/O signals (see § **6**). CAEN has developed for its digitizer series a new and more flexible configuration management that has been introduced from the release 3.8 of the ROC FPGA firmware and allows the LVDS I/Os signals to be programmed in terms of direction (INPUT/OUTPUT) and functionality by groups of 4. Only the description of the new configuration modes is given in this paragraph.

The new management is enabled by setting to 1 the bit[8] of the *FRONT PANEL I/O CONTROL* register, that is set to 0 by default.

THE USER MUST SET BIT[8] = 1 AT 0x811C IN ORDER TO ENABLE THE NEW LVDS I/Os CONFIGURATION MODES

NOTE ABOUT LVDS I/Os CONFIGURATIONS IMPLEMENTED IN ROC FW RELEASES <3.8

*THE STANDARD FIRMWARE OF V1743 MAKES ALSO AVAILABLE THE OLD CONFIGURATIONS (bit[8] = 0). USERS WHOSE SOFTWARE BASES ON THE OLD LVDS I/Os CONFIGURATION MANAGEMENT CAN REFER TO THE USER MANUAL OF THE RELEVANT DIGITIZER OR CAN CONTACT CAEN (see § **13**) FOR INFORMATION.*

SINCE THIS COULD BE NO LONGER GUARANTEED IN THE FUTURE, THE USER IS HEARTLY RECOMMENDED TO TAKE THE NEW CONFIGURATION MANAGEMENT AS REFERENCE!

The direction of the signals are set by the bits[5:2] in the *FRONT PANEL I/O CONTROL* register:

Bit[2] → LVDS I/O[3:0]

Bit[3] → LVDS I/O[7:4]

Bit[4] → LVDS I/O[11:8]

Bit[5] → LVDS I/O[15:12]

Where setting the bit to 0 enables the relevant signals in the group as INPUT, while 1 enables them as OUTPUT.

When enabled (i.e. bit[8] = 1), the new management allows each group of 4 signals of the LVDS I/O 16-pin connector to be configured in one of the 4 following modes (according to bits[15:0] in the *FRONT PANEL LVDS I/O NEW FEATURES* register):

- Mode 0 (bits[n+3:n] = 0000): REGISTER
- Mode 1 (bits[n+3:n] = 0001): TRIGGER
- Mode 2 (bits[n+3:n] = 0010): nBUSY/nVETO
- Mode 3 (bits[n+3:n] = 0011): LEGACY

where n = 0, 4, 8, 12.

Note:. Whatever option is set, the LVDS I/Os are always latched with the trigger and the relevant status of the 16 signals is always written into the header Pattern field (see § **Event Structure**) the user can then choose to readout it or not

	REGISTER	TRIGGER	nBUSY/nVETO	LEGACY
LVDS IN [15:12]	Reg[15:12]	*Not available*	15: nRunIn 14: nTriggerIn 13: nVetoIn 12: nBusyIn	15: *reserved* 14: *reserved* 13: *reserved* 12: nClear_TTT
LVDS IN [11:8]	Reg[11:8]	*Not available*	11: nRunIn 10: nTriggerIn 9: nVetoIn 8: nBusyIn	11: reserved 10: reserved 9: reserved 8: nClear_TTT
LVDS IN [7:4]	Reg[7:4]	*Not available*	7: nRunIn 6: nTriggerIn 5: nVetoIn 4: nBusyIn	7: reserved 6: reserved 5: reserved 4: nClear_TTT
LVDS IN [3:0]	Reg[3:0]	*Not available*	3: nRunIn 2: nTriggerIn 1: nVetoIn 0: nBusyIn	3: reserved 2: reserved 1: reserved 0: nClear_TTT

Tab. 8.2: Features description when LVDS group is configured as INPUT

	REGISTER	TRIGGER	nBUSY/nVETO	LEGACY
LVDS IN [15:12]	Reg[15:12]	TrigOut_Ch[7:4]	15: nRun 14: nTrigger 13: nVeto 12: nBusy	15: Run 14: Trigger 13: DataReady 12: Busy
LVDS IN [11:8]	Reg[11:8]	TrigOut_Ch[3:0]	11: nRun 10: nTrigger 9: nVeto 8: nBusy	11: Run 10: Trigger 9: DataReady 8: Busy
LVDS IN [7:4]	Reg[7:4]	TrigOut_Ch[7:4]	7: nRun 6: nTrigger 5: nVeto 4: nBusy	7: Run 6: Trigger 5: DataReady 4: Busy
LVDS IN [3:0]	Reg[3:0]	TrigOut_Ch[3:0]	3: nRun 2: nTrigger 1: nVeto 0: nBusy	3: Run 2: Trigger 1: DataReady 0: Busy

Tab. 8.3: Features description when LVDS group is configured as OUTPUT

Mode 0: REGISTER

Direction is INPUT: the logic level of the LVDS I/O signals can be read through the *FRONT PANEL I/O DATA* register.

Direction is OUTPUT: the logic level of the LVDS I/O signals can be written through the *FRONT PANEL I/O DATA* register.

Mode 1: TRIGGER

Direction is INPUT: *Not available*.

Direction is OUTPUT: the *TrgOut_Ch[(n+3):n]* signals (n = 0, 4) consist of the local channel triggers coming directly from the mezzanines, where a local trigger is defined in § **Trigger Management**.

Mode 2: nBUSY/nVETO

nBusy signal

nBusyIn (INPUT) is an active low signal which, if enabled, is used to generate the *nBusy* signal (OUTPUT) as below.

The *Busy* signal (fed out on LVDS I/Os or TRG-OUT LEMO connector) is:

Almost_Full OR (**LVDS_BusyIn** AND **BusyIn_enable**)

where

- *Almost_Full* indicates the filling of the Buffer Memory up to a programmable level (12-bit range) set in the *MEMORY BUFFER ALMOST FULL LEVEL* register;
- *LVDS_BusyIn* is available in nBUSY/nVETO configuration (see **Tab. 8.2**);
- *BusyIn_enable* is set in the *ACQUISITION CONTROL* register, bit[8].

nVETO signal

Direction is INPUT: *nVETOIn* is an active low signal which, if enabled (i.e. *ACQUISITION CONTROL* register, bit[9] = 1), is used to veto the generation of the common trigger propagated to the channels for the event acquisition.

Direction is OUTPUT: the *nVETO* signal is the copy of *nVETOIn*.

nTrigger signal

Direction is INPUT: *nTriggerIn* is an active low signal which, if enabled, is a real trigger able to cause the event acquisition. It can be propagated to TRG-OUT LEMO connector or to the individual triggers.

Direction is OUTPUT: *nTrigger* signal is the copy of the trigger signal propagated to the TRG-OUT LEMO connector.

nRun signal

Direction is INPUT: *nRunIn* is an active low signal which can be used as Start for the digitizer (i.e. *ACQUISITION CONTROL* register, bits[1:0] = 11). It is possible to program the Start on the level or on the edge of the *nRunIn* signal (*ACQUISITION CONTROL* register, bit[11]).

Direction is OUTPUT: *nRun* signal is the inverse of the internal Run of the board.

Mode 3: LEGACY

Legacy Mode has been introduced in order the LVDS connector (properly programmed) to be able to feature the same I/O signals available in the ROC FPGA firmware revisions lower than 3.8.

nClear_TTT signal

It is the only signal available as INPUT. It is the Trigger Time Tag (TTT) reset, like in the old configuration.

Busy signal

The *Busy* signal is active high and it is exactly the inverse of the *nBusy* signal (see § **Mode 2: nBUSY/nVETO**).

In case the *MEMORY BUFFER ALMOST FULL LEVEL* register is set to 0x0 and the *BusyIn* signal is disabled, the *Busy* is the *FULL* signal present in the old configuration.

DataReady signal

The *DataReady* is an active high signal indicating that the board has data available for readout (the same as the *DRDY* front panel LED does).

Trigger signal

The active high *Trigger* signal is the copy of the acquisition trigger (common trigger) sent from the motherboard to the mezzanines (it is neither the signal provided out on the TRG-OUT LEMO connector nor the inverse of the signal sent to the LVDS connector).

Run signal

The *Run* signal is active high and represents the inverse of the *nRun* signal (see § **Mode 2: nBUSY/nVETO**).

Analog Monitor

V1743 houses a 12-bit (100MHz) DAC with 0÷1 V dynamics on a 50 Ω load, whose input is controlled by the ROC FPGA and the signal output (driving 50 Ω) is available on the MON/Σ output connector (see **Fig. 2.1** and § **6**). MON output of more boards can be summed by an external Linear Fan In.

The DAC control logic implements four operating modes according to the value of bits[2:0] in *MONITOR DAC MODE* register:

- Trigger Majority Mode (*Monitor Mode* = 000)
- Test Mode (*Monitor Mode* = 001)
- Buffer Occupancy Mode (*Monitor Mode* = 011)
- Voltage Level Mode (*Monitor Mode* = 100)

Trigger Majority Mode (*Monitor Mode* = 000)

It is possible to generate a Majority signal with the DAC: a voltage signal whose amplitude is proportional to the number of channels under/over threshold (1 step = 125 mV); this allows, via an external discriminator, to produce a common trigger signal, as the number of triggering channels has exceeded a particular threshold.

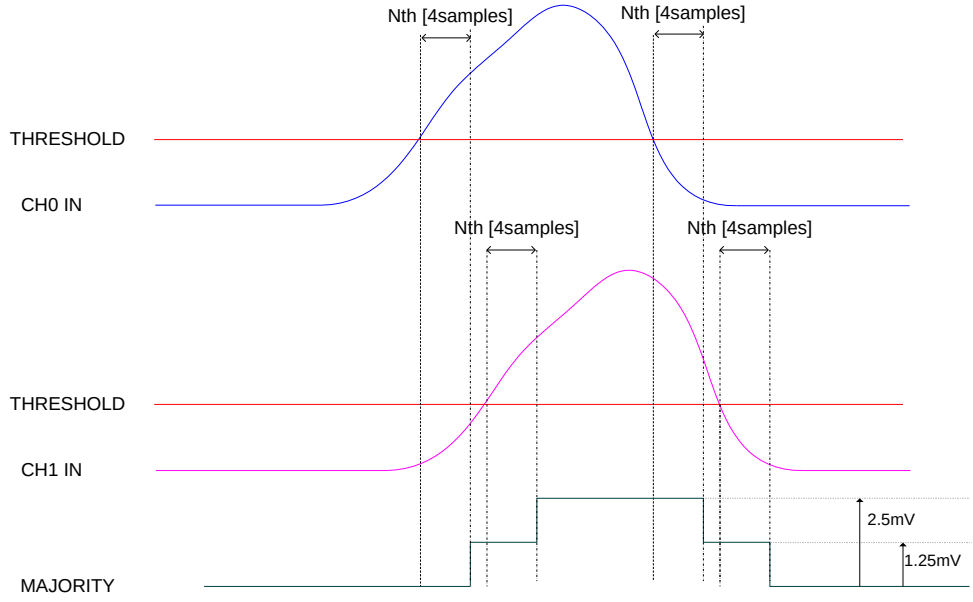


Fig. 8.18: Majority logic (2 channels over threshold; bit[6]= 0 in *Channel Configuration* register

In this mode, the MON output provides a signal whose amplitude is proportional to the number of channels over the trigger threshold. The amplitude step (= +1 channel over threshold) is 125 mV.

Test Mode (*Monitor Mode* = 001)

In this mode the MON output provides a sawtooth signal with 1-V amplitude and 24.41-kHz frequency.

Buffer Occupancy Mode (*Monitor Mode* = 011)

In this mode, MON output provides a voltage value proportional to the number of buffers filled with events (step: 1 buffer = 0.976 mV).

This mode allows to test the readout efficiency: in fact if the average event readout throughput is as fast as trigger rate, then MON out value remains constant; otherwise if MON out value grows in time, this means that readout rate is slower than trigger rate.

Voltage Level Mode (*Monitor Mode* = 100)

In this mode, MON out provides a voltage value programmable via the 12-bit 'N' parameter written in the *SET MONITOR DAC* register (0x8138), with: V_{mon} = 1/4096*N (Volt).

Test Pattern Pulser

Each input channel is equipped with an individual pulser. Whereas the pulse amplitude is fixed (~0.7 V with no cable plugged, half this value otherwise), the pattern can be programmed over 16 consecutive bits of the SAMLONG main clock and will be sent every 3.5 µs (see example on **Fig. 8.19**). This permits an easy testing of the board functionality, as well as it gives the possibility to use the board as a reflectometer. As this pulse pattern is produced from an autonomous clock source, trigger can be set on the discriminators.

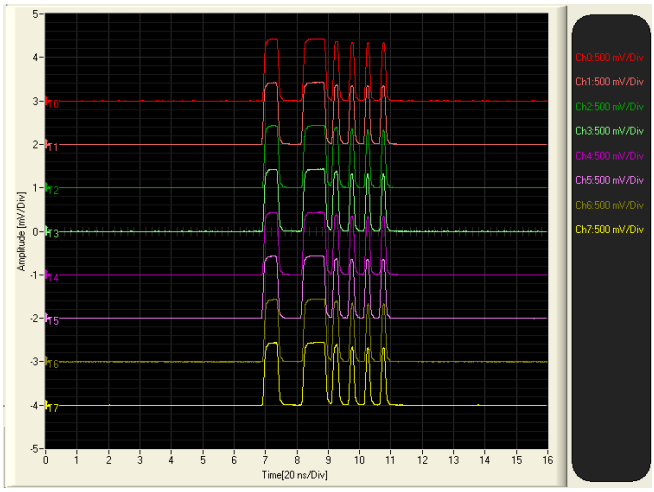


Fig. 8.19: FPGA Test Pulse with 0xC755 pattern

Each channel can make use of his pulser as a reflectometer. An example of this application is shown on **Fig. 8.20**, where a 40-ns wide square pulse produced internally is sent to a 1-meter open cable connected to the board.

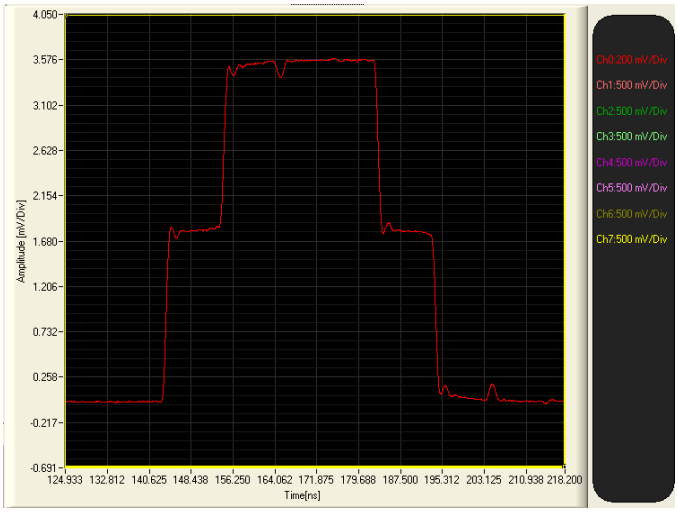


Fig. 8.20: FPGA Test Pulse in reflectometer mode

Hit Rate Monitor

Each input channel is equipped with an individual hit rate monitor. As shown on **Fig. 8.21**, the latter is based on two counters, one counting the number of hits crossing the programmed discriminator threshold (TRIG_COUNT), the other counting the time elapsed with a 1-MHz clock (TIME_COUNT). These counters are reset and restarted after each read access. Their content is stored into the event data (see § **Event Structure**). As soon as any of them saturates, both are frozen, and thus their values are always valid. The rate counters work up to ~400 MHz and, if this information is memorized long enough in the software along events, rate measurement can work as low as ~0.1 Hz.

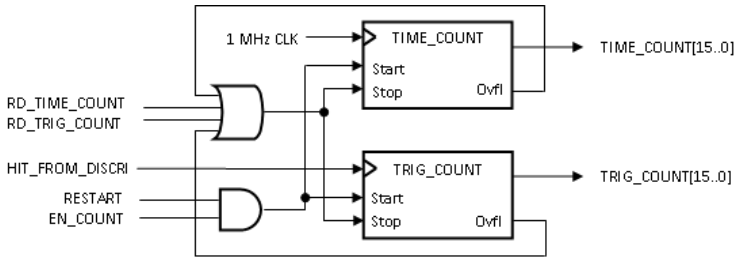


Fig. 8.21: Principle of the Hit Rate Monitor

Reset, Clear and Default Configuration

Global Reset

Global Reset is performed at Power-ON of the module or via software by write access to the *SW RESET* register. It allows to clear the data off the Output Buffer, the event counter and performs a FPGAs global reset, which restores the FPGAs to the default configuration. It initializes all counters to their initial state and clears all detected error conditions.

Memory Reset

The Memory Reset clears the data off the Output Buffer.

The Memory Reset can be forwarded via a write access to *SW CLEAR* register.

Timer Reset

The Timer Reset allows to initialize the timer which allows to tag an event. The Timer Reset can be forwarded with a pulse sent to the front panel Trigger Time Tag Reset input (see § **Front Panel LVDS I/Os**).

VMEBus Interface

The module is provided with a fully compliant VME64/VME64X interface, whose main features are:

- EUROCARD 9U Format
- J1/P1 and J2/P2 with either 160 pins (5 rows) or 96 (3 rows) connectors
- A24, A32 and CR-CSR address modes
- D32, BLT/MBLT, 2eVME, 2eSST data modes
- MCST write capability
- CBLT data transfers
- RORA interrupter
- Configuration ROM

Addressing Capabilities

- Base address: the module works in A24/A32 mode The Base Address of the module is selected through four rotary switches (see **Fig. 7.1**), then it is validated only with either a Power-ON cycle or a System Reset (see § **Global Reset**).

ADDRESS MODE	ADDRESS RANGE	NOTES
A24	[0x000000:0xFF0000]	SW2 and SW3 ignored

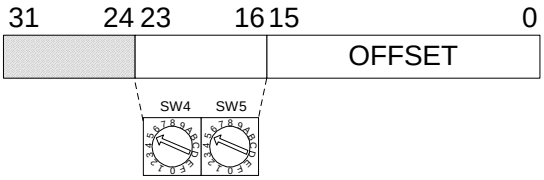


Fig. 8.22: A24 addressing

ADDRESS MODE	ADDRESS RANGE	NOTES
A32	[0x00000000:0xFFFF0000]	-

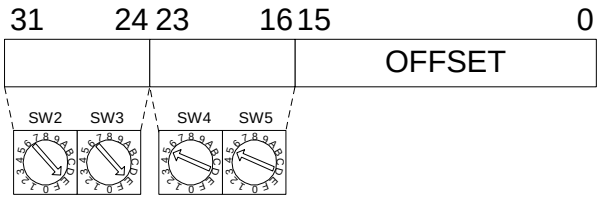


Fig. 8.23: A32 addressing

- CR/CSR address: the addressing is based on the slot number taken from the relevant backplane lines. The recognised Address Modifier for this cycle is 2F. *This feature is implemented only on versions with 160-pin connectors*.

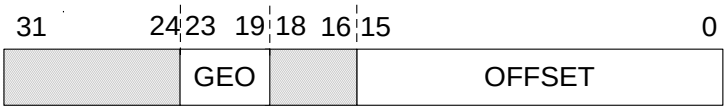


Fig. 8.24: CR/CSR addressing

Address Relocation

RELOCATION ADDRESS register (0xEF10, bits[15:0]) allows to set via software the board Base Address (valid values ≠ 0). Such register allows to overwrite the rotary switches settings; its setting is enabled via *VME CONTROL* register (0xEF00, bit[6]). The used addresses are:

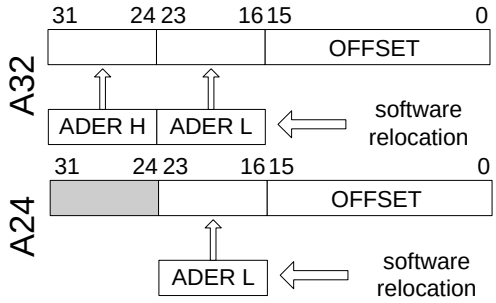


Fig. 8.25: Software relocation of base address

Data Transfer Capabilities and Events Readout

In V1743, each pair of input channels share a SRAM memory in the channel FPGA that is organized into buffers. Once they are written in the memory, events become available for readout via VMEbus or Optical Link. During the memory readout, the board can continue to store more events (independently from the readout) on the free buffers. This guarantees that no dead time due to the acquisition process (i.e. readout) occurs until the memory becomes full. The only dead time the board remains affected is due to the A/D conversion.

Although the memories are SRAMs, addresses are taken from a FIFO. Therefore, data are read from the memories sequentially, according to the selected Readout Logic, from a memory space mapped on 4 Kb (0x0000÷0x0FFC).

The events are readout sequentially and completely, starting from the Header of the first available event, followed by the Trigger Time Tag, the Event Counter and all the samples of the group channels (from 0 to 1). Once an event is completed, the relevant memory buffer becomes free and ready to be written again (old data are lost). After the last word in an event, the first word (Header) of the subsequent event is readout. It is not possible to readout an event partially.

The board supports D32 single data readout, Block Transfer BLT32 and MBLT64, 2eVME and 2eSST cycles. Sustained readout rate is up to 60 MB/s with MBLT64, up to 100 MB/s with 2eVME and up to 160 MB/s with 2eSST.

Single D32 Transfer

This mode allows to readout a word per time, from the header (actually 4 words) of the first available event, followed by all the words until the end of the event, then the second event is transferred. The exact sequence of the transferred words is shown in § **Event Structure**.

It is suggested, after the 1st word is transferred, to check the TOTAL EVENT SIZE information and then do as many cycles as necessary (actually TOTAL EVENT SIZE -1) in order to read completely the event.

Block Transfer D32/D64, 2eVME

The Block Transfer readout mode allows to read N complete events sequentially, where N is set via the *BLT EVENT NUMBER* register (address 0xEF1C) or by using the *SetMaxNumEventsBLT* function of the CAENDigitizer library (consult **[RD4]** at p. 19).

The event is configurable as indicated in the introduction of the paragraph, namely:

[Event Size] = [8*(Buffer Size)] + [16 bytes]

Then, it is necessary to perform as many cycles as required in order to readout the programmed number of events.

It is suggested to enable BERR signal during BLT32 cycles, in order to end the cycle avoiding filler readout. The last BLT32 cycle will not be completed, it will be ended by BERR after the #N event in memory is transferred (see **Fig. 8.26**).

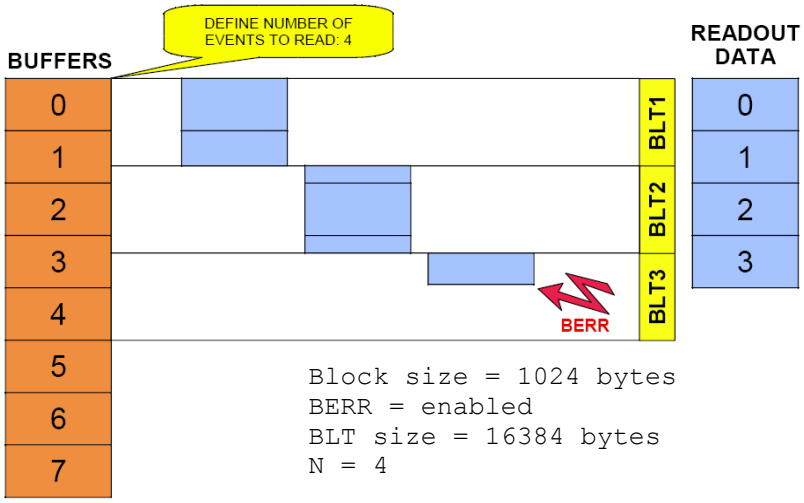


Fig. 8.26: Example of BLT readout

Since some 64-bit CPU cut off the last 32- bit word of a transferred block, if the number of words composing such block is odd, it is necessary to add a dummy word (which has then to be removed via software) in order to avoid data loss. This can be achieved by setting the ALIGN64 bit in the *VME CONTROL* register (0xEF00, bit[5]).

MBLT64 cycle is similar to the BLT32 cycle, except that the address and data lines are multiplexed to form 64 bit address and data buses.

The 2eVME allows to achieve higher transfer rates thanks to the requirement of only two edges of the two control signals (DS and DTACK) to complete a data cycle

Chained Block Transfer D32/D64

The V1743 allows to readout events from more daisy chained boards (Chained Block Transfer mode).

The technique which handles the CBLT is based on the passing of a token between the boards; it is necessary to verify that the used VME crate supports such cycles.

Several contiguous boards, in order to be daisy chained, must be configured as “first”, “intermediate” or “last” via *MCST BASE ADDRESS AND CONTROL* register. A common Base Address is then defined via the same register; when a BLT cycle is executed at the address CBLT_Base + 0x0000 ÷ 0x0FFC, the “first” board starts to transfer its data, driving DTACK properly; once the transfer is completed, the token is passed to the second board via the IACKIN-IACKOUT lines of the crate, and so on until the “last” board, which completes the data transfer and asserts BERR (which has to be enabled): the Master then ends the cycle and the slave boards are rearmed for a new acquisition.

If the size of the BLT cycle is smaller than the events size, the board which has the token waits for another BLT cycle to begin (from the point where the previous cycle has ended).

Optical Link Access

The board houses a Daisy chainable Optical Link (communication path which uses optical fiber cables as physical transmission line) able to transfer data at 80 MB/s, therefore it is possible to connect up to eight (8) V1743 to a single Optical Link Controller by using the A2818 PCI card or up to thirty-two (32) V1743 with the A3818 PCIe multi-link card. Detailed information on CAEN PCI/PCIe Controllers can be find at www.caen.it:

Home / Products / Modular Pulse Processing Electronics / PCI/PCIe / Optical Controller

The parameters for read/write accesses via Optical Link are the same used by VME cycles (Address Modifier, Base Address, data Width, etc); wrong parameter settings cause a Bus Error.

Bit[3] of the *VME CONTROL* register (address 0xEF00) allows to enable the module to broadcast an interrupt request on the Optical Link; the enabled Optical Link Controllers propagate the interrupt on the PCI bus as a request from the Optical Link is sensed.

VME and Optical Link accesses take place on independent paths and are handled by board internal controller, with VME having higher priority; anyway it is better to avoid accessing the board via VME and Optical Link simultaneously

9 Drivers & Libraries

Drivers

In order to interface with the V1743, CAEN provides the drivers for all the different types of physical communication channels featured by the board and compliant with Windows and Linux OS:

- **Optical Link Drivers** are managed by the A2818 PCI card or the A3818 PCIe card. The driver installation package is available on CAEN website in the "Software/Firmware" area at the A2818 or A3818 page (**login required**)

Note: For the installation of the Optical Link driver, refer to the User Manual of the specific Controller.

- **USB 2.0 Drivers** are managed by the V1718 USB-to-VME Bridge. The driver installation package is available on CAEN website in the "Software/Firmware" area at the V1718 page (**login required**)

Note: For the installation of the USB driver, refer to the User Manual of the V1718 Bridge.

Libraries

CAEN libraries are a set of middleware software required by CAEN software tools (including WaveCatcher) for a correct functioning. These libraries, including also demo and example programs, represent a powerful base for users who want to develop customized applications for the digitizer control (communication, configuration, readout, etc.):

- **CAENDigitizer** is a library of functions designed specifically for the Digitizer family and it supports also the boards running the DPP firmware. The CAENDigitizer library is based on the CAENComm library. For this reason, **the CAENComm libraries must be already installed on the host PC before installing the CAENDigitizer**.

  The CAENDigitizer installation package is available on CAEN website in the 'Download' area at the CAENDigitizer Library page. Reference document: **[RD4]**.

- **CAENComm** library manages the communication at low level (read and write access). The purpose of the CAENComm is to implement a common interface to the higher software layers, masking the details of the physical channel and its protocol, thus making the libraries and applications that rely on the CAENComm independent from the physical layer. Moreover, the CAENComm requires the CAENVMELib library (access to the VME bus) even in the cases where the VME is not used. This is the reason why **CAENVMELib has to be already installed on your PC before installing the CAENComm**.

  The CAENComm installation package, and the link to the required CAENVMELib, is available on CAEN website in the 'Download' area at the CAENComm Library page. Reference document: **[RD5]**.

Note: For Windows only, all libraries are automatically installed through the standalone CAEN software tools. Linux users have to install them apart.

CAENComm (and so the CAENDigitizer) supports the following communication channels:

PC → USB (V1718) → VMEbus → V1743

PC → PCI/PCIe (A2818/A3818) → CONET → V1743

PC → PCI/PCIe (A2818/A3818) → CONET (V2718) → VMEbus → V1743

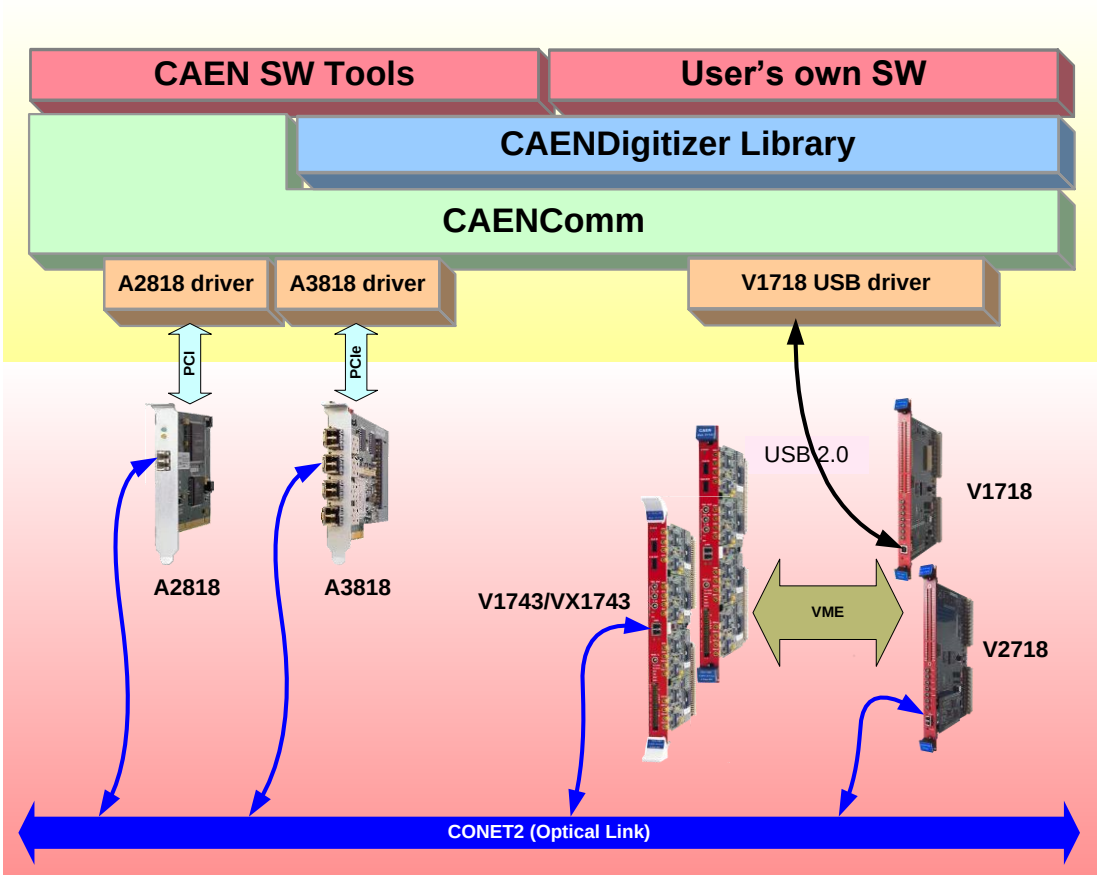


Fig. 9.1: Drivers and software layers

10 Software Tools

CAEN provides software tools to interface the V1743, which are available for free download on www.caen.it at:

Home / Products / Firmware/Software / Digitizer Software

WaveCatcher

The DT5743 can be fully controlled through the **WaveCatcher** software.

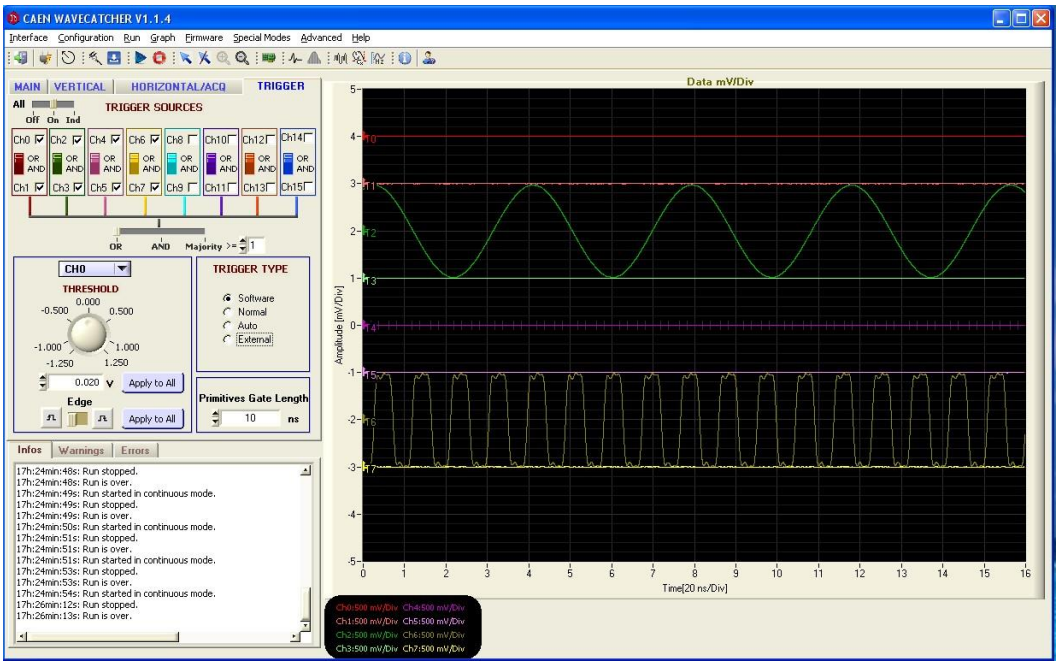


Fig. 10.1: WAVECatcher software for DT5743

WaveCatcher software is a complete oscilloscope-like tool made by CNRS/IN2P3/LAL and capable to control a single board belonging to the CAEN 743 Digitizer series.

This tool offers a graphical user friendly interface which permits to take benefit of all the functionalities of the hardware: sampling frequency, different trigger modes, waveforms and charge data acquisition, channel pulses, etc..

WaveCatcher also features different tools for on-line measurements and histograms plotting: graphical cursors, noise level, raw hit rates, charge amplitude and time measurements, time distance histograms between channels (fixed threshold and digital CFD methods), charge histograms, FFT, etc.

All acquired data and computed measurements can be saved to files for further replay or off-line analysis.

WaveCatcher installation package can be downloaded on CAEN web site **(login required)** at:

Home / Products / Firmware/Software / Digitizer Software / Readout Software / WaveCatcher

Find the program detailed description and usage descripted in **[RD6].**

Note: WaveCatcher is available for Windows OS (32 and 64-bit). The program is stand-alone (all the required CAEN libraries are installed locally with the program). Only the drivers for the specific communication link must be installed apart by the user.

CAENUpgrader

CAENUpgrader is a software composed of command line tools together with a Java Graphical User Interface.

Specifically for the DT5743, CAENUpgrader allows in few easy steps to:

- Upload different firmware versions on the board
- Select which copy of the stored firmware must be loaded at power-on.
- Read the firmware release of the board and the bridge (when used)
- upgrade the internal PLL
- get the board info file, useful in case of support

Note: CAENupgrader doesn't allow to generate the firmware file to configure the PLL. This file needs to be provided by CAEN on the user's specification through the Support service (see § **13**)

The program requires additional software to be installed: CAENComm and CAENVMELib libraries (see § **9**), and the third-party Java SE6 (or later).

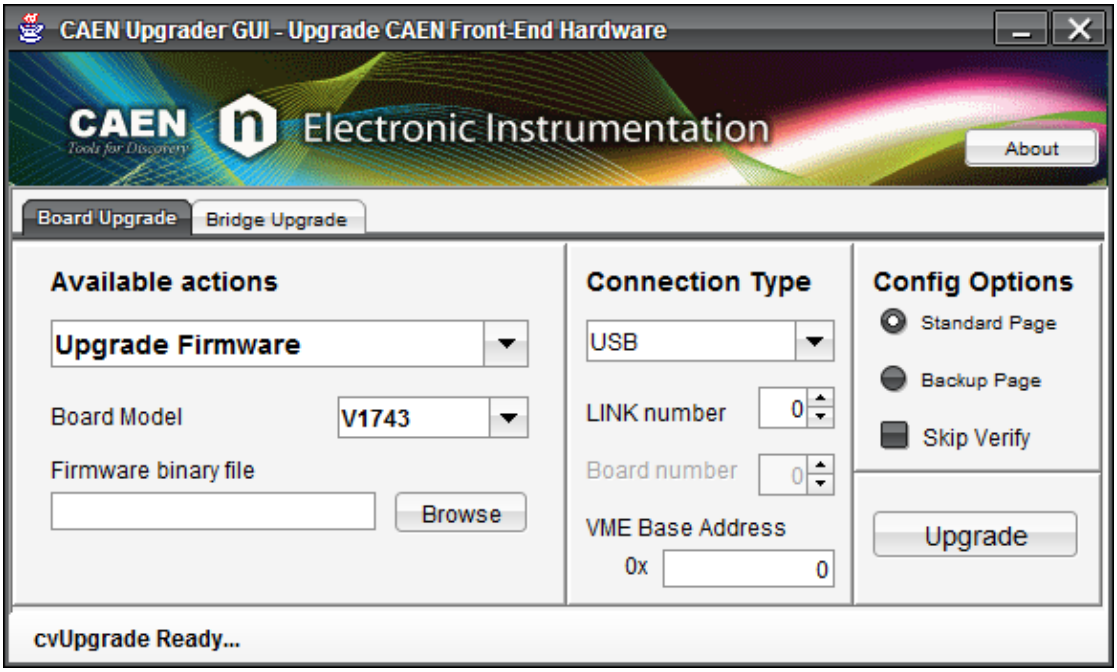


Fig. 10.2: CAENUpgrader Graphical User Interface

CAENUpgrader installation package can be downloaded on CAEN web site **(login required)** at:

Home / Products / Firmware/Software / Digitizer Software / Configuration Tools / CAENUpgrader

The reference document for installation instructions and program detailed description is **[RD1]**.

Note: Windows version of CAENUpgrader is stand-alone (all the required CAEN libraries are installed locally with the program). Only the drivers for the specific communication link must be installed apart by the user. On the opposite side, the version for Linux needs the required libraries to be already installed apart by the user.

CAENComm Demo

CAENComm Demo is a simple program developed in C/C++ source code and provided both with Java and LabVIEW GUI interface. The demo mainly allows for a full board configuration at low level by direct read/write access to the registers and may be used as a debug instrument.

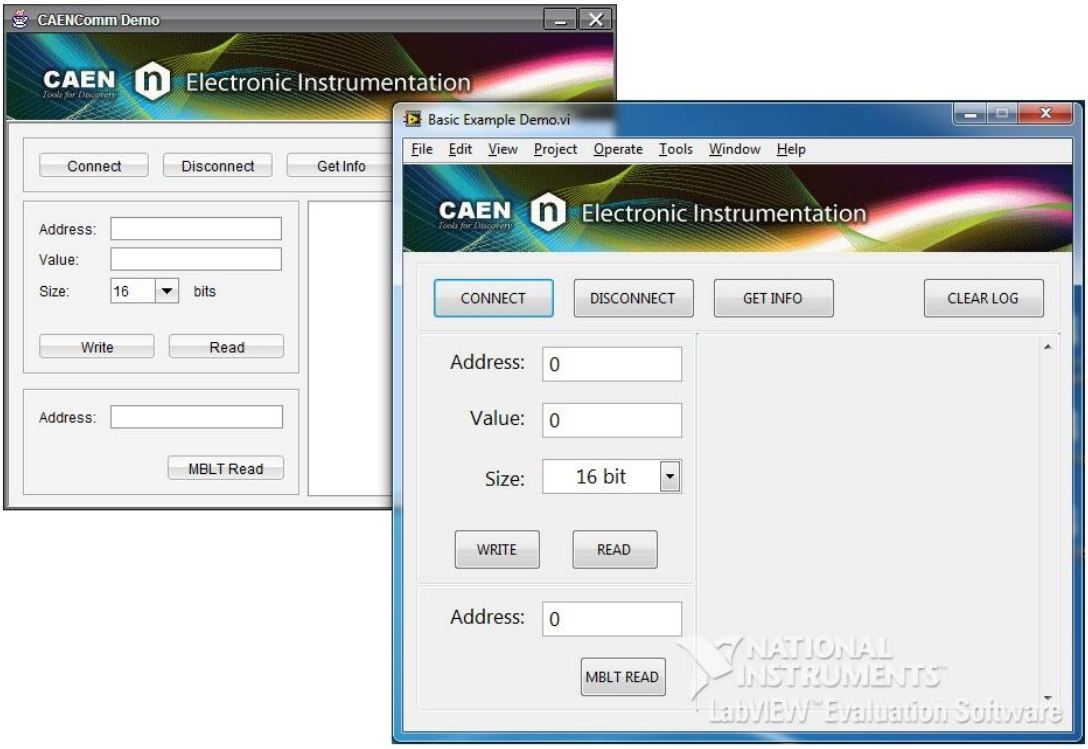


Fig. 10.3: CAENComm Demo Java and LabVIEW graphical interface

CAENComm Demo can operate with Windows OSs, 32 and 64-bit. It requires CAENComm and CAEVMElib libraries as additional software to be installed (see § **9**).

The Demo is included in the CAENComm library installation Windows package, which can be downloaded on CAEN web site (**login required**) at:

Home / Products / Firmware/Software / Digitizer Software / Software Libraries / CAENComm Library

11 HW Installation

- The V1743 fits into 6U VME crates.
- **The V1743 cannot be operated with CAEN crates VME8001/8002/8004**.
- VX1743 versions require VME64X compliant crates
- Use only crates with forced cooling air flow
- Turn the crate OFF before board insertion/removal
- Remove all cables connected to the front panel before board insertion/removal

CAUTION: this product needs proper cooling:

USE ONLY CRATES WITH FORCED COOLING AIR FLOW SINCE OVERHEAT MAY DEGRADE THE MODULE PERFORMANCES!

V1743/VX1743 CANNOT BE OPERATED WITH CAEN CRATES VME8001/8002/8004!

CAUTION: this product needs proper handling.

ALL CABLES MUST BE REMOVED FROM THE FRONT PANEL BEFORE EXTRACTING THE BOARD FROM THE CRATE!

Power ON Sequence

To power ON the board, follow this procedure:

1. Insert the V1743 into the crate;
2. power up the crate.

Power ON Status

At power ON the module is in the following status:

- the Output Buffer is cleared;
- registers are set to their default configuration

After the power ON, the front panel LEDs status is that only the NIM and PLL LOCK remain ON (see **Fig. 11.1**).

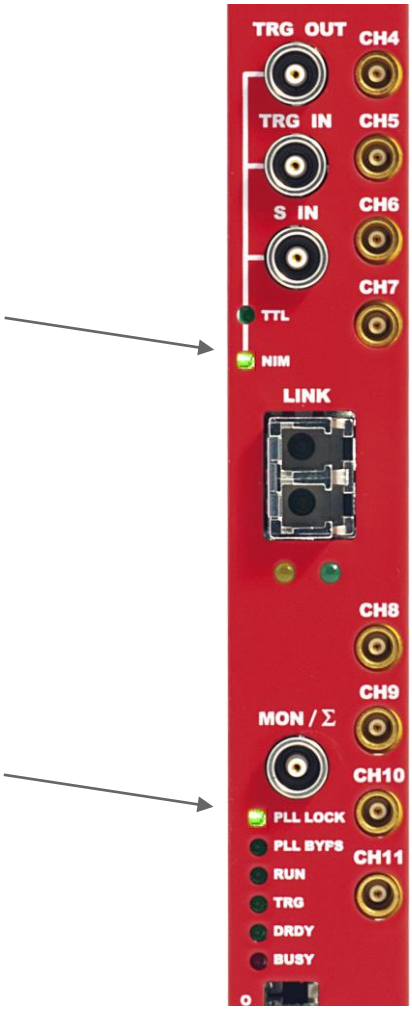


Fig. 11.1: Front panel LEDs status at power ON

12 Firmware Upgrades

The board hosts one FPGA on the mainboard and one FPGA on each mezzanine (i.e. one FPGA per 4 channels). The channel FPGAs firmware is identical. A unique file is provided that will updated all the FPGAs at the same time.

ROC FPGA MAINBOARD FPGA (Readout Controller + VME interface):

FPGA Altera Cyclone EP1C20.

AMC FPGA CHANNEL FPGA (ADC readout/Memory Controller):

FPGA Altera Cyclone EP3C16

The firmware is stored onto on-board FLASH memory. Two copies of the firmware are stored in two different pages of the FLASH, called Standard (STD) and Backup (BKP).

At Power-ON, a microcontroller reads the FLASH memory and programs the module with the firmware version that is the STD one by default.

VME digitizers in the 740 family are equipped with an on-board dedicated SW1 dip switch, set on STD position by default, allowing to select the FLASH page to be read at power-on (see § **7**).

Firmware updates are available for download on CAEN website (www.caen.it) in the “Software/Firmware” tab at the DT5743 web page **(login required)**.

It is possible to upgrade the board firmware via VMEbus or Optical Link by writing the FLASH with the CAENUpgrader software (see § **10**).

IT IS STRONGLY SUGGESTED TO OPERATE THE DIGITIZER UPON THE STD COPY OF THE FIRMWARE. UPGRADES ARE SO RECOMMENDED ONLY ON THE STD PAGE OF THE FLASH. THE BKP COPY IS TO BE INTENDED ONLY FOR RECOVERY USAGE. IF BOTH PAGES RESULT CORRUPTED, THE USER WILL NO LONGER BE ABLE TO UPLOAD THE FIRMWARE VIA USB OR OPTICAL LINK AGAIN AND THE BOARD NEEDS TO BE SENT TO CAEN IN REPAIR!

In case of failures while programming the STD page of the FLASH, which compromise the communication with the V1743, the user can perform the following recovering procedure as first attempt:

- Force the board to reboot loading the copy of the firmware stored on the BKP page of the FLASH. For this purpose, power off the crate, switch the dedicated SW1 switch to BKP position and power on the crate.

- Use CAENUpgrader to read the firmware revision (in this case the one of the BKP copy). If this succeeds, it is possible now to communicate again with the board.

- Use CAENUpgrader to load again the firmware on the STD page, then power-cycle in order the board to get operative again.

In case also this procedure fails, the board needs to be sent back to CAEN in repair (see § **13** for contacts).

Firmware File Description

The programming file, that has the extension ***.cfa*** (CAEN Firmware Archive), is a sort of archive format file aggregating all the DPP firmware files compatible with the same family of digitizers.

The firmware file name follows this general scheme:

CFA and its name follows this general scheme:

x743_revX.Y_W.Z.CFA

where:

- x743 are all the boards the file is compliant to: DT5743, N6743, V1743, VX1743
- X.Y is the major/minor revision number of the mainboard FPGA

W.Z is the major/minor revision number of the channel FPGA

13 Technical Support

CAEN support services are available for the user by accessing the *Support & Services* area on CAEN website at www.caen.it.

Returns and Repairs

Users who need for product(s) return and repair have to fill and send the Product Return Form (PRF) in the *Returns and Repairs* area at *Home / Support & Services*, describing the specific failure. A printed copy of the PRF must also be included in the package to be shipped.

Contacts for shipping are reported on the website at *Home / Contacts*.

Technical Support Service

CAEN makes available the technical support of its specialists at the e-mail addresses below:

support.nuclear@caen.it
(for questions about the hardware)

support.computing@caen.it
(for questions about software and libraries)

CAEN SpA is acknowledged as the only company in the world providing a complete range of High/Low Voltage Power Supply systems and Front-End/Data Acquisition modules which meet IEEE Standards for Nuclear and Particle Physics. Extensive Research and Development capabilities have allowed CAEN SpA to play an important, long term role in this field. Our activities have always been at the forefront of technology, thanks to years of intensive collaborations with the most important Research Centres of the world. Our products appeal to a wide range of customers including engineers, scientists and technical professionals who all trust them to help achieve their goals faster and more effectively.

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