TENTATIVE Lecture and Lab Schedule for ECE 241F, 2018

Sept 30 Developes of the course topics convoid, many hospidopen (middler list), and the convoided from the list is executed to the convoided from the list is executed to the convoided from the convoided	Week	Topics covered	Textbook Sections	Lab Exercises
Braary numbers, hex numbers Introduction to logic expressions. AND, OR, NOT directs ball using switches. AND, OR, NOT gates Boolean applicar (stall), adoms, nules, identities; proof of identities using perfect induction (i.e., furit habbes, rigipation empirylation of Boolean expressions; liming diagrams, when labeles are induction (i.e., furit habbes, rigipation empirylation of Boolean expressions; liming diagrams, when Department and fertic sate price semi-identities Simple synthesis of logic circuits; sum-deproductis (SOP) form; minterms; canonical SOP; product-of-earse from (POS); marderms; canonical POS; examples of the label Label Example logic functions; 2-to-1 multiplexer, XOR gate, full-adder, right-carry adder, 2-7, 2-8, 3-2 Sept 14 Example logic functions; 2-to-1 multiplexer, XOR gate, full-adder, right-carry adder, 2-7, 2-8, 3-2 Form (MAM) and MOR logic retrovies; convert SOP is NAND-NAND, POS is NOR-NON. Verifig introduction, including hierarchy Verifig introduction, including hierarchy Appendix A Sept 24 Introduction to Fleat Programmable Gate Arrays (FPCAs), lockup tables; Introduction to Fleat Programmable Gate Arrays (FPCAs), lockup tables; Introduction to Fleat Programmable Gate Arrays (FPCAs), lockup tables; Introduction to CAD tools in CAD tools in CAD tools in CAD tools introduction to K-rape (2-3, 4 variables), More examples of K-rape use, including as gaide to adject in maripulation Oxt Introduction to CAD tools in CAD too	Sept 3	exam), overview of how the lab exercises are organized (students work in groups of two), marks assigned for preparation and lab performance); Quick overview of digital systems and Moore's law, examples of digital systems; Transistors as simple on-off switches	Chapter 1	
Introduction to logic expressions, AND, OR, NOT circuits built using evitches; AND, OR, VOT gate exprosions tutul tables, simple example of logic corout with AND, OR, OR, OR, VOT gate exprosions tutul tables, simple example of logic corout with AND, OR, OR, OR, OR, OR, OR, OR, OR, OR, OR	Sept 10	Project intro, videos		
OR, NOT gates primote, tuth tables; simple example of logic circuit with AND, OR, NOT gate symbols, superiority pates Bootean algebra: duality, actions, utilise; proof of identities using perfert induction (i.e., tuth babes; algebraic anaptiation of Bootean cresscens; firming diagrams; Vern Diagrams and their use to prove some identities Simple symbles of logic circuits sum-of-protecties (SOP) beam, minterms; canonical slophic manipulation Infroit to Lab 1 Sept 17 Sept NAND and NOR logic networks; convert SOP to NAND-NAND, POS to NOR-NOR-NOR-NOR-NOR-NOR-NOR-NOR-NOR-NOR-		Binary numbers, hex numbers	3.1	
induction (i.e., tith labeles), algebraic manipulation of Boolean expressions; timing diagrams; Ven Degarram and their use to provide some identifies of a project and their use to provide some interest of soft product-of-sums from (PS)s; maximum of more and production of the production of the production of the project and published manipulation into Lab 1 Sept 17 Fearing Product-of-sum strong (PS)s; maximum of productions; 250-7 multiplesser, XOR gate, full added, rypole-carry adder, 70-7-7, 47-7, 47-7-		OR, NOT gate symbols; truth tables; simple example of logic circuit with AND, OR,	2.1 – 2.4	
SOP, product-for-sums from (POS); maxterms; canonical POS; examples of algebraic manipulation. Intro La La 1 Intro La La 1 Intro La 1 Sept 17 Expr 17 Expr 18 Sept 17 Expr 18 Verilog introduction, including hierarchy Verilog introduction in Field Programmable Gate Arrays (FPGAs), lookup tables; introduction to Field Programmable Gate Arrays (FPGAs), lookup tables; introduction to GAD tools Introduction to Cast of a logic circuit terminology implicant, prime implicant (Ph), essential Ph, cover, minimum-cost cover; introduction to Knapp, dorthough intro		induction (i.e., truth tables); algebraic manipulation of Boolean expressions; timing	2.5	
Example logic functions: 2-lo-1 multiplexer, XOR gate, full-adder, ripple-carry adder, Project 2, 28, 3.2 Lab 1: Building Circuits Using 7400-Series Chips 7-7-89, NADD and NOR logic networks; convert SOP to NAND-NAND, POS to NOR NOR. Verilog introduction, including hierarchy Verilog introduction, including hierarchy Verilog introduction, including hierarchy Verilog introduction to Field Programmable Gate Arrays (FPGAs), lookup tables: Introduction to Field Programmable Gate Arrays (FPGAs), lookup tables: Introduction to CAD tools Verilog circuit, terminology: implicant, prime implicant (PI), sesential PI, cover, minimum-cost cover; introduction to K-maps (2, 3, 4 variables) More examples of K-maps use, including as a guide to adjectivate manipulation Verilog latches in Irelay case statements Verilog Istiches in Irelay, case statements Verilog Istiches in Irelay Verilog Istiches in Irelay, case statements Verilog Istiches in Irelay Verilog Istiches Istiches Verilog Istiches Verilog Istiches Verilog Istiches		SOP; product-of-sums form (POS); maxterms; canonical POS; examples of	2.6	
7-seg: NAND and NOR logic networks; convert SÖP to NAND-NAND, POS to NOR-NOR. Verilog introduction, including hierarchy 2		Intro to Lab 1	B.5	
Appendix A Bott State Machines Worling, and can consider also do the version but use Verling, and can consider also doing the Schematic design the Sch	Sept 17	7-seg; NAND and NOR logic networks; convert SOP to NAND-NAND, POS to NOR-	2.7, 2.8, 3.2	Lab 1: Building Circuits Using 7400-Series Chips
Introduction to Field Programmable Gate Arrays (FPGAs), lookup tables; Introduction to Cot Dotols Introduction to Cot Programmable Gate Arrays (FPGAs), lookup tables; Introduction to to cost of a logic circuit; terminology: implicant, prime implicant (PI), essential PI, cover, minimum-cost cover, introduction to K-maps (2, 3, 4 variables) More examples of K-maps use, including as a quide to algebraic mainplation 2.8.3 Lab 2: Multiplexers, Hierarchy, and HEX Displays Multiplexe		Verilog introduction, including hierarchy		Quartus Introduction (you must at least do the version that uses Verilog, and can consider also doing the Schematic design version). Download tutorials from https://www.altera.com/support/training/university/materials-tutorials.html ; perform tutorial steps outside of
sesential PI, cover, minimum-cost cover, introduction to K-maps (2, 3.4 variables) More examples of K-maps use, including as a guide to algebraic manipulation Oct 1	Sept 24		B.6.5, 2.9	are tab using simulation only
Svariable K-maps; don't cares, examples, including 7-seg with don't cares 2.8.3		essential PI, cover, minimum-cost cover; introduction to K-maps (2, 3, 4 variables)	2.11 – 2.14	Lab 2: Multiplexers, Hierarchy, and HEX Displays
Gated D latch, D flip-flops, Filip-flop reset/preset, setup and hold times Verilog latches in if-else, case statements Registers, shift registers, Verilog for registers, blocking vs non-blocking FFs in FPGAs Oct 15 Counters: ripple and synchronous counters; Verilog for counters, enable inputs Timing, skew Oct 22 Finite state machines intro ESM state assignment, binary encoding, one-hot, Verilog code for FSMs Cary lookahead adders, multipliers Nov 5 Signed numbers; 2's complement; adders/subtractors, arithmetic overflow Carry lookahead adders, multipliers Nov 12 Arithmetic coding with Verilog Combinational circuits: implementing logic functions using only multiplexers, Shannon's Expansion Logic Synthesis using LUTs Nov 26 Nov 26 More simple processor Transistors and gates, structure Passing 1's and 0's, transmission gates, fan-in	Oct 1		2.8.3	
Oct 8 Verilog latches in if-else, case statements			5.1 - 5.4, 5.7	Lab 3: The case statement, Adders, and ALUs
Registers, shift registers, Verilog for registers, blocking vs non-blocking FFs in FPGAs Oct 15 Oct 15 Oct 27 FFs in FPGAs Oct 29 FSM state assignment, binary encoding, one-hot, Verilog code for FSMs FSM state assignment, binary encoding, one-hot, Verilog code for FSMs Oct 29 FSM timing issues (Moore vs Mealy models) RAM and ROM, including FPGA embedded memory Discussion of course project, incl VGA and videos Nov 5 Signed numbers; 2's complement, adders/subtractors, arithmetic overflow Carry lookahead adders, multipliers Nov 12 Arithmetic coding with Verilog Combinational circuits: implementing logic functions using only multiplexers, Shannon's Expansion Logic Synthesis using LUTs Nov 19 Decoders, other combinational circuits; Verilog code FSM State Minimization Design example: Introduction to processors Transistors and gates, structure Passing 1's and 0's, transmission gates, fan-in S, 5, 5, 10, 5, 13 S, 5, 5 Lab 4: Latches, Flip-flops, and Registers Lab 5: Clocks and Counters 6, 2, 6, 4, 6, 5 6, 2, 6, 4, 6, 5 B, 9 Lab 6: Finite State Machines Lab 7: Memory and VGA Display Lab 7: Memory and VGA Display Froject 1 B, 6, 5 Nov 19 Project 2 Project 2 Project 3 Project 3	Oct 8		A.11.1 – A.11.4	Thanksgiving Monday Oct. 8, 2018
FFs in FPGAs		Registers, shift registers, Verilog for registers, blocking vs non-blocking		
Counters; ripple and synchronous counters; Verilog for counters, enable inputs Timing, skew Oct 22 Finite state machines intro FSM state assignment, binary encoding, one-hot, Verilog code for FSMs Oct 29 FSM timing issues (Moore vs Mealy models) RAM and ROM, including FPGA embedded memory Discussion of course project, incl VGA and videos Nov 5 Signed numbers; 2's complement; adders/subtractors, arithmetic overflow Carry lookahead adders, multipliers Nov 12 Arithmetic coding with Verilog Combinational circuits: implementing logic functions using only multiplexers, Shannon's Expansion Logic Synthesis using LUTs Nov 19 Decoders, other combinational circuits; Verilog code FSM State Minimization Design example: Introduction to processors Nov 26 More simple processor Transistors and gates, structure Passing 1's and 0's, transmission gates, fan-in Lab 5: Clocks and Counters 6.2, 6.4, 6.5 6.3 Lab 6: Finite State Machines Lab 7: Memory and VGA Display 1. A 1. Project 1 Project 1 Project 2 Project 2 Project 3 Project 3				
Finite state machines intro FSM state assignment, binary encoding, one-hot, Verilog code for FSMs 6.2, 6.4, 6.5	Oct 15			Lab 4: Latches, Flip-flops, and Registers
FSM state assignment, binary encoding, one-hot, Verilog code for FSMs Oct 29 FSM timing issues (Moore vs Mealy models) RAM and ROM, including FPGA embedded memory Discussion of course project, incl VGA and videos Nov 5 Signed numbers; 2's complement; adders/subtractors, arithmetic overflow Carry lookahead adders, multipliers Nov 12 Arithmetic coding with Verilog Combinational circuits: implementing logic functions using only multiplexers, Shannon's Expansion Logic Synthesis using LUTs Nov 19 Decoders, other combinational circuits; Verilog code FSM State Minimization Design example: Introduction to processors Nov 26 More simple processor Transistors and gates, structure Passing 1's and 0's, transmission gates, fan-in RAM and ROM, including FPGA embedded memory B.9. B.9 Lab 6: Finite State Machines Lab 7: Memory and VGA Display A.1 Project 1 Project 1 Project 1 Project 2 Project 2 Project 2 Project 3 Project 3	Oct 22			
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Discussion of course project, incl VGA and videos Nov 5 Signed numbers; 2's complement; adders/subtractors, arithmetic overflow Carry lookahead adders, multipliers Nov 12 Arithmetic coding with Verilog Combinational circuits: implementing logic functions using only multiplexers, Shannon's Expansion Logic Synthesis using LUTs Nov 19 Decoders, other combinational circuits; Verilog code FSM State Minimization Design example: Introduction to processors Nov 26 More simple processor Transistors and gates, structure Passing 1's and 0's, transmission gates, fan-in Project 3 Project 3 Project 3	Oct 29			
Carry lookahead adders, multipliers 8.4, 3.6 Nov 12 Arithmetic coding with Verilog Combinational circuits: implementing logic functions using only multiplexers, Shannon's Expansion Logic Synthesis using LUTs 8.6.5 Nov 19 Decoders, other combinational circuits; Verilog code FSM State Minimization FSM State More simple processor Transistors and gates, structure Passing 1's and 0's, transmission gates, fan-in Lab 7: Memory and VGA Display A.1 Project 1 Project 1 Project 2 Project 2 Project 3			B.9	Lab 6: Finite State Machines
Carry lookahead adders, multipliers 3.4, 3.6 Nov 12 Arithmetic coding with Verilog Combinational circuits: implementing logic functions using only multiplexers, Shannon's Expansion Logic Synthesis using LUTs Nov 19 Decoders, other combinational circuits; Verilog code FSM State Minimization Design example: Introduction to processors Transistors and gates, structure Passing 1's and 0's, transmission gates, fan-in A.1 Project 1 B.6.5 Project 2 Project 2 Project 3	Nov 5	Signed numbers; 2's complement; adders/subtractors, arithmetic overflow	3.3	
Combinational circuits: implementing logic functions using only multiplexers, Shannon's Expansion Logic Synthesis using LUTs Nov 19 Decoders, other combinational circuits; Verilog code FSM State Minimization Design example: Introduction to processors Nov 26 More simple processor Transistors and gates, structure Passing 1's and 0's, transmission gates, fan-in Project 1 Project 1 Project 1 Project 2 Project 2 Project 2 Project 3		Carry lookahead adders, multipliers	3.4, 3.6	Lab 7: Memory and VGA Display
Combinational circuits: implementing logic functions using only multiplexers, Shannon's Expansion Logic Synthesis using LUTs Nov 19 Decoders, other combinational circuits; Verilog code FSM State Minimization Design example: Introduction to processors Nov 26 More simple processor Transistors and gates, structure Passing 1's and 0's, transmission gates, fan-in Project 1 Project 1 Project 1 Project 2 Project 2 Project 2 Project 3	Nov 12	Arithmetic coding with Verilog	3.5	
Shannon's Expansion Logic Synthesis using LUTs Nov 19 Decoders, other combinational circuits; Verilog code FSM State Minimization Design example: Introduction to processors Nov 26 More simple processor Transistors and gates, structure Passing 1's and 0's, transmission gates, fan-in B.6.5 Project 2 Project 2 Project 3 Project 3				Project 1
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Nov 26 More simple processor Transistors and gates, structure Passing 1's and 0's, transmission gates, fan-in B.1 – B.3, B.8.1 B.8.7 – B.8.9		•	6.6	Project 2
Transistors and gates, structure Passing 1's and 0's, transmission gates, fan-in B.1 – B.3, B.8.1 B.8.7 – B.8.9		Design example: Introduction to processors	7.1 – 7.2	
Transistors and gates, structure B.1 – B.3, B.8.1 Passing 1's and 0's, transmission gates, fan-in B.8.7 – B.8.9	Nov 26	More simple processor		Project 3
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	Dec 3			

Informal tutorials will be held commencing Tuesday Sept. 11, 6-7pm, room is MY306, except October 16 in GB244.