

Jordan Ditzler
ECE 448-201
Lab 1 Report

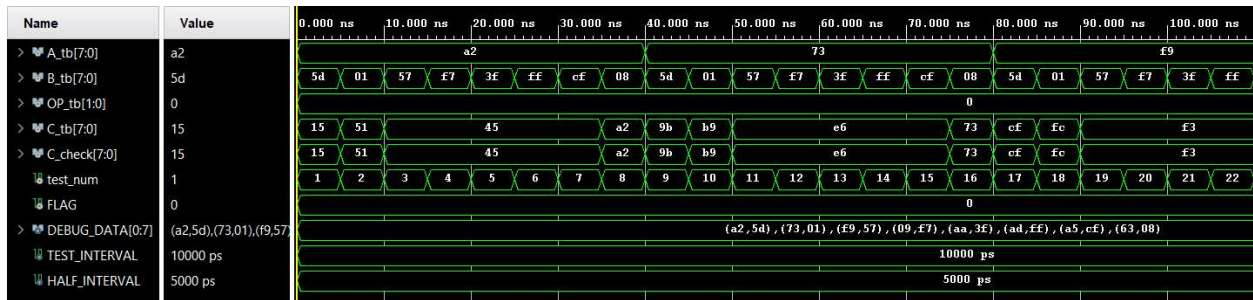
Introduction

We are to develop testbenches in VHDL for the given PSMs, find out which are faulty, and report on what about the respective faulty PSM is wrong.

Tasks

Part 1

CVRS_PSM_1 Report



```

Tcl Console  x Messages  Log
[Icons: Search, Zoom In, Zoom Out, Run, Stop, Refresh, Save, Delete]

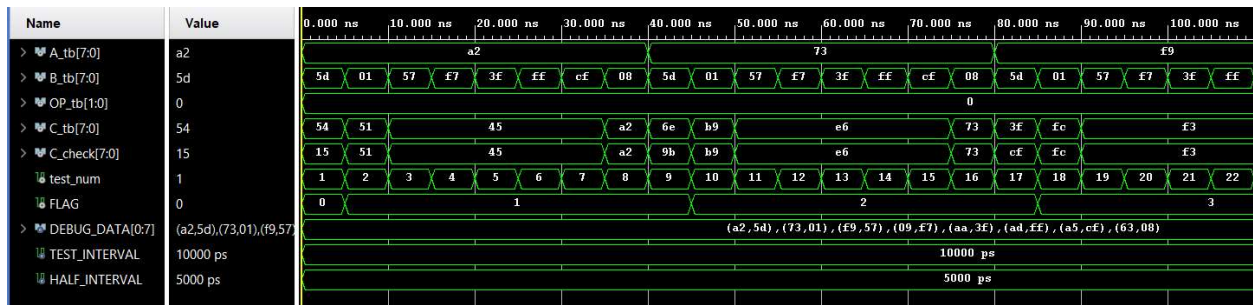
# if { [string length $curr_wave] == 0 } {
#   if { [llength [get_objects]] > 0 } {
#     add_wave /
#     set_property needs_save false [current_wave_config]
#   } else {
#     send_msg_id Add_Wave-1 WARNING "No top level signals found. Simulator
#   }
# }
# }

# run 1500ns
Ran 256 tests and all succeeded!
Note: End of testbench.
Time: 1300 ns  Iteration: 0  Process: /CVRS_tb/simulation  File: C:/Users/Jo:
INFO: [USF-XSim-96] XSim completed. Design snapshot 'CVRS_tb_behav' loaded.
INFO: [USF-XSim-97] XSim simulation ran for 1500ns
launch_simulation: Time (s): cpu = 00:00:02 ; elapsed = 00:00:08 . Memory (M

```

CVRS_PSM_1 is not faulty and is working as intended.

CVRS_PSM_2 Report



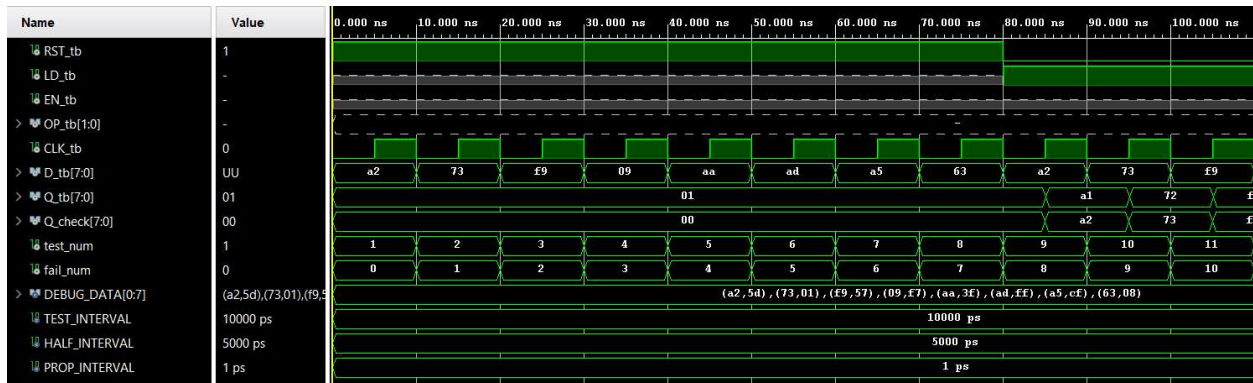
Tcl Console × **Messages** **Log**

C expected was '0'0'0'0'0'0'0'0'0'0' but C actual was '1'1'1'1'1'1'1'1'1'1'.
 Test #245 failed!
 C expected was '0'0'0'0'0'0'0'0'0'0'0' but C actual was '1'1'1'1'1'1'1'1'1'1'.
 Test #246 failed!
 C expected was '0'0'0'0'0'0'0'0'0'0'0' but C actual was '1'1'1'1'1'1'1'1'1'1'.
 Test #247 failed!
 C expected was '0'0'0'0'0'0'0'0'0'0'0' but C actual was '1'1'1'1'1'1'1'1'1'1'.
 Test #248 failed!
 C expected was '0'0'0'0'0'0'0'0'0'0'0' but C actual was '1'1'1'1'1'1'1'1'1'1'.
 Ran 256 tests and 89 failed!
 PSM calculations are not accurate!
 Note: End of testbench.
 Time: 1300 ns Iteration: 0 Process: /CVRS tb/simulation File: C:/Users/Jordan/Doc

CVRS_PSM_2 is faulty and is NOT working as intended. For opcodes “00” and “01 (ror and rol respectively), the PSM is prone to error on the first cycle after A has changed. For opcodes “10” and “11” (sra and sll respectively), the PSM is prone to error throughout the entire testing phase and follows no obvious pattern. During these opcodes, only some A values will produce a correct result, while other A values will fail to produce any correct result.

Part 2

SRS_PSM_1 Report



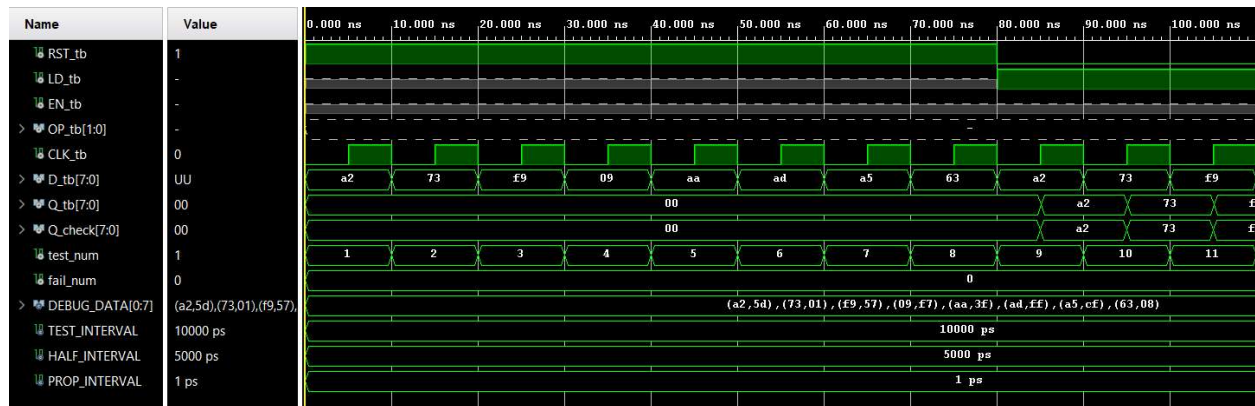
```

Tcl Console x Messages Log
Q expected was '0'0'1'1'1'0'0'0'0'1' but Q actual was '0'1'0'0'0'0'0'0'0'.
Test #44 failed!
Q expected was '0'1'1'1'0'0'0'0'1'0' but Q actual was '0'0'0'0'0'0'0'0'0'.
Test #45 failed!
Q expected was '0'0'1'1'1'0'0'0'0'1' but Q actual was '0'0'0'0'0'0'0'0'0'.
Test #46 failed!
Q expected was '0'1'1'1'0'0'0'0'1'0' but Q actual was '0'0'0'0'0'0'0'0'0'.
Test #47 failed!
Q expected was '0'0'1'1'1'0'0'0'0'1' but Q actual was '0'0'0'0'0'0'0'0'0'.
Test #48 failed!
Q expected was '0'1'1'1'0'0'0'0'1'0' but Q actual was '0'0'0'0'0'0'0'0'0'.
Ran 48 tests and 46 failed!
PSM calculations are not accurate!
Note: End of testbench.
Time: 480003 ps Iteration: 0 Process: /SRS_tb/simulation File: C:/Users/Jordan/Doc
INFO: [USF-XSim-96] XSim completed. Design snapshot 'SRS_tb_behav' loaded.

```

SRS_PSM_1 is faulty and is NOT working as intended. The RST signal does not make the output x00, but rather makes it x01. The LD signal does not set Q to D, but rather sets it to D - 1. While the EN signal is HI, none of the OP signals work as intended and all are wrong.

SRS_PSM_2 Report



```

Tcl Console x Messages Log
[Icons]

#   } else {
#       send_msg_id Add_Wave-1 WARNING "No top level signals found. Simulat
#   }
# }
# run 1000ns
Ran 48 tests and all succeeded!
Note: End of testbench.
Time: 480003 ps Iteration: 0 Process: /SRS_tb/simulation File: C:/Users
INFO: [USF-XSim-96] XSim completed. Design snapshot 'SRS_tb_behav' loaded.
INFO: [USF-XSim-97] XSim simulation ran for 1000ns
launch_simulation: Time (s): cpu = 00:00:02 ; elapsed = 00:00:08 . Memory

```

CVRS_PSM_1 is not faulty and is working as intended.