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ECE 448-201

Lab 4 Report

List of Completed Tasks

- Task 1: Browsing/Idle Mode
- Task 2: Software Random Initialization
- Task 3: Sorting
- Task 4: Cycle Count Display Mode
- Task 5: Changeable Size of Memory to Sort

Execution Time for $14 \geq k \geq 9$

k Value	Hardware Clock Cycles	Hardware Time (ms)	Software Clock Cycles	Software Time (ms)	Ratio of Execution Time
9	262307	2624	4225049	42251	16.10726744
10	1048727	10488	16839623	168397	16.05720364
11	4194475	41945	67237719	672378	16.03006789
12	16777399	167775	268697353	2686974	16.01543559
13	67109027	671091	1074275123	10742752	16.00790789
14	268435607	2684357	4296055835	42960559	16.00404612

Resource Utilization

#Slices	#LUTs	#FFs	#BRAMs
680	1853	1553	40

Conclusion

The hardware-accelerated sorting algorithm was roughly 16x more efficient in sorting than its c++ software counterpart. This speed increase is massive, and honestly very surprising; I've heard of hardware acceleration being used before, but I had no idea of the speed benefits it provided. Selection sort was implemented for the software sorting algorithm. All base tasks were completed and are working correctly. The bonus task was not attempted.