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ECE 448-201

# Lab 1 Report

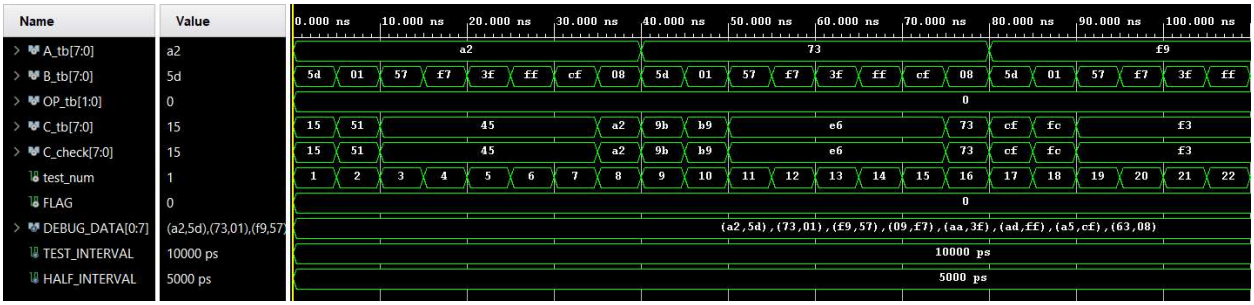
# Introduction

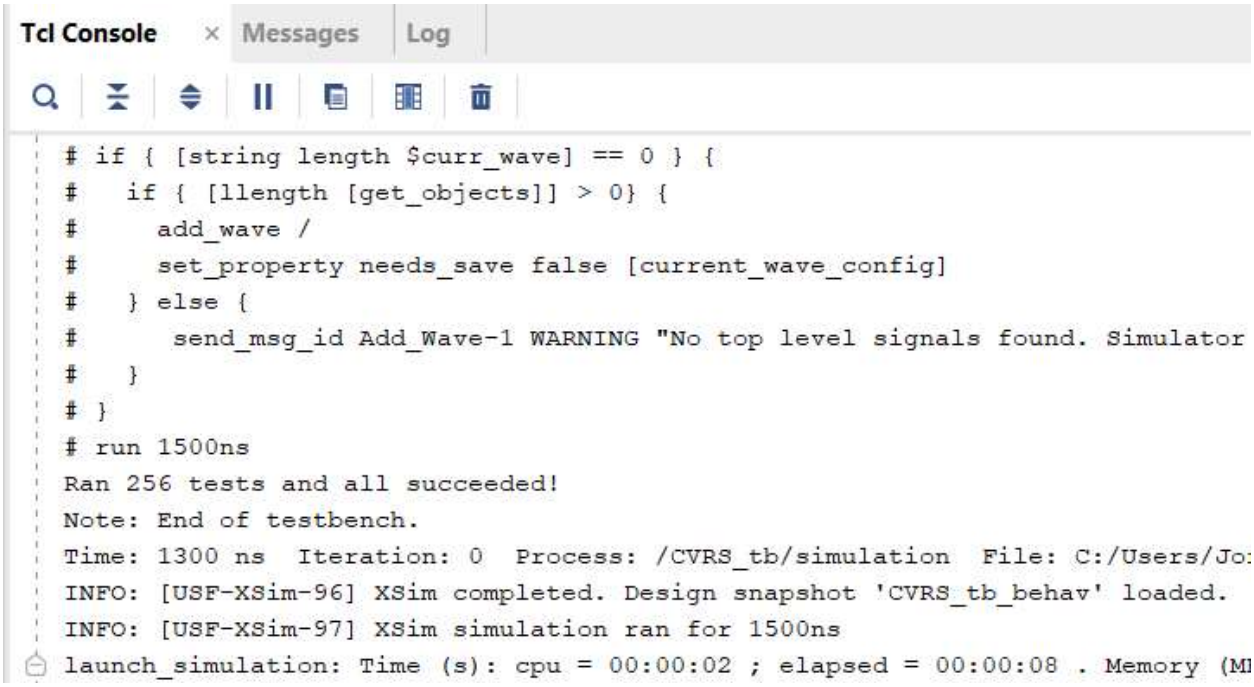
We are to develop testbenches in VHDL for the given PSMs, find out which are faulty, and report on what about the respective faulty PSM is wrong.

# Tasks

## Part 1

CVRS_PSM_1 Report




CVRS_PSM_1 is not faulty and is working as intended.

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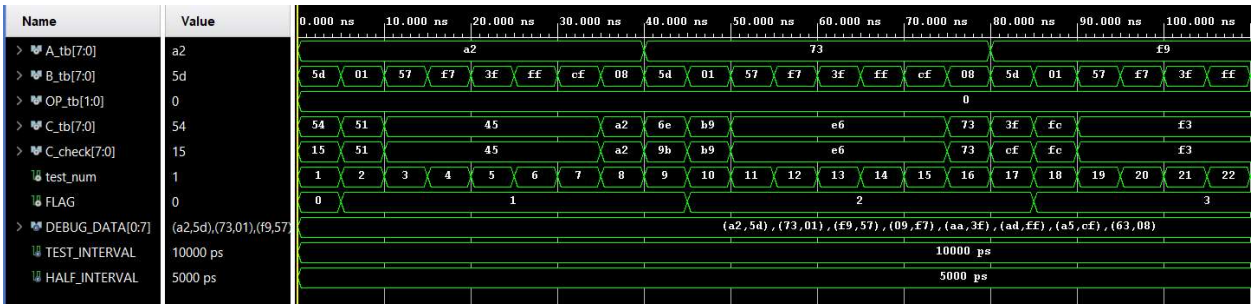
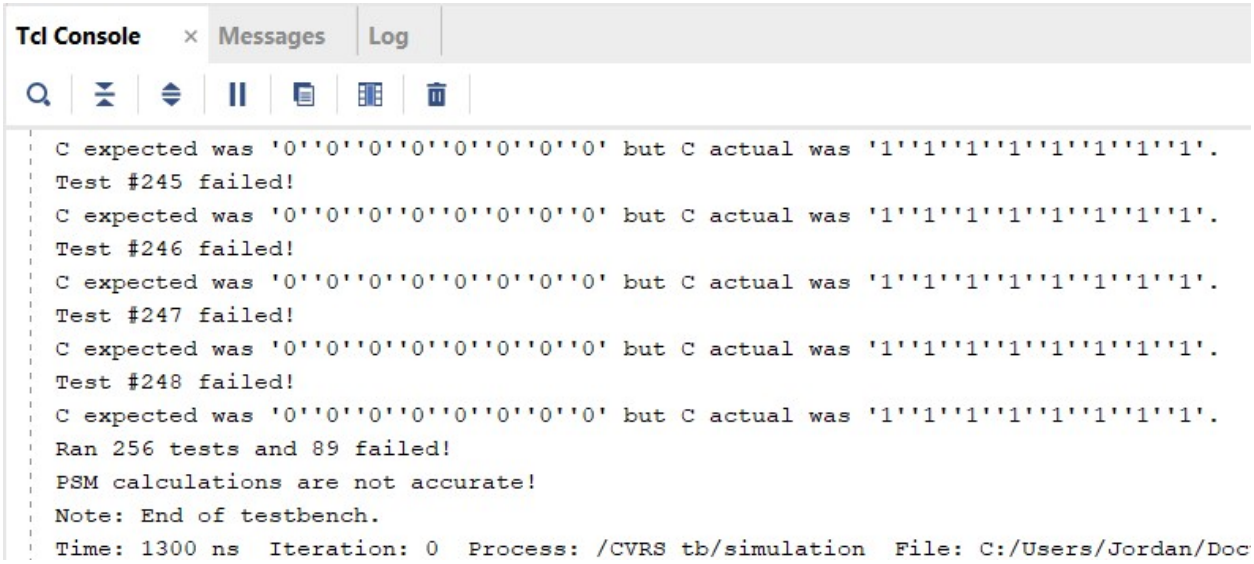
CVRS_PSM_2 Report

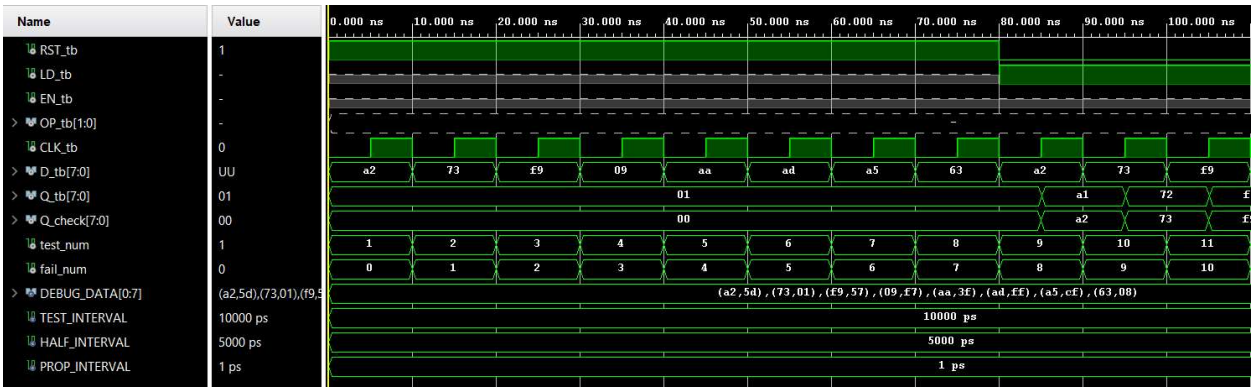


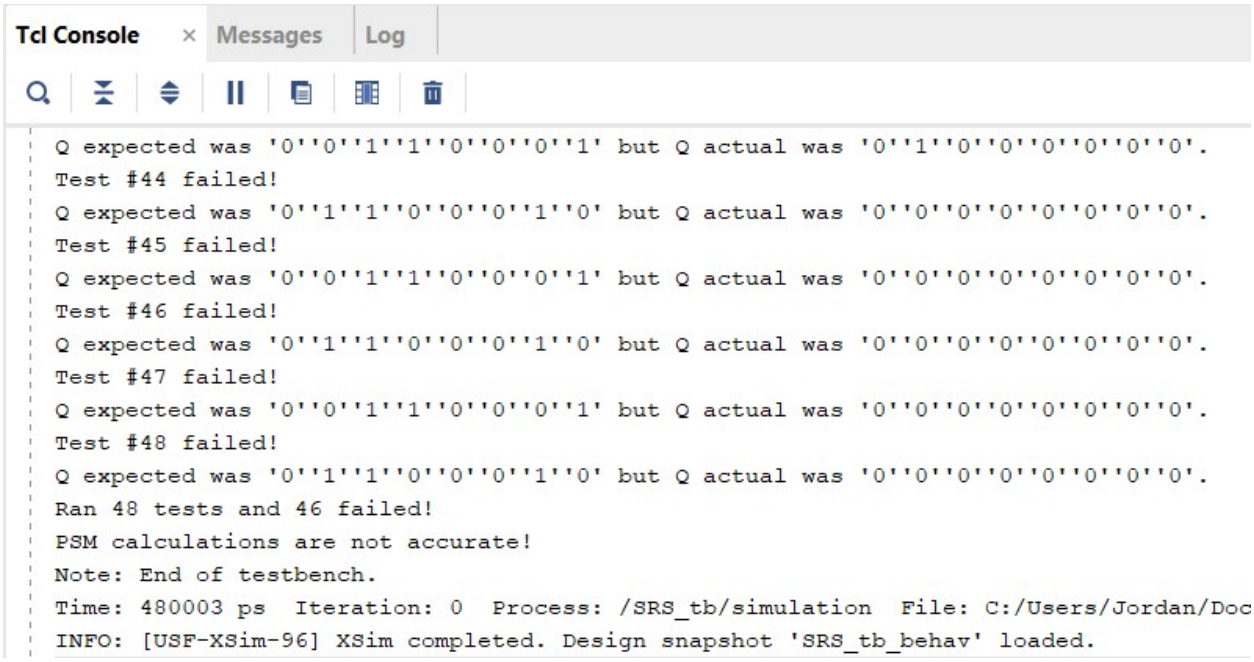




CVRS_PSM_2 is faulty and is NOT working as intended. For opcodes “00” and “01 (ror and rol respectively), the PSM is prone to error on the first cycle after A has changed. For opcodes “10” and “11” (sra and sll respectively), the PSM is prone to error throughout the entire testing phase and follows no obvious pattern. During these opcodes, only some A values will produce a correct result, while other A values will fail to produce any correct result.

**Part 2**

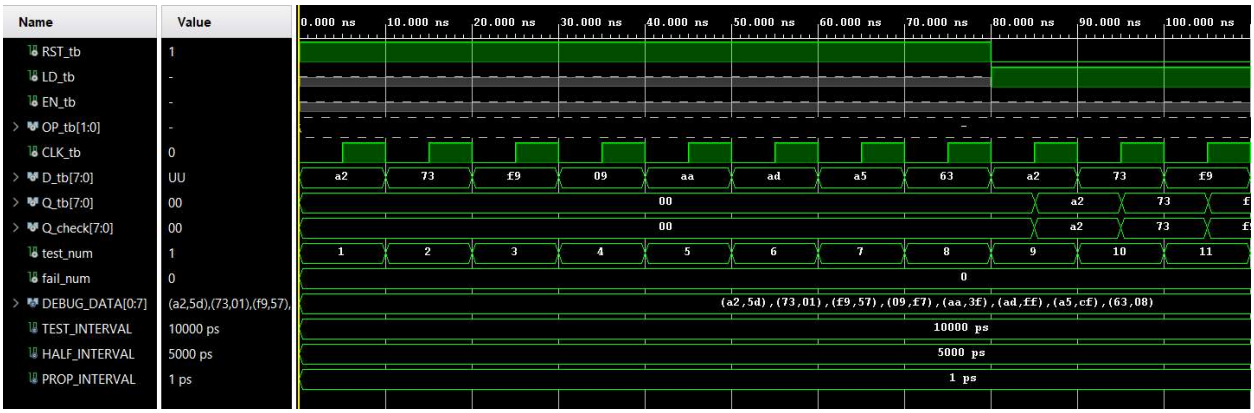
SRS_PSM_1 Report




SRS_PSM_1 is faulty and is NOT working as intended. The RST signal does not make the output x00, but rather makes it x01. The LD signal does not set Q to D, but rather sets it to D - 1. While the EN signal is HI, none of the OP signals work as intended and all are wrong.

SRS_PSM_2 Report





CVRS_PSM_1 is not faulty and is working as intended.