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Modeling and Real-Time Control of Multizone Thermal Processing System for Photoresist Processing

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ABSTRACT: We present a real time, in situ method to control the spatial temperature uniformity of a semiconductor substrate during the various bake steps in the lithography sequence. Significantly, the wafer temperature settles down to steady state within 50 s under closed-loop control. The corresponding maximum temperature nonuniformity during transient is less than 1 °C and the steady state temperature nonuniformity is less than 0.1 °C. Specifically, we have developed a complete thermal diffusion model for the entire bake plate-and-wafer system, so that the transient thermal behavior is accurately captured during the baking process. By monitoring the bake plate temperature and fitting the data into the model, an updated model can be estimated and the desired wafer temperature can then be calculated and controlled in real time. Experimental results confirm the efficacy of the approach and its superiority over traditional run-to-run control techniques.

INTRODUCTION

The lithography sequence in semiconductor manufacturing consists of a number of thermal processing steps during photoresist processing, as shown in Figure 1.[1−3] Temperature uniformity control is an important issue in photoresist processing with stringent specifications and has a significant impact on the line width or critical dimension (CD). Variation in CD results in scrap products. The most temperature sensitive step in the lithography sequence is the postexposure bake step. Requirements call for the temperature to be controlled within 0.1 °C across the wafer at temperatures between 70 and 150 °C.[4,5] A number of recent investigations also showed the importance of proper bake plate operation, both in steady-state and transient, on CD control.[2,6−8] Two approaches exist in addressing this issue in industry. The first approach involves the development of less temperature sensitive photoresist. As outline by the International Technology Roadmap for Semiconductors (ITRS) roadmap,[9] there are currently no known manufacturing solutions and much work is required. The second approach is the development of algorithms[10,11] and more advanced thermal processing systems[12] for temperature and CD control, which is the approach undertaken in this work.

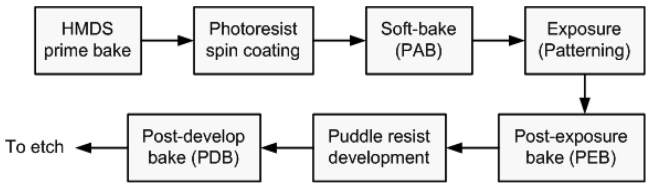

Figure 1. Typical steps in the lithography sequence.

Thermal processing of semiconductor wafers is commonly performed by placement of the substrate on a heated bake plate for a given period of time. The heated bake plate is held at a constant temperature by a feedback controller that adjusts the heater power in response to a temperature sensor embedded in the bake plate near the surface. State-of-the-art heating systems consist of more heating zones. The wafers are usually placed on proximity pins to minimize contamination. When a wafer at room temperature is placed on the bake plate, the temperature of the bake plate invariably drops first but recovers gradually because of closed-loop control. Different air gap sizes will result in different temperature drops in the bake plate due to the difference in the air gap thermal resistance between the wafer and the bake plate. A warped wafer will thus result in deviation of the wafer temperatures from its desired set points across the wafer surface.

Production wafers usually do not have temperature sensors embedded in them. Commercial bake plates are usually calibrated based on test wafers with embedded sensors. However, as the processes are subjected to process drifts and disturbances, a fixed temperature set point is not able to address the issues. Any correction is therefore executed based on run-to-run control techniques, which depend on the sampling frequency of the wafers.

We have demonstrated previously that information of the average air gap between the wafer and the bake plate can be obtained with the use of system theory tools.[4] The relationship between the wafer and plate temperatures at steady-state can then be derived from physical modeling of the baking process. By monitoring the maximum plate temperature drop, the average air gap in each heating zone can be estimated, and we are able to calculate the new bake plate temperature set point to achieve the desirable steady-state wafer temperature.[4] One of the major drawbacks of the mentioned approach is that it does

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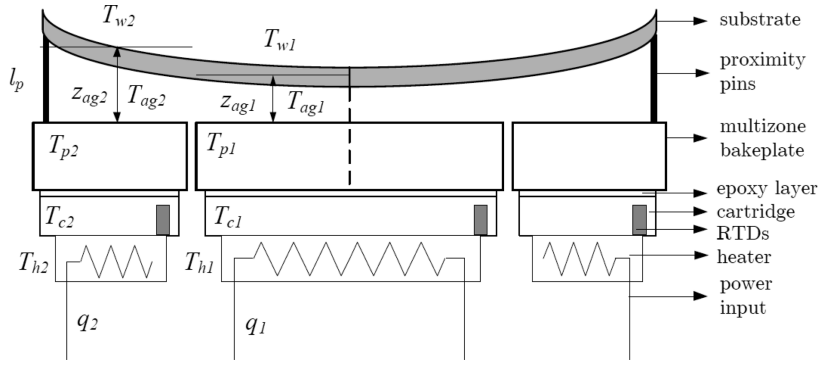

Figure 2. Schematic diagram of the thermal processing system.

not take into account the dynamic performance of the wafer temperature, although an improvement of steady state temperature uniformity is obtained from about 1.1 °C to less than 0.1 °C when compared to conventional approaches where a simple feedback controller is used to regulate the plate temperature. The previous approach[4] makes use of conduction thermal resistance terms which are strictly accurate only during steady state. Consequently, that gives rise to significant modeling error during the initial transient phase. It has also been reported that even though the resultant range of steady-state temperatures was minimized, the consequent gain in CD uniformity cannot be realized. This is attributed to the temperature distribution while rising to the postexposure bake (PEB) temperature.[5]

In this work, we propose a real-time wafer temperature control method to minimize temperature nonuniformity in the baking steps and improve the dynamic performance of the wafer temperature. In contrast, our present model adopts the full thermal diffusion formalism so that the thermal behavior during the initial transient period is properly captured. We are thus able to extract the average air gap thicknesses between the bake plate and wafer in each of the heating zones and consequently the wafer temperature in real-time. The experimental result shows the feasibility of the proposed approach and significant improvement is obtained when compared with conventional method and our earlier proposed approach.[4]

THERMAL MODELING OF THE SYSTEM

The multizone programmable thermal processing system used in this work is shown in Figures 2 and 3. In the baking process, the bake plate is heated up by the cartridge heater attached to it. Resistive heating elements and sensors are embedded in each of the heater cartridge, which are connected to the main heater plate via epoxy. The bake plate consists a total of 64 of these heating elements in four annular rings (The center ring/circle has 4 elements, the second to fourth annular rings has 12, 20, and 28 elements, respectively). Depending on application, the number of heating zones of the bake plate can be easily configured by simple connection of these heating elements. In the actual experimental work, the system is configured as a dual-zone system. The inner zone consists of 16 heating elements, the outer zone consists of 48 heating elements. Each heating zone is configured with its own temperature sensor and electronics embedded in the cartridge for feedback control. The fact that the zones are spatially disjointed ensures no direct thermal coupling between the zones. Detailed description of the programmable thermal processing system can be found in the work of Tay et al.[4]

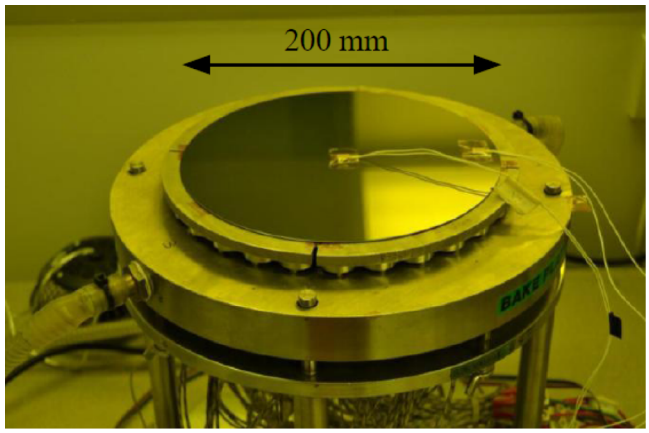

Figure 3. Photo of the thermal processing system.

Energy balances on the elements in the system can be carried out to obtain a thermal model as follows:

$$C_w\dot{T}_w = q_w^{in} + q_w^{out} + q_w^{top} + q_w^{bottom} \quad (1)$$

$$C_{ag}\dot{T}_{ag} = q_{ag}^{in} + q_{ag}^{out} + q_{ag}^{top} + q_{ag}^{bottom} \quad (2)$$

$$C_p\dot{T}_p = q_p^{in} + q_p^{out} + q_p^{top} + q_p^{bottom} \quad (3)$$

$$C_c\dot{T}_c = q_c^{in} + q_c^{out} + q_c^{top} + q_c^{bottom} \quad (4)$$

$$C_h\dot{T}_h = q_h^{in} + q_h^{out} + q_h^{top} + q_h^{bottom} + q^{input} \quad (5)$$

where T is the temperature above the ambient, C the thermal capacitance, q^{in}, q^{out}, q^{top}, and q^{bottom} the heat flows into the element from inner zone, outer zone, top surface, and bottom surface, respectively, q^{input} the heater power and the subscripts w, ag, p, c, and h represent the wafer, the air gap, the bake plate, the cartridge, and the heater, respectively. Detailed description of each of the terms are presented in the Appendix.

In the system, the wafer and the bake plate can be discretized into N zones to simulate their temperature response. For each discrete element, heat will be transferred from the adjacent inner and outer elements. We have

$$q_i^{in} = kA_i^{side}\frac{T_{i-1} - T_i}{r_{i-1}} \quad (6)$$

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$$q_i^{\text{out}} = kA_{i+1}^{\text{side}}\frac{T_{i+1} - T_i}{r_i} \tag{7}$$

where k is the thermal conductivity, A^{side} the contact area between the adjacent elements, and r_i the distance between the elements i and $i + 1$.

For the edge element, the side surface is exposed to the ambient, so we have

$$q_n^{\text{out}} = h_{\text{lm}}\cdot A_{\text{lm}}^{\text{side}}(-T_{\text{a}}) \tag{8}$$

where the subscript lm represents the different layers in the system, which are namely the wafer, the bake plate, the cartridge and the heater. Variable h is the convection coefficient, which can be calculated as follows:[13]

$$h = \frac{k}{L}\bar{N}_{\text{u}} \tag{9}$$

where $\bar{N}_{\text{u}}$ is the Nusselt number, and we have[13]

$$\bar{N}_{\text{u}} = \left\{0.6 + \frac{0.387Ra^{1/6}}{[1 + (0.559/\text{Pr})^{9/16}]^{8/27}}\right\}^2 \tag{10}$$

The wafer top surface is exposed to the surroundings and so we have

$$q_n^{\text{top}} = h^{\text{top}}\cdot A_{\text{w}}^{\text{top}}(-T_{\text{w}}) \tag{11}$$

where $A_{\text{w}}^{\text{top}}$ is the area of the top of the wafer exposed to the ambient. The convection coefficient h^{top} can be calculated from the following:[13]

$$\bar{N}_{\text{u}}^{\text{top}} = 0.54Ra^{1/4} \tag{12}$$

The air gap between the wafer and bake plate is about 210 μm.[4] The main mode of heat transfer between two materials separated by air depends on both the air-gap and the temperature difference between the two materials.[14] When this gap is below 5.8 mm, and their temperature difference is considerably smaller than 200 °C, the heat transfer mechanism is essentially conductive[14] and given by the following:

$$q_{\text{w}}^{\text{bottom}} = -k_{\text{ag}}A_{\text{ag}}\left.\frac{\partial T_{\text{ag}}}{\partial z_{\text{ag}}}\right|_{\text{boundary}} \tag{13}$$

where z is the thickness. The effect of radiative heat transfer is negligible at the temperature range that we are interested.[15]

Since the governing thermal transport between the elements in the system is conductive, at the boundary layer of two adjacent elements, we have

$$-k_\alpha A_\alpha\left.\frac{\partial T_\alpha}{\partial z_\alpha}\right|_{\text{boundary}} = -k_\beta A_\beta\left.\frac{\partial T_\beta}{\partial z_\beta}\right|_{\text{boundary}} \tag{14}$$

where the subscripts α and β represent the two vertical adjacent layers.

At the bottom layer of the system, the heater is exposed to the ambient, and we have

$$q_n^{\text{bottom}} = h_{\text{bottom}}\cdot A_{\text{h}}^{\text{bottom}}\cdot(-T_{\text{h}}) \tag{15}$$

where $A_{\text{h}}^{\text{bottom}}$ is the area of the bottom of the heater exposed to the ambient. The convection coefficient h_{bottom} can be calculated from the following:[13]

$$\bar{N}_{\text{u}}^{\text{bottom}} = 0.27Ra^{1/4} \tag{16}$$

Most thermophysical properties are temperature dependent. However, for the temperature range of interest from 15 to 150 °C, it is reasonable to assume that they remain fairly constant and can be obtained from handbooks[16] as tabulated in Table 1.

Table 1. Physical Parameters of the Thermal Processing System[16]

	property	value
wafer (silicon)	density, ρ	2330 kg m^{-3}
	specific heat capacity, c_v	750 J K^{-1} kg^{-1}
	thermal conductivity, k	99 W m^{-1} K^{-1}
	convection coefficient, h	3.3824 W m^{-2} K^{-1}
	thickness, z	0.700 mm
	diameter	200 mm
air	density, ρ	1.1 kg m^{-3}
	specific heat capacity, c_v	1000 J K^{-1} kg^{-1}
	thermal conductivity, k	0.03 W m^{-1} K^{-1}
bake plate (aluminum)	density, ρ	2700 kg m^{-3}
	specific heat capacity, c_v	917 J K^{-1} kg^{-1}
	thermal conductivity, k	250 W m^{-1} K^{-1}
	convection coefficient, h	7.271 W m^{-2} K^{-1}
	thickness, z	6.8 mm
	diameter	220 mm
epoxy	thermal conductivity, k	0.35 W m^{-1} K^{-1}
	thickness, z	0.02 mm
cartridge (aluminum)	density, ρ	2700 kg m^{-3}
	specific heat capacity, c_v	917 J K^{-1} kg^{-1}
	thermal conductivity, k	250 W m^{-1} K^{-1}
	convection coefficient, h	4.86 W m^{-2} K^{-1}
	thickness, z	4.4 mm
	diameter	10 mm
heater (aluminum)	density, ρ	2700 kg m^{-3}
	specific heat capacity, c_v	917 J K^{-1} kg^{-1}
	thermal conductivity, k	250 W m^{-1} K^{-1}
	convection coefficient, h	2.7828 W m^{-2} K^{-1}
	thickness, z	5.4 mm
	diameter	6 mm

The modeling eqs 1−16 are expressed in state-space form in the Appendix. To assess the quality of the proposed system model, we perform conventional baking process experiment and compare the simulation with the experimental results. In this work, we will only simulate the system dynamics for a two-zone system. Our objective is to demonstrate that the proposed model succeeds in predicting the experimental wafer temperatures using the bake plate temperature and the input signal without resorting to the use of any fitting parameter and is therefore useful for scaling up.

In the experiment, a flat wafer at room temperature is dropped on the baking system with a proximity pin height of 140 μm. This causes the bake plate temperature to drop at first but recovers gradually because of closed-loop control. Two proportional-integral (PI) controllers are used to control the temperature of the two zones of the bake plate. Figure 4 shows the comparison result of the simulation and experimental bake plate temperatures and wafer temperatures when the air gap thickness is 140 μm.

It can be seen that the agreement between of the wafer temperatures from simulation and experimental results is excellent, thereby verifying the effectiveness of the proposed

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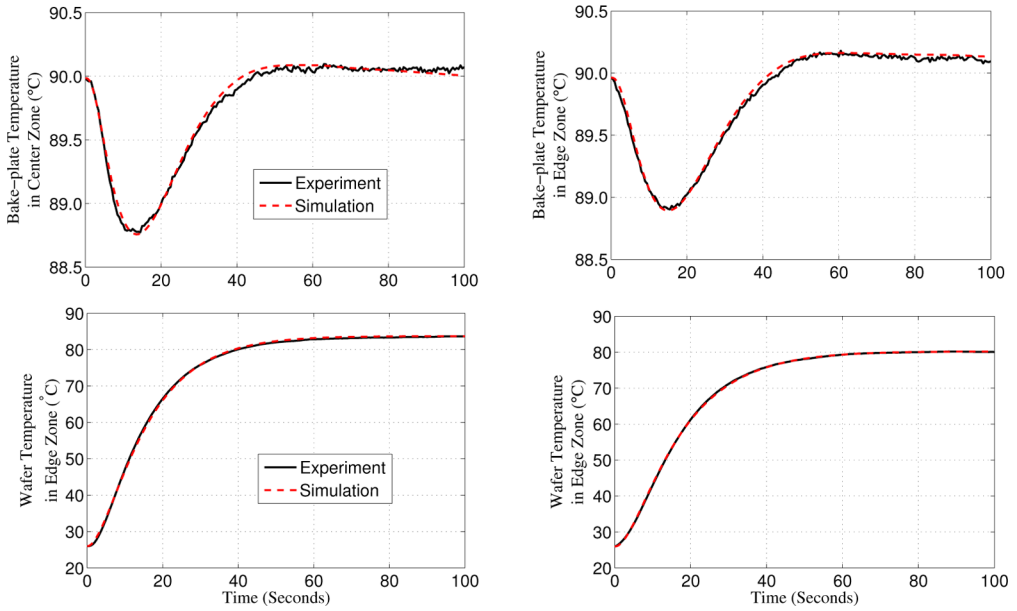

Figure 4. Bake plate and wafer temperature in simulation and experiment with air gap thickness of 140 μm using the calculated model.

thermal model. Being confident of our system modeling, we then conduct real-time control experiment with the system model.

CONTROL STRUCTURE AND EXPERIMENT RESULT

Experiment Setup. Most of the experimental conditions are similar to refs and 4. The experimental setup for the baking of 200 mm wafer is shown in Figure 2. Resistance temperature detectors (RTDs) are attached to the wafer[15,17] for temperature measurement. The wafer is dropped onto the bake plate by aligning the major flat surface of the wafer with the proximity pins. A control-system software was developed using the National Instruments LabView programming environment[18] to create a multivariable PI control framework and a dynamic temperature control system.

Control Structure. Figure 4 shows the high quality modeling fit with experimental data for the case of a flat wafer. However, during actual wafer processing, wafers can warp (due to other preprocessing steps); once a wafer warped, the air gap between the wafer and the plate will change as shown in Figure 2.

The proposed approach required detailed information of the system in order to identify the average air gap during subsequent processing. On the basis of the 2-zone system model, we can develop a state-space model[19] with the air gap thicknesses of the two zones as unknowns. Detailed description of the thermal model in state-space form is given in the Appendix. The thermal model in state-space format is given by eq A.1 in the Appendix where $z_{ag(i)}$ represents the air gap in the respective zones. In the experiment, the bake plate temperature readings and input control signals are collected and fitted into the model (eq A.1) to extract the air gap thicknesses and wafer temperatures using the gray-box modeling function (idgrey.m) from Matlab system identification toolbox.[19] The estimated air gap thicknesses for the 2 zones under different experimental conditions are tabulated in Table 2. This approach is particularly useful since we understand the physics of the thermal system and can represent the thermal system using ordinary differential equations.

Table 2. Estimated Air Gap Thickness and Wafer Warpage Using the Real-Time Control Method with the Proximity Pin Height of 210 μm

		estimated air gap thickness		deviation from flat wafer		
wafer	exp run	center zone (μm)	edge zone (μm)	center zone (μm)	edge zone (μm)	extracted wafer warpage (μm)
flat wafer	(2)	208	214	−2	4	4
70 μm warpage	(4)	146	182	−64	−28	72
140 μm warpage	(6)	86	158	−124	−52	144

Figure 5 shows the control systems framework, the bake plate temperatures, T_{p1} and T_{p2}, and the control signal, u_1 and

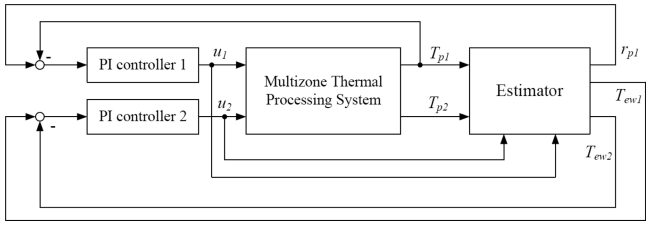

Figure 5. Block diagram of control structure where r_{p1}, T_{ew1}, and T_{ew2} are the desired plate reference temperature in zone 1 based on the estimated air gaps, the estimated wafer temperatures in zones 1 and 2, respectively.

u_2, in the two zone system are measured and sent to the estimator. The "Estimator" block estimates the new air gap thickness based on the control signals and bake plate temperatures. The estimated air gap thickness, t_{ag}, is then used to determine the set point, r_{p1}, of the bake plate and the estimated wafer temperatures, T_{ew1} and T_{ew1}, are used to control the wafer temperature uniformity in the process.

Using this method, we can real-time estimate the air gap thickness and wafer temperature and consequently regulate the control signal online to achieve desired wafer temperature and

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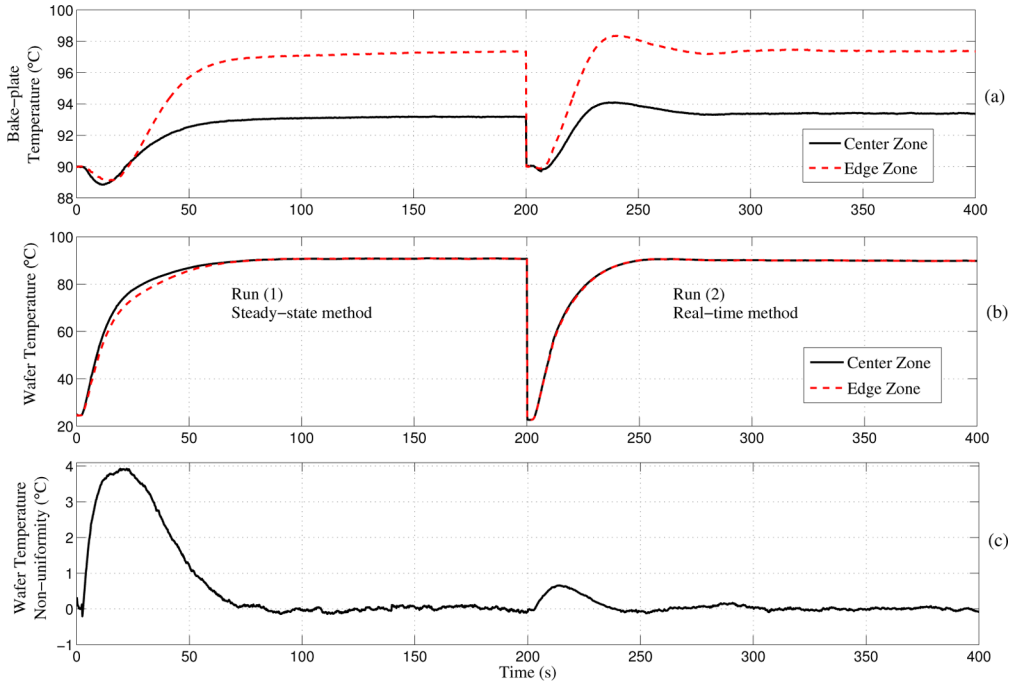

Figure 6. Temperature profile of bake plate and wafer when a flat wafer is dropped on bake plate with proximity pin height of 210 μm. The bake plate temperatures, wafer temperatures and wafer temperature nonuniformity during the baking process are shown in subplots (a), (b), and (c), respectively.

minimize temperature nonuniformity in the whole process. Furthermore, with the estimated air gap thickness in steady state, we can extract the wafer warpage profile.

Experimental Result. To demonstrate our approach, a flat wafer is first dropped on the bake plate with a proximity pin height of 210 μm. The initial air gap is fixed at 210 μm, i.e., the condition for a flat wafer. The final estimated air gaps are tabulated in Table 2. A good measure of the extent of warpage is to measure the deviation of the average air gap from the proximity pin height. For the flat wafer, we can see that deviations are close to zero as expected.

Figure 6 shows the bake plate and wafer temperature profiles using the steady-state temperature control method[4] and the proposed real-time control method. To validate our results, two temperature sensors (in this case RTDs) are embedded into the wafer surface at locations corresponding to the center of each zone to monitor the wafer temperature. Figure 6 consists of two experimental runs, (1) and (2). Run (1) corresponds to the steady-state control approach[4] when the wafer is dropped on the bake plate. The air gaps are first estimated based on the maximum bake plate temperature drops. Then the new bake plate temperatures are set based on the estimated air gap thickness as shown in Figure 6a. Notice that the wafer temperature is controlled at 90 °C with a steady-state temperature nonuniformity of about 0.1 °C as shown in Figure 6b,c. However, since the new bake plate temperature set points are implemented about 20 s after the wafer is dropped to allow the maximum temperature drop point to occur as well as for computational delay of the corresponding air gap, the wafer can only reach steady state after about 80 s as shown in Figure 6b. Furthermore, the wafer has a temperature nonuniformity of about 4 °C in transient period as shown in Figure 6c.

Next, real-time control of the wafer temperature is implemented. Figure 6b,c of run (2) shows that the wafer temperature is controlled to 90 °C within 50 s with a maximum temperature nonuniformity that is less than 1 °C during the transient and steady state temperature nonuniformity that is less than 0.1 °C. The corresponding maximum temperature nonuniformity and root-mean-square error (RMS) during the thermal processing for experimental runs (1) and (2) are also shown in Table 3. It can be seen that the temperature nonuniformity RMS in the heating process is decreased from 1.48 to 0.18, an improvement of over 80%.

Table 3. Performance Comparison of the Steady-State Wafer Temperature Control Method[4] and Our Proposed Method

wafer	method	exp run	max. nonuniformity (°C)	RMS
flat wafer	steady-state	(1)	3.93	1.48
	real-time	(2)	0.66	0.18
70 μm warpage	steady-state	(3)	4.35	1.78
	real-time	(4)	0.71	0.20
140 μm warpage	steady-state	(5)	4.68	1.62
	real-time	(6)	1.07	0.29

The feasibility of the approach is further demonstrated by heating warped wafer. First, the wafer with center-to-edge warpage of 70 μm is dropped on the same bake plate with the proximity pin height of 210 μm. Wafer warpage is created mechanically as described by Tay et al.[3,4] and shown in Figure 2. On the basis of the final estimated air gap thickness together with the proximity pin height, the profile of the wafer can be obtained by extrapolation. An estimated warpage of 72 μm from center-to-edge for the warped wafer is obtained which is close to the known warpage of 70 μm.

The temperature results using the steady-state and real-time control methods are tabulated in Table 3 and shown in Figure 7 as experimental runs (3) and (4). It can be seen that for the warped wafer, using the real-time control method, wafer

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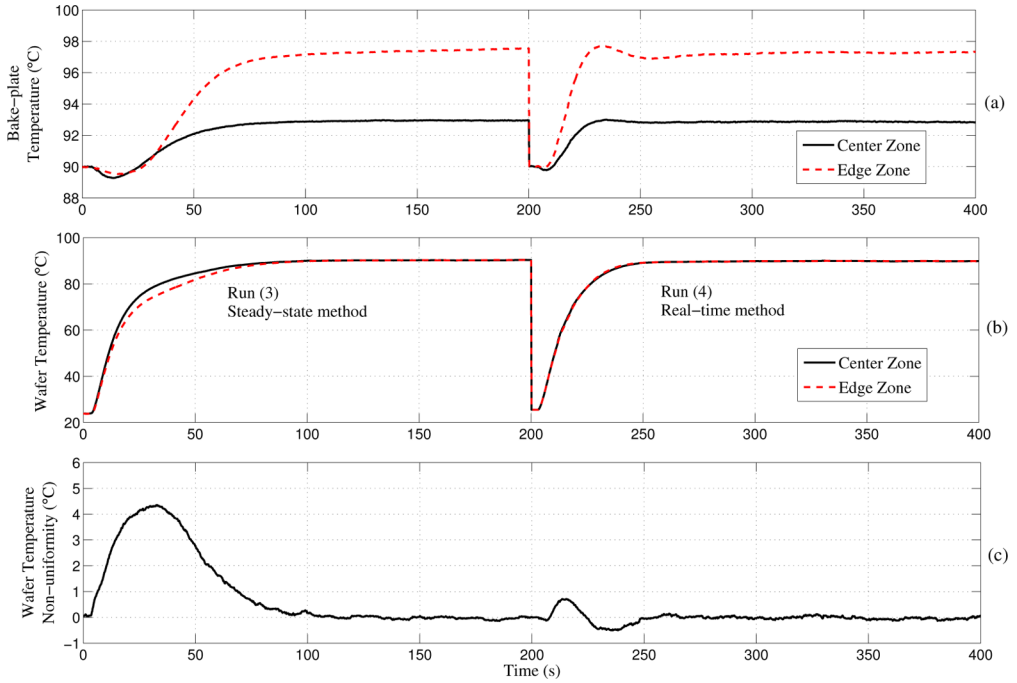

Figure 7. Temperature profile of bake plate and wafer when a wafer with center-to-edge warpage of 70 μm is dropped on bake plate with proximity pin height of 210 μm. The bake plate temperatures, wafer temperatures and wafer temperature nonuniformity during the baking process are shown in subplots (a), (b), and (c), respectively.

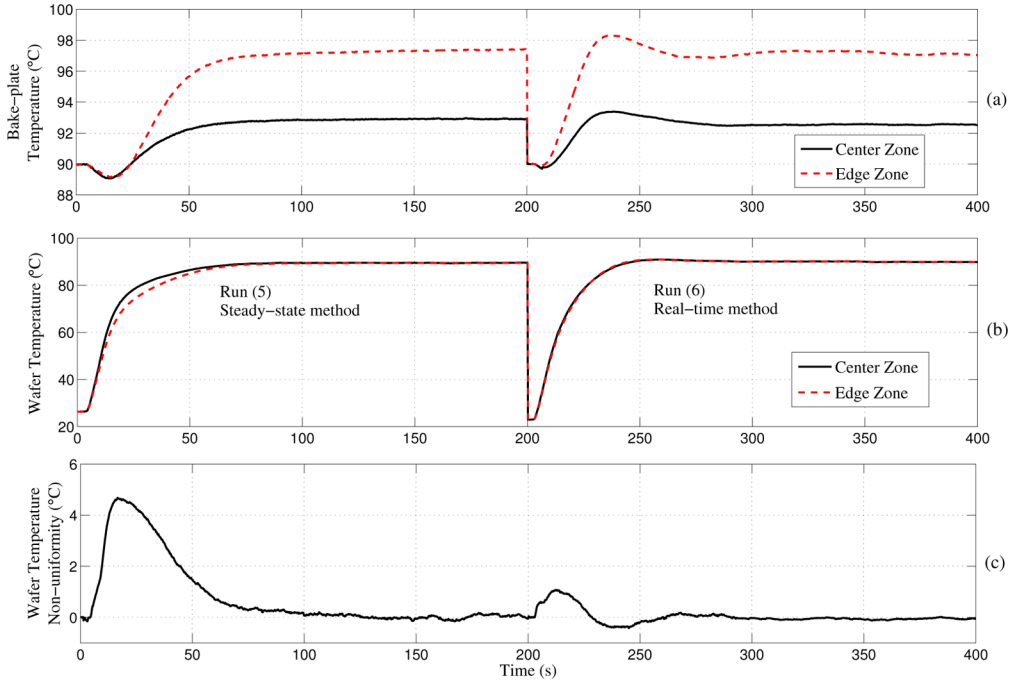

Figure 8. Temperature profile of bake plate and wafer when a wafer with center-to-edge warpage of 140 μm is dropped on bake plate with proximity pin height of 210 μm. The bake plate temperatures, wafer temperatures and wafer temperature nonuniformity during the baking process are shown in subplots (a), (b), and (c), respectively.

temperature can reach the steady-state temperature within 50 s, with a maximum temperature nonuniformity that is less than 1 °C during the transient and steady state temperature nonuniformity that is less than 0.1 °C.

Next, a wafer with center-to-edge warpage of 140 μm is dropped on the same bake plate with the proximity pin height of 210 μm to verify the effectiveness of the method in detecting different warped wafer. The extracted wafer profile is based on the final estimated air gap. The estimated warpage of 144 μm from center-to-edge is also closed to the known warpage of 140 μm.

The corresponding temperature results are tabulated in Tables 2 and 3 and shown in Figure 8 as experimental run (5) and run (6). As expected, using the real-time control method, the 140 μm warped wafer can also reach the steady-state temperature within 50 s, with a much better temperature

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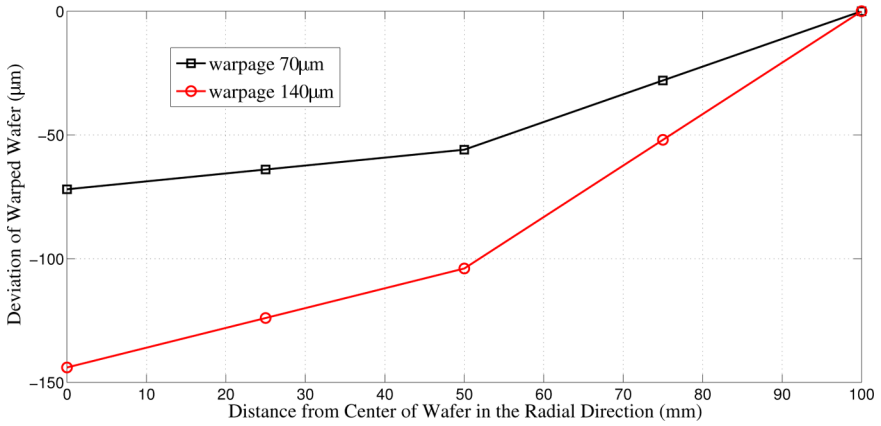

Figure 9. Estimated profile of the warped wafers with center-to-edge warpage of 70 and 140 μm based on experimental runs (4) and (6), respectively.

uniformity than steady-state control method (Figure 9). We note that both approaches described herein are superior to existing practice in the industry where any compensation is done in a run-to-run control approach.[9]

CONCLUSIONS

The lithography manufacturing process will continue to be a critical area in semiconductor manufacturing that limits the performance of microelectronics. Enabling advancements by computational, control, and signal processing methods are effective in reducing the enormous costs and complexities associated with the lithography sequence. In this work, we have demonstrated an in situ approach to real-time detection of wafer warpage and control of the wafer temperature uniformity in the heating process. Wafer temperature uniformity in transient period has been improved greatly compared to the previously reported steady-state method. With the proposed approach, the root-mean-square wafer temperature nonuniformity during the thermal process has improved by more than 80%. The proposed approach can also be scaled up for larger wafers by increasing the number of sensors, actuators, and controllers.

APPENDIX: DERIVATION OF STATE-SPACE MODEL OF THE SYSTEM

Energy balances on the elements in the system can be carried out to obtain the model as shown in eqs 1−5. The system is discretized into N zones.

For the wafer, we define

$$\frac{1}{R_{w(i)}} = \frac{1}{r_{w(i-1)}} + \frac{1}{r_{w(i)}} + \frac{1}{r_{aw(i)}} + \frac{1}{r_{wag(i)}}$$

where

$$r_w(i) = \begin{cases} \dfrac{\Delta r}{k_w A_{ws(i)}} & 1 \le i \le N-1 \\ \dfrac{1}{h_w A_{ws(N)}} & i = N \end{cases}$$

$$r_{aw}(i) = \frac{1}{h_w A_{wz(i)}} \qquad 1 \le i \le N$$

$$r_{wag}(i) = \frac{z_{ag(i)}/2k_a + z_w/2k_w}{A_{wag(i)}} \qquad 1 \le i \le N$$

Each of the heat flow terms on the right-hand side of eq 1 is given by the following:

$$q^{in}_{w(i)} = \frac{k_w A_{ws(i-1)}}{\Delta r}(T_{w(i-1)} - T_{w(i)}) \qquad 2 \le i \le N$$

$$q^{out}_{w(i)} = \begin{cases} \dfrac{k_w A_{ws(i)}}{\Delta r}(T_{w(i+1)} - T_{w(i)}) & 1 \le i \le N-1 \\ h_w A_{ws(N)}(-T_{w(N)}) & i = N \end{cases}$$

$$q^{top}_{w(i)} = h_w A_{wz(i)}(-T_{w(i)}) \qquad 1 \le i \le N$$

$$q^{bottom}_{w(i)} = \frac{A_{wag(i)}(T_{ag(i)} - T_{w(i)})}{z_{ag(i)}/2k_a + z_w/2k_w} \qquad 1 \le i \le N$$

Equation 1 can then be expressed as follows:

$$C_{w(i)}\dot{T}_{w(i)}(t) = \frac{1}{r_{w(i-1)}}T_{w(i-1)}(t) + \frac{1}{r_{w(i)}}T_{w(i+1)}(t) + \frac{1}{r_{wag(i)}}T_{ag(i)}(t) - \frac{1}{R_{w(i)}}T_{w(i)}(t)$$

In state-space form, we accordingly have

$$F_{ww}(i, i) = -\frac{1}{C_{w(i)}R_{w(i)}} \qquad 1 \le i \le N$$

$$F_{ww}(i, i+1) = \frac{1}{C_{w(i)}r_{w(i)}} \qquad 1 \le i \le N-1$$

$$F_{ww}(i, i-1) = \frac{1}{C_{w(i)}r_{w(i-1)}} \qquad 2 \le i \le N$$

$$F_{wag}(i, i) = \frac{1}{C_{w(i)}r_{wag(i)}} \qquad 1 \le i \le N$$

For the air gap, we define

$$\frac{1}{R_{ag(i)}} = \frac{1}{r_{ag(i-1)}} + \frac{1}{r_{ag(i)}} + \frac{1}{r_{wag(i)}} + \frac{1}{r_{agp(i)}}$$

where

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$$r_{ag}(i) = \begin{cases} \dfrac{\Delta r}{k_a A_{ags(i)}} & 1 \le i \le N-1 \\ \dfrac{1}{h_{ag} A_{ags(N)}} & i = N \end{cases}$$

$$r_{agp}(i) = \frac{z_{ag(i)}/2k_a + z_p/2k_p}{A_{agp(i)}} \qquad 1 \le i \le N$$

Each of the heat flow terms on the right-hand side of eq 2 is given by the following:

$$q^{in}_{ag(i)} = \frac{k_a A_{ags(i-1)}}{\Delta r}(T_{ag(i-1)} - T_{ag(i)}) \qquad 2 \le i \le N$$

$$q^{out}_{ag(i)} = \begin{cases} \dfrac{k_a A_{ags(i)}}{\Delta r}(T_{ag(i+1)} - T_{ag(i)}) & 1 \le i \le N-1 \\ h_{ag} A_{ags(N)}(-T_{ag(N)}) & i = N \end{cases}$$

$$q^{top}_{ag(i)} = \frac{A_{wag(i)}(T_{w(i)} - T_{ag(i)})}{z_{ag(i)}/2k_a + z_w/2k_w} \qquad 1 \le i \le N$$

$$q^{bottom}_{ag(i)} = \frac{A_{agp(i)}(T_{p(i)} - T_{ag(i)})}{z_{ag(i)}/2k_a + z_p/2k_p} \qquad 1 \le i \le N$$

Equation 2 can then be expressed as follows:

$$C_{ag(i)}\dot{T}_{ag(i)}(t) = \frac{1}{r_{ag(i-1)}}T_{ag(i-1)}(t) + \frac{1}{r_{ag(i)}}T_{w(i+1)}(t) + \frac{1}{r_{wag(i)}}T_{w(i)}(t) + \frac{1}{r_{agp(i)}}T_{p(i)}(t) - \frac{1}{R_{ag(i)}}T_{ag(i)}(t)$$

In state-space form, we accordingly have

$$F_{agag}(i, i) = -\frac{1}{C_{ag(i)}R_{ag(i)}} \qquad 1 \le i \le N$$

$$F_{agag}(i, i+1) = \frac{1}{C_{ag(i)}r_{ag(i)}} \qquad 1 \le i \le N-1$$

$$F_{agag}(i, i-1) = \frac{1}{C_{ag(i)}r_{ag(i-1)}} \qquad 2 \le i \le N$$

$$F_{agw}(i, i) = \frac{1}{C_{ag(i)}r_{wag(i)}} \qquad 1 \le i \le N$$

$$F_{agp}(i, i) = \frac{1}{C_{ag(i)}r_{agp(i)}} \qquad 1 \le i \le N$$

For the bake plate, we define

$$\frac{1}{R_{p(i)}} = \frac{1}{r_{ip(i)}} + \frac{1}{r_{op(i)}} + \frac{1}{r_{agp(i)}} + \frac{1}{r_{pc(i)}} + \frac{1}{r_{pe(i)}}$$

where

$$r_{ip}(i) = \frac{t_{p(i)}}{k_p A_{ips(i)}} \qquad 2 \le i \le N$$

$$r_{op}(i) = \begin{cases} \dfrac{t_{p(i)}}{k_p A_{ops(i)}} & 1 \le i \le N-1 \\ \dfrac{1}{h_p A_{ps(N)}} & i = N \end{cases}$$

$$r_{pc}(i) = \frac{z_p/2k_p + z_c/2k_c}{A_{pc(i)}} + R_{ex(i)} \qquad 1 \le i \le N$$

$$r_{pe}(i) = \frac{1}{h_p A_{pa(i)}} \qquad 1 \le i \le N$$

Each of the heat flow terms on the right-hand side of eq 3 is given by the following:

$$q^{in}_{p(i)} = \frac{k_p A_{ips(i)}}{t_{p(i)}}(T_{p(i-1)} - T_{p(i)}) \qquad 2 \le i \le N$$

$$q^{out}_{p(i)} = \begin{cases} \dfrac{k_p A_{ops(i)}}{t_{p(i)}}(T_{p(i+1)} - T_{p(i)}) & 1 \le i \le N-1 \\ h_p A_{ps(N)}(-T_{p(N)}) & i = N \end{cases}$$

$$q^{top}_{p(i)} = \frac{A_{agp(i)}(T_{ag(i)} - T_{p(i)})}{z_{ag(i)}/2k_a + z_p/2k_p} \qquad 1 \le i \le N$$

$$q^{bottom}_{p(i)} = \frac{(T_{c(i)} - T_{p(i)})}{\frac{z_p/2k_p + z_c/2k_c}{A_{pc(i)}} + R_{ex(i)}} + h_p A_{pa(i)}(-T_{p(i)}) \qquad 1 \le i \le N$$

where $R_{ex(i)} = ((z_{ex})/(k_{ex}A_{pc(i)}))$ is the thermal resistance of epoxy layer of element *i*.

Equation 3 can then be expressed as follows:

$$C_{p(i)}\dot{T}_{p(i)}(t) = \frac{1}{r_{ip(i)}}T_{p(i-1)}(t) + \frac{1}{r_{op(i)}}T_{p(i+1)}(t) + \frac{1}{r_{agp(i)}}T_{ag(i)}(t) + \frac{1}{r_{pc(i)}}T_{c(i)}(t) - \frac{1}{R_{p(i)}}T_{p(i)}(t)$$

In state-space form, we accordingly have the following:

$$F_{pp}(i, i) = -\frac{1}{C_{p(i)}R_{p(i)}} \qquad 1 \le i \le N$$

$$F_{pp}(i, i-1) = \frac{1}{C_{p(i)}r_{ip(i)}} \qquad 2 \le i \le N$$

$$F_{pp}(i, i+1) = \frac{1}{C_{p(i)}r_{op(i)}} \qquad 1 \le i \le N-1$$

$$F_{pag}(i, i) = \frac{1}{C_{p(i)}r_{agp(i)}} \qquad 1 \le i \le N$$

$$F_{pc}(i, i) = \frac{1}{C_{p(i)}r_{pc(i)}} \qquad 1 \le i \le N$$

For the cartridge heater, we define

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$$\frac{1}{R_{c(i)}} = \frac{1}{r_{c(i)}} + \frac{1}{r_{pc(i)}} + \frac{1}{r_{ch(i)}} + \frac{1}{r_{ce(i)}}$$

where

$$r_c(i) = \frac{1}{h_c A_{cs(i)}} \qquad 1 \le i \le N$$

$$r_{ch}(i) = \frac{z_c/2k_c + z_h/2k_h}{A_{ch(i)}} \qquad 1 \le i \le N$$

$$r_{ce}(i) = \frac{1}{h_c A_{ca(i)}} \qquad 1 \le i \le N$$

Each of the heat flow terms on the right-hand side of eq 4 is given by the following:

$$q_{c(i)}^{side} = h_c A_{cs(i)}(-T_{c(i)}) \qquad 1 \le i \le N$$

$$q_{c(i)}^{top} = \frac{(T_{p(i)} - T_{c(i)})}{\frac{z_p/2k_p + z_c/2k_c}{A_{pc(i)}} + R_{ex(i)}} \qquad 1 \le i \le N$$

$$q_{c(i)}^{bottom} = \frac{A_{ch(i)}\cdot(T_{h(i)} - T_{c(i)})}{z_c/2k_c + z_h/2k_h} + h_c A_{ca(i)}(-T_{c(i)})$$

$$1 \le i \le N$$

Equation 4 can then be expressed as follows:

$$C_{c(i)}\dot{T}_{c(i)}(t) = \frac{1}{r_{pc(i)}}T_{p(i)}(t) + \frac{1}{r_{ch(i)}}T_{h(i)}(t) - \frac{1}{R_{c(i)}}T_{c(i)}(t)$$

In state-space form, we accordingly have the following:

$$F_{cc}(i, i) = -\frac{1}{C_{c(i)}R_{c(i)}}, \qquad 1 \le i \le N$$

$$F_{cp}(i, i) = \frac{1}{C_{c(i)}r_{pc(i)}} \qquad 1 \le i \le N$$

$$F_{ch}(i, i) = \frac{1}{C_{c(i)}r_{ch(i)}} \qquad 1 \le i \le N$$

Finally, for the heater, we define

$$\frac{1}{R_{h(i)}} = \frac{1}{r_{h(i)}} + \frac{1}{r_{ch(i)}} + \frac{1}{r_{he(i)}}$$

where

$$r_h(i) = \frac{1}{h_h A_{hs(i)}} \qquad 1 \le i \le N$$

$$r_{he}(i) = \frac{1}{h_h A_{ha(i)}} \qquad 1 \le i \le N$$

Each of the heat flow terms on the right-hand side of eq 5 is given by the following:

$$q_{h(i)}^{side} = h_h A_{hs(i)}(-T_{h(i)}) \qquad 1 \le i \le N$$

$$q_{h(i)}^{top} = \frac{A_{ch(i)}\cdot(T_{p(i)} - T_{c(i)})}{z_c/2k_c + z_h/2k_h} \qquad 1 \le i \le N$$

$$q_{h(i)}^{bottom} = h_h A_{ha(i)}(-T_{h(i)}) \qquad 1 \le i \le N$$

Equation 5 can then be expressed as follows:

$$C_{h(i)}\dot{T}_{h(i)}(t) = \frac{1}{r_{ch(i)}}T_{c(i-1)}(t) - \frac{1}{R_{h(i)}}T_{h(i)}(t) + q^{input}$$

In state-space form, we accordingly have

$$F_{hh}(i, i) = -\frac{1}{C_{h(i)}R_{h(i)}} \qquad 1 \le i \le N$$

$$F_{hc}(i, i) = \frac{1}{C_{h(i)}r_{ch(i)}} \qquad 1 \le i \le N$$

Combining all the terms, the thermal model is then given by the following:

$$\dot{T} = \begin{bmatrix} \dot{T}_w \\ \dot{T}_{ag} \\ \dot{T}_p \\ \dot{T}_c \\ \dot{T}_h \end{bmatrix} = \begin{bmatrix} F_{ww} & F_{wag} & 0_{NN} & 0_{NN} & 0_{NN} \\ F_{agw} & F_{agag} & F_{agp} & 0_{NN} & 0_{NN} \\ 0_{NN} & F_{pag} & F_{pp} & F_{pc} & 0_{NN} \\ 0_{NN} & 0_{NN} & F_{cp} & F_{cc} & F_{ch} \\ 0_{NN} & 0_{NN} & 0_{NN} & F_{hc} & F_{hh} \end{bmatrix} \cdot \begin{bmatrix} T_w \\ T_{ag} \\ T_p \\ T_c \\ T_h \end{bmatrix} + \begin{bmatrix} 0_N \\ 0_N \\ 0_N \\ 0_N \\ G_{hh} \end{bmatrix} \cdot q^{input} \tag{A.1}$$

where

$$G_{hh} = \begin{bmatrix} 1/C_{h(1)} & 0 & \cdots & 0 \\ 0 & 1/C_{h(2)} & & \vdots \\ \vdots & & \ddots & 0 \\ 0 & \cdots & 0 & 1/C_{h(N)} \end{bmatrix}$$

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Notes

The authors declare no competing financial interest.

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