OV32C Setting Application Notes

* **Initial Setting (revision 220422)**

The initial setting initializes sensor registers after power on. The setting for each format only includes different registers between different formats.

Initial Revision 220422

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| Registers | Description |
| 0x340c | 0x20 (default) -> 0x30 |
| (Added reg06) |  |
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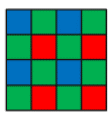
* 01\_6528x4896 15.0fps (revision 220422)
  + Input clock: 24 MHz
  + MIPI DPHY 4 lane, RAW 10, 1500 Mbps/lane,
  + MIPI clock: 750 MHz (1500 Mbps)
  + Frame rate: 15.0 fps (= 96000000 / 1224 / 5228)
  + Sensor internal clock: 96 MHz and 180 MHz
  + HTS: 1224 clocks
  + VTS: 5228 lines
  + V-blank: 4.208 ms (330 lines)
  + Bayer pattern: The 1st line is BCGC…, the 2nd line is CBCG…, the 3rd line is GCRC…, and the 4th line is CGCR…  
    
  + Minimum exposure: 4 lines
  + Maximum exposure: VTS - 8 = 5228 - 8 = 5220 lines
  + Output is mirror off, flip normal
  + Sensor orientation: pad 1 is oriented up on PCB
  + Image on full array:

Full Array (0, 0) --- (6559, 4927).

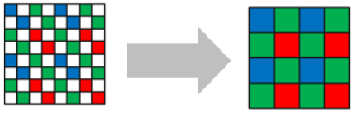
Perform windowing to 6528x4896.

Revision 220422

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| Registers | Description |
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* **02\_3264x2448 30.0fps (revision 220422)**
  + Input clock: 24 MHz
  + MIPI DPHY 4 lane, RAW 10, 800 Mbps/lane
  + MIPI clock: 400 MHz (800 Mbps)
  + Frame rate: 30.0 fps (= 96000000 / 1224 / 2614)
  + Sensor internal clock: 96 MHz and 180 MHz
  + HTS: 1224 clocks
  + VTS: 2614 lines
  + V-blank: 2.091 ms (164 lines)
  + Bayer pattern (Fusion): First line is BGBG…, second line is GRGR… for VC0   
    
  + Minimum exposure: 2 lines
  + Maximum exposure: VTS - 4 = 2614 - 4 = 2610 lines
  + Output is mirror off, flip normal
  + Sensor orientation: pad 1 is oriented up on PCB
  + Image on full array:

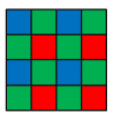
Full Array (0, 0) --- (6559, 4927), as shown in the left-side in the figure below:



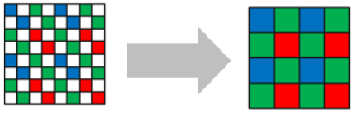
2C1-diagonal bin to 3280x2464, then perform windowing to 3264x2448.

Revision 220422

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| Registers | Description |
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* **03\_1920x1080 60.0fps (revision 220422)**
  + Input clock: 24 MHz
  + MIPI DPHY 4 lane, RAW 10, 800 Mbps/lane
  + MIPI clock: 400 MHz (800 Mbps)
  + Frame rate: 60.0 fps (= 96000000 / 1224 / 1306)
  + Sensor internal clock: 96 MHz and 180 MHz
  + HTS: 1224 clocks
  + VTS: 1306 lines
  + V-blank: 2.856 ms (224 lines)
  + Bayer pattern (Fusion): First line is BGBG…, second line is GRGR… for VC0   
    
  + Minimum exposure: 2 lines
  + Maximum exposure: VTS - 4 = 1306- 4 = 1302 lines
  + Output is mirror off, flip normal
  + Sensor orientation: pad 1 is oriented up on PCB
  + Image on full array:

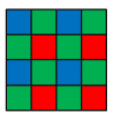
Full Array (0, 0) --- (6559, 4927), as shown in the left-side in the figure below:



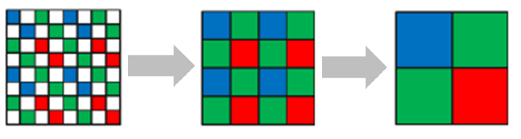
Crop to (1344, 1368) --- (5215, 3559), 2C1-diagonal bin to 1936x1096, then perform windowing to 1920x1080.

Revision 220422

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| Registers | Description |
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* 04\_1280x720 120.0fps (revision 220422)
  + Input clock: 24 MHz
  + MIPI DPHY 4 lane, RAW 10, 700 Mbps/lane
  + MIPI clock: 350 MHz (700 Mbps)
  + Frame rate: 120.3 fps (= 96000000 / 1224 / 652)
  + Sensor internal clock: 96 MHz and 180 MHz
  + HTS: 1224 clocks
  + VTS: 652 lines
  + V-blank: 3.698 ms (290 lines)
  + Bayer pattern (Fusion): First line is BGBG…, second line is GRGR… for VC0   
    
  + Minimum exposure: 2 lines
  + Maximum exposure: VTS - 4 = 652 - 4 = 648 lines
  + Output is mirror off, flip normal
  + Sensor orientation: pad 1 is oriented up on PCB
  + Image on full array:

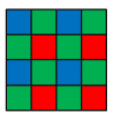
Full Array (0, 0) --- (6559, 4927), as shown in the leftmost-side in the figure below:



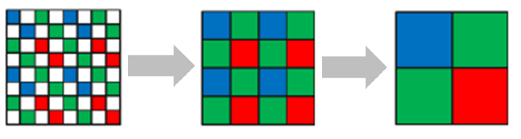
Crop to (656, 1008) --- (5903, 3919), 2C1-diagonal bin + 2x2 analog bin to 1312x728, then perform windowing to 1280x720.

Revision 220422

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| Registers | Description |
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* 05\_1632x1224 30.0fps (revision 220422)
  + Input clock: 24 MHz
  + MIPI DPHY 4 lane, RAW 10, 800 Mbps/lane
  + MIPI clock: 400 MHz (800 Mbps)
  + Frame rate: 30.0 fps (= 96000000 / 1224 / 2614)
  + Sensor internal clock: 96 MHz and 180 MHz
  + HTS: 1224 clocks
  + VTS: 2614 lines
  + V-blank: 2.066 ms (162 lines)
  + Bayer pattern (Fusion): First line is BGBG…, second line is GRGR… for VC0   
    
  + Minimum exposure: 2 lines
  + Maximum exposure: VTS - 4 = 2614 - 4 = 2610 lines
  + Output is mirror off, flip normal
  + Sensor orientation: pad 1 is oriented up on PCB
  + Image on full array:

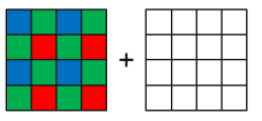
Full Array (0, 0) --- (6559, 4927), as shown in the leftmost-side in the figure below:



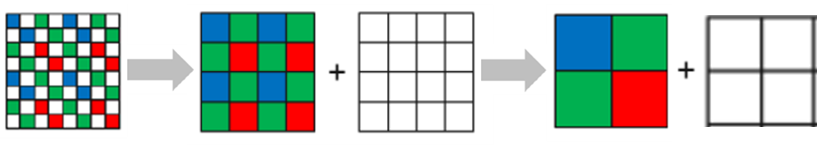
2C1-diagonal bin + 2x2 analog bin to 1640x1232, then perform windowing to 1632x1224.

Revision 220422

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| Registers | Description |
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* 06\_1632x1224 30.0fps (revision 220426)
  + Input clock: 24 MHz
  + MIPI DPHY 4 lane, RAW 10, 800 Mbps/lane
  + MIPI clock: 400 MHz (800 Mbps)
  + Frame rate: 30.0 fps (= 96000000 / 1224 / 2614)
  + Sensor internal clock: 96 MHz and 180 MHz
  + HTS: 1224 clocks
  + VTS: 2614 lines
  + V-blank: 2.066 ms (162 lines)
  + Bayer pattern (RAW): First line is BGBG…, second line is GRGR… for VC0   
    
  + Minimum exposure: 2 lines
  + Maximum exposure: VTS - 4 = 2614 - 4 = 2610 lines
  + Output is mirror off, flip normal
  + Sensor orientation: pad 1 is oriented up on PCB
  + Image on full array:

Full Array (0, 0) --- (6559, 4927), as shown in the leftmost-side in the figure below:



2C1-diagonal bin + 2x2 analog bin to 1640x1232, then perform windowing to 1632x1224.

Revision 220426

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| Registers | Description |
| Newly added. |  |
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