TABLE 4.3 A SAMPLE CHANGE COUNTER DEVELOPMENT STRATEGY

		Date	
Name	7.0	Instructor	
Team	Example Team B Data	III GUI GOIOI	1
Part/Level	Change Counter/System	Cycle	1

		Су	cie I	.00	; (Сус	le H	our	s
Reference	Functions	1	2	3		1	2	3	
1.1	Compare modified program with prior version		Χ	L	_			_	4
1.2	Identify added and deleted LOC		180		_		18	4	_
	Count added and deleted LOC			10	0		<u> </u>	10	긔
1.3	Count total LOC in modified program				\Box		1_		
1.4	Attach line labels		50				5		
1.5	Provide change label header	50		_	1	5	1_		
1.6 1.7	Maintain change record history in header		100		_		10	1	
	Retain prior change history		<u> </u>	\perp	<u> </u>		\perp	\perp	_
1.8	New program source file with change info.	120				12	1	\perp	
1.9	Write for one programming language	Х					\perp		
1.10	Enhance to three languages								
1.11	Print program listing with change labels	50				5		_	
1.12	Print line numbers on listing		50	0 1	50		<u> </u>	5 '	15
1.13	Print program change report		T		75			17	7.5
1.14	Count text lines with coding standard		T		Х				
2.1	Count LOC with syntax counter		T						
2.2	OC Jeden and deleted I OC		7	₹					
2.3	t lines as added and deleted	T	7	<					
2.4	Live deleted pairs for change LOC	1	\top					\perp	
2.5	- II I-u - oction	X							
3.1	- difference in order	\top		Х					
3.2	- vorsion ()	1	10	20		T		10	
3.3	intermetion in label	5	0				5		
3.4	Provide charge from all the	5	0			T	5		
3.5		٦,	7			T			
3.6	note project data in label	1;	< T			T			L
3.	the with change number	-	1	50				15	
4.	1 Label each changed line with change that	\top	_		150	7			15
4.	2 Retain deleted line in comment	+			50	7			E
4.	Note previously deleted and added lines	+	\neg			T			Γ.
4.	4 Insert line numbers before listing lines	十		50				5	Γ
4.58	1 Where lines too long, roll to next line	十	_		150	5			1
4.58	2 Retain LOC count when rolling lines		-		T	\top			T
4	6 Retain original program indenting	\dashv	+	X		+	_		T
4	7 Indent rolled lines to middle of listing	- 1	85	50	10	0	18.5	5	1
	System control and overhead		505		-	-+	50.5	73	7
Totals								1	

TABLE 5.1 SAMPLE PLANNED-VALUE CALCULATIONS

		Cumulative	Plan Value	Cumulative
Task	Plan Hours	Hours	(PV)	PV
Launch and strategy	29.5	29.5	13.38	13.38
Planning	· 27.5	57.0	12.47	25.85
Requirements	17.0	74.0	7.71	33.56
System test plan	2.5	76.5	1.13	34.69
Requirements inspection	2.0	78.5	.91	35.60
High-level design	43.0	121.5	19.50	55.10
Integration test plan	2.0	123.5	.91	56.01
HLD inspection	5.0	128.5	2.27	58.28
Detailed design	14.0	142.5	6.35	64.63
Detailed design review	3.0	145.5	1.36	65.99
Test development	6.5	152.0	2.94	68.93
Detailed design inspection	2.5	154.5	1.13	70.07
Code	15.0	169.5	6.80	76.87
Code review	6.5	176.0	2.94	79.82
Compile	2.5	178.5	1.13	80.95
Code inspection	2.5	181.0	1.13	82.09
Unit test	1.5	182.5	.68	82.77
Build and integration	5.5	188.0	2.49	85.26
System Test	6.5	194.5	2.94	88.21
Documentation ·	9.0	203.5	4.08	92.29
Postmortem	17.0	220.5	7.71	100.00
Total	220.5		100.00	

TABLE 5.4 TSPi SIZE SUMMARY: FORM SUMS

	Plan	Assem	bly _		Actual	X	_		
Name	Example Team B Data					Date	*		
Team	Change Counter/Syste	m			· · · · · · · · · · · · · · · · · · ·	Date	uctor	1	
Part/Level						Cyci			
						—— <u> </u>	· .		
Product or Part Names and/or Numbers	Size Measure	Base	Deleted	Modified	Added	Reused	New and Changed	Total	Total New Reuse
SRS	Text Pages	-			11		11	11	
HLD	HLD Pages				18		18	18	
Main	DLD Lines				31		. 31	- — <u> </u>	
	LOC				160		160	160	
LOC	DLD Lines				16		16	16	
	LOC				12		12	12	
									-
Compare	DLD Lines				116		116	116	
	LOC				480		480	480	
indent	DLD Lines				102		102	102	
	LOC				182		182	182	
						 .			
Output	DLD Lines				 52		52	 52	\dashv
	. LOC				127		127	127	\dashv
							<u> </u>		
				 .					
									\dashv
									\dashv
Totals	Text Pages							11	\dashv
	HLD Pages				18		 - 18		
	DLD Lines			 , -	317			<u> </u>	
	LOC				961			 961	
									\dashv

TABLE 5.6 SAMPLE TASK PLANNING TEMPLATE: FORM TASK

2 5.0

5 2.0

5

5.5

5.0

2.0

3.0

73.4 73.3 68.6 64.8 68.8

2.0

3.0

2.0

3.0

2.0

3.0

Dc 5

Pm S

Documentation

Postmortem

Totals

Mgt. and misc.

Name .		Date	
Team .	Example Team B Data	Instructor	,
Part/Level	Change Counter/System	Cvcle	1

1			Task				•,	F	Plan Ho	ours				P	lan S	ize/V	alue		A	ctual	
	Phase	Part	Task Name		# Engineers	Team Leader	Development Manager	Planning Manager	Quality/Process Manager	Support Manager	Total Team Hours	Cumulative	υ	iize nits	Size	Week No.	Planned Value	Cumulative PV	Hours	Cumulative Hours	Wook No
ſ	St	5	Launch and strategy		5	2.9	5	1.3	1.3	1.3	11.8	11.8	3 Pa	ges	2	1	3.4	3.4	12.3	12.3	1
	Mg	5	Mgt. and misc.		5	3.0	3.0	3.0	3.0	3.0	15.0	26.8	3			1	4.3	7.7	. 10.0	22.3	1
	PI	5	Plan - task and schedu	le	5	4.5	4.5	9.0	4.5	4.5	27.0	53.8	3			2	7.7	15.4	13.3	35.6	2
	Pl	5	Generate Q&T plans		5	3.5	3.5	3.5	5.0	3.5	19.0	72.8	3			2	5.4	20.8	9.9	45.5	2
	Mg	5	Mgt, and misc.		5	3.0	3.0	3.0	3.0	3.0	15.0	87.8	3			3	4.3	25.1	3.4	48.9	2
	Rq	S	Review need statement	;	5	4.0	6.5	2.0	2.0	2.0	16,5	104.3	3 Pa	ges	3	3	4.7	29.9	17	65.9	2
Ī	Rq	5	Produce SRS		5	4.0	5.5	2.0	2.0	2.0	15.5	119.8	3 Pa	ges	54	3	4.4	34.3	15,6	81.4	2
	Rq	5	System test plan		0						0.0	119.8	3			3	0.0	34.3	0.0	81.4	2
	Rq	8	Req. inspection		4	2.0		2.0	2.0	2.0	8.0	127.8	3 Pa	ges	5	3	2.3	36.6	2.8	84.2	2
	Mg	5	Mgt. and misc.		5	2.0	2.0	2.0	2.0	2.0	10.0	137.8	3			4	2.9	39.5	5.9	90.1	2
	Hd	5	High-level design		5	2.0	3.5	1.0	2.0	1.0	9.5	147.3	3 Pa	ges	10	4	2.7	42.2	16.5	106.6	4
 Hd	Hd s	Inter	SDS gration plan	2	5 	4.0	2.0	2.0	2.0	4.0	18.0	165.3	5 Pa	ges 	20	1.1	48.5	47.3 4.0	9.5	1 16.1	4
Hd	5		Inspection	5	2.5	0.3	2.5	2.5	2.5	10.3			ages	10	5	2.9	51.4				ł
Mg	5		and misc.	5	2.0	2.0	2.0	2.0		-	-		идоо	1.0	5	2.9	54.3				
Dd	Р		illed design	4	3.0	3.0	3.0	1	3.0	12.0			ines	137	5	3.4	57.7		-		
Dr	Р	DLD	revlew	4	2.0	2.0	2.0	1	2.0	8.0		-+	Ines	137	5	. 2.3	60.0		192.4		
Td	5	Test	development	1					1,5	1,5	5 21	1.0		1	5	0,4	60.5				
DI	Р	DLD	Inspection	5	3.0	3.0	3.0	3.0	3.0	15.0	226	5.0 L	Ines	137	5	4.3	64.8				
Cd	Р	Code	;	5	3.6	3,6	3.6	3.6	3.6	18.0	244	l.O L	ines	410	5	5.2	69.9	8.1	209.4		
Cr	Р	Code	review	5	3.0	3.0	3,0	3.0	3.0	15.0	259	0.0 L	ОС	410	5	4.3	74.2	7.3	216.7	7 5	
Ср	P	Com	plle	5	0.4	0.4	0.4	0.4	0.4	2.0	26	1.0 L	ос	410	5	0.6	74.8	1.0	217.7	7 5	
Ci	Р	Code	inspection	5	1.0	1.0	1.0	1.0	1.0	5.0	266	5.0 L	ос	410	5	1.4	76.2	2.7	220.4	4 5	
UT	Р	Unit	test	5	1.5	1.5	1.5	1.5	1.5	7.5	273	5.5 L	ос	410	5	2.1	78.4	18.7	239.1	5	
Mg	5	Mgt.	and misc.	5	4.0	4,0	4.0	4.0	4.0	20.0	293	5.5			6	5.7	84.1	11.2	250.3	3 6	
St	5	Bulla	and integration	3		2.0		2.0	2.0	6.0	299	9.5 L	ос	410	6	1.7	85.8	1.6	251.8	3 6	
St	5	Syst	em test	3		4.0		4.0	4,0	12.0	31	i.5 L	ос	410	6	3.4	89.3	15.0	266.9	9 6	
_	ı . l				1 .	1	1	1	1		-1				1			1	7		1

10.0

10.0

17.5

349

321.5

331.5

349.0

Pages

15 6 2.9

6 2.9

6

92.1

95.0

5.0 100

100

1.6

2.0

9.5

280

268.4

270.4

280.0

6

6

6

TABLE 5.7 SAMPLE SCHEDULE PLANNING TEMPLATE: FORM SCHEDULE

Name		 Date	
Team	Example Team B Data	 Instructor	
	Change Counter/System	 Cycle	_ 1

			Plan		Actual					
Week No.	Date	Direct Hours	Cumulative Hours	Cumulative Planned Value	Team Hours	Cumulative Hours	Week Earned Value	Cumulative Earned Value		
1	9/14	26.8	26.8	7.7	27.0	27.0	7.7	7.7		
2	9/21	56.5	83.3	20.9	44.4	71.4	22.2	29.9		
3	9/28	47,0	130.3	36.6	35.8	107.2	9.6	39.5		
4	10/5	47.8	178.1	48.5	64.0	171.2	9.0	48.5		
5	10/12	107.0	285.1	78.4	75.4	246.6	29.9	78.4		
6	10/19	63.9	349.0	100.0	33.4	280.0	21.6	100.0		
					-					

TABLE 5.8 TSPI QUALITY CRITERIA: STANDARD QUAL

Measure	Goal	Comments
Percent Defect Free (PDF)		
Compile	> 10%	-
Unit Test	> 50%	
Integration Test	> 70%	
System Test	> 90%	
Defects/KLOC		
Total defects injected	. 75–150	If not PSP trained, use 100-200.
Compile	< 10	All defects flagged by compiler
Unit Test	< 5	Only major defects
Build and integration	< 0.5	Only major defects
System Test	< 0.2	Only major defects
Defect Ratios	10.2	Crity major delects
DLD review defects/unit test defects	> 2.0	Only major defects
Code review defects/compile defects	> 2.0	
Development Time Ratios	>2.0	Only major defects
Requirements inspection/requirements time	> 0.25	Industry distribution 4
HLD inspection/HLD time	> 0.25	Include elicitation time
DLD/coding time		Design work only, not studies
DLD review/DLD time	. > 1.00	
Code review/code time	> 0.5	
Review and Inspection Rates	> 0.5	
Requirements pages/hour	< 2	Single-spaced text pages
HLD pages/hour	. <5	Formatted design logic
DLD text lines/hour Code LOC/hour	<.100	Pseudocode lines equal about 3 LOC each
0000 200/1001	< 200	Logical LOC
Defect Injection Rates		I
Requirements defects/hour	0.25	Orbination
HLD defects/hour	0.25	Only major defects
DLD defects/hour	2.0	Only major defects
Code defects/hour	4.0	Only design defects
Compile defects/hour	0,3	Only major defects
Unit test defects/hour	0.2	All defects flagged by the compiler
Defect Removal Rates	0.2	Only major defects
Requirements inspection defects/hour	0.5	
HLD inspection defects/hour	0.5	Only major defects
DLD review defects/hour	0.5	Only major defects
DLD inspection defects/hour	2.0	Only design defects
Code review defects/hour	0.5	Only design defects
Code inspection defects/hour	6.0	Only major defects
Phase Yields	1.0	Only major defects
Requirements inspections		
Design reviews and inspections	~ 70%	Not counting editorial comments
Code reviews and inspections	~ 70%	Using state analysis, trace tables
Compile	~ 70%	Using personal checklists
Unit test at 5 or fewer defects/KLOC	~ 50%	90+ % of syntax defects
Build, integration, system test – at < 1.0 defects/KLOC	~ 90%	For high defects/KLOC: 50-75%
Process Yields	~ 80%	For high defects/KLOC: 30-65%
Before compile		
Before unit test	> 75%	Assuming sound design methods
	> 85%	Assuming logic checks in reviews
Before build and integration	> 97.5%	For small products, 1 defect max.
Before system test	> 99%	For small products did to

> 99%

For small products, 1 defect max.

TABLE 5.9 A QUALITY PLAN EXAMPLE: FORM SUMQ

Name		Date	
	Example Team B Data	Instructor	
rount	Change Counter/System	Cycle	

Summary Rates	Plan 1.17	Actual 3.43
LOC/hour	1.17 -	
% Reuse (% of total LOC)		
% New Reuse (% of N&C LOC)		
Percent Defect-Free (PDF)	80_	20
In compile	90	
In unit test	<u> </u>	
In build and integration	99	
In system test		
Defect/page	12	0
Requirements inspection		0
HLD inspection		
Defects/KLOC	20.2	55.2
DLD review	6.1	
DLD inspection	65.0	
Code review		28.
Compile		
Code inspection	4.1	
Unit test	0.4	
Build and integration		6.2
System test	151.2	
Total development	101.2	
Defect Ratios	13	0.90
Code review/Compile	4.3	3.3
DLD review/Unit test	4.5	
Development time ratios (%)	25	;
Requirements inspection/Requirements		
HLD inspection/HLD		49
DLD/code		2
DLD review/DLD	<u> </u>	
Code review/code	2,23	
A/FR		
Review rates	177 1	30.
DLD lines/hour	27.3	
Code LOC/hour	21,0	
Inspection rates	0.63	3.9
Requirement pages/hour		
HLD pages/hour	9.13	
DLD lines/hour	<u>9.13</u> 82.00	
Code LOC/hour		

TABLE 5.9 (continued)

Name		Date		
Team	Example Team B Data	Instructor		
Part/Level	Change Counter/System	Cycle	1	

efect-injection Rates (Defects/Hr.)	Plan	Actual
Requirements .	0.25	0.00
HLD	<u> </u>	0.00
DLD		2.1
Code	2.06	5.6
Compile	0.50	9.80
Unit test	0.00	0.3
Build and integration	0,00	0.0
System test	0.00	0.0
efect-removal Rates (Defects/Hr.)		
Requirements inspection	<u> </u>	. 0.0
HLD inspection	0.64	<u>In</u>
DLD review	1.03	5.0
DLD inspection	<u> </u>	1.6
Code review	1.78	3.5
Compile	3.10	26.4
Code inspection	0.87	0,0
Unit test	0.22	0.8
Build and integration	0.02	3.8
System test	0.00	0.4
hase Yields		
Requirements inspection	70	Ir
HLD inspection	70	lr
DLD review	70	58.
Test development		
DLD inspection	70	40.
Code review	70	40.
Compile	50	56.
Code inspection	70	0.
Unit test	90	59.
Build and integration	80	54.
System test	80	100.
System test		
rocess Yields	<i>8</i> 1,3	74
% before compile	97.0	· 86.
% before unit test	99.7	93.
% before build and integration	. 99.9	96.
% before system test	·	30.
% before system delivery		

TABLE 5.10 SAMPLE TSPI PLAN SUMMARY: FORM SUMP

Name

Build and integration

System test

Documentation

Name			Date	
Team	Example Team B Data		Instructor	
Part/Level	Change Counter/System		Cycle	1
Product :	Size ents pages (SRS)		Plan 5	Actual
Other text	pages			11
High-level	design pages (SDS)		10	18
	lesign lines		137	316
Base LOC	(B) (measured)			
Deleted	LOC (D)			
Modified	LOC (M)		(Estimated)	(Counted)
Added L	OC (A)		(Estimated)	(Counted)
Added	100 (A)		410	961
Reused	LOC (R)		(N–M)	(T-B+D-R)
Total Name			(Estimated)	(Counted)
iolai New	and Changed LOC (N)		410_	961
Total LOC	(T)		(Estimated)	(A+M)
10101 200			410	961
Total New	Reuse LOC		(N+B-M-D+R)	(Measured)
Estimated	Object LOC (E)			
Upper Pred	diction Interval (70%)			
Lower Pred	diction Interval (70%)			
	nase (hours)	Plan	Actual	Actual %
Launch	ment and miscellaneous	87.5	61.5	21.95
	and planning	<u>11.8</u> 46.0	12.3	4.39
Requirer	nents	32.0	<u>23.2</u> 32.6	8.29
System t			- 02.0	11.64
Requirer	nents inspection	8.0	2.8	1,00
High-leve	el design	27.5	26.0	9.29
	on test plan	4.0	4.0	1.43
High-leve	el design inspection	10.2		
Impleme	ntation planning			
Detailed		12.0	40.3	14.39
Test deve	design review	8.0	10.6	3.79
	design inspection	1.5		
Code	acaign mapeomon	<u> </u>	<u>8,9</u>	3.18
Code rev	iew	15.0	<u>8.0</u> 7.3	2.86
Compile	-	2.0	1.0	2.61 0.36
Code ins	pection	5.0	2.7	0.96
Unit test	·	7.5	18.7	6.68
D				

6.0

12.0

10.0

0.54

5.36

0.57

15.0

1.6

TABLE 5.10 (continued)

Name .		Date	
Team .	Example Team B Data	Instructor	
Part/Level	Change Counter/System	Cycle	1

Time in Phase (hours)	Plan	Actual	Actual %
Postmortem	10.0	2.0	0.71
Total	349.0	280.0	
Total Time UPI (70%)			
Total Time LPI (70%)			
Defects injected	Plan	Actual	Actual %
Strategy and planning			
Requirements	8		
System test plan			
Reguirements inspection			
High-level design	7		-
Integration test plan			
High-level design inspection		•	
Detailed design	9	85	51.81
Detailed design review		9	5.49
Test development	•		
Detailed design inspection			
Code	37	46	28.04
Code Code review		7	4.29
Compile	1	10	6.10
Code inspection · Unit test		6	3.66
	· · · · · · · · · · · · · · · · · · ·		
Build and integration		1	0.6
System test	62	164	
Total Development		Actual ·	Actual %
Defects Removed	Plan	Actual	Actual %
Strategy and planning			
Requirements			
System test plan			*****
Requirements inspection	5.60		
High-level design			
Integration test plan			
High-level design inspection	6.58		- 24
Detailed design		- 4	2.44
Detailed design review	8.27	53	32.3
Test development			
Detailed design inspection	2.48	15	9.15
Code		11_	6.7
Code review	26.65	26	15.85
Compile	6.21	27	16.46
Code inspection	4.35		
Unit test	1.68	16_	9.76
Duttel and take medical	0.15	6_	3.66
Build and integration			
System test	0.03	6 164	3.66

TABLE 7.4 SAMPLE STRAT FORM WITH COMPONENT ALLOCATION

Name		Date	
Hamo		Instructor	
Team		mon doto.	
	•	Cycle	
Part/Level		- ,	

		Сус	Cycle LOC		Cycle Hours		
Reference	Functions	1	2	3	1	2	3
	Diff					1_	-
1.1	Compare modified program with prior version		Α				↓_
1.2	Identify added and deleted LOC		Α			┷	1_
2.3	Compare for added and deleted LOC		Λ			<u> </u>	\perp
4.1	Label each change with change number (P)		Α			\perp	-
	Counter						\perp
1.3	Count added and deleted LOC			В		_	1
1.4	Count total LOC in modified program			В	ļ		
2.1	Count text lines with coding standard			В	_		\bot
2.4	Count changed lines as added and deleted		В		_		4-
3.3	Count new programs as version 0		В		_	4	\perp
4.5s2	Retain LOC count when rolling lines (P)			В	1	_	\bot
	Listing				L		\bot
1.5	Attach line labels		С		_	_	_ _
1.6	Provide change label header	С			L		_
1.7	Maintain change record history in header		С		1_		_
1.8	Retain prior change history			C/D	\perp	\perp	
3.1	Comment header section	D					
3.2	List prior program modifications in order		D	L	\perp	_	
3.4	Latermetics in label	D			_		_
3.5	to to to to lobol	D	_	<u> </u>	_		\perp
3.6		C/D			\perp		\perp
3.7	iinot data in lahel	C/D			_	_	\perp
4.1	the shange number (P)		D	1	\perp		\rightarrow
4.2			<u> </u>	C		\perp	
4.3				C	\perp		_
4.5s1	in the most line		С				_
4.582	the controlling lines (P)			CI	2		_
4.6	indonting		_	C/			
4.7	u u u middle of lieting		D		\perp		
7.	File			\perp		_	
1.9	Sile with change info	E					
	Report		1		_		
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