|  |  |  |  |
| --- | --- | --- | --- |
| **DRC Interface Control Document** | | | |
|  | **Ocupoint** | **Digital Design** | **Document Revision** |
| **Y. Khalil** | **1.3** |
| **Mechanical Design** | **Part Number** |
| **78 John Miller Way, STE 349** | **E. Pentland** | **0C-919-5-01** |
| **Kearny, NJ 07032** | **Systems Design** | **Release Date** |
| **862-239-1311** | **M. Orr** | **28 January 2024** |
| **CAGE Code** | **Approvals** | **Author** | **Program** |
| **7FWQ2** | **M. Orr** | **M. Orr** | **Big Bend** |
| **INFORMATION FOR PROGRAM USE ONLY** | | | |

# Section 1 Introduction

This ICD provides the documentation and detailed information required to understand, interface, and control the Digital Replacement Card (DRC). The DRC is a 90-Pin reprogrammable general purpose FPGA circuit card assembly (CCA) with 16-Channels of low-speed DAC and 8-Channels of switchable high-speed ADC/DAC.

|  |
| --- |
| A white object with a black background  Description automatically generated |
| Figure 1. DRC CCA |

Hardware Support

The following part numbers are support by the highest level version of the ICD below.

|  |  |  |
| --- | --- | --- |
| Name | Part Number | ICD Version |
| Digital Replacement Card (DRC) | 0C-063-1-01 | 1.3 |
| Table 1. HW Support | | |

Changelog

|  |  |  |
| --- | --- | --- |
| Version | Date | Notes |
| Initial Draft Release 1.0 | 22 February 2024 | Initial release |
| SWRI feedback updates 1.1 | 19 March 2024 | Added LEDs control table 9b, table 12b,-6V comments in section 4. |
| Post Board Fab Updates 1.2 | 20 June 2024 | Pin routing changes, AFE7222 LVDS -> CMOS operation |
| Setup Procedure Revision 1.3 | 18 September 2024 | Changes to setup procedure section for TCA6424 |
| Table 2. Changelog | | |

# Section 2 Specifications

* **Xilinx Zynq Ultra-Scale+ MPSoC ZU3, XCZU3EG1**
* **Quad, ARM® Cortex™-A53 Processors**
* **Dual, Arm Cortex R5 Real-Time Processors**
* **ARM Mail 400, GPU**
* **8-Channel High Speed 65 MSPS ADCs**
* **8-Channel High Speed 130 MSPS DACs**
* **16-Channel Low Speed DACs , 0 to 10V**
* **1 GB DDR4**
* **64 MB quad SPI flash**
* **JTAG edge connector**
* **90-pin G254001 Backplane Connector**
* **10 Pin low profile UART Connector**
* **-40C to 85C Operation\***
* **+15V, -15V, +5V Input**
* **Power dissipation between 3W and 6W**

# Section 3 Block Diagrams

The three major subsystems of the DRC are FPGA Subsystem, Digital to Analog Conversion Subsystem (DAC) and Analog to Digital (ADC) Subsystem. Programming/Debugging the FPGA Subsystem is achieved using a 6-pin edge connector that allows JTAG interfaces to the FPGA and a 10-pin low profile connector that allows UART, SPI interfaces to the FPGA. The FPGA PL GPIOs, DAC Subsystem, ADC Subsystem are accessible through the 90-pin backplane connector. The DRC has a output switch matrix (Pin Multiplexer) that allows multi-function pin usage on the backplane.

|  |
| --- |
|  |
| Figure 2. DRC System Architecture |

|  |
| --- |
|  |
| Figure 3. DRC Functional Diagram |

# Section 4 Interfaces

Mechanical Interface

The DRC Mechanically interfaces to the system through a 90-pin G254001 Backplane Connector. The DRC contains two removable keyed pins that can be installed to prevent insertion into backplane slots that do not match key.

|  |
| --- |
|  |
| Figure 4. 90-Pin DRC Connnector |

Electrical Interface

The DRC receives power from the system over the +5V, -15V and +15V pins. On some backplane profiles Pin 17 can be -6V. Ocupoint does not use -6V and will incorporate the –15V supply as a negative reference to avoid negative I/O voltage clamping.

|  |  |
| --- | --- |
| 90-PIN CONNECTOR | SIGNAL |
| 1 | GND |
| 13 | 15V |
| 15 | -15V |
| 30 | 5V |
| 31 | GND |
| 60 | 5V |
| 61 | GND |
| 90 | 5V |
| Table 3. Power Interface | |

Receive Interface

The DRC contains eight high-speed ADCs that can sample up to 65MSPS. The outputs are wired from the four AFE7222 devices to the following pins through a switch.

|  |  |
| --- | --- |
| 90-PIN CONNECTOR | SIGNAL |
| 51 | HS\_ADC0A |
| 21 | HS\_ADC0B |
| 48 | HS\_ADC1A |
| 17 | HS\_ADC1B |
| 46 | HS\_ADC2A |
| 33 | HS\_ADC2B |
| 50 | HS\_ADC3A |
| 55 | HS\_ADC3B |
| Table 4. HS ADC Pins | |
| Note: Table HS\_ADC3A -> SCH ADC\_3\_IN\_A | |

Transmit Interface

The DAC subsystem contains 16 low speed DACs and can be switched into the following pins using the LTC2666 DACs

|  |  |
| --- | --- |
| 90-PIN CONNECTOR | SIGNAL |
| 36 | LS0\_DAC00 |
| 10 | LS0\_DAC01 |
| 40 | LS0\_DAC02 |
| 74 | LS0\_DAC03 |
| 35 | LS0\_DAC04 |
| 34 | LS0\_DAC05 |
| 6 | LS0\_DAC06 |
| 3 | LS0\_DAC07 |
| 17 | LS1\_DAC00 |
| 48 | LS1\_DAC01 |
| 21 | LS1\_DAC02 |
| 51 | LS1\_DAC03 |
| 2 | LS1\_DAC04 |
| 32 | LS1\_DAC05 |
| 33 | LS1\_DAC06 |
| 46 | LS1\_DAC07 |
| Table 5. LS DAC Pins | |
| Note: Table LS0\_DAC06 -> SCH VOUT6\_0 | |

Or using the high-speed DACs from the AFE7222. The high speed DACs can output signals up to 130 MSPS.

|  |  |
| --- | --- |
| 90-PIN CONNECTOR | SIGNAL |
| 21 | HS\_DAC0A |
| 51 | HS\_DAC0B |
| 17 | HS\_DAC1A |
| 48 | HS\_DAC1B |
| 33 | HS\_DAC2A |
| 46 | HS\_DAC2B |
| 2 | HS\_DAC3A |
| 32 | HS\_DAC3B |
| Table 6. HS DAC Pins | |
| Note: Table HS\_DAC2A -> SCH DAC\_2\_OUT\_A | |

Digital Interfaces

Five FPGA to LS DAC pins provide control of the LTC2666 devices.

|  |  |  |
| --- | --- | --- |
| FPGA PIN (LOC\_BANK\_LANE) | LTC2666 | SCH LABEL |
| C16\_26P\_L5 | SDI | LSDATA |
| E16\_26P\_L9 | SDO | LSDOUT |
| E17\_26N\_L9 | SCK | LSCLK |
| C15\_25N\_L8 |  |  |
| E18\_26P\_L11 | CS\_A | SENL0 |
| D15\_25N\_L6 | CS\_B | SENL1 |
| Table 7. LTC2666 SPI Pins | | |

FPGA to HS DAC/ADC

The DRC contains four (0-3) TI AFE7222 devices. Each device contains dual DACs and dual ADCs. This enables the DRC to have 8 channels of high-speed ADC (65MSPS) and DAC (130MSPS). The control interface pins to the devices are shown below.

|  |  |  |
| --- | --- | --- |
| FPGA PIN (LOC\_BANK\_LANE) | AFE7222\_X | SCH LABEL |
| Y4\_64N\_L22 | SDATA | SDATA |
| Y3\_64N\_L23 | SDOUT | SDOUT |
| W3\_64P\_L23 | SCLK | SCLK |
| W2\_64N\_L16 | RESET | RESET |
| R13\_44P\_L11 | CLKINN | CLKIN\_N |
| R14\_44N\_L11 | CLKINP | CLKIN\_P |
| W4\_64P\_L22 | SEN\_0 | SEN0 |
| L1\_65P\_L8 | SEN\_1 | SEN1 |
| D1\_66N\_L8 | SEN\_2 | SEN2 |
| A9\_66P\_L23 | SEN\_3 | SEN3 |
| Table 8. AFE7222 SPI & SAMPLE CLOCK Pins | | |

|  |  |  |  |
| --- | --- | --- | --- |
| FPGA PIN (LOC\_BANK\_LANE) | AFE7222(0) | FPGA PIN (LOC\_BANK\_LANE) | AFE7222(1) |
| Y5\_64N\_L21 | DATA0\_0 | M2\_65P\_L9 | DATA0\_1 |
| W5\_64P\_L21 | DATA1\_0 | M1\_65N\_L8 | DATA1\_1 |
| Y6\_64N\_L20 | DATA2\_0 | N2\_65N\_L9 | DATA2\_1 |
| W6\_64P\_L20 | DATA3\_0 | N1\_65P\_L7 | DATA3\_1 |
| Y7\_64N\_L19 | DATA4\_0 | P2\_65P\_L12 | DATA4\_1 |
| W7\_64P\_L19 | DATA5\_0 | P1\_65N\_L7 | DATA5\_1 |
| Y8\_64N\_L10 | DATA6\_0 | R2\_65N\_L12 | DATA6\_1 |
| Y9\_64N\_L8 | DATA7\_0 | K4\_65N\_L10 | DATA7\_1 |
| W9\_64P\_L8 | DATA8\_0 | L4\_65P\_L11 | DATA8\_1 |
| Y10\_64N\_L9 | DATA9\_0 | M4\_65N\_L11 | DATA9\_1 |
| W10\_64P\_L9 | DATA10\_0 | N4\_65P\_L22 | DATA10\_1 |
| Y11\_64N\_L7 | DATA11\_0 | P4\_65N\_L22 | DATA11\_1 |
| W8\_64P\_L10 | DCLK\_0 | J4\_65P\_L10 | DCLK\_1 |
| FPGA PIN (LOC\_BANK\_LANE) | **AFE7222(2)** | **FPGA PIN (LOC\_BANK\_LANE)** | **AFE7222(3)** |
| E2\_66N\_L12 | DATA0\_2 | B9\_66N\_L23 | DATA0\_3 |
| E1\_66P\_L7 | DATA1\_2 | A8\_66P\_L13 | DATA1\_3 |
| F2\_66P\_L5 | DATA2\_2 | B8\_66N\_L13 | DATA2\_3 |
| F1\_66N\_L7 | DATA3\_2 | A7\_66P\_L21 | DATA3\_3 |
| G2\_66N\_L5 | DATA4\_2 | B7\_66N\_L21 | DATA4\_3 |
| G1\_66P\_L2 | DATA5\_2 | B4\_66N\_L19 | DATA5\_3 |
| H2\_66P\_L4 | DATA6\_2 | A4\_66P\_L19 | DATA6\_3 |
| J2\_66N\_L4 | DATA7\_2 | B3\_66N\_L10 | DATA7\_3 |
| J1\_66P\_L1 | DATA8\_2 | A3\_66P\_L10 | DATA8\_3 |
| K2\_66P\_L3 | DATA9\_2 | B2\_66P\_L9 | DATA9\_3 |
| K1\_66N\_L1 | DATA10\_2 | C1\_66P\_L8 | DATA10\_3 |
| L2\_66N\_L3 | DATA11\_2 | D2\_66P\_L12 | DATA11\_3 |
| H1\_66N\_L2 | DCLK\_2 | C8\_66P\_L15 | DCLK\_3 |
| Table 9. FPGA to AFE7222 Data Pins | | | |
| NOTE: DATA7\_1 represents ADCDATA7 & DACDATA7 on AFE7222#1 (connected together on PCB) | | | |

FPGA to LEDs

Four General Purpose LEDs will be connected to Bank 26 and can be controlled by writing to the following pins.

|  |  |
| --- | --- |
| FPGA PIN (LOC\_BANK\_LANE) | DRC LED |
| F16\_26N\_L10 | LED1 |
| F17\_26P\_L12 | LED2 |
| F18\_26N\_L12 | LED3 |
| E19\_26N\_L11 | LED4 |
| Table 9B LED FPGA Pin Map | |

FPGA to Backplane

Xilinx Zynq Ultrascale+ XCZU3 Banks in SFVC784 Package

|  |
| --- |
| A close-up of several different colored squares  Description automatically generated |
| Figure 5. FPGA I/O Banks |

|  |
| --- |
| A crossword puzzle with different colored squares  Description automatically generated |
| Figure 6. FPGA Pin Mapping to I/O Banks |

|  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 90-Pin Connector | | FPGA PIN (LOC\_BANK\_LANE) | | Description | | SCH LABEL | | 90-Pin  Connector | FPGA PIN (LOC\_BANK\_LANE) | Description | SCH LABEL |
| 1 | | NC | | GND | | GND | | 31 | NC | GND | GND |
| 2 | | U4\_65P\_L16 | | SP4T\_1 | | SP4T\_P2 | | 32 | T5\_65N\_L2 | SP4T\_4 | SP4T\_P32 |
| 3 | | D17\_26N\_L6 | | SPDT\_1,3/5 DP | | SPDT\_P3/5\_P | | 33 | T6\_65N\_L1 | SP4T\_5 | SP4T\_P33 |
| 4 | | A17\_26N\_L1 | | 4/6 DP | | SPDT\_P6/4\_P | | 34 | C18\_26P\_L7 | SPDT\_4,34/35 DP | SPDT\_P34/35\_P |
| 5 | | D16\_26P\_L6 | | 3/5 DP | | SPDT\_P3/5\_N | | 35 | C19\_26N\_L7 | SPDT\_5,34/35 DP | SPDT\_P34/35\_N |
| 6 | | A16\_26P\_L1 | | SPDT\_2,4/6 DP | | SPDT\_P6/4\_N | | 36 | D19\_26N\_L8 | SPDT\_6 | SPDT\_P36 |
| 7 | | C9\_66P\_L24 | | 7/8 DP | | P7/8\_P | | 37 | C6\_65P\_L24 | SE | P37 |
| 8 | | D9\_66N\_L24 | | 7/8 DP | | P7/8\_N | | 38 | D6\_65N\_L24 | SE | P38 |
| 9 | | B16\_26P\_L4 | | 9/10 DP | | SPDT\_P10/9\_P | | 39 | C12\_25P\_L5 | SE | P39 |
| 10 | | B17\_26N\_L4 | | SPDT\_3,9/10 DP | | SPDT\_P10/9\_N | | 40 | A15\_26N\_L3 | SPDT\_7 | SPDT\_P40 |
| 11 | | E4\_66P\_L14 | | 11/12 DP | | P11/12\_P | | 41 | C5\_65P\_L21 | SE | P41 |
| 12 | | F4\_66N\_L14 | | 11/12 DP | | P11/12\_N | | 42 | D5\_65N\_L21 | SE | P42 |
| 13 | | NC | | 15V | | V15P0 | | 43 | T4\_65N\_L15 | SE | P43 |
| 14 | | G5\_65P\_L13 | | SE | | P14 | | 44 | H5\_65N\_L13 | SE | P44 |
| 15 | | NC | | -15V | | -V15P0 | | 45 | T2\_64P\_L17 | 45/75 DP | P45/75\_P |
| 16 | | V18\_24P\_L5 | | 16/87 DP | | P16/87\_P | | 46 | T7\_64N\_L6 | SP4T\_6 | SP4T\_P46 |
| 17 | | T8\_64N\_L5 | | SP4T\_2 | | SP4T\_P17 | | 47 | V1\_64N\_L24 | 47/77 DP | P47/77\_P |
| 18 | | U5\_64P\_L14 | | 18/19 DP | | P18/19\_P | | 48 | T9\_64N\_L3 | SP4T\_7 | SP4T\_P48 |
| 19 | | V5\_64N\_L14 | | 18/19 DP | | P18/19\_N | | 49 | V2\_64P\_L16 | SE | P49 |
| 20 | | V8\_64N\_L4 | | SE | | P20 | | 50 | B14\_26P\_L2 | SPDT\_9 | SPDT\_P50 |
| 21 | | R8\_64P\_L5 | | SP4T\_3 | | SP4T\_P21 | | 51 | U11\_64P\_L2 | SP4T\_8 | SP4T\_P51 |
| 22 | | U9\_64P\_L1 | | 22/74 DP | | P22 | | 52 | V9\_64N\_L1 | SE | P52 |
| 23 | | V10\_64N\_L12 | | SE | | P23 | | 53 | T11\_44P\_L9 | 53/54 DP | P53/54\_P |
| 24 | | V12\_44P\_L7 | | SE | | P24 | | 54 | T12\_44N\_L9 | 53/54 DP | P53/54\_N |
| 25 | | U14\_44P\_L6 | | SE | | P25 | | 55 | B15\_26N\_L2 | SPDT\_10 | SPDT\_P55 |
| 26 | | U15\_44N\_L6 | | SE | | P26 | | 56 | V14\_44P\_L5 | SE | P56 |
| 27 | | U16\_24P\_L7 | | SE | | P27 | | 57 | V15\_44N\_L5 | SE | P57 |
| 28 | | U17\_24N\_L7 | | SE | | P28 | | 58 | V16\_24P\_L6 | SE | P58 |
| 29 | | U18\_24P\_L8 | | SE | | P29 | | 59 | V17\_24N\_L6 | SE | P59 |
| 30 | | NC | | 5V | | V5P0 | | 60 | NC | 5V | V5P0 |
| Table 10. DRC 90-Pin Output Wiring | | | | | | | | | | | |
| NOTE: PAIRS 3/5, 4/6, 47/77 ARE INVERTED ON FPGA. 22/74 NOT CONNECTED TO DIFF PAIR ON FPGA | | | | | | | | | | | |
| 90-Pin Connector | **FPGA PIN (LOC\_BANK\_LANE)** | | Description | | SCH LABEL | |
| 61 | NC | | GND | | GND | |
| 62 | B13\_25N\_L12 | | 62/63 DP | | P62/63\_P | |
| 63 | B12\_25P\_L12 | | 62/63 DP | | P62/63\_N | |
| 64 | E13\_25N\_L3 | | 64/65 DP | | P64/65\_P | |
| 65 | E12\_25P\_L3 | | 64/65 DP | | P64/65\_N | |
| 66 | D11\_25P\_L9 | | 66/67 DP | | P66/67\_P | |
| 67 | E11\_25N\_L9 | | 66/67 DP | | P66/67\_N | |
| 68 | E9\_66P\_L22 | | 68/69 DP | | P68/69\_P | |
| 69 | F9\_66N\_L22 | | 68/69 DP | | P68/69\_N | |
| 70 | C4\_66P\_L12 | | 70/71 DP | | P70/71\_P | |
| 71 | D4\_66N\_L12 | | 70/71 DP | | P70/71\_N | |
| 72 | G4\_66P\_L6 | | 72/73 DP | | P72/73\_P | |
| 73 | H4\_66N\_L6 | | 72/73 DP | | P72/73\_N | |
| 74 | A14\_26P\_L3 | | SPDT\_8,22/74 DP | | SPDT\_P74 | |
| 75 | U2\_64N\_L17 | | 45/75 DP | | P45/75\_N | |
| 76 | W18\_24P\_L1 | | 76/86 DP | | P76/86\_P | |
| 77 | U1\_64P\_L24 | | 47/77 DP | | P47/77\_N | |
| 78 | Y19\_24N\_L2 | | 78/88 DP | | P78/88\_P | |
| 79 | U7\_64P\_L13 | | 79/80 DP | | P79/80\_P | |
| 80 | V7\_64N\_L13 | | 79/80 DP | | P79/80\_N | |
| 81 | U8\_64P\_L4 | | SE | | P81 | |
| 82 | R10\_64P\_L12 | | 82/83 DP | | P82/83\_P | |
| 83 | T10\_64N\_L12 | | 82/83 DP | | P82/83\_N | |
| 84 | U12\_44P\_L8 | | 84/85 DP | | P84/85\_P | |
| 85 | U13\_44N\_L8 | | 84/85 DP | | P84/85\_N | |
| 86 | W19\_24N\_L1 | | 76/86 DP | | P76/86\_N | |
| 87 | V19\_24N\_L5 | | 16/87 DP | | P16/87\_N | |
| 88 | Y18\_24P\_L2 | | 78/88 DP | | P78/88\_N | |
| 89 | U19\_24N\_L8 | | SE | | P89 | |
| 90 | NC | | 5V | | V5P0 | |
| Table 10. DRC 90-Pin Output Wiring | | | | | | |
| NOTE: 78/88, 62/63, 64/65 REV POL | | | | | | |

JTAG Interface

|  |  |  |  |
| --- | --- | --- | --- |
| EDGE Connector | FPGA Signal Name | SCH LABEL | FPGA Pin |
| 1 | GND | GND |  |
| 2 | PS\_SRST\_B | JTAG\_RST | T29 |
| 3 | PS\_ TCK | TCK | T30 |
| 4 | PS\_TDI | TDI | R29 |
| 5 | PS\_TDO | TDO | R30 |
| 6 | PS\_TMS | TMS | R28 |
| Table 11. JTAG Pins | | | |

# Section 5 Control

Operational Mode Control

The functionality of DRC can be changed by the 4-way switch that is connected to pins 2,17,21,32,33,46,48,51 of the 90-pin backplane interface connector. The 4-way switches connected to each of the pins allow multiple functions to be routed to the backplane pin. The four functions are Low Speed DAC, High Speed DAC, High Speed ADC, or FPGA IO.

|  |  |  |
| --- | --- | --- |
| Operational  Mode | Configuration | Description |
| 1 | LS DAC | 90 Pin connector configured for Low-Speed DAC outputs |
| 2 | FPGA PL | 90 Pin connector configured for FPGA GPIO |
| 3 | HS ADC | 90 Pin connector configured for High-Speed ADC inputs |
| 4 | HS DAC | 90 Pin connector configured for High-Speed DAC outputs |
| Table 12.DRC Operational configurations | | |

The TCA6424A is a 24-bit I/O expander that controls QTY (8) 4-way switches used to route different functionality to the backplane. The I2C Address of the TCA6424A is “34d” or “0x22h” and the connectivity between the ports of the IO expander and the SP4T switches are shown in the table below. Note: the manufacturer skips P8, P9, P18, P19. The outputs are connected to the two control pins (A0(SCHEMATIC - SWX\_CTRL1) and A1(SCHEMATIC - SWX\_CTRL2)) of the TMUX6104PWR SP4T switches. The truth table for the switch is shown below.

For example, to switch functionality of low speed DAC to pin 2 on the backplane, then I/O expander ports P00 and P01 must be low to select port #1 of SP4T switch #1.

|  |
| --- |
| A diagram of a computer chip  Description automatically generated |
| Figure 7. TCA6424A Pinout |

To configure the TCA6424A is as follows:

1. Setup TCA6424A ports to function as outputs (port bit = 0) in the TCA6424A three 8-bit configuration registers (0xC,0xD,0xE) representing all 24 pins that can function as outputs or inputs. Unused ports will be configured as inputs (port bit = 1).
   1. Byte 1 = Device Address (0x22) followed by a 0 (write) -> 0x22 << 1 -> 0x44
   2. Byte 2 = configure port command
      1. Use 0x0C for individual register writes
      2. Use 0x8C to auto increment register
   3. Following Bytes = configuration bytes (All used pins as outputs. All unused pins don’t matter, but will set as inputs).
   4. Option 1:
      1. Write {0x22 << 1, 0x0C, 0x00} to configure P7-0 as outputs
      2. Write {0x22 << 1, 0x0D, 0x00} to configure P17-10 as outputs
      3. Write {0x22 << 1, 0x0E, 0xFE} to configure P20 as output, P27-21 unused and set as inputs
   5. Option 2:
      1. Write {0x22 << 1, 0x8C, 0x00, 0x00, 0xFE} in one transaction
2. Write value desired to the P00 - P27 pins at register addresses 0x04, 0x05,0x06.
   1. In this case we just want to set P01 and P02 low.
   2. Write: {0x22 << 1, 0x04, 0xF9} this sets register4[1111 1001]
   3. Using register address 0x84, you can write all ports at once. Ex {0x22 << 1, 0x84, 0xF9, 0x00, 0x00}

|  |
| --- |
| A white grid with black numbers  Description automatically generated |
| Table 12B. TCA6424A Default Register 4,5,6 (output port, 8-bit registers) |

|  |
| --- |
| A screenshot of a video game  Description automatically generated |
| Figure 8. TCA6424A I2C Setup |

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| TCA6424A  PORT | TMUX6104  CONTROL | DRC  OUTPUT  PIN | TCA6424A  PORT | TMUX6104  CONTROL | DRC  OUPTUT  PIN | TCA6424A  PORT | TMUX6104  CONTROL | DRC  OUPTUT  PIN |
| P00 | SW0\_CTRL2 | 51 | P10 | SW0\_CTRL1 | 51 | P20 | P17\_EN | 17 |
| P01 | SW1\_CTRL2 | 21 | P11 | SW1\_CTRL1 | 21 | P21 |  |  |
| P02 | SW2\_CTRL2 | 48 | P12 | SW2\_CTRL1 | 48 | P22 |  |  |
| P03 | SW3\_CTRL2 | 17 | P13 | SW3\_CTRL1 | 17 | P23 |  |  |
| P04 | SW4\_CTRL2 | 46 | P14 | SW4\_CTRL1 | 46 | P24 |  |  |
| P05 | SW5\_CTRL2 | 33 | P15 | SW5\_CTRL1 | 33 | P25 |  |  |
| P06 | SW6\_CTRL2 | 32 | P16 | SW6\_CTRL1 | 32 | P26 |  |  |
| P07 | SW7\_CTRL2 | 2 | P17 | SW7\_CTRL1 | 2 | P27 |  |  |
|  | Table 13. IO EXPANDER Output port to DRC output pin | | | | | | | | |
| NOTE: SINCE P17 MAY HAVE -6V ON SOME BACKPLANES, P20 ON THE TCA6424A IS USED TO ENABLE THAT SWITCH. SWITCH MUST BE DISABLED WHEN -6V IS ON P17. | | | | | | | | | |

Switch Control SP4T (TMUX6104PWR) Truth Table

|  |  |  |  |
| --- | --- | --- | --- |
| EN | VCTL 1 | VCTL 2 | Switch Port # |
| L | X | X | NO CONNECTION |
| H | L | L | 1 |
| H | L | H | 2 |
| H | H | L | 3 |
| H | H | H | 4 |
|  | Table 14. SP4T Truth Table | | |

SPDT Switch control is handled by the SiP directly. The following Table are the FPGA pin assignments to control the SPDT switches.

|  |  |  |  |
| --- | --- | --- | --- |
| FPGA PIN (LOC\_BANK\_LANE) | 90-PIN CONNECTOR | FUNCTION A | FUNCTION B |
| F10\_66N\_L16 | 3 | LS0\_DAC07 | D17\_26N\_L6 |
| C13\_25N\_L5 | 6 | LS0\_DAC06 | A16\_26P\_L1 |
| D14\_25P\_L6 | 10 | LS0\_DAC01 | B17\_26N\_L4 |
| E8\_65P\_L20 | 34 | LS0\_DAC05 | C18\_26P\_L7 |
| F7\_66N\_L20 | 35 | LS0\_DAC04 | C19\_26N\_L7 |
| D10\_66N\_L17 | 36 | LS0\_DAC00 | D19\_26N\_L8 |
| D13\_25N\_L4 | 40 | LS0\_DAC02 | A15\_26N\_L3 |
| E15\_25N\_L7 | 50 | HS\_ADC3A | B14\_26P\_L2 |
| E14\_25P\_L7 | 55 | HS\_ADC3B | B15\_26N\_L2 |
| C14\_25P\_L8 | 74 | LS0\_DAC03 | A14\_26P\_L3 |
| Table 15. SP4T Truth Table | | | |
| NOTE: 90-PIN CONNECTOR Pin 3 corresponds to SPDT SEL Label P3\_SEL on schematic. Function A corresponds to Path A(SXA) <-> Pin 3(DX) path in Table 16. | | | |

TMUX4053BQBR (SPDT)

|  |  |
| --- | --- |
| SELX | PATH |
| L | SXA<->DX |
| H | SXB<->DX |
| Table 16. SPDT Truth Table | |

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| 90-PIN Backplane Pin | Switch Port # | | | |  |  |
| 1 | 2 | 3 | 4 | SP4T # | SPDT # |
| 2 | LS1\_DAC04 | U4\_65P\_L16 | NC | HS\_DAC3A | 7 |  |
| 17 | LS1\_DAC00 | T8\_64N\_L5 | HS\_ADC1B | HS\_DAC1A | 3 |  |
| 21 | LS1\_DAC02 | R8\_64P\_L5 | HS\_ADC0B | HS\_DAC0A | 1 |  |
| 32 | LS1\_DAC05 | T5\_65N\_L2 | NC | HS\_DAC3B | 6 |  |
| 33 | LS1\_DAC06 | T6\_65N\_L1 | HS\_ADC2B | HS\_DAC2A | 5 |  |
| 46 | LS1\_DAC07 | T7\_64N\_L6 | HS\_ADC2A | HS\_DAC2B | 4 |  |
| 48 | LS1\_DAC01 | T9\_64N\_L3 | HS\_ADC1A | HS\_DAC1B | 2 |  |
| 51 | LS1\_DAC03 | U11\_64P\_L2 | HS\_ADC0A | HS\_DAC0B | 0 |  |
| 3 | LS0\_DAC07 | D17\_26N\_L6 |  |  |  | 1 |
| 6 | LS0\_DAC06 | A16\_26P\_L1 |  |  |  | 2 |
| 10 | LS0\_DAC01 | B17\_26N\_L4 |  |  |  | 3 |
| 34 | LS0\_DAC05 | C18\_26P\_L7 |  |  |  | 4 |
| 35 | LS0\_DAC04 | C19\_26N\_L7 |  |  |  | 5 |
| 36 | LS0\_DAC00 | D19\_26N\_L8 |  |  |  | 6 |
| 40 | LS0\_DAC02 | A15\_26N\_L3 |  |  |  | 7 |
| 74 | LS0\_DAC03 | A14\_26P\_L3 |  |  |  | 8 |
| 50 | HS\_ADC3A | B14\_26P\_L2 |  |  |  | 9 |
| 55 | HS\_ADC3B | B15\_26N\_L2 |  |  |  | 10 |
| Table 17. Backplane pin and multi-function assignment based on Switch port selected | | | | | | |

Low Speed DAC Control

Dual LTC2666-16 devices are used for the 16 low speed digital to analog converters (DAC) and are accessible through the PL of the FPGA. Both LTC2666 devices (LTC2666(0) and LTC2666(1)) share MOSI, MISO, SCLK lines and have independent chip select (CS) lines. The CS lines will be held high by default and must be toggled low for the SPI command to be clocked in. The LTC2666-16 is a 16-bit device and is configured for output between 0-10V represented by 0xFFFFh or 0-65535d. Each device consists of 8 channels (DAC0-DAC7). The device is SPI controlled with 24-bit SPI message. 4 bits are used for commands codes and 4 bits are used for DAC addressing.

|  |  |
| --- | --- |
|  |  |
| Command Codes | DAC Addresses |
| Table 17. LTC2666 SPI Configuration | |

The 24-bit structure is as follows:

|  |
| --- |
|  |
| Figure 9. SPI Timing diagram LTC2666 |

An example of the 24-bit SPI command **0x30 FFFF** can be broken down to: COMMAND WORD= “0011,” *Write Code to DAC n, Update DAC n (Power Up)*, ADDRESS WORD = “0000”, *Write to DAC 0*, DATA WORD = “FFFF”, *data value 65535 decimal representing 10V output*. The SPI message in this example is broken down into three 8-bit transfers. The timing of the SPI word and the output of DAC 0 is shown on the oscilloscope CH1 at 10V is shown below.

|  |
| --- |
| A screenshot of a computer  Description automatically generated |
| A screen shot of a graph  Description automatically generated |
| Figure 10. Setting DAC 0 to 10V, 65535 (0x30 FFFF) |

To update DAC 1 to 10V, the 24-bit SPI command **0x31 FFFF** can be broken down to: COMMAND WORD= “0011,” *Write Code to DAC n, Update DAC n (Power Up)*, ADDRESS WORD = “0001”, *Write to DAC 1*, DATA WORD = “FFFF”, *or data value 65535 decimal representing 10V output*. The SPI message in this example is broken down into three 8-bit transfers. The timing of the SPI word and the output of DAC 1 is shown on the oscilloscope CH2 at 10V is shown below.

|  |
| --- |
| A screenshot of a computer  Description automatically generated |
|  |
| Figure 11. Setting DAC 1 to 10V, 65535 (0x31 FFFF) |

To update DAC 0 to 5V, the 24-bit SPI command **0x30 8000** can be broken down to: COMMAND WORD= “0011,” *Write Code to DAC n, Update DAC n (Power Up)*, ADDRESS WORD = “0000”, *Write to DAC 0*, DATA WORD = “8000”, *or data value 32768 decimal representing 5V output*. The SPI message in this example is broken down into three 8-bit transfers. The timing of the SPI word and the output of DAC 0 is shown on the oscilloscope CH1 at 5V is shown below.

|  |
| --- |
| A screenshot of a computer  Description automatically generated |
| A screen shot of a device  Description automatically generated |
| Figure 12. Setting DAC 0 to 5V, 32768 (0x30 8000) |

To update DAC 1 to 5V, the 24-bit SPI command **0x31 FFFF** can be broken down to: COMMAND WORD= “0011,” *Write Code to DAC n, Update DAC n (Power Up)*, ADDRESS WORD = “0001”, *Write to DAC 1*, DATA WORD = “8000”, *or data value 32768 decimal representing 5V output*. The SPI message in this example is broken down into three 8-bit transfers. The timing of the SPI word and the output of DAC 1 is shown on the oscilloscope CH2 at 5V is shown below.

|  |
| --- |
| A screenshot of a computer  Description automatically generated |
|  |
| Figure 13. Setting DAC 1 to 5V, 32768 (0x31 8000) |

High Speed DAC / ADC Control

The DRC contains four AFE7222 devices that provide 8 channels of 65MSPS ADC and 8-channels of 130MSPS DAC. Independent control of each device is done through the SPI bus (different Enable lines for each device). The FPGA SPI control pins to the AFE7222 devices are in table 18. The format is 12bit address bits and 8 bits data. There are 141 registers that control the Tx and Rx control of the AFE7222 (config0 to config140)

|  |
| --- |
|  |
| Figure 14. AFE7222 Block Diagram |

|  |  |
| --- | --- |
| FPGA PIN | AFE7222\_X |
| Y4\_64N\_L22 | SDATA |
| Y3\_64N\_L23 | SDOUT |
| W3\_64P\_L23 | SCLK |
| W4\_64P\_L22 | SEN0 |
| L1\_65P\_L8 | SEN1 |
| D1\_66N\_L8 | SEN2 |
| A9\_66P\_L23 | SEN3 |
| Table 18. SPI control pins AFE7222 | |

|  |
| --- |
|  |
| Figure 15. AFE7222 SPI Write format |

Data input (DAC) and output (ADC) of the AFE7222 is done over 12 CMOS signals shared as a bus between the ADCs and DACs. Each AFE7222 has its own 12 bit parallel data bus, along with a bit clock signal.

|  |
| --- |
|  |
| Figure 16. AFE7222 Data timing |

|  |  |  |  |
| --- | --- | --- | --- |
| FPGA PIN (LOC\_BANK\_LANE) | AFE7222(0) | FPGA PIN (LOC\_BANK\_LANE) | AFE7222(1) |
| Y5\_64N\_L21 | DATA0\_0 | M2\_65P\_L9 | DATA0\_1 |
| W5\_64P\_L21 | DATA1\_0 | M1\_65N\_L8 | DATA1\_1 |
| Y6\_64N\_L20 | DATA2\_0 | N2\_65N\_L9 | DATA2\_1 |
| W6\_64P\_L20 | DATA3\_0 | N1\_65P\_L7 | DATA3\_1 |
| Y7\_64N\_L19 | DATA4\_0 | P2\_65P\_L12 | DATA4\_1 |
| W7\_64P\_L19 | DATA5\_0 | P1\_65N\_L7 | DATA5\_1 |
| Y8\_64N\_L10 | DATA6\_0 | R2\_65N\_L12 | DATA6\_1 |
| Y9\_64N\_L8 | DATA7\_0 | K4\_65N\_L10 | DATA7\_1 |
| W9\_64P\_L8 | DATA8\_0 | L4\_65P\_L11 | DATA8\_1 |
| Y10\_64N\_L9 | DATA9\_0 | M4\_65N\_L11 | DATA9\_1 |
| W10\_64P\_L9 | DATA10\_0 | N4\_65P\_L22 | DATA10\_1 |
| Y11\_64N\_L7 | DATA11\_0 | P4\_65N\_L22 | DATA11\_1 |
| W8\_64P\_L10 | DCLK\_0 | J4\_65P\_L10 | DCLK\_1 |
| FPGA PIN (LOC\_BANK\_LANE) | **AFE7222(2)** | **FPGA PIN (LOC\_BANK\_LANE)** | **AFE7222(3)** |
| E2\_66N\_L12 | DATA0\_2 | B9\_66N\_L23 | DATA0\_3 |
| E1\_66P\_L7 | DATA1\_2 | A8\_66P\_L13 | DATA1\_3 |
| F2\_66P\_L5 | DATA2\_2 | B8\_66N\_L13 | DATA2\_3 |
| F1\_66N\_L7 | DATA3\_2 | A7\_66P\_L21 | DATA3\_3 |
| G2\_66N\_L5 | DATA4\_2 | B7\_66N\_L21 | DATA4\_3 |
| G1\_66P\_L2 | DATA5\_2 | B4\_66N\_L19 | DATA5\_3 |
| H2\_66P\_L4 | DATA6\_2 | A4\_66P\_L19 | DATA6\_3 |
| J2\_66N\_L4 | DATA7\_2 | B3\_66N\_L10 | DATA7\_3 |
| J1\_66P\_L1 | DATA8\_2 | A3\_66P\_L10 | DATA8\_3 |
| K2\_66P\_L3 | DATA9\_2 | B2\_66P\_L9 | DATA9\_3 |
| K1\_66N\_L1 | DATA10\_2 | C1\_66P\_L8 | DATA10\_3 |
| L2\_66N\_L3 | DATA11\_2 | D2\_66P\_L12 | DATA11\_3 |
| H1\_66N\_L2 | DCLK\_2 | C8\_66P\_L15 | DCLK\_3 |
| Table 19. FPGA to AFE7222 Data Pins | | | |
| NOTE: DATA7\_1 represents ADCDATA7 & DACDATA7 on AFE7222#1 (connected together on PCB) | | | |