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PROGRAM: HCS

COURSE CODE: HCS113

1. **The five stages for the instruction pipeline are:**
   i. Instruction fetch.
   ii. Decode.
   iii. Execute.
   iv. Memory access.
   v. Write back.
2.
   a) **Calculating the number of clock cycles that would be required to complete these 4 instructions.**
   Firstly, we would consider the maximum delay in each stage:
   - For **IF** the maximum delay is **2 cycles** for **I2**
   - For **ID** the maximum delay is **3 cycles** for **I3**
   - For **EX** the maximum delay is **3 cycles** for **I2**
   - For **WB** the maximum delay is **2 cycles** for **I4**

   Adding the maximum delays together to find the total number of clock cycles:
   Total number of clock cycles = IF max delay + ID max delay + EX max delay + WB max delay
   Total number of clock cycles = 2 + 3 + 3 + 2
   ∴ **Total number of clock cycles** = 10

   b) **Calculating the speed up.**

$$Speed\ up\ = \frac{Number\ of\ stages\ \times Clock\ cycles\ per\ instruction\ without\ pipeling}{Number\ of\ stages + \ Pipeline\ overhead\ per\ instruction}$$

$$Speed\ up\ = \frac{4\ \times 10}{4 + 4 - 1}$$

$$Speed\ up\ = \frac{40}{7}$$

$$Speed\ up\ \approx 5.741$$