DESIGN SPECIFICATION

for

OCP2APB BRIDGE

REFERENCES

[1] Open Core Protocol Specification 3.0
[2] AMBA APB Protocol Specification 2.0

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FIGURES LIST

1. DESIGN OVERVIEW

This design is an OCP2APB bridge, with an intended functionality of bridging OCP master and APB slave peripherals, making communication between them possible. A block diagram of an intended application of this design is shown on fig. 1.

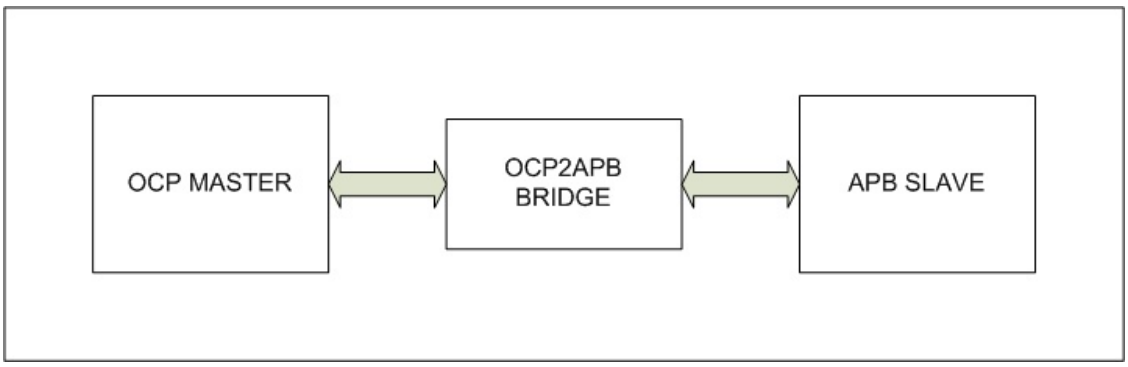

Figure 1: Intended application of design

1.1 ARCHITECTURE DESCRIPTION

The architecture of the OCP2APB bridge is shown on fig. 2. It consists of three registers: Address register, Data write register and Data read registers. They are used to temporarily store data and address sent from both master and slave. They have a reset input, which is asserted low, and a clock enable input, which is asserted high. For the needs of a properly functioning SResp and PSlverr signals a D filp flop is a part of the architecture, and it is used to delay the PSlverr signal for one clock signal. At the center of the OCP2APB bridge is the Control unit, realized as a finite state machine (FSM). Because of the higher level of complexity of the control FSM, a whole section will be dedicated to its description.

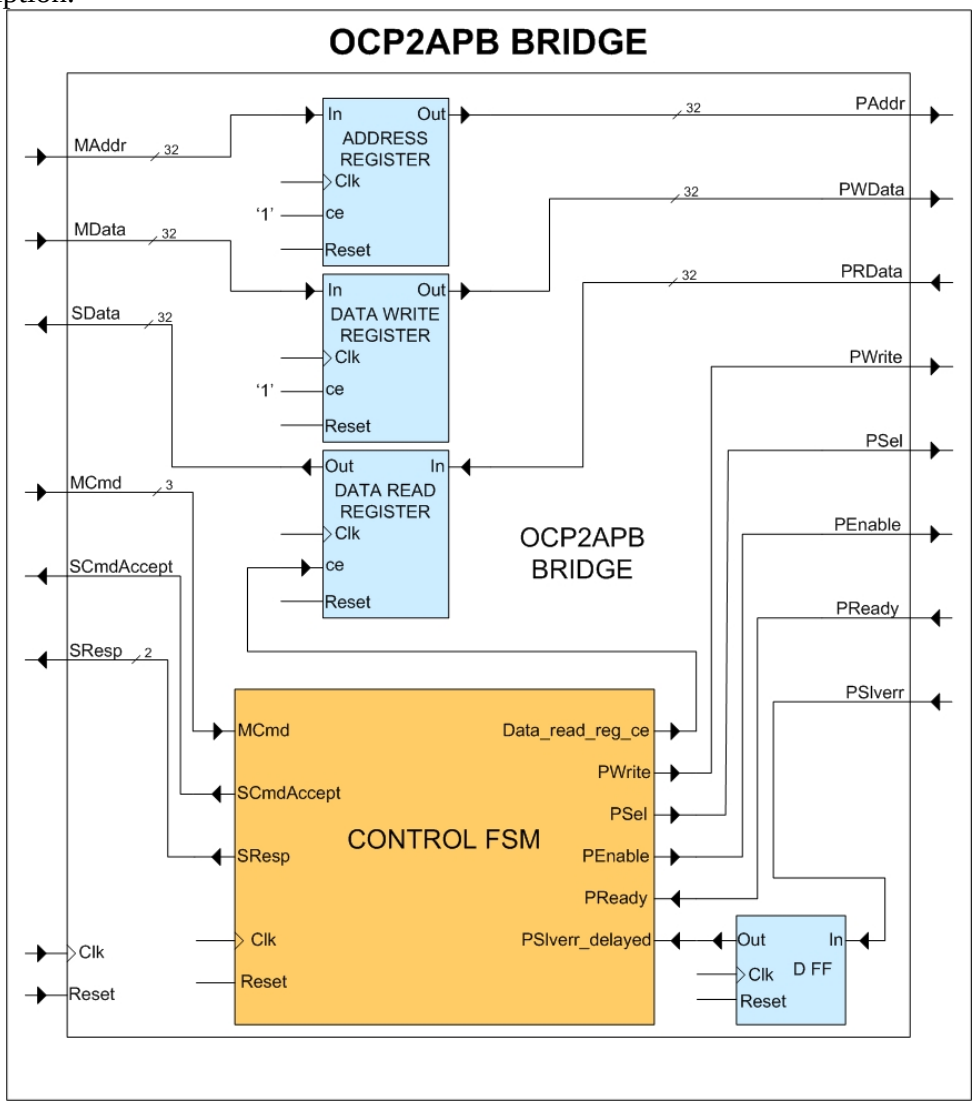

Figure 2: OCP2APB bridge architecture

1.2 DESIGN INTERFACE DESCRIPTION

The OCP2APB bridge has two interfaces: an OCP interface and an APB interface. The list of signals in each interface is listed in the three tables below.

Table 1. Clk and Reset signals

Name	Direction	Width	Signal
Clk	in	1	Clock signal
Reset	in	1	Reset signal

Table 2. List of OCP interface signals

Name	Direction	Width	Signal
MAddr	in	32	Master address signal
MData	in	32	Master data signal
SData	out	32	Slave data signal
MCmd	in	3	Master command signal
SCmdAccept	out	1	Slave command accept signal
SResp	out	2	Slave response signal

Table 3. List of APB interface signals

Name	Direction	Width	Signal
PAddr	out	32	Master address signal
PWData	out	32	Master data signal
PRData	in	32	Slave data signal
PWrite	out	1	Read/Write signal
PSel	out	1	Master select slave signal
PEnable	out	1	Master enable slave signal
PReady	in	1	Slave ready signal
PSlverr	in	1	Slave error indication

1.2.1 SIGNALS DESCRIPTION

Clk:
Clock signal, positive polarity
Reset:
Reset signal, asserted low
MAddr:
Master OCP address signal
MData:
Master OCP data signal, from OCP master to OCP slave, used during write command
SData:
Slave OCP data signal, from OCP slave to OCP master, used during read command
MCmd:
Master OCP command signal, used to send information on command to slave. Only IDLE (OPCode "000"), READ (OPCode "001") and WRITE (OPCode "010") are supported
SCmdAccept:
Slave OCP command accept response signal. When '0', slave has not processed the command, so the master must keep the MCmd, MData and MAddr signals asserted. When '1', the slave has processed the command, and the OCP transaction is over.
SResp:
Slave OCP response signal. Informs the master if data is valid (OPCode "01") or an error has happened (OPCode "11"). No slave response is a NULL (OPCode "00").
PAddr:
Master APB address signal
PWData:
Master APB data signal, from APB master to APB slave, used during write command
PRData:
Slave APB data signal, from APB slave to APB master, used during read command
PWrite:
Read (asserted high) and write (asserted low) APB command signal, from master to slave
PSel:
Master APB select slave signal, indicates to slave that master is ready for a transaction
PEnable:
Master APB enable slave signal, indicates the start of the access phase
PReady:
APB Slave ready signal, indicates that the slave is ready for a new transaction
PSlverr:
APB Slaver error indication signal, indicates that there has been an error during a read transaction

1.3 CONTROL FSM DESCRIPTION

The Control FSM is realised as a Moore machine with nine states. The state diagram is shown on fig. 3. The fist state is IDLE, and is the state after reset. Depending on the OCP MCmd signal from the master, the next state can be RD_SETUP or WR_SETUP (read or write setup state). Those states are the states when the bridge selects the APB slave and sends the command. The transition to the next state from both read and write setup states is unconditional. In the next state, RD_WAIT or WR_WAIT (read or write wait), if the ready signal from the APB slave is not asserted, the machine will stay in the same state, and assert the APB slave enable signal. If the slave signals it is ready, the next state is the RD_ACCESS or WR_ACCESS state (read or write access state). In the write access state, the bridge asserts the OCP slave command accept signal, signaling the end of an OCP write transaction. In the read access state, the bridge does the same and also checks the slave error delayed signal. If there was no error, the next state is RD_RESP_DV (read response data valid), where the slave signals the master OCP with the slave response signal that the data is valid, and sends the data (because of the timing differences in the data signals the clock enable of the data read register is deserted in this state). If there was an error, the next state is RD_RESP_ERR (read response error), where the slave signals an error the master OCP with the slave response signal, and sends the data anyway.

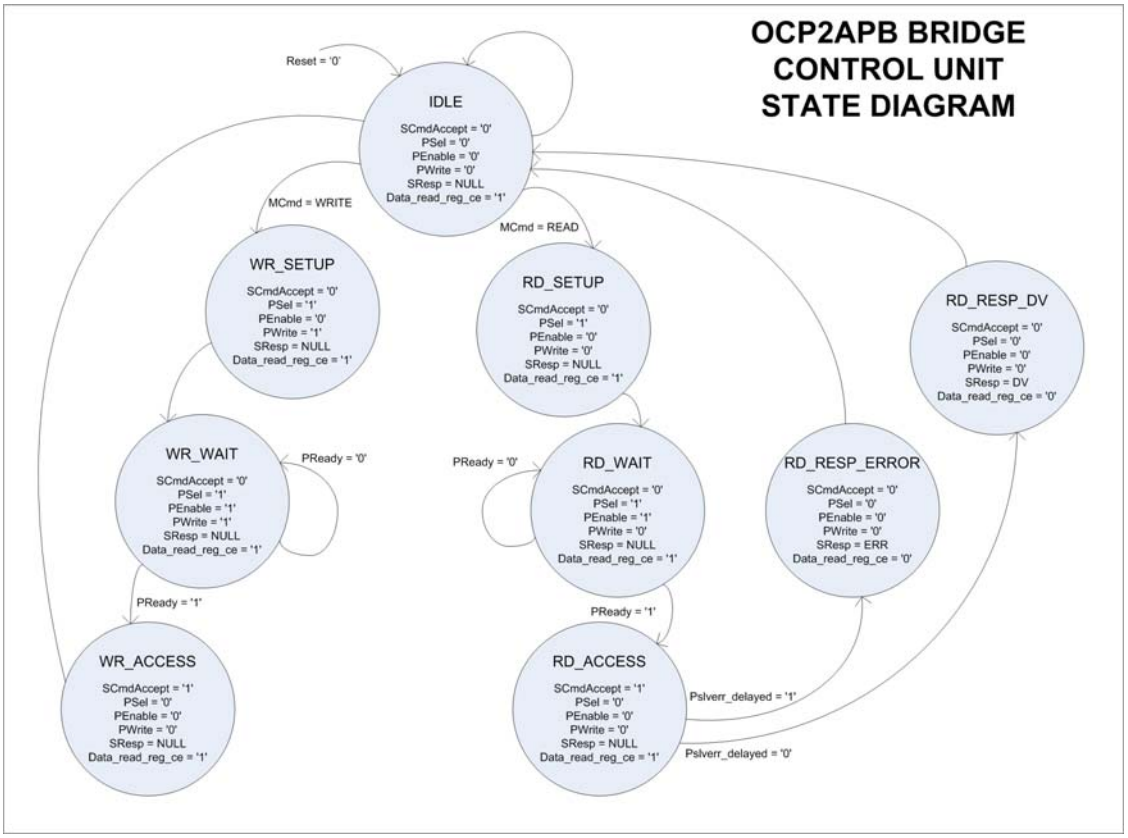

Figure 3: Control unit state diagram

2. TYPICAL WAVEFORMS

2.1 WRITE TRANSACTION

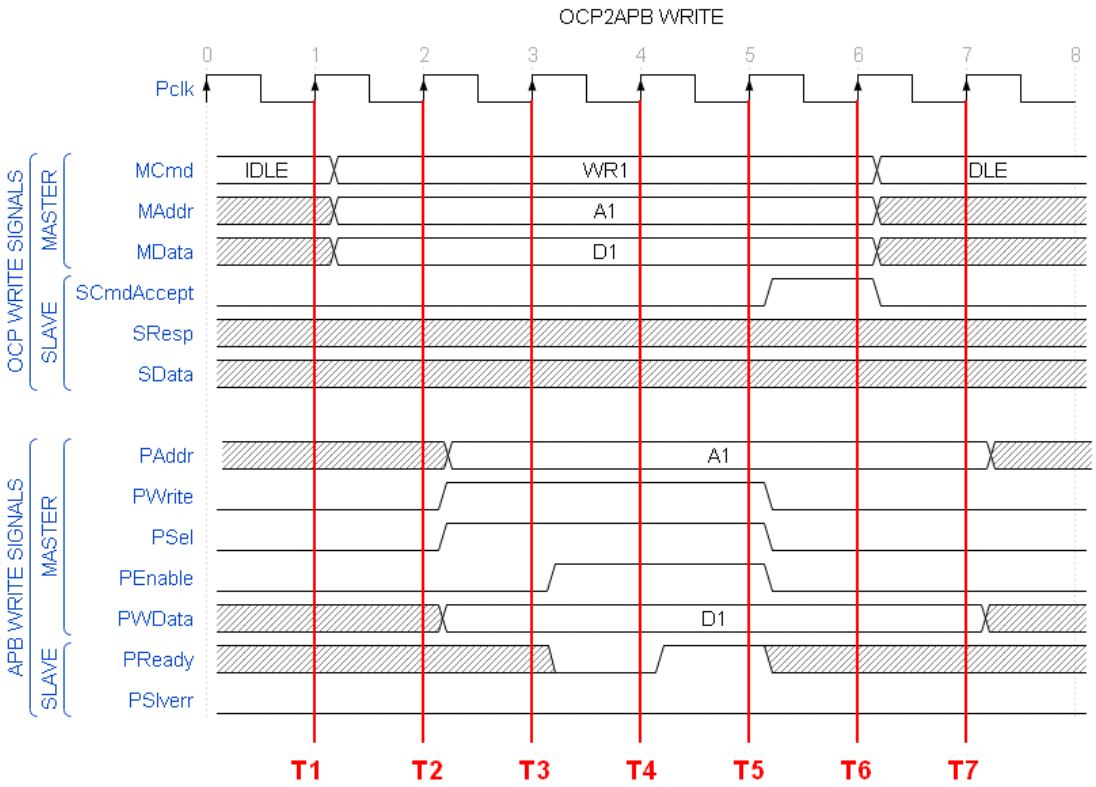

Figure 4: Write transaction

A typical write transaction (with wait states) is shown in figure 4.

T1 – The master OCP changes MCmd to WR1 MAddr to A1 and MData to D1. The APB output is still undefined, because the new values have not been written in the registers of the bridge. The Control FSM (CFSM) state is still IDLE because MCmd has not yet been registered.

T2 – The new values are written in the registers of the bridge, so they are visible at the APB interface. The CFSM state is now WR_SETUP, because the write command has been detected, so PWrite and PSel are asserted.

T3 – The APB slave registers the asserted PWrite and PSel signals and deserts the PReady signal as it is not ready to receive the data. The CFSM state is now WR_WAIT. The PEnable signal is asserted, signaling the start of the access phase (wait state to be precise).

T4 – The low PReady is registered, so the CFSM state stays WR_WAIT and the output signals do not change. However, the APB slave signals that it is ready to receive data by asserting the PReady signal.

T5 – The high PReady signal is registered so the CFSM state changes to WR_ACCESS. The SCmdAccept signal is asserted, signaling the OCP master that the transaction has been completed. PWrite, PSel and PEnable are deserted so the APB slave does not care about other signals.

T6 – The OCP master registers the SCmdAccept signal and changes the MCmd to IDLE. The CFSM state changes to IDLE, deserting the SCmdAccept signal.

T7 – The old value of MData, Sdata and Maddres are written in the registers of the bridge, and can be seen on the output signals, even though they are not important to the APB slave (because PSel is '0').

2.2 READ TRANSACTION

2.2.1 READ TRANSACTION WITHOUT ERROR

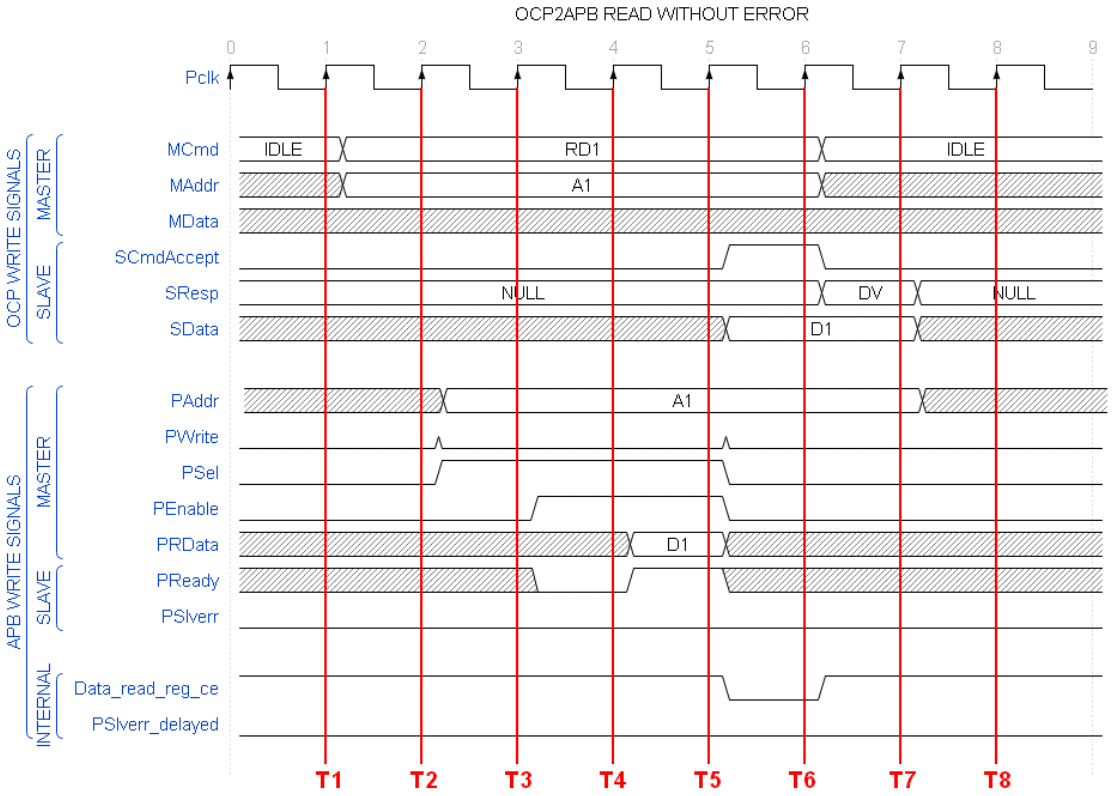

Figure 5: Read transaction without error

A typical read transaction (with wait states, without error) is shown in figure 5.

T1 – The master OCP changes MCmd to RD1 and MAddr to A1. The APB output is still undefined, because the new values have not been written in the registers of the bridge. The Control FSM (CFSM) state is still IDLE, because MCmd has not yet been registered.

T2 – The new values from the OCP master are written in the registers of the bridge, so they are visible at the APB interface. The CFSM state is now RD_SETUP, because the read command has been detected, so PWrite and PSel are asserted.

T3 – The APB slave registers the asserted PWrite and PSel signals and deserts the PReady signal as it is not ready to send the data. The CFSM state is now RD_WAIT. The PEnable signal is asserted, signaling the start of the access phase (wait state to be precise).

T4 – The low PReady signal is registered, so the CFSM state stays RD_WAIT and the output signals do not change. However, the APB slave signals that it is ready to send data by asserting the PReady signal and driving data on the SData bus.

T5 – The high PReady signal is registered, so the CFSM state changes to RD_ACCESS. The SCmdAccept signal is asserted, signaling the OCP master that the transaction has been completed. PWrite, PSel and PEnable are deserted so the APB slave does not care about other signals. The APB slave deserts the PReady signal and stops driving data on the SData bus. In order to keep the data provided by the slave in the current clock cycle, data_read_reg_ce is asserted in order to prevent writing undefined data into the data read register of the bridge.

T6 – The OCP master registers the SCmdAccept signal and changes the MCmd to IDLE. Because the PSlverr_delayed signal is not asserted, there has been no error, and the CFSM state changes to RD_RESP_DV, deserting the SCmdAccept signal, and asserting the SResp signal to DV (data valid). The data_read_reg_ce is deserted, as there is no need to enable write in the data read register.

T7 – The old value of Maddres is written in the register of the brige, and can be seen on the output signals, even though it is not important to the APB slave (because PSel is '0'). The CFSM state changes to IDLE, changing SResp to NULL.

2.2.2 READ TRANSACTION WITH ERROR

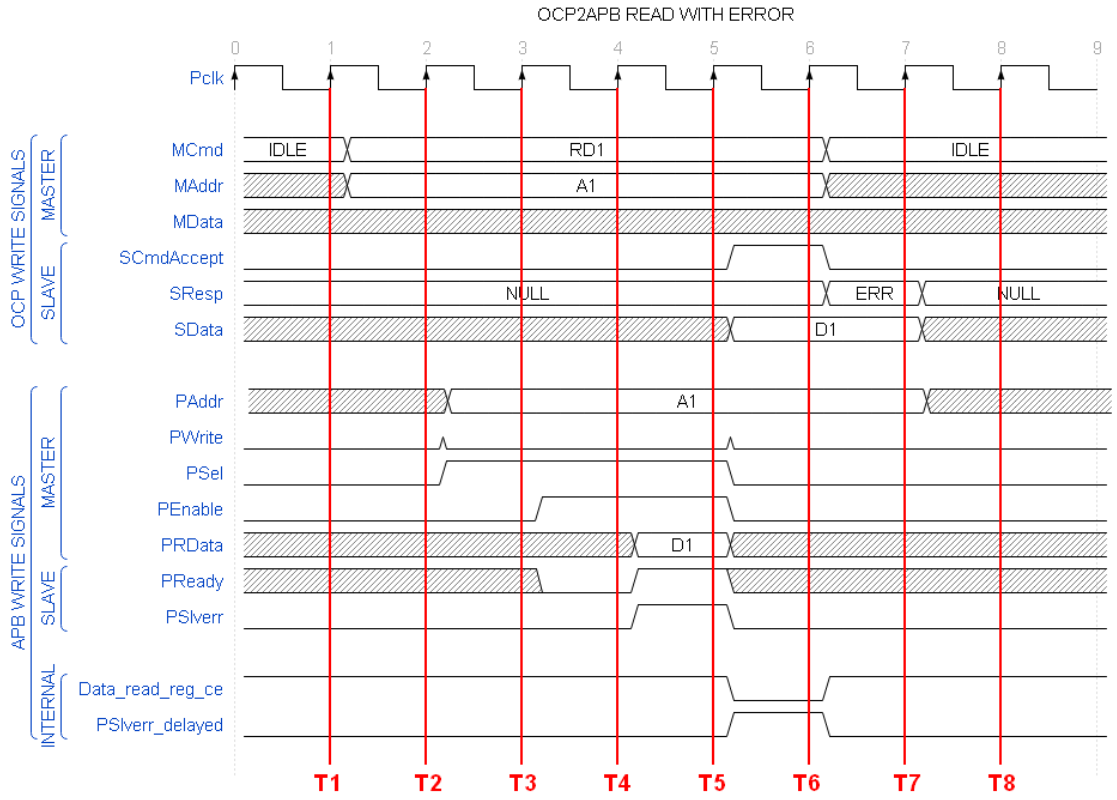

Figure 6: Read transaction with error

A typical read transaction (with wait states, with error) is shown in figure 5.

T1 – The master OCP changes MCmd to RD1 and MAddr to A1. The APB output is still undefined, because the new values have not been written in the registers of the bridge. The Control FSM (CFSM) state is still IDLE, because MCmd has not yet been registered.

T2 – The new values from the OCP master are written in the registers of the bridge, so they are visible at the APB interface. The CFSM state is now RD_SETUP, because the read command has been detected, so PWrite and PSel are asserted.

T3 – The APB slave registers the asserted PWrite and PSel signals and deserts the PReady signal as it is not ready to send the data. The CFSM state is now RD_WAIT. The PEnable signal is asserted, signaling the start of the access phase (wait state to be precise).

T4 – The low PReady signal is registered, so the CFSM state stays RD_WAIT and the output signals do not change. However, the APB slave signals that it is ready to send data by asserting the PReady signal and driving data on the SData bus.

T5 – The high PReady signal is registered, so the CFSM state changes to RD_ACCESS. The SCmdAccept signal is asserted, signaling the OCP master that the transaction has been completed. PWrite, PSel and PEnable are deserted so the APB slave does not care about other signals. The APB slave deserts the PReady signal and stops driving data on the SData bus. In order to keep the data provided by the slave in the current clock cycle, data_read_reg_ce is asserted in order to prevent writing undefined data into the data read register of the bridge.

T6 – The OCP master registers the SCmdAccept signal and changes the MCmd to IDLE. Because the PSlverr_delayed signal is asserted, there has been an error, and the CFSM state changes to RD_RESP_ERR, deserting the SCmdAccept signal, and asserting the SResp signal to ERR (error). The data_read_reg_ce is deserted, as there is no need to enable write in the data read register.

T7 – The old value of Maddres is written in the register of the brige, and can be seen on the output signals, even though it is not important to the APB slave (because PSel is '0'). The CFSM state changes to IDLE, changing SResp to NULL.