

# Ognjen Glamočanin

COMPUTER SCIENCE PHD STUDENT

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## Education

### EPFL, Ecole Polytechnique Fédérale de Lausanne

PHD IN COMPUTER SCIENCE

- Power side-channel security of shared FPGAs in the cloud
- Thesis advisors: Dr. Mirjana Stojilović and Prof. Babak Falsafi

Lausanne, Switzerland

Expected grad: August 2023

### Sorbonne Université, Paris VI

M.S. IN COMPUTER SCIENCE

Paris, France

2017 – 2018

### University of Novi Sad, Faculty of Technical Sciences

B.S. WITH HONOURS IN ELECTRICAL ENGINEERING

Novi Sad, Serbia

2013 – 2017

## Work Experience

### ARM

CPU MICROARCHITECTURE AND DESIGN INTERN

Sophia Antipolis, France

Mar 2018 – Aug 2018

- Analyzed CPU microarchitectural events for the purposes of power consumption estimation during cycle accurate simulation
- Used ML techniques to model correlation between events and simulated layout-level power consumption
- Enabled power estimation in early microarchitecture design stages by integrating power prediction in a cycle-accurate simulator

### FROBAS D.O.O.

MACHINE LEARNING HARDWARE ACCELERATION INTERN

Novi Sad, Serbia

Nov 2016 – Jun 2017

- Design and verification of an ML hardware accelerator for multi-layer perceptron (MLP) artificial neural networks (ANNs)

### ELSYS EASTERN EUROPE

HARDWARE FUNCTIONAL VERIFICATION INTERN

Belgrade, Serbia

Jul 2016 – Oct 2016

- Used SystemVerilog and the UVM methodology to build a functional verification environment for an OCP2UART bridge

## Publications

### Temperature Impact on Remote Power Side-Channel Attacks on Shared FPGAs

DATE

O. GLAMOČANIN, H. BAZAZ, M. PAYER, M. STOJILović

2023

- Analysis of temperature impact on FPGA-voltage sensors and remote power-analysis attacks.
- Impact of temperature effects on ML-based power side-channel attacks.

### The Side-Channel Metrics Cheat Sheet

CSUR

K. PAPAGIANNOPOULOS\*, O. GLAMOČANIN\*, M. AZOUAOU\*, D. ROS\*, F. REGAZZONI\*, M. STOJILović\* (\* EQUAL CONTRIBUTION)

2022

- Analysis and comparison of methods for power side-channel security evaluation, with extensive experimental examples.
- Work accompanied with an open-source library of metrics for side-channel analysis.

### Improving First-Order Threshold Implementations of SKINNY

INDOCRYPT

A. CAFORIO, D. COLLINS, O. GLAMOČANIN, AND S. BANIK

2021

- An efficient threshold implementation protection against power side-channel attacks for the SKINNY cipher.
- Experimental evaluation showing no existence of first-order power side-channel leakage.

### Shared FPGAs and the Holy Grail: Protections Against Side-Channel and Fault Attacks

DATE

O. GLAMOČANIN, D. G. MAHMOUD, F. REGAZZONI, AND M. STOJILović

2021

- Analysis of recently proposed methods for protection against side-channel and fault attacks in shared FPGAs.
- Insights on the versatility and inter-operability of the countermeasures, with an emphasis on future research directions.

### Are Cloud FPGAs Really Vulnerable to Power-Analysis Attacks?

DATE

O. GLAMOČANIN, L. COULON, F. REGAZZONI, AND M. STOJILović

2020

- Implementation of an FPGA-based voltage sensor on the state-of-the-art cloud FPGAs: Xilinx UltraScale+ on AWS F1 instances.
- Demonstration that remote power side-channel attacks are possible on cloud-scale FPGAs, and pose a serious threat to FPGA multitenancy.

### Built-In Self-Evaluation of First-Order Power Side-Channel Leakage for FPGAs

ISFPGA

O. GLAMOČANIN, L. COULON, F. REGAZZONI, AND M. STOJILović

2020

- Demonstration that FPGA-based voltage sensors can be used for remote power side-channel leakage estimation.
- Design of a first remote power side-channel leakage assessment system, allowing side-channel security reevaluation on deployed devices.

## Honors & Awards

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|------|---|-------------|
| 2018 | <b>EPFL EDIC Fellowship,</b><br>Fellowship for first-year PhD students  | Switzerland |
| 2017 | <b>French Government Scholarship for International Students,</b><br>Full scholarship for master studies in France | France      |
| 2016 | <b>Dr Vladan Desnica Award,</b><br>Best student of the microcomputer electronics track                            | Serbia      |

## Teaching Experience

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### EPFL

Lausanne, Switzerland

TEACHING ASSISTANT

Feb 2019 – ongoing

- **Computer Architecture:** Head TA, managing the course and lab sessions in CPU micro-architecture for 2<sup>nd</sup> year B.S. students
- **System Programming Project:** Leading lab sessions in C for 2<sup>nd</sup> year B.S. students
- **Information, Computation, Communication:** Head TA, managing the course and leading lab sessions in Python and C for 1<sup>st</sup> year B.S. students

### University of Novi Sad

Novi Sad, Serbia

TEACHING ASSISTANT

Sep 2016 – Jun 2017

- **Electrical Circuit Theory:** Leading computer lab sessions in MATLAB for 2<sup>nd</sup> year B.S. students
- **Systems and Signals:** Leading computer lab sessions in MATLAB for 2<sup>nd</sup> year B.S. students

## Technical Skills

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<b>Programming languages:</b>	C/C++ (10yrs), Python (6yrs), SystemVerilog, MATLAB
<b>Scripting languages:</b>	Python, Bash, TCL
<b>Hardware description languages:</b>	VHDL (9yrs), Verilog, SystemC
<b>CAD EDA tools:</b>	Xilinx ISE, Xilinx Vivado and Vitis, Cadence NCSim

## Languages

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<b>Serbian:</b>	Mother tongue
<b>English:</b>	fluent (level C2)
<b>French:</b>	fluent (level C1)
<b>German:</b>	beginner (level A1)

## Extracurricular Activities

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### The Illuminations of Jules Verne

Novi Sad, Serbia

FESTIVAL COORDINATOR

2012 – 2015

- Head coordinator of the music part of the festival of light, music and lanterns *The Illuminations of Jules Verne*
- Created and coordinated the music program, logistics
- <https://www.facebook.com/ZilvernovskeIluminacije/>