Ognjen **Glamočanin**

Computer Science PhD Student

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Education

EPFL, Ecole Polytechnique Fédérale de Lausanne — *Lausanne, Switzerland*

PhD in Computer Science — ***Expected grad: August 2023***

- Power side-channel security of shared FPGAs in the cloud
- Thesis advisors: Dr. Mirjana Stojilović and Prof. Babak Falsafi

Sorbonne Université, Paris VI — *Paris, France*

M.S. in Computer Science — *2017 – 2018*

University of Novi Sad, Faculty of Technical Sciences — *Novi Sad, Serbia*

B.S. with Honours in Electrical Engineering — *2013 – 2017*

Work Experience

ARM — *Sophia Antipolis, France*

CPU Micro-Architecture and Design Intern — *Mar 2018 – Aug 2018*

- Fast CPU power consumption estimation using correlation between CPU events and simulated layout-level power consumption
- Integrated the power prediction model in the cycle-approximate CPU simulator and enabled fast power consumption estimation

FROBAS D.O.O. — *Novi Sad, Serbia*

Machine Learning Hardware Acceleration Intern — *Nov 2016 – Jun 2017*

- Design and verification of an ML hardware accelerator for multi-layer perceptron (MLP) artificial neural networks (ANNs)

ELSYS EASTERN EUROPE — *Belgrade, Serbia*

Hardware Functional Verification Intern — *Jul 2016 – Oct 2016*

- Used SystemVerilog and the UVM methodology to build a complete functional verification environment for an OCP2UART bridge

Publications

Temperature Impact on Remote Power Side-Channel Attacks on Shared FPGAs — *DATE*

O. Glamočanin, H. Bazaz, M. Payer, M. Stojilović — *2023*

- Analysis of temperature impact on FPGA-voltage sensors and remote power analysis attacks.
- Impact of temperature effects on ML-based side-channel attacks.

The Side-Channel Metrics Cheat Sheet — *CSUR*

K. Papagiannopoulos, **O. Glamočanin**, M. Azouaoui, D. Ros, F. Regazzoni, M. Stojilović — *2022*

- Detailed analysis of methods used for power side-channel security evaluation, accompanied with an extensive experimental evaluation.
- Work accompanied by an open-source library of metrics for side-channel analysis.

Improving First-Order Threshold Implementations of SKINNY — *INDOCRYPT*

A. Caforio, D. Collins, **O. Glamočanin**, and S. Banik — *2021*

- An efficient implementation of the threshold implementation protection against power side-channel attacks for the SKINNY cipher.
- Extensive experimental evaluation showing no existence of first-order power side-channel leakage.

Shared FPGAs and the Holy Grail: Protections Against Side-Channel and Fault Attacks — *DATE*

O. Glamočanin, D. G. Mahmoud, F. Regazzoni, and M. Stojilović — *2021*

- Detailed analysis of recently proposed methods for protecting against side-channel and fault attacks in shared FPGAs.
- Insights on the versatility and inter-operability of the countermeasures, with an emphasis on future research directions.

Are Cloud FPGAs Really Vulnerable to Power-Analysis Attacks? — *DATE*

O. Glamočanin, L. Coulon, F. Regazzoni, and M. Stojilović — *2020*

- Implemented an FPGA-based voltage sensor on the state-of-the-art cloud FPGAs: Xilinx UltraScale+ on AWS F1 instances.
- Showed that remote power side-channel attacks are possible on cloud-scale FPGAs, and pose a serious threat to FPGA multitenancy.

Built-In Self-Evaluation of First-Order Power Side-Channel Leakage for FPGAs — *ISFPGA*

O. Glamočanin, L. Coulon, F. Regazzoni, and M. Stojilović — *2020*

- Demonstrated that FPGA-based voltage sensors can be used for remote power side-channel leakage estimation.
- Designed a system for remote power side-channel leakage assessment, allowing side-channel security reevaluation on deployed devices.

Honors & Awards

2018 **EPFL EDIC Fellowship**, *Switzerland*
Fellowship for first-year PhD students

2017 **French Government Scholarship for International Students**, *France*
Full scholarship for master studies in France

2016 **Dr Vladan Desnica Award**, *Serbia*
Best student of the microcomputer electronics track

Teaching Experience

EPFL
Lausanne, Switzerland

Teaching Assistant
Feb 2019 – ongoing

- **Computer Architecture**: Head TA, managing the course and lab sessions in CPU micro-architecture for 2nd year B.S. students
- **System Programming Project**: Leading lab sessions in C for 2nd year B.S. students
- **Information, Computation, Communication**: Head TA, managing the course and leading lab sessions in Python and C for 1st year B.S. students

University of Novi Sad
Novi Sad, Serbia

Teaching Assistant
Sep 2016 – Jun 2017

- **Electrical Circuit Theory**: Leading computer lab sessions in MATLAB for 2nd year B.S. students
- **Systems and Signals**: Leading computer lab sessions in MATLAB for 2nd year B.S. students

Technical Skills

Programming languages: C/C++ (10yrs), Python (6yrs), SystemVerilog, MATLAB
Scripting languages: Python, Bash, TCL
Hardware description languages: VHDL (9yrs), Verilog, SystemC
CAD EDA tools: Xilinx ISE, Xilinx Vivado and Vitis, Cadence NCSim

Languages

Serbian: Mother tongue
English: fluent (level C2)
French: fluent (level C1)
German: beginner (level A1)

Extracurricular Activities

The Illuminations of Jules Verne
Novi Sad, Serbia

Festival Coordinator
2012 – 2015

- Head coordinator of the music part of the festival of light, music and lanterns *The Illuminations of Jules Verne*
- Created and coordinated the music program, logistics
- `https://www.facebook.com/ZilvernovskeIluminacije/`